To our customers,

Old Company Name in Catalogs and Other Documents

On April 1st, 2010, NEC Electronics Corporation merged with Renesas Technology Corporation, and Renesas Electronics Corporation took over all the business of both companies. Therefore, although the old company name remains in this document, it is a valid Renesas Electronics document. We appreciate your understanding.

Renesas Electronics website: http://www.renesas.com

April 1st, 2010
Renesas Electronics Corporation

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RENESAS

RENESAS TECHNICAL UPDATE

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Product Category	MPU&MCU			Document No.	TN-SH7-A694A/E	Rev.	1.00
Title	Notes about using Deep Standby Mode of SH7265/SH7205			Information Category	Technical Notification		
Applicable Product	SH7265 Group SH7205 Group	Lot No.		Reference Document	SH7265 Group Hardware Manual (REJ09B0351-0100) SH7205 Group Hardware Manual (REJ09B0372-0100)		
		ALL					

We would like to inform you of addition of notes about canceling deep standby mode by an interrupt in hardware manual of applicable products.

Before change

Section 33 (SH7265) / 30 (SH7205) Power-Down Modes

33.3.7 (SH7265) / 30.3.7 (SH7205) Deep Standby Mode

(2) Canceling Deep Standby Mode

(a)Canceling by an interrupt

When the falling edge or rising edge of the NMI pin (selected by the NMI edge select bit (NMIE) in interrupt control register 0 (C0ICR0, C1ICR0) of the interrupt controller (INTC)) or the falling edge or rising edge of an IRQ pin (IRQ7 to IRQ0 allocated to PJ3 to PJ0 and PC3 to PC0) (selected by the IRQn sense select bits (IRQn1S and IRQn0S) in interrupt control register 1 (C0ICR1, C1ICR1) of INTC) is detected, clock oscillation is started after waiting for the power supply stabilization time.

The clock output phase of the CKIO pin may be unstable immediately after an interrupt is detected and until deep standby mode is canceled. When deep standby mode is canceled on the falling edge of the NMI pin, the NMI pin should be high when the CPU enters deep standby mode (when the clock pulse stops) and should be low when the CPU returns from deep standby mode (when the clock is initiated after the oscillation settling). When deep standby mode is canceled by the rising edge of the NMI pin, the NMI pin should be low when the CPU enters deep standby mode (when the clock pulse stops) and should be high when the CPU returns from deep standby mode (when the clock is initiated after the oscillation settling). (This is the same with the IRQ pin.)

After change (addition of red letters)

Section 33 (SH7265) / 30 (SH7205) Power-Down Modes

33.3.7 (SH7265) / 30.3.7 (SH7205) Deep Standby Mode

(2) Canceling Deep Standby Mode

(a)Canceling by an interrupt

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The clock output phase of the CKIO pin may be unstable immediately after an interrupt is detected and until deep standby mode is canceled. When deep standby mode is canceled on the falling edge of the NMI pin, the NMI pin should be high when the CPU enters deep standby mode (when the clock pulse stops) and should be low when the CPU returns from deep standby mode (when the clock is initiated after the oscillation settling). When deep standby mode is canceled by the rising edge of the NMI pin, the NMI pin should be low when the CPU enters deep standby mode (when the clock pulse stops) and should be high when the CPU returns from deep standby mode (when the clock is initiated after the oscillation settling). (This is the same with the IRQ pin.)

Also, about NMI and the all interrupt pins (IRQ) which are selected by DSSSR to cancel deep standby mode, regardless whether they will really cancel deep standby mode or not,

(1) For the pins which are set as rising edge, those should be low when the CPU enters deep standby mode

(2) For the pins which are set as falling edge, those should be high when the CPU enters deep standby mode