To our customers,

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GRADE A

MESC TECHNICAL NEWS No.M16C-44-0001

M16C/80 Group Cautions for Using DMA

1. Affected devices

• M16C/80 Group

2. Cautions

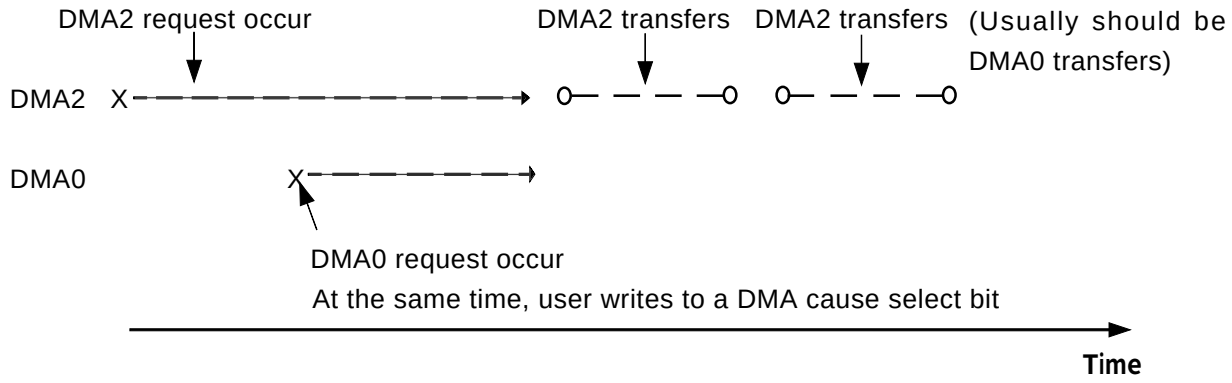
There is a possibility that the DMAC will execute 2 transfers upon receiving only 1 DMA request or control of the MCU may be lost depending on timing. This may happen if the conditions below are true.

(1) While DMA request A is occurring, a DMA request occurs which has a higher priority level than A at the same time a Software DMA request bit (bit 7 of DMA control register) for DMA0-DMA3 is being cleared to '0'.

(2) While DMA request A is occurring and a write to any bit in the DMA request cause select bit section of the DMA request cause select register for DMA0-DMA3 occurs.

DMA priority : DMA0 > DMA1 > DMA2 > DMA 3
High ----------LOW

Example of timing: In this case, DMA request A is on DMA 2 and DMA request B on DMA 0.



3. Countermeasure

3.1 If you are using the conditions below, you do not need to use the countermeasures

(1) All DMAs are disabled when writing to DMA cause select register.

(2) None of the enabled DMA requests occur when writing to a DMA cause select register.

If your condition is not satisfy, please countermeasure either (3),(4).

(3) If you write to the DMA request cause select register in order to clear the DMA request bit, please delete this instruction of clearing the DMA request cause select bit. It is not needed.
When a DMA requests occur with M16C/80 and the DMA channel condition does not accept the request (as when the DMA is Disabled or Transfer counter is '0'), a DMA transfers will not take place and the DMA request bit will be cleared automatically without software intervention.

(4) If you wish to change any of the DMA request cause select bits in the DMA request select cause register, please also write '1' to the Software DMA request bit at the same time.
But, please do the above with DMA in disabled conditions.

Ex: In case of use the DMA0 with single transfer and change the DMA cause to Timer A0

```
push.w    R0                ;Stack R0 register
stc       DMD0,R0           ;Read DMA mode registers
and.b     #11111100b,R0L    ;Clear DMA0 transfer mode select bit to '00'
ldc       R0,DMD0           ;Disable DMA0
mov.b     #10000011b,DM0SL  ;Select Timer A0 (Write '1' to DMA request bit at same time)
mov.b     R0L,R0L           ;Dummy cycle
or.b      #00000001b,R0L    ;Set single transfer mode to DMA0
ldc       R0,DMD0           ;Enable DMA0
pop.w     R0                ;Replace R0
```