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RENESAS TECHNICAL UPDATE

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Product Category	MPU/MCU		Document No.	TN-H8*-A439A/E	Rev.	1.00
Title	Error correction regarding EERPOM Blank Check Control Register.		Information Category	Technical Notification		
Applicable Product	H8SX 1720 Group, H8SX 1720S Group	Lot No. All lots	Reference Document	Refer to the "Reference Documents" section below		

Thank you for your consistent patronage of Renesas semiconductor products.

We would like to inform you of the correction of errors regarding EEPROM Blank Check Control Register in the H8SX 1720/1720S Group Hardware Manuals.

Please read the following carefully before using the H8SX Group products.

EEPBCCNT (EEPROM Blank Check Control Register) specifies the address and size of the EEPROM area for blank check command.

When BCSIZE is 0 and BCADR bits specify the start address for blank checking, if any bit of BCADR[10:8] were set to “1”, the size of the area for blank checking would exceed the size of erasure block units (2Kbytes). Therefore the write value of BCADR[10:8] should always be all “0” to prevent a malfunction.

Figure 1 shows the address range when all bit of BCADR[10:0] are set to “1” and the rightfully necessary address range.

EEPROM Blank Check Control Register)(EEPBCCNT)

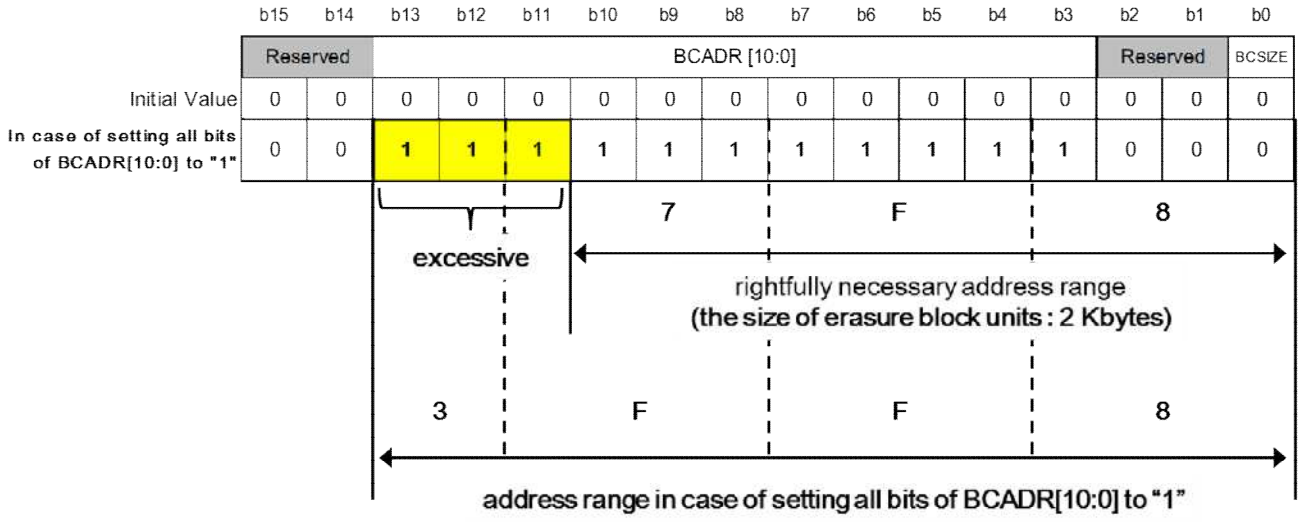

Figure1 . Address range in case of setting all bits of BCADR[10:0] to “1” and the rightfully necessary address range.

[Corrections in the Hardware Manuals]

Accordingly, we would like to correct the Hardware Manuals as follows.

21.3.9 EEPROM Blank Check Control Register (EEPBCCNT)

■Before correction

21.3.9 EEPROM Blank Check Control Register (EEPBCCNT)

Bit	15	14	13	12	11	10	9	8
Bit Name	—	—	BCADR	BCADR	BCADR	BCADR	BCADR	BCADR
Initial Value:	0	0	0	0	0	0	0	0
R/W:	R	R	R/W	R/W	R/W	R/W	R/W	R/W

Bit	7	6	5	4	3	2	1	0
Bit Name	BCADR	BCADR	BCADR	BCADR	BCADR	—	—	BCSIZE
Initial Value:	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R	R	R/W

Bit	Bit Name	Initial Value	R/W	Description
15, 14	—	All 0	R	Reserved These bits are always read as 0. Otherwise, operation cannot be guaranteed.
13 to 3	BCADR	All 0	R/W	Blank Check Address Setting These bits specify the address for blank checking by the blank check command when the size of the area for blank check is eight bytes (BCSIZE bit = 0). When BCSIZE is 0, the start address for blank checking is the setting value of EEPBCCNT (the value set in BCADR shifted toward MSB by 3 bits) added to the erasure block start address specified when a blank check command is issued.
2, 1	—	All 0	R	Reserved These bits are always read as 0. Otherwise, operation cannot be guaranteed.
0	BCSIZE	0	R/W	Blank Check Size Setting Specifies the size of the area for blank checking by the blank check command. 0: 8 bytes 1: 2 Kbytes

■After correction

21.3.9 EEPROM Blank Check Control Register (EEPBCCNT)

Bit	15	14	13	12	11	10	9	8
Bit Name	—	—	—	—	—	BCADR	BCADR	BCADR
Initial Value:	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R/W	R/W	R/W

Bit	7	6	5	4	3	2	1	0
Bit Name	BCADR	BCADR	BCADR	BCADR	BCADR	—	—	BCSIZE
Initial Value:	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R	R	R/W

Bit	Bit Name	Initial Value	R/W	Description
15 to 11	—	All 0	R	Reserved These bits are always read as 0. Otherwise, operation cannot be guaranteed.
10 to 3	BCADR	All 0	R/W	Blank Check Address Setting These bits specify the address for blank checking by the blank check command when the size of the area for blank check is eight bytes (BCSIZE bit = 0). When BCSIZE is 0, the start address for blank checking is the setting value of EEPBCCNT (the value set in BCADR shifted toward MSB by 3 bits) added to the erasure block start address specified when a blank check command is issued.
2, 1	—	All 0	R	Reserved These bits are always read as 0. Otherwise, operation cannot be guaranteed.
0	BCSIZE	0	R/W	Blank Check Size Setting Specifies the size of the area for blank checking by the blank check command. 0: 8 bytes 1: 2 Kbytes

[Behavior in case of setting the blank check address beyond the size of erasure block units (=2 Kbytes)]

The behavior in case of malfunction at setting any or all bit of BCADR[10:8] to "1" is shown below (3 cases). Figure 2 to 4 show the normal case and three examples of malfunction.

【Note】 Case 1 to 3 (Figure.2 to 4) describe only the 32 Kbytes EEPROM . For the 16 Kbytes EEPROM, the address in the figure shall be replaced as H'E05000→H'E01000, H'E05800→H'E01800, H'E06000→H'E02000, H'E06800→H'E02800, H'E07000→H'E03000, H'E07800→H'E03800, H'E08000→H'E04000.

(1) Case 1 : 2 Kbytes ≦ BCADR[10:0] setting < 8 Kbytes (Figure. 2)

->The other erasure block will be blank-checked than the set erasure block.

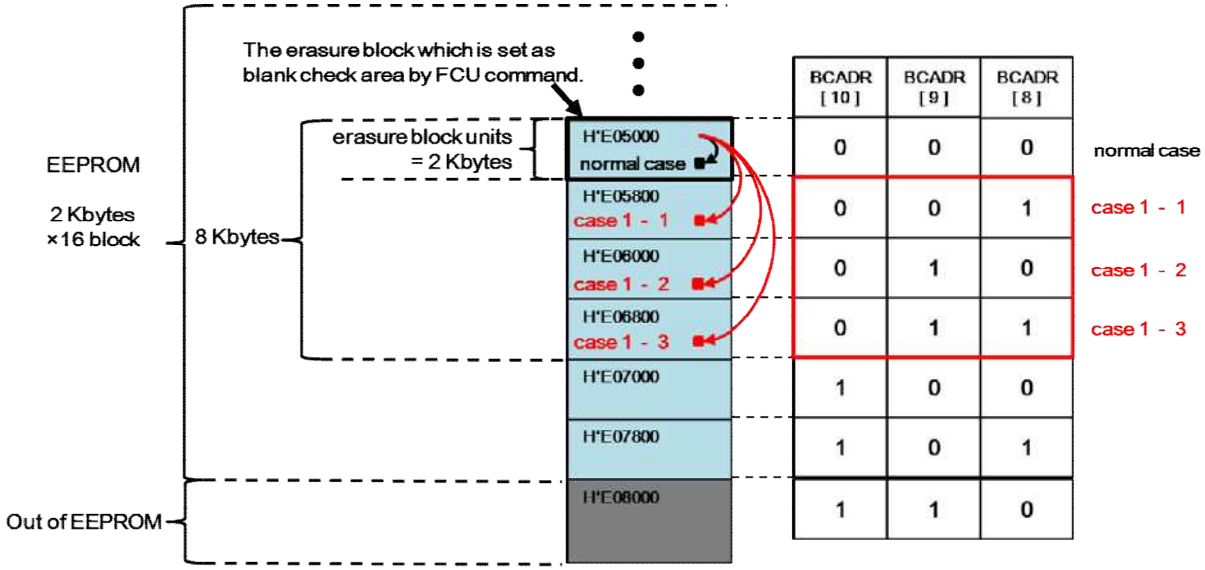

Figure 2 . Example of malfunction (Case1)

(2) Case 2 : 8 Kbytes ≦ BCADR[10:0] setting (Figure. 3)

->The address more than 8 Kbytes returns to the top of the set eraser block and the recalculated address block will be blank-checked.

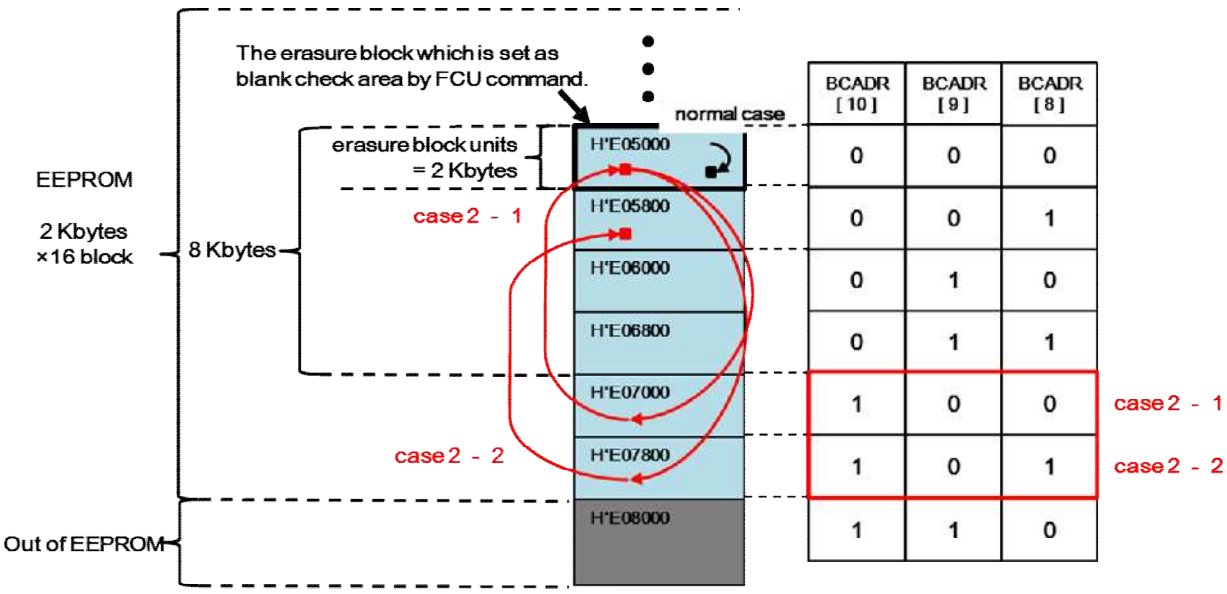

Figure 3 . Example of malfunction (Case 2)

(3) Case 3 : Setting the address beyond the EEPROM area (Figure. 4)

->FCU firmware will return the result of blank check which is not guaranteed. And the error will not occur.

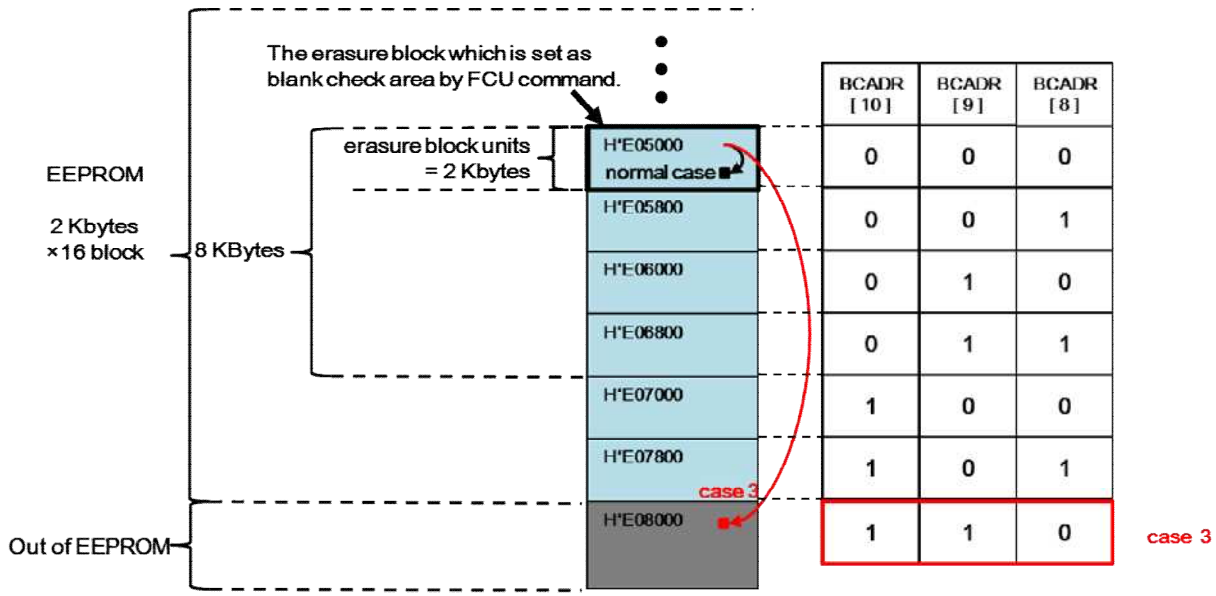

Figure 4 . Example of malfunction (Case 3)

[Reference Documents]

H8SX/1720 Group Hardware Manual （R01UH0369EJ0300）Rev.3.00

H8SX/1720S Group Hardware Manual （R01UH0370EJ0200）Rev.2.00

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