Date: Nov. 21, 2019

RENESAS TECHNICAL UPDATE

TOYOSU FORESIA, 3-2-24, Toyosu, Koto-ku, Tokyo 135-0061, Japan
Renesas Electronics Corporation

Product Category	MPU/MCU		Document No.	TN-SY*-A0045A/E	Rev.	1.00
Title	Errata for User's Manual regarding the IIC		Information Category	Technical Notification		
Applicable Product	Renesas Synergy™ S128 MCU Group	Lot No. All	Reference Document	S128 Microcontroller Group User's Manual Rev.1.10		

The specified Renesas Synergy S128 User's Manual has incorrect statements about the IIC.

Page 753 of 1232

Incorrect

In slave mode, when a restart condition is detected (a start condition is detected with ICCR2.BBSY = 1 and ICCR2.MST = 0)

Correct

In slave mode, when a restart condition is detected (a restart condition is detected with ICCR2.BBSY = 1 and ICCR2.MST = 0)

Page 759 of 1232

Incorrect

The NACKE bit specifies whether to continue or discontinue the transfer operation when NACK is received from the slave device in transmit mode. Normally, set this bit to 1.

Correct

The NACKE bit specifies whether to continue or discontinue the transfer operation when NACK is received ~~from the slave device~~ in transmit mode. Normally, set this bit to 1.

Page 765 of 1232

Incorrect

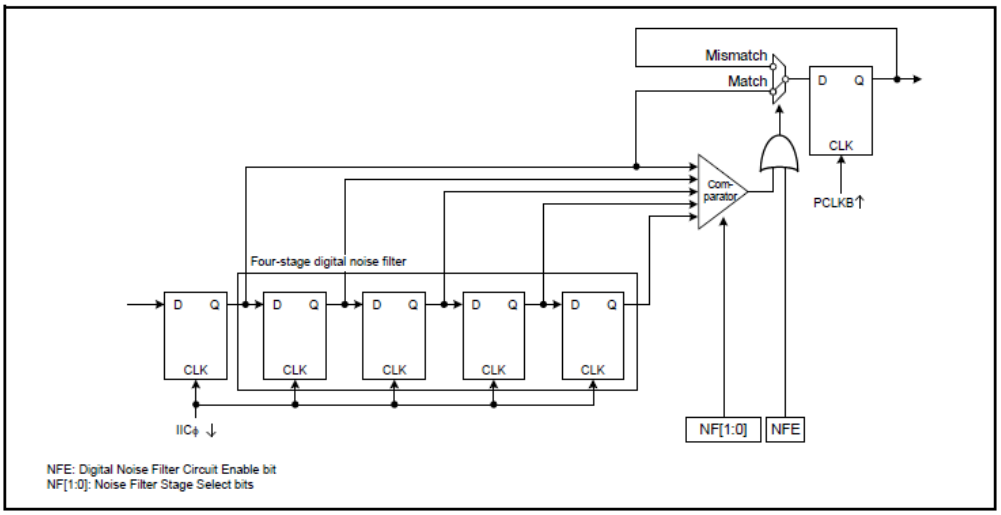
The IIC can also set the AL flag to indicate the detection of arbitration loss during NACK transmission in master mode or during data transmission in slave mode.

Correct

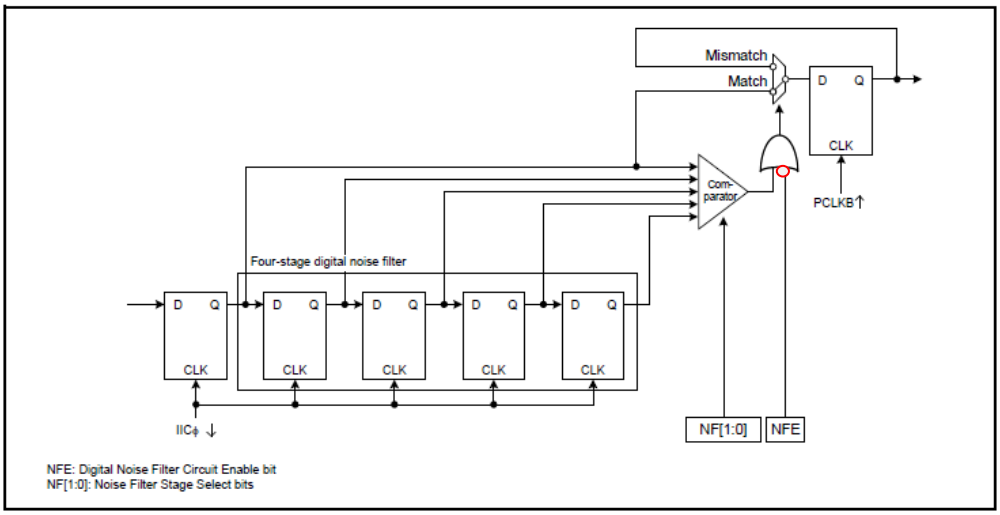
The IIC can also set the AL flag to indicate the detection of arbitration loss during NACK transmission ~~in master mode~~ or during data transmission ~~in slave mode~~.

Page 791 of 1232

Incorrect Figure



Correct Figure



Page 794 of 1232

Incorrect

The IIC module provides detection of device-ID address in compliance with the I2C bus specification (Rev. 03). When the IIC receives 1111 100b as the first byte after a start or restart condition was issued with the DIDE bit in ICSER set to 1, it recognizes the address as a device ID, sets the DID flag in ICSR1 to 1 on the rising edge of the eighth SCL clock cycle when the subsequent R/W# bit is 0, then compares the second and subsequent bytes with its own slave address.

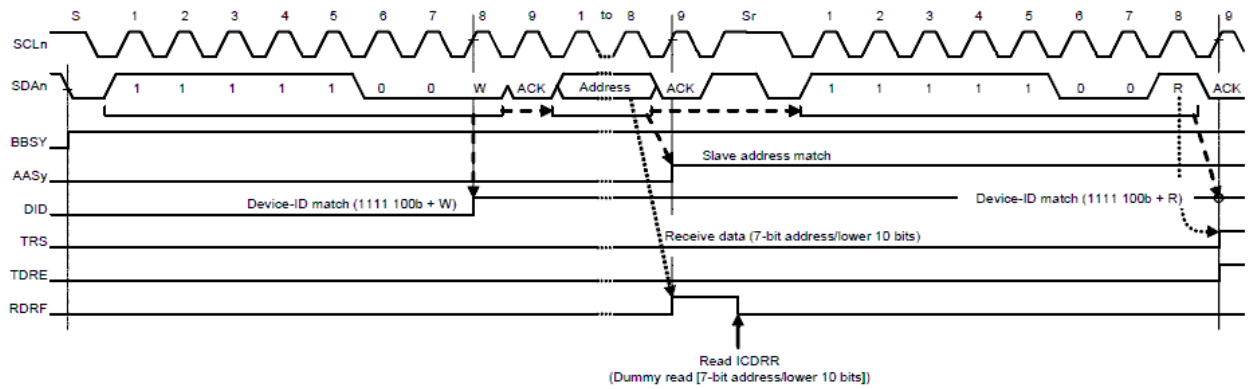
Correct

The IIC module provides detection of device-ID address in compliance with the I2C bus specification (Rev. 03). When the IIC receives 1111 100b as the first byte after a start or restart condition was issued with the DIDE bit in ICSER set to 1, it recognizes the address as a device ID, sets the DID flag in ICSR1 to 1 on the rising edge of the 9th SCL clock cycle when the subsequent R/W# bit is 0, then compares the second and subsequent bytes with its own slave address.

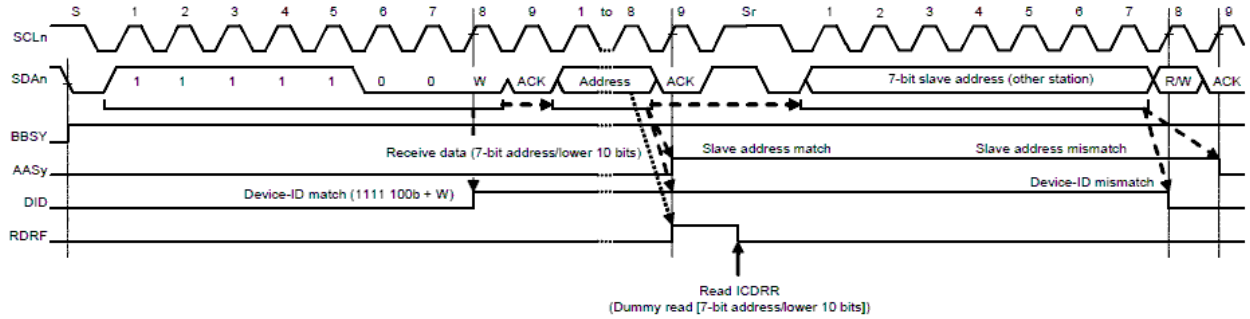
Page 794 of 1232

Incorrect Figure

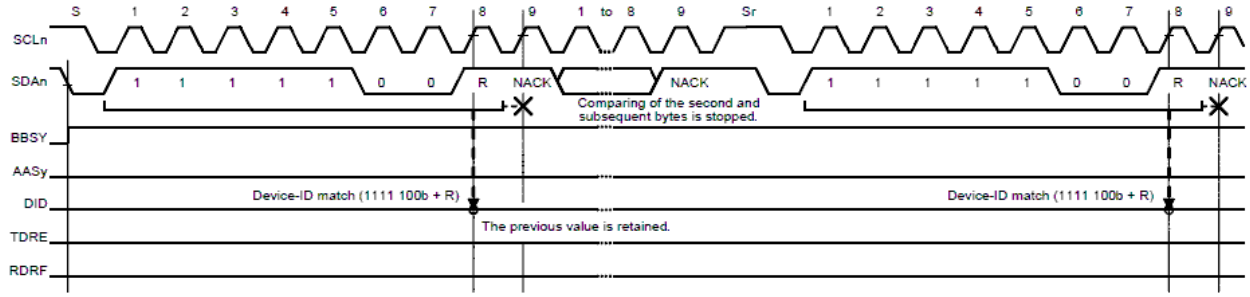
Device-ID reception



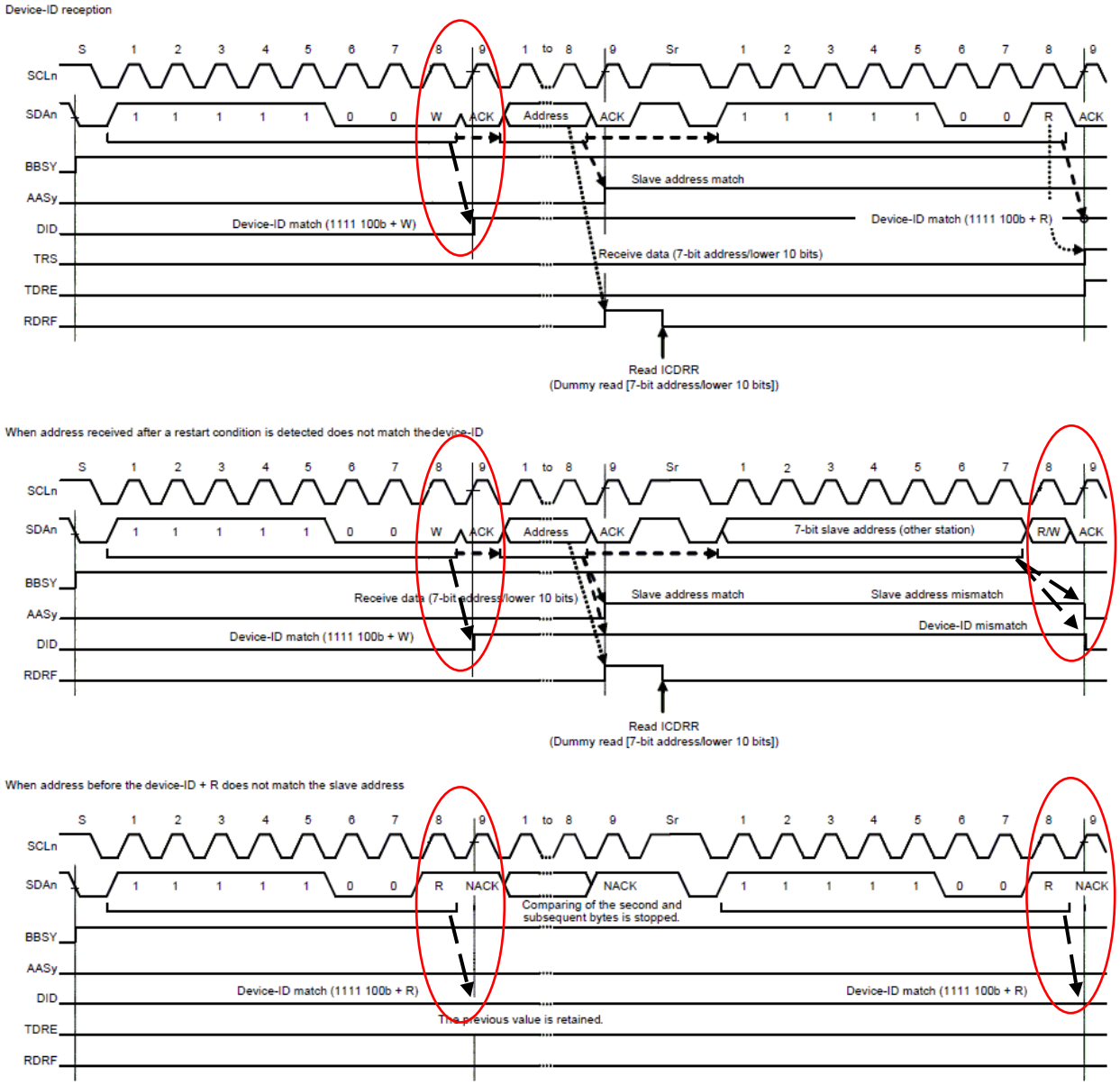
When address received after a restart condition is detected does not match thedevice-ID



When address before the device-ID + R does not match the slave address

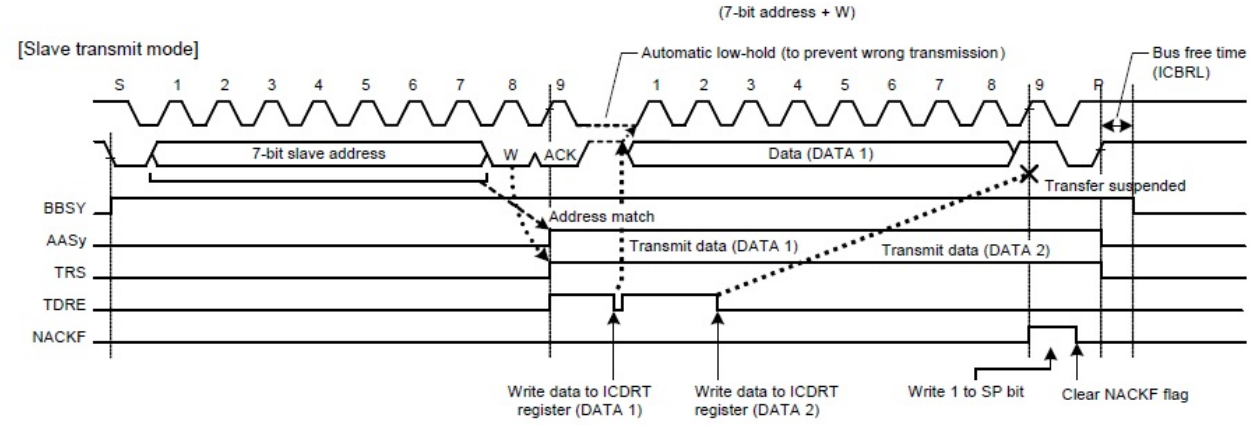


Correct Figure

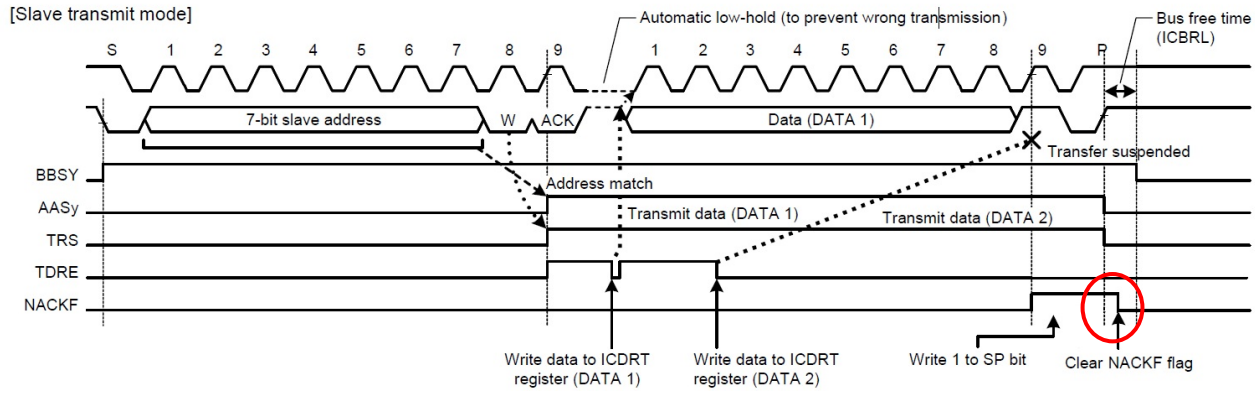


Page 807 of 1232

Incorrect Figure



Correct Figure



Page 816 of 1232

Incorrect

Therefore, more extra clock cycles can be output consecutively by software writing 1 to the CLO bit after having read CLO = 0.

Correct

If the BBSY flag is 1, SCL terminal keeps low output, if BBSY flag is 0, SCL terminal keeps high output. Additional clock cycles can be output consecutively by writing 1 to the CLO bit with software after reading the bit as 0.

Page 816 of 1232

Incorrect

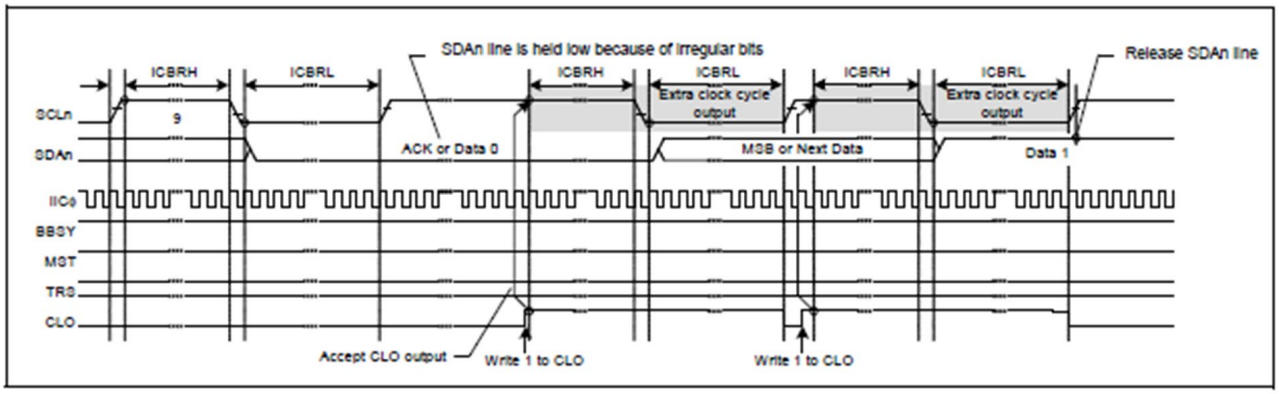
Use this function with the MALE bit in ICFER set to 0 (master arbitration-lost detection disabled). If the MALE bit is set to 1 (enabled), arbitration is lost when the value of the SDAO bit in ICCR1 does not match the state of the SDAn line.

Correct

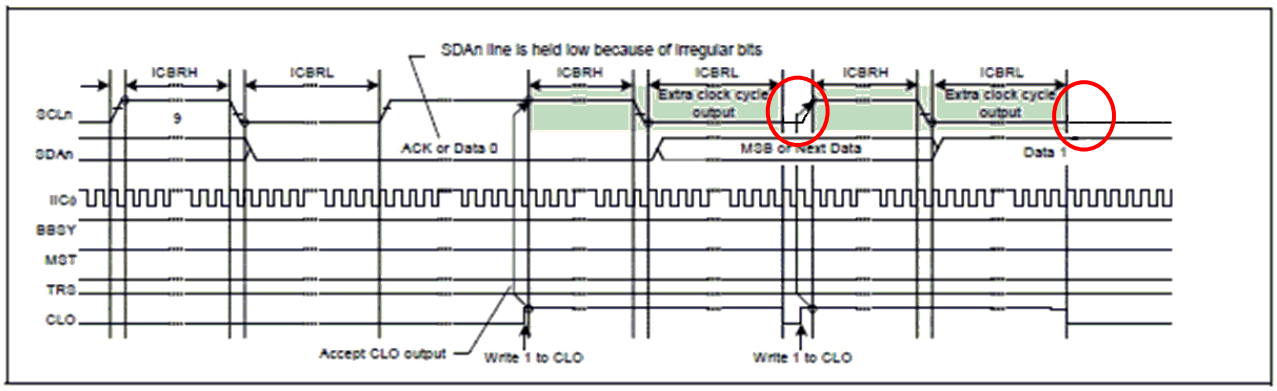
~~Use this function with the MALE bit in ICFER set to 0 (master arbitration-lost detection disabled). If the MALE bit is set to 1 (enabled), arbitration is lost when the value of the SDAO bit in ICCR1 does not match the state of the SDAn line.~~

Page 817 of 1232

Incorrect Figure



Correct Figure



Page 820 of 1232

Incorrect Table

Registers		Reset	IIC reset (ICE = 0, IICRST = 1)	Internal reset (ICE = 1, IICRST = 1)	Start or restart condition detection	Stop condition detection
ICCR1	ICE, IICRST	At a At a reset	Saved	Saved	Saved	Saved
	SCLO, SDAO		At a reset	At a reset		
	Others			Saved		
ICCR2	BBSY	At a reset	At a reset	Saved	Set	Saved
	ST			At a reset	Saved	Saved
	TRS,MST				Set or saved	At a reset
	Others				At a reset	At a reset or Saved
ICMR1	BC[2:0]	At a reset	At a reset	At a reset	At a reset	Saved
	Others			Saved	Saved	
ICMR2		At a reset	At a reset	Saved	Saved	Saved
ICMR3		At a reset	At a reset	Saved	Saved	Saved
ICFER		At a reset	At a reset	Saved	Saved	Saved
ICSER		At a reset	At a reset	Saved	Saved	Saved
ICIER		At a reset	At a reset	Saved	Saved	Saved
ICSR1		At a reset	At a reset	At a reset	Saved	At a reset
ICSR2	TDRE, TEND	At a reset	At a reset	At a reset	Saved	At a reset
	START				Set	
	STOP				Saved	Set
	Others				Saved	Saved
ICWUR		At a reset	At a reset	Saved	Saved	Saved
SARL0, SARL1, SARL2 SARU0, SARU1, SARU2		At a reset	At a reset	Saved	Saved	Saved
ICBRH, ICBRL		At a reset	At a reset	Saved	Saved	Saved
ICDRT		At a reset	At a reset	Saved	Saved	Saved
ICDRR		At a reset	At a reset	Saved	Saved	Saved
ICDRS		At a reset	At a reset	At a reset	Saved	Saved
ICWUR2	WUSEN	At a reset	At a reset	Saved	Saved	Saved
	Others					Set, reset, or saved
Timeout function		At a reset	At a reset	Operation	Operation	Operation
Bus free time measurement		At a reset	At a reset	Operation	Operation	Operation

Correct Table

Registers		Reset	IIC reset (ICE = 0, IICRST = 1)	Internal reset (ICE = 1, IICRST = 1)	Start or restart condition detection	Stop condition detection
ICCR1	ICE, IICRST	At a reset	Saved	Saved	Saved	Saved
	SCLO, SDAO		At a reset	At a reset		
	Others			Saved		
ICCR2	BBSY	At a reset	At a reset	Saved	Set	At a reset
	ST, RS			At a reset	At a reset	Saved
	SP					At a reset
	TRS				Set or saved	
	MST					
ICMR1	BC[2:0]	At a reset	At a reset	At a reset	At a reset	Saved
	Others			Saved	Saved	
ICMR2		At a reset	At a reset	Saved	Saved	Saved
ICMR3	ACKBIT	At a reset	At a reset	Saved	Saved	At a reset
	Others					Saved
ICFER		At a reset	At a reset	Saved	Saved	Saved
ICSER		At a reset	At a reset	Saved	Saved	Saved
ICIER		At a reset	At a reset	Saved	Saved	Saved
ICSR1		At a reset	At a reset	At a reset	Saved	At a reset
ICSR2	TEND	At a reset	At a reset	At a reset	Saved	At a reset
	TDRE				Set or saved	
	START				Set	
	STOP				Saved	Set
	Others				Saved	Saved
ICWUR		At a reset	At a reset	Saved	Saved	Saved
SARL0, SARL1, SARL2 SARU0, SARU1, SARU2		At a reset	At a reset	Saved	Saved	Saved
ICBRH, ICBRL		At a reset	At a reset	Saved	Saved	Saved
ICDRT		At a reset	At a reset	Saved	Saved	Saved
ICDRR		At a reset	At a reset	Saved	Saved	Saved
ICDRS		At a reset	At a reset	At a reset	Saved	Saved
ICWUR2	WUSEN	At a reset	At a reset	Saved	Saved	Saved
	Others					Set, reset, or saved
Timeout function		At a reset	At a reset	At a reset	Operation	Operation
Bus free time measurement		At a reset	At a reset	Operation	Operation	Operation