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RENESAS TECHNICAL UPDATE

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Product Category	MPU/MCU		Document No.	TN-RX*-A164A/E	Rev.	1.00
Title	Errata to RX65N Group, RX651 Group User's Manual: Hardware		Information Category	Technical Notification		
Applicable Product	RX65N Group, RX651 Group	Lot No. All	Reference Document	RX65N Group, RX651 Group User's Manual: Hardware Rev.1.00 (R01UH0590EJ0100)		

This document describes corrections to the RX65N Group, RX651 Group User's Manual: Hardware, Rev.1.00.
The corrections are indicated in red.

No.	Section Number	Summary
1	1. Overview	Note 4 is added to the realtime clock function in Table.1.1 Outline of Specifications.
2	23. Multi-Function Pin Controller (MPC)	Bit Name of the ADRHMS2 bit in 23.2.24 External Bus Control Register 0 (PFBCR0) is corrected.
3	41. Quad Serial Peripheral Interface (QSPI)	Title and description of 41.4.3 are modified.
4	43. SD Host Interface (SDHI)	Descriptions of b8 to b11 in 43.2.13 SD Error Status Register (SDERSTS1) are corrected.
5	44. SD Slave Interface (SDSI)	Expression in 44.1 Overview is modified.
6	50. 12-Bit A/D Converter (S12ADFa)	Description of operating modes in Table 50.1 in 50.1 Overview is corrected.
7	51. 12-Bit D/A Converter (R12DA)	The last sentence in (3) in 51.3 Operation is deleted.
8	51. 12-Bit D/A Converter (R12DA)	The second sentence in (4), description below Figure 51.3, and Figure 51.4 in 51.3.1 Measure against Interference between D/A and A/D Conversion are deleted.
9	57. Electrical Characteristics	Values of supply current under deep software standby mode in Table 57.5 DC Characteristics (3) in 57.2 DC Characteristics are corrected.
10	57. Electrical Characteristics	Values of reference power supply current in Table 57.6 DC Characteristics (4) in 57.2 DC Characteristics are corrected.
11	57. Electrical Characteristics	Table 57.x DC Characteristics (5) is added to 57.2 DC Characteristics.

No.1 1.1 Outline of Specifications

Note 4 is added to Table 1.1 as follows:

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Table 1.1 Outline of Specifications (5/8)

Classification	Module/Function	Description
Timers	Realtime clock (RTCd) *4	• Clock sources: Main clock, sub clock • Selection of the 32-bit binary count in time count/second unit possible • Clock and calendar functions • Interrupt sources: Alarm interrupt, periodic interrupt, and carry interrupt • Battery backup operation • Time-capture facility for three values • Event linking by the ELC
	Watchdog timer (WDTA)	• 14 bits × 1 channel • Select from among 6 counter-input clock signals (PCLKB/4, PCLKB/64, PCLKB/128, PCLKB/512, PCLKB/2048, PCLKB/8192)
	Independent watchdog timer (IWDTa)	• 14 bits × 1 channel • Counter-input clock: IWDT-dedicated on-chip oscillator • Dedicated clock/1, dedicated clock/16, dedicated clock/32, dedicated clock/64, dedicated clock/128, dedicated clock/256 • Window function: The positions where the window starts and ends are specifiable (the window defines the timing with which refreshing is enabled and disabled). • Event linking by the ELC

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Table 1.1 Outline of Specifications (8/8)

Classification	Module/Function	Description
Safety	Clock frequency accuracy measurement circuit (CAC)	• Monitors the clock output from the main clock oscillator, sub-clock oscillator, low- and high-speed on-chip oscillators, the PLL frequency synthesizer, IWDT-dedicated on-chip oscillator, and PCLKB, and generates interrupts when the setting range is exceeded.
	Data operation circuit (DOC)	• The function to compare, add, or subtract 16-bit data
Encryption function	AESa*2	• Key lengths: 128, 192, and 256 bits • Support for CFB, OFB, and CMAC operating modes • Speed of calculations: 128-bit key length in 22 cycles 192-bit key length in 26 cycles 256-bit key length in 30 cycles • Compliant with FIPS PUB 197
	True random number generator (RNGa)*2	• Length of random numbers: 16 bits • Generation of random-number-generated interrupts after a number is generated • Random number generation time: 1.9 ms (typ)
Operating frequency		Up to 120 MHz
Power supply voltage		VCC = AVCC0 = AVCC1 = VCC_USB = 2.7 to 3.6 V, 2.7 ≤ VREFH0 ≤ AVCC0, V_{BATT} = 2.0 to 3.6 V
Operating temperature		D-version: –40 to +85°C G-version: –40 to +105°C (in planning)
Package		145-pin TFLGA (PTLG0145KA-A) 144-pin LFQFP (PLQP0144KA-B) 100-pin TFLGA (PTLG0100JA-A) 100-pin LFQFP (PLQP0100KB-B)
On-chip debugging system		• E1 emulator (JTAG and FINE interfaces) • E20 emulator (JTAG interface)

Note 1. Magic Packet™ is a registered trademark of Advanced Micro Devices, Inc.
Note 2. The product part number differs according to whether or not it supports encryption.
Note 3. The product part number differs according to whether or not it includes an SDHI (SD host interface) / SDSI (SD slave interface).
Note 4. When the realtime clock is not to be used, initialize the registers in the realtime clock by referring to section 31.6.7, Initialization Procedure When the Realtime Clock is Not to be Used.

No.2 23.2.24 External Bus Control Register (PFBCR0) (Page 809 of 2468)

Bit name of the ADRHMS2 bit is corrected as follows:

Before correction

Bit	Symbol	Bit Name	Description	R/W
		Omitted		
b1	ADRHMS	A16 to A23 Output Enable	See Table 23.20	R/W
b2	ADRHMS2	A16 to A20 Output Enable		R/W
		Omitted		

After correction

Bit	Symbol	Bit Name	Description	R/W
		Omitted		
b1	ADRHMS	A16 to A23 Output Enable	See Table 23.20	R/W
b2	ADRHMS2	A16 to A23 Output Enable 2		R/W
		Omitted		

No.3 41.4 Usage Notes (Page 1955 of 2468)

Title and description of section 41.4.3 are modified as follows:

Before correction

41.4.3 When Using SPI Mode 3 in Single-/Dual-/Quad-SPI Operation

When using the serial flash memory in single-/dual-/quad-SPI operation, set the SPCMDn.CPOL and CPHA bits (n = 0 to 3) to 1 before using SPI mode 3.

After correction

41.4.3 When Using Serial Flash Memory

When using the serial flash memory in dual- or quad-SPI operating mode, set the SPCMDn.CPOL and CPHA bits (n = 0 to 3) to 1 and select SPI mode 3. SPI mode 0 to 2 cannot be used. In addition, set the SPCMDn.SPNDEN, SLNDEN, and SCKDEN bits to 1 to secure delay period.

No.4 43.2.13 SD Error Status Register 1 (SDERSTS1) (Page 1982 of 2468)

Descriptions of b8 to b11 is corrected as follows:

Before correction

Bit	Symbol	Bit Name	Description	R/W
Omitted				
b8	RSPCRCE0	Response CRC Error Flag 0	0: CRC error detected in command *1 response 1: No CRC error detected in command *1 response	R
b9	RSPLENE1	Response CRC Error Flag 1	0: CRC error detected in command *2 response 1: No CRC error detected in command *2 response (by setting the SDCMD.CMDIDX[5:0] bits, the error that occurs by issuing CMD12 is indicated by the RSPCRCE0 flag)	R
b10	RDCRCE	Read Data CRC Error Flag	0: CRC error detected in read data 1: No CRC error detected in read data	R
b11	CRCTKE	CRC Status Token Error Flag	0: Error detected in CRC status token 1: No error detected in CRC status token	R
Omitted				

After correction

Bit	Symbol	Bit Name	Description	R/W
Omitted				
b8	RSPCRCE0	Response CRC Error Flag 0	0: No CRC error detected in command *1 response 1: CRC error detected in command *1 response	R
b9	RSPLENE1	Response CRC Error Flag 1	0: No CRC error detected in command *2 response 1: CRC error detected in command *2 response (the error that occurs for CMD12 with the setting of the SDCMD.CMDIDX[5:0] bits is indicated by the RSPCRCE0 flag)	R
b10	RDCRCE	Read Data CRC Error Flag	0: No CRC error detected in read data 1: CRC error detected in read data	R
b11	CRCTKE	CRC Status Token Error Flag	0: No error detected in CRC status token 1: Error detected in CRC status token	R
Omitted				

No.5 44.1 Overview (Page 2018 of 2468)

Description of line 3 in section 44.1 is modified as follows:

Before correction

frequencies up to 50 MHz, and is thus able to realize superior throughput in 20 Mbytes per second and above.

After correction

frequencies up to 50 MHz, and is thus able to realize superior throughput in 25 Mbytes per second.

No.6 50.1 Overview (Page 2141 of 2468)

Description of operating modes in Table 50.1 is corrected as follows:

Before correction

Operating modes can be set independently for three units.

After correction

Operating modes can be set independently for two units.

No.7 51.3 Operation (Page 2287 of 2468)

Last sentence in (3) in section 51.3 is deleted as follows:

Before correction

(3) If the DADR0 register is written to again, the conversion is started. The conversion result is output after the conversion time tDCONV has elapsed.
When the DAADSCR.DAADST bit is 1 (measure against interference between D/A and A/D conversion is enabled), it takes a maximum of one A/D conversion time for D/A conversion to start. When ADCLK is faster than the peripheral module clock, it may take longer than one A/D conversion time.

After correction

(3) If the DADR0 register is written to again, the conversion is started. The conversion result is output after the conversion time tDCONV has elapsed.
When the DAADSCR.DAADST bit is 1 (measure against interference between D/A and A/D conversion is enabled), it takes a maximum of one A/D conversion time for D/A conversion to start.

No.8 51.3.1 Measure against Interference between D/A and A/D Conversion

Descriptions when ADCLK is faster than the peripheral module clock in section 51.3.1 are deleted.

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The second sentence in (4) in section 51.3.1 is deleted as follows:

Before correction

(4) Set the DADR0 register. When ADCLK is faster than the peripheral module clock, it may take longer than one A/D conversion time for D/A conversion to start.

After correction

(4) Set the DADR0 register.

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The following description and Figure 51.4 in section 51.3.1 are deleted:

When ADCLK is faster than PCLK, the 12-bit D/A converter may not be able to capture a 12-bit A/D converter synchronous D/A conversion enable input signal for one ADCLK cycle which is output between A/D conversion 1 and A/D conversion 2.

Figure 51.4 shows example when the 12-bit D/A converter cannot capture the 12-bit A/D converter synchronous D/A conversion enable input signal. In this case, post-D/A conversion value A is continuously output as the DA0 signal.

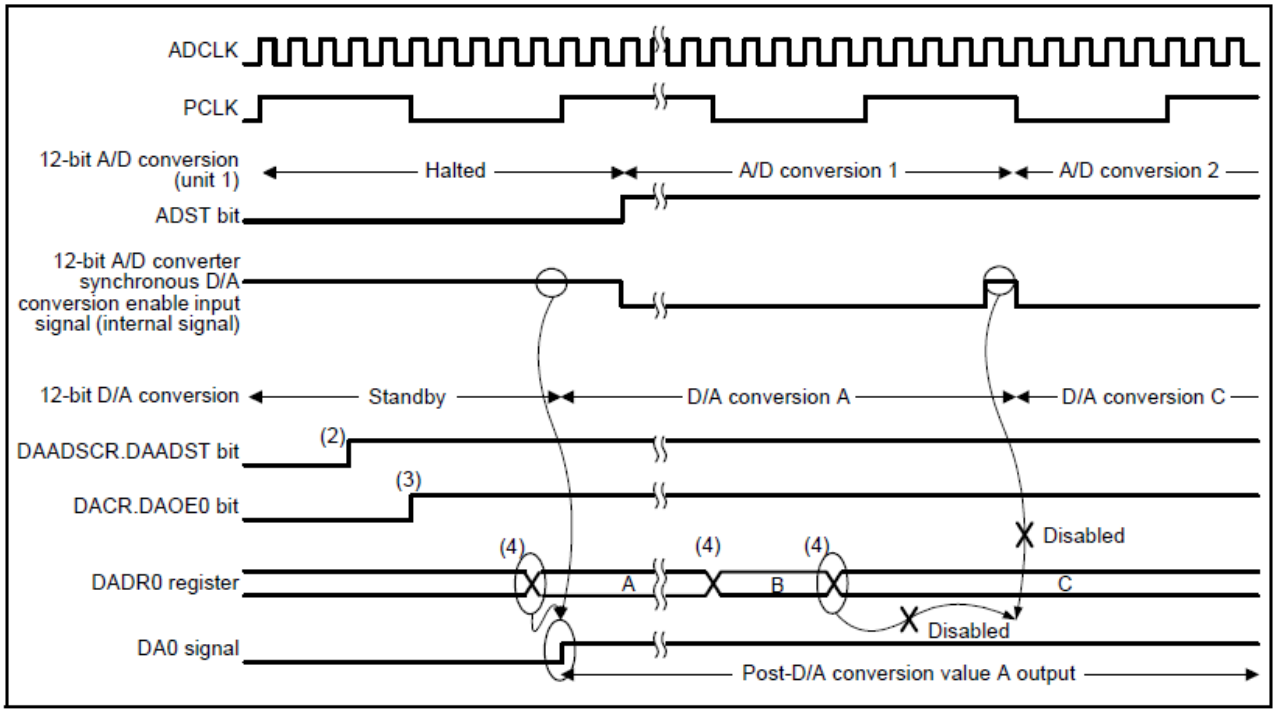

Figure 51.4 Example When the 12-Bit D/A Converter Cannot Capture the 12-Bit A/D Converter Synchronous D/A Conversion Enable Input Signal

No.9 57.2 DC Characteristics (Page 2385 of 2468)

Values of supply current in deep software standby mode are corrected as follows:

Before Correction:

Item				Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Supply current*1	Omitted			I_{CC}*3	Omitted				
	Deep software standby mode	Power supplied to standby RAM and USB resume detecting unit (USB0 only)			—	15.5	51	µA	
		Power not supplied to standby RAM and USB resume detecting unit (USB0 only)	Power-on reset circuit and low-power consumption function disabled*5		—	11.5	29		
			Power-on reset circuit and low-power consumption function enabled*6		—	4.9	20		
		Increased by RTC operation	When a crystal oscillator for low clock loads is in use		—	1	—		
			When a crystal oscillator for standard clock loads is in use		—	2	—		
	Omitted				Omitted				

After Correction

Item				Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Supply current*1	Omitted			I_{CC}*3	Omitted				
	Deep software standby mode	Power supplied to standby RAM and USB resume detecting unit (USB0 only)			—	15.5	61	µA	
		Power not supplied to standby RAM and USB resume detecting unit (USB0 only)	Power-on reset circuit and low-power consumption function disabled*5		—	11.5	38		
			Power-on reset circuit and low-power consumption function enabled*6		—	4.9	29		
		Increased by RTC operation	When a low C_L crystal is in use		—	1	—		
			When a standard C_L crystal is in use		—	2	—		
	Omitted				Omitted				

No.10 57.2 DC Characteristics (Page 2386 of 2468)

Values of reference power supply current in Table 57.6 are corrected as follows:

Before correction

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Omitted							
Reference power supply current	During 12-bit A/D conversion (unit 0)	AI_{REFH}	—	25	40	μA	IVREFH0
	Waiting for 12-bit A/D conversion (unit 0)		—	0.07	0.4	μA	IVREFH0
	12-bit A/D converter in standby mode (unit 0)		—	0.07	0.2	μA	IVREFH0
Omitted							

After correction

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Omitted							
Reference power supply current	During 12-bit A/D conversion (unit 0)	AI_{REFH}	—	38	60	μA	IVREFH0
	Waiting for 12-bit A/D conversion (unit 0)		—	0.07	0.4	μA	IVREFH0
	12-bit A/D converter in standby mode (unit 0)		—	0.07	0.2	μA	IVREFH0
Omitted							

No.11 57.2 DC Characteristics (Page 2386 of 2468)

The following table DC Characteristics (5) is added:

After Correction

Table 57.x DC Characteristics (5)
Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = 2.7 to 3.6 V, 2.7 V ≤ VREFH0 ≤ AVCC0,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = 0 V,
$T_a = T_{opr}$

Item	Package	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Power dissipation*1	PLQP0144KA-B	Pd	—	—	0.383	W	Ta = 85°C
	PLQP0100KB-B		—	—	0.371	W	
	PTLG0145KA-A		—	—	0.459	W	
	PTLG0100JA-A		—	—	0.571	W	

Caution: To ensure the LSI's reliability, do not exceed the values specified in the table above.
Note 1. This is the power consumption of the entire chip including power consumed in the output buffer.

End of document