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RENESAS TECHNICAL UPDATE

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Product Category	MPU/MCU		Document No.	TN-RX*-A170A/E	Rev.	1.00
Title	Errata to RX24T Group User's Manual: Hardware		Information Category	Technical Notification		
Applicable Product	RX24T Group	Lot No. All	Reference Document	RX24T Group User's Manual: Hardware Rev.1.00 (R01UH0576EJ0100)		

This document describes corrections to the RX24T Group User's Manual: Hardware, Rev.1.00.

The corrections are indicated in red as shown below.

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The package code in Table 1.3 is corrected as follows.

Before correction

Table 1.3 List of Products

Group	Part No.	Package	ROM Capacity	RAM Capacity	E2 DataFlash	Operating Frequency (max.)	Operating Temperature
RX24T	R5F524TAADFP	PLQP0100KB-A	256 Kbytes	16 Kbytes	8 Kbytes	80 MHz	–40 to +85°C
	R5F524TAADFF	PLQP0080JA-A					
	R5F524TAADFN	PLQP0080KB-A					
	R5F524T8ADFP	PLQP0100KB-A	128 Kbytes				
	R5F524T8ADFF	PLQP0080JA-A					
	R5F524T8ADFN	PLQP0080KB-A					

After correction

Table 1.3 List of Products

Group	Part No.	Package	ROM Capacity	RAM Capacity	E2 DataFlash	Operating Frequency (max.)	Operating Temperature
RX24T	R5F524TAADFP	PLQP0100KB-B	256 Kbytes	16 Kbytes	8 Kbytes	80 MHz	–40 to +85°C
	R5F524TAADFF	PLQP0080JA-A					
	R5F524TAADFN	PLQP0080KB-B					
	R5F524T8ADFP	PLQP0100KB-B	128 Kbytes				
	R5F524T8ADFF	PLQP0080JA-A					
	R5F524T8ADFN	PLQP0080KB-B					

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Description of the third paragraph in section 20.2.15, Timer General Register (TGR) is corrected as follows.

Before correction

MTU0.TGRE and MTU0.TGRF, and MTU9.TGRE and MTU9.TGRF function as compare registers. When the MTU0.TCNT and MTU9.TCNT count match the MTU0.TGRE value, an A/D converter start request can be issued. The TGRF register can also be designated for operation as a buffer register. TGR buffer register combination is TGRE and TGRF. MTU5.TGRU, MTU5.TGRV, and MTU5.TGRW function as compare match, input capture, or external pulse width measurement registers

After correction

MTU0.TGRE and MTU0.TGRF, and MTU9.TGRE and MTU9.TGRF function as compare registers. When the MTU0.TCNT count matches the MTU0.TGRE value or the MTU9.TCNT count matches the MTU9.TGRE value, an A/D converter start request can be issued. The TGRF register can also be designated for operation as a buffer register. TGR buffer register combination is TGRE and TGRF. MTU5.TGRU, MTU5.TGRV, and MTU5.TGRW function as compare match, input capture, or external pulse width measurement registers.

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Description of the MTU.TSTRA.CSTn bits in section 20.2.17, Timer Start Registers (TSTRA, TSTRB, TSTR) is corrected as follows.

Before correction

CSTn Bits (Counter Start n) (n = 0, 1, 2, 3, 4, 9)

Each bit starts or stops TCNT in the corresponding channel.

If 0 is written to the CSTn bit during operation with the MTIOC pin designated for output, the counter stops but the output compare signal level from the MTIOC pin is retained. If TIOR is written to while the CSTn bit is 0, the pin output level will be changed to the specified initial output value.

After correction

CSTn Bits (Counter Start n) (n = 0, 1, 2, 3, 4, 9)

Each bit starts or stops TCNT in the corresponding channel.

If 0 is written to the CSTn bit during operation with the MTIOC pin designated for output, the counter stops. At this time, initial output level specified in the TOCR1A or TOCR2A register is output from the MTIOC pin in complementary PWM mode or reset-synchronized PWM mode. In any mode other than complementary PWM mode and reset synchronous PWM mode, the output compare signal level from the MTIOC pin is retained. If TIOR is written to while the CSTn bit is 0, the pin output level will be changed to the specified initial output value.

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Description of the MTU.TSTRB.CSTn bits in section 20.2.17, Timer Start Registers (TSTRA, TSTRB, TSTR) is corrected as follows.

Before correction

CSTn Bits (Counter Start n) (n = 6, 7)

Each bit starts or stops TCNT in the corresponding channel.

If 0 is written to the CSTn bit during operation with the MTIOC pin designated for output, the counter stops but the output compare signal level from the MTIOC pin is retained. If TIOR is written to while the CSTn bit is 0, the pin output level will be changed to the specified initial output value.

After correction

CSTn Bits (Counter Start n) (n = 6, 7)

Each bit starts or stops TCNT in the corresponding channel.

If 0 is written to the CSTn bit during operation with the MTIOC pin designated for output, the counter stops. At this time the MTIOC pin output the initial output level set in the TOCR1B or TOCR2B register in complementary PWM mode or reset-synchronized PWM mode, but the output compare signal level from the MTIOC pin is retained in the other modes.

If TIOR is written to while the CSTn bit is 0, the pin output level will be changed to the specified initial output value.

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Description of [3] in Figure 20.42, Procedure for Setting Cascade Connection 32-Bit Phase Counting Mode in section 20.3.6.2 is corrected as follows.

Before correction

[3] Start counting in MTU1 and MTU2 by setting the TSTRA register to 00001111b.

After correction

[3] Start counting in MTU1 and MTU2 by setting the TSTRA.CST1 and CST2 bits to 1 simultaneously.

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Description of the third paragraph in [6] of Figure 20.47, Example of Complementary PWM Mode Setting Procedure in section 20.3.8 (1) is corrected as follows.

Before correction

Only when the double buffer function is used, set the PWM output duty value - 1 in the buffer registers (MTU3.TGRE, MTU4.TGRE, and MTU4.TGRF).

After correction

Only when the double buffer function is used, set the buffer registers (MTU3.TGRE, MTU4.TGRE, and MTU4.TGRF).

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Description of the sixth paragraph in (c), Initial Setting of section 20.3.8 (2) is corrected as follows.

Before correction

Set the respective (initial PWM duty – 1) values in three buffer registers B (MTU3.TGRE, MTU4.TGRE, and MTU4.TGRF (MTU6.TGRE, MTU7.TGRE, and MTU7.TGRF)) only when the double buffer function is used.

After correction

Set three buffer registers B (MTU3.TGRE, MTU4.TGRE, and MTU4.TGRF (MTU6.TGRE, MTU7.TGRE, and MTU7.TGRF)) only when the double buffer function is used.

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The sixth row in Table 20.78 of section 20.3.8 (2) (c) is corrected as follows.

Before correction

MTU3.TGRE, MTU4.TGRE, MTU4.TGRF MTU6.TGRE, MTU7.TGRE, MTU7.TGRF	Initial PWM duty ratio – 1 value for each phase (only when double buffer function is used)

After correction

MTU3.TGRE, MTU4.TGRE, MTU4.TGRF MTU6.TGRE, MTU7.TGRE, MTU7.TGRF	Initial PWM duty ratio value for each phase (only when double buffer function is used)

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The following description is added to section 20.6.5, Contention between TCNT Write and Increment Operations.

After correction

Input capture is performed regardless of occurrence of contention when the count clock of MTU1 or MTU2 is selected for the source of the input capture.

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Descriptions of the OSF1 flag in section 21.2.8, Output Level Control/Status Register 1 (OCSR1) is modified as follows.

Before correction

OSF1 Flag (Output Short Flag 1)

This flag indicates that any one of the three pairs of two-phase MTU3 and MTU4 pins for MTU complementary PWM output to be compared has simultaneously become an active level.

[Setting condition]

- When any one of the three pairs of two-phase outputs has simultaneously become an active level

[Clearing condition]

— omitted —

After correction

OSF1 Flag (Simultaneous Conduction Flag 1)

This flag indicates that at least one of the three pairs of two-phase output pins assigned to ports P71 to P76 for MTU complementary PWM output (MTU3 and MTU4) has simultaneously become at the active level. If the output disabling control for the corresponding pins is not enabled, this flag does not become 1.

For setting the active level, refer to section 21.2.10, Active Level Setting Register 1 (ALR1).

[Setting condition]

- When the MTIOC3B and MTIOC3D pins simultaneously go to the active level[*1] while the value of the POECR2.MTU3BDZE bit is 1.
- When the MTIOC4A and MTIOC4C pins simultaneously go to the active level[*1] while the value of the POECR2.MTU4ACZE bit is 1.
- When the MTIOC4B and MTIOC4D pins simultaneously go to the active level[*1] while the value of the POECR2.MTU4BDZE bit is 1.

Note 1. The setting condition is judged only by the level of the pin regardless the setting of the MPC.PmnPFS register.

[Clearing condition]

— omitted —

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Descriptions of the OSF2 flag in section 21.2.9, Output Level Control/Status Register 2 (OCSR2) is modified as follows.

Before correction

OSF2 Flag (Output Short Flag 2)

This flag indicates that any one of the three pairs of two-phase MTU6 and MTU7 pins for MTU complementary PWM output to be compared has simultaneously become an active level.

[Setting condition]

- When any one of the three pairs of two-phase outputs has simultaneously become an active level

[Clearing condition]

— omitted —

After correction

OSF2 Flag (Simultaneous Conduction Flag 2)

This flag indicates that at least one of the three pairs of two-phase output pins for MTU complementary PWM output (MTU6 and MTU7) has simultaneously become an active level. If the output disabling control for the corresponding pins is not enabled, this flag does not become 1.

For setting the active level, refer to section 21.2.11, Active Level Setting Register 2 (ALR2).

[Setting condition]

- When the MTIOC6B and MTIOC6D pins simultaneously go to the active level[*1] while the value of the POECR2.MTU6BDZE bit is 1.
- When the MTIOC7A and MTIOC7C pins simultaneously go to the active level[*1] while the value of the POECR2.MTU7ACZE bit is 1.
- When the MTIOC7B and MTIOC7D pins simultaneously go to the active level[*1] while the value of the POECR2.MTU7BDZE bit is 1.

Note 1. The setting condition is judged only by the level of the pin regardless the setting of the MPC.PmnPFS register.

[Clearing condition]

— omitted —

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Description of (a) Transmit Processing Flow in section 27.3.10.1 (9) is modified as follows.

Before correction

When transmitting data, the CPU will be notified of the completion of data transmission after the last writing of data for transmission if the SPII interrupt is enabled.

After correction

When transmitting data, the CPU will be notified of the completion of data transmission by enabling the SPI interrupt after the last writing of data for transmission.
The completion of data transmission can also be checked by polling to see if the SPSR.IDLNF flag has become 0, instead of using the SPII interrupt. However, one cycle of PCLK is required for the time from when data for transmission is written in the SPDR register to when the IDLNF flag becomes 1. After the last data is written in the SPDR register, discard the value of the SPSR register once not to judge the condition with the IDLNF flag which has not yet become 1, and read and use the value of the SPSR.IDLNF flag to confirm the completion of data transmission.

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Description of the second paragraph in section 29.6.6, Notes on Entering Low Power Consumption States is corrected as follows.

Before correction

Set the ADCSR.ADST bit to 0 by following the procedure in Figure 29.36 Procedure for Clear Operation by Software through the ADCSR.ADST Bit. Then wait for two clock cycles of ADCLK before entering the module stop mode or software standby mode.

After correction

Set the ADCSR.ADST bit to 0 by following the procedure in Figure 31.36 Procedure for Clear Operation by Software through the ADCSR.ADST Bit. Then wait for three clock cycles of ADCLK before entering the module stop mode or software standby mode.

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Table 35.25 in section 35.3.5, Timing of On-Chip Peripheral Modules is corrected as follows.

Before correction

Item		Symbol	Min.	Max.	Unit*1	Test Conditions
Simple SPI	SCK clock cycle output (master)	t_{SPcyc}	4	65536	t_{Pcyc}	Figure 35.40
	SCK clock cycle input (slave)		6	65536	t_{Pcyc}	
	Omitted					

After correction

Item		Symbol	Min.	Max.	Unit*1	Test Conditions
Simple SPI	SCK clock cycle output (master)	t_{SPcyc}	4	65536	t_{Pcyc}	Figure 35.40
	SCK clock cycle input (slave)		6	—	t_{Pcyc}	
	Omitted					

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Table 35.34 in section 35.7, D/A Conversion Characteristics is modified as follows.

Before correction

Item	Min.	Typ.	Max.	Unit	Test Conditions
Resolution	—	—	8	Bit	
Conversion time	—	—	3.0	µs	
Absolute accuracy	—	—	±3.0	LSB	

After correction

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Resolution	—	—	—	8	Bit	
Conversion time	t_{DCONV}	—	—	3.0	µs	
Absolute accuracy	—	—	—	±3.0	LSB	

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