Date: Oct. 30, 2023

RENESAS TECHNICAL UPDATE

TOYOSU FORESIA, 3-2-24, Toyosu, Koto-ku, Tokyo 135-0061, Japan
Renesas Electronics Corporation

Product Category	MPU/MCU		Document No.	TN-RA*-A0099A/E	Rev.	1.00
Title	The corrections in GPT chapter		Information Category	Technical Notification		
Applicable Product	RA6T2 Group	Lot No. All	Reference Document	Renesas RA6T2 Group User's Manual: Hardware Rev.1.30		

The descriptions of GPT are added as follows.

Before correction

21.2.7 GTCSR : General PWM Timer Clear Source Select Register

(omission)

CSCMSC[2:0] bit (Compare Match/Input Capture/Synchronous counter clearing Source Counter Clear Enable)
Select enable or disable for the counter clear of the GTCNT counter by compare match/input capture/synchronous counter clearing group.
Since the compare match by the register that is performing the buffer operation (including the wave mode specific case) does not occur, the counter clear enable setting that makes the target register of the buffer operation the compare match factor is invalid.
In complementary PWM mode, the counter clear enable setting for compare match of the GTCCRB register, GTCCRE register, and GTCCRF register is invalid even when the buffer operation is not performed.

After correction

21.2.7 GTCSR : General PWM Timer Clear Source Select Register

(omission)

CSCMSC[2:0] bit (Compare Match/Input Capture/Synchronous counter clearing Source Counter Clear Enable)
Select enable or disable for the counter clear of the GTCNT counter by compare match/input capture/synchronous counter clearing group.
If counter clearing by compare match/input capture is enabled, it can be handled as synchronous clearing by inter channel cooperation which is written in section 21.3.8.3.
If this bit is set to "001b" or "010b" and counter clearing by input capture (excluding compare match) is allowed, set the same factor as the input capture factor selected in GTICmSR (m=A, B) register to the counter clearing factor in GTCSR register.
In addition, when the timer prescaler is not used (when GTCR.TPCS[3:0]=0000b), the input capture by other channel factors (set GTICASR.ASOC or GTICBSR.BSOC to "1") can be used as a counter clear factor. The input capture by other channel factors cannot be used as the synchronous clearing factor for other channels but can be used as a counter clearing factor for own channel. In this case, GTCSR configuration is not required.
Since the compare match by the register that is performing the buffer operation (including the wave mode specific case) does not occur, the counter clear enable setting that makes the target register of the buffer operation the compare match factor is invalid.
In complementary PWM mode, the counter clear enable setting for compare match of the GTCCRB register, GTCCRE register, and GTCCRF register is invalid even when the buffer operation is not performed.

Before correction

21.2.12 GTCR : General PWM Timer Control Register

Base address: GPT32n = 0x4016_9000 + 0x0100 × n (n = 0 to 9)
Offset address: 0x2C

Bit position	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	-	-	-	CKEG[1:0]		TPCS[3:0]				-	-	-	MD[3:0]			
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	SSCEN	-	-	CPSCD	SSCGRP[1:0]		SCGTIOC	ICDS	-	-	-	-	-	-	-	CST
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
(omission)			
12	CPSCD	Complementary PWM Mode Synchronous Clear Disable*2 0: Enable synchronous counter clear by other channel other than the section of trough in complementary PWM mode 1: Disable synchronous counter clear by other channel other than the section of trough in complementary PWM mode	R/W*1
(omission)			
19:16	MD[3:0]	Mode Select*3 0 0 0 0: Saw-wave PWM mode 1(single buffer or double buffer possible) (omission)	R/W*1
(omission)			

Note 1. When in complementary PWM mode, no matter which register of master channel/slave channel 1/slave channel 2 is written, three channels are written at the same time.
Note 2. This bit is only available in GPT324 to GPT329.
In GPT320 to GPT323, this bit is read as 0. The write value should be 0.
Note 3. MD[3] bit is only available in GPT324 to GPT329. GPT320 to GPT323 only support Saw-wave PWM mode and Triangle-wave PWM mode except Saw-wave PWM mode 2.

After correction

21.2.12 GTCR : General PWM Timer Control Register

Base address: GPT32n = 0x4016_9000 + 0x0100 × n (n = 0 to 9)
Offset address: 0x2C

Bit position	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	-	-	-	CKEG[1:0]		TPCS[3:0]				-	-	-	MD[3:0]			
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	SSCEN	-	-	-	SSCGRP[1:0]		SCGTIOC	ICDS	-	-	-	-	-	-	-	CST
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
(omission)			
12	-	These bits are read as 0. The write value should be 0.	R/W
(omission)			
19:16	MD[3:0]	Mode Select*2 0 0 0 0: Saw-wave PWM mode 1(single buffer or double buffer possible) (omission)	R/W*1
(omission)			

Note 1. When in complementary PWM mode, no matter which register of master channel/slave channel 1/slave channel 2 is written, three channels are written at the same time.
Note 2. MD[3] bit is only available in GPT324 to GPT329. GPT320 to GPT323 only support Saw-wave PWM mode and Triangle-wave PWM mode except Saw-wave PWM mode 2.

Before correction

Table 21.18 GTPR Buffer Transfer Timing in Complementary PWM Mode

	Complementary PWM mode 1	Complementary PWM mode 2	Complementary PWM mode 3, 4
GTPDBR ↓ Temporary register P	After one GTCLK cycle from GTCCRD register write of slave channel 2 (GPT32n+2)	After one GTCLK cycle from GTCCRD register write of slave channel 2 (GPT32n+2)	After one GTCLK cycle from GTCCRD register write of slave channel 2 (GPT32n+2)
Temporary register P ↓ GTPBR	(1) When data is transferred to temporary register P during upcounting middle section: After one GTCLK cycle from data transfer to temporary register P (2) When data is transferred to temporary register P during a section other than up-counting middle section: At the end of trough section	(1) When data is transferred to temporary register P during down-counting middle section: After one GTCLK cycle from data transfer to temporary register P (2) When data is transferred to temporary register P during a section other than down-counting middle section: At the end of crest section	(1) When data is transferred to temporary register P during middle section: After one GTCLK cycle from data transfer to temporary register P (2) When data is transferred to temporary register P during a section other than middle section: At the end of crest/ trough sections
GTPBR ↓ GTPR	At the end of crest section Synchronous clear	At the end of trough section Synchronous clear	At the end of crest section At the end of trough section Synchronous clear

After correction

Table 21.18 GTPR Buffer Transfer Timing in Complementary PWM Mode

	Complementary PWM mode 1	Complementary PWM mode 2	Complementary PWM mode 3, 4
GTPDBR ↓ Temporary register P	After one GTCLK cycle from GTCCRD register write of slave channel 2 (GPT32n+2)	After one GTCLK cycle from GTCCRD register write of slave channel 2 (GPT32n+2)	After one GTCLK cycle from GTCCRD register write of slave channel 2 (GPT32n+2)
Temporary register P ↓ GTPBR	(1) When data is transferred to temporary register P during upcounting middle section: After one GTCLK cycle from data transfer to temporary register P (2) When data is transferred to temporary register P during a section other than up-counting middle section: At the end of trough section	(1) When data is transferred to temporary register P during down-counting middle section: After one GTCLK cycle from data transfer to temporary register P (2) When data is transferred to temporary register P during a section other than down-counting middle section: At the end of crest section	(1) When data is transferred to temporary register P during middle section: After one GTCLK cycle from data transfer to temporary register P (2) When data is transferred to temporary register P during a section other than middle section: At the end of crest/ trough sections
GTPBR ↓ GTPR	At the end of crest section Counter clear in up-counting middle section and crest section (Including counter clear by setting GTCSR.CP1CCE)	At the end of trough section Counter clear in down-counting middle section and trough section	At the end of crest section At the end of trough section Counter clear

Before correction

21.3.8.3 Synchronous Clear Operation by Inter Channel Cooperation

(omission)

Figure 21.110 shows an example of synchronous clear operation by inter channel cooperation and Table 21.50 shows an example for setting synchronous clear operation by inter channel cooperation.

After correction

21.3.8.3 Synchronous Clear Operation by Inter Channel Cooperation

(omission)

Figure 21.110 shows an example of synchronous clear operation by inter channel cooperation and Table 21.50 shows an example for setting synchronous clear operation by inter channel cooperation.
Table 21.x1 shows synchronous clear factor register setting, and Figure 21.110 shows an example of synchronous clear operation by inter channel cooperation, and Table 21.50 and Table 21.x2 show examples for setting synchronous clear operation by inter channel cooperation.

Table 21.x1 Synchronous clear factor register setting

Synchronous clear factor by inter channel cooperation	Setting register	Setting value
GTCCRA register compare match/input capture	GTINTAD.SCFA	1b
	GTCSR.CSCMSC[2:0]	001b
GTCCRB register compare match/input capture	GTINTAD.SCFB	1b
	GTCSR.CSCMSC[2:0]	010b
GTCCRC register compare match	GTINTAD.SCFC	1b
	GTCSR.CSCMSC[2:0]	011b
GTCCRD register compare match	GTINTAD.SCFD	1b
	GTCSR.CSCMSC[2:0]	100b
GTCCRE register compare match	GTINTAD.SCFE	1b
	GTCSR.CSCMSC[2:0]	101b
GTCCRF register compare match	GTINTAD.SCFF	1b
	GTCSR.CSCMSC[2:0]	110b
Overflow of saw-wave up-count	GTINTAD.SCFPO	1b
Underflow of saw-wave down-count	GTINTAD.SCFPU	1b
Clear caused by GTIOCnA/GTIOCnB pin	GTCR.SCGTIOC	1b

Before correction

Figure 21.110 Example of Synchronous Clear Operation by Inter Channel Cooperation (GPT320 is saw-wave and counter is cleared by the rising edge of the GTIOC0A, GPT321 is triangle wave, GPT324,5,6 are complementary PWM mode. GPT320,1,4,5,6 are the same synchronous set/clear group)

After correction

Figure 21.110 Example of Synchronous Clear Operation by Inter Channel Cooperation
(Clear caused by GTIOCnA/GTIOCnB pin)
(GPT320 is saw-wave and counter is cleared by the rising edge of the GTIOC0A, GPT321 is triangle wave, GPT324,5,6 are complementary PWM mode. GPT320,1,4,5,6 are the same synchronous set/clear group)

Before correction

Table 21.50 Example for Setting Synchronous Clear Operation by Inter Channel Cooperation

No.	Step Name	Description
		(omission)
6	Inter channel cooperation synchronous clear setting (Source channel)	Set the GTINTAD register and GTCR.SCGTIOC bit in the source channel of inter channel cooperation synchronous clear to enable synchronous clear. When complementary PWM mode, set GTINTAD of the master channel. In Figure 21.110, GPT320.GTCR.SCGTIOC bit is 1.
7	Inter channel cooperation synchronous clear setting (Cleared channels)	Set GTCSR.CSCMSC[2:0] bits in the cleared channels of inter channel cooperation synchronous clear to select the counter clear by synchronous counter clearing group. When complementary PWM mode, set GTCSR of the master channel. In Figure 21.110, GTCSR.CSCMSC[2:0] bits of GPT321 and GPT324 is 111b.
8	Set group of inter channel cooperation synchronous clear	Set the same value to GTCR.SSCGRP[1:0] bits in the source channel and cleared channels of inter channel cooperation synchronous clear and set them in the same synchronous set/clear group. When complementary PWM mode, set GTCR of the master channel.
9	Enable inter channel cooperation synchronous clear	Set GTCR.SSCEN bits in the source channel and cleared channels of inter channel cooperation synchronous clear to enable synchronous clear.

After correction

Table 21.50 Example for Setting Synchronous Clear Operation by Inter Channel Cooperation
(Clear caused by GTIOCnA/GTIOCnB pin)

No.	Step Name	Description
		(omission)
6	Inter channel cooperation synchronous clear setting (Source channel)	Set the GTINTAD register, GTCSR.CSCMSC[2:0] bit, and GTCR.SCGTIOC bit in the source channel of inter channel cooperation synchronous clear to enable synchronous clear. When complementary PWM mode, set GTINTAD of the master channel. In Figure 21.110, GPT320.GTCR.SCGTIOC bit is 1.
7	Inter channel cooperation synchronous clear setting (Cleared channels)	Set GTCSR.CSCMSC[2:0] bits in the cleared channels of inter channel cooperation synchronous clear to select the counter clear by synchronous counter clearing group. In Figure 21.110, GTCSR.CSCMSC[2:0] bits of GPT321, GPT324, GPT325, and GPT326 is 111b.
8	Set group of inter channel cooperation synchronous clear	Set the same value to GTCR.SSCGRP[1:0] bits in the source channel and cleared channels of inter channel cooperation synchronous clear and set them in the same synchronous set/clear group. When complementary PWM mode, set GTCR of the master channel.
9	Enable inter channel cooperation synchronous clear	Set GTCR.SSCEN bits in the source channel and cleared channels of inter channel cooperation synchronous clear to enable synchronous clear.

Table 21.x2 Example for Setting Synchronous Clear Operation by Inter Channel Cooperation
(Clear caused by the GTCCRA input capture using the GTIOCnA/GTIOCnB pin)

No.	Step Name	Description
1	Set operating mode	Set the operating mode with the GTCR.MD[2:0] bits or GTCR.MD[3:0] bits.
2	Set count direction	Select the count direction (up or down) with GTUDDTYC.
3	Select count clock	Select the count clock with GTCR.TPCS[3:0] bits of the corresponding channel.
4	Set cycle	Set the cycle in GTPR of the corresponding channel. When complementary PWM mode, set the cycle in GTPR of the master channel.
5	Set initial value for counter	Set the initial value in the GTCNT counter of the corresponding channel.
6	Inter channel cooperation synchronous clear setting (Source channel)	Set the input capture factor using GTIOCnA/B pin to GTICASR and set the same factor as the GTICSASR to the GTCSR as the count clearing factor. In addition, set GTINTAD.SCFA bit = 1b and CTCSR.CSCMSC[2:0] bit = 001b to enable sunchronous clear by the GTCCRA input capture. When complementary PWM mode, set GTINTAD of the master channel.
7	Inter channel cooperation synchronous clear setting (Cleared channels)	Set GTCSR.CSCMSC[2:0] bits in the cleared channels of inter channel cooperation synchronous clear to 111b and select the counter clear by synchronous counter clearing group.
8	Set group of inter channel cooperation synchronous clear	Set the same value to GTCR.SSCGRP[1:0] bits in the source channel and cleared channels of inter channel cooperation synchronous clear and set them in the same synchronous set/clear group. When complementary PWM mode, set GTCR of the master channel.
9	Enable inter channel cooperation synchronous clear	Set GTCR.SSCEN bits in the source channel and cleared channels of inter channel cooperation synchronous clear to enable synchronous clear.

21.3.8.4. Input Capture Operation by Inter Channel Cooperation

The events of compare match, input capture, saw-wave up-count overflow, saw-wave down-count underflow, the crest and trough of triangle-wave and complementary PWM mode and the count clock can be used as the input capture factor for the GTCCRm (m=A or B) of other channels. The input capture factor by inter channel cooperation can be set by the GTICCR of the channel that generates the input capture factor. And input capture by other channel factors can be enable by GTICmSR.mSOC bit(m=A or B) in the captured channels. The channels that generate input capture factors and the channels that are captured are set to the same input capture group by GTICCR.ICmGRP[1:0] bit(m=A or B).

Figure 21.x1 shows an example of input capture operation by inter channel cooperation and Table 21.x3 shows an example for setting input capture operation by inter channel cooperation.

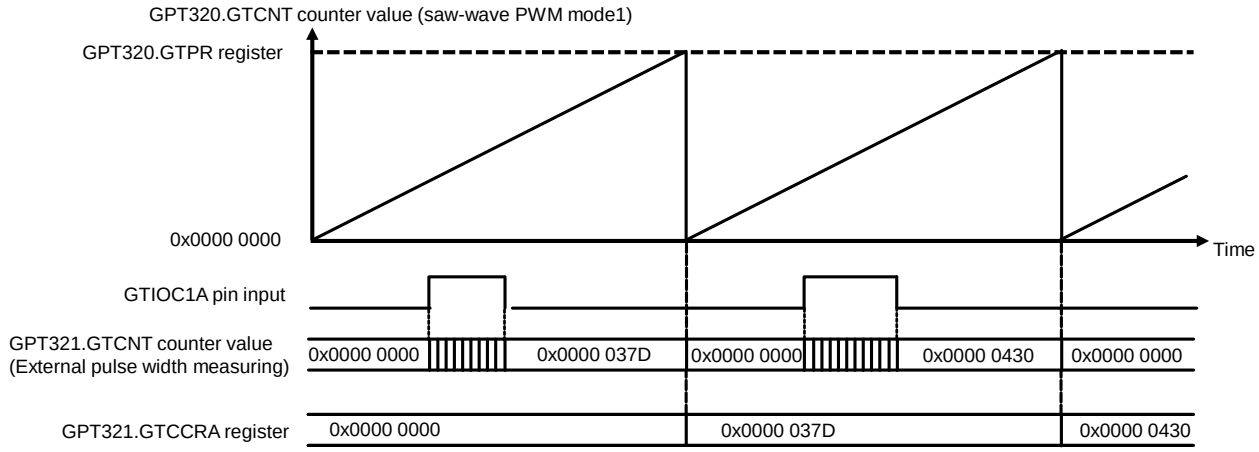

Figure 21.x1 Example of Input Capture Operation by Inter Channel Cooperation (Channel 1 is captured by the overflow of Channel 0)

Table 21.x3 Example for Setting Input Capture Operation by Inter Channel Cooperation

No.	Step Name	Description
1	Set operating mode	Set the operating mode with GTCR.MD[2:0] bits or GTCR.MD[3:0] bits. In Figure 21.x1, 000b or 0000b (saw-wave PWM mode 1) is set to GPT320.
2	Set external pulse width measuring function	Enable external pulse width measuring function with GTUPSR.USILVL[3:0] bits for up-counting operation and GTDNSR.DSILVL[3:0] bits for down-counting operation and select the input pin and level to measure. In Figure 21.x1, GTUPSR.USILVL[3:0] = “0011b” (count up when GTIOCnA pin is 1)
3	Set count direction	Select the count direction (up or down) with GTUDDTYC. In Figure 21.x1, for GPT320,lower 2 bits of GTUDDTYC is set to 11b, and then lower 2 bits of GTUDDTYC is set to 01b (up-counting).
4	Select count clock	Select the count clock with GTCR.TPCS[3:0] bits of the corresponding channel.
5	Set cycle	Set the cycle in GTPR of the corresponding channel. When complementary PWM mode, set the cycle in GTPR of the master channel.
6	Set initial value for counter	Set the initial value in the GTCNT counter of the corresponding channel.
7	Set counter clear factor to the inter channel cooperation input capture (Cleared channels)	Set GTCSR.CSCMSC[2:0] bits in the channel to be cleared by input capture by inter channel cooperation to 001b, 010b, and select input capture as counter clear factor. In figure 21.x1, GPT321.GTCSR.CSCMSC[2:0] bits are 001b.
8	Inter channel cooperation input capture setting (Source channel)	Set the input capture factor using GTICCR in the source channels of inter channel cooperarion input capture. In figure 21.x1, GPT320.GTICCR.ICAFPO bit is 1b.
9	Inter channel cooperation input capture setting (Captured channels)	Set GTICmSR.mSOC bit (m=A or B) in the captured channels to allow input capture to GTCCRm (m=A or B) by other channel factors. In figure 21.x1, GPT321.GTICASR.ASOC bit is 1b.
10	Set group of inter channel cooperation input capture	Set the same value to GTICCR.ICmGRP[1:0] bits (m=A or B) in the source channels and cleared channels of inter channel cooperation input capture and set them in the same input capture group.

Before correction

21.10.3 Setting Range for GTCNT Counter
Other than the Saw-wave PWM mode 2 and Complementary PWM mode, the GTCNT counter register must be set with the range of 0 ≤ GTCNT ≤ GTPR.

21.10.4 Starting and Stopping the GTCNT Counter
The control timing of starting and stopping the GTCNT counter by the GTCR.CST bit synchronizes the count clock that is selected in GTCR.TPCS[3:0]. When GTCR.CST is updated, the GTCNT counter starts/stops after a count clock that is selected in GTCR.TPCS[3:0]. Therefore, an event generated before the GTCNT counter actually starts is ignored, resulting in situations in which an event is accepted or an interrupt occurs after GTCR.CST is set to 0.

After correction

21.10.3 Setting Range for GTCNT Counter
Other than the Saw-wave PWM mode 2 and Complementary PWM mode, the GTCNT counter register must be set with the range of 0 ≤ GTCNT ≤ GTPR.
If GTCNT counter > GTPR register is set and the counter start, the count operation performs following three cases.
(1) In triangle-waves
After the start of counting, GTCNT counter = GTPR register and GTST.TCUF flag = 0 are set, then the counter performs down-counting.
(2) In saw-wave up-counting
After the start of counting, GTCNT counter = 0 is set, then the counter performs up-counting.
(3) In saw-wave down-counting
After the start of counting, once GTCNT counter = 0 is set, next GTCNT counter = GTPR register is set, then the counter performs down-counting.

21.10.x1. Setting Range of GTPBR and GTPDBR in complementary PWM mode
In complementary PWM modes 1, 3, and 4, if GTPR buffer transfer occurs at the end of the crest section, set GTPBR and GTPDBR value to the restricted range(GTPBR≧GTPR-GTDVU, GTPDBR≧GTPR-GTDVU) so that GTPR value after the buffer transfer is not less than GTCNT counter value of the master channel at the end of the crest section. When GTPR buffer transfer occurs at the end of the trough section or clearing counter, there is no restriction on the setting range of GTPBR and GTPDBR.

21.10.4 Starting and Stopping the GTCNT Counter
The control timing of starting and stopping the GTCNT counter by the GTCR.CST bit synchronizes the count clock that is selected in GTCR.TPCS[3:0]. When GTCR.CST is updated, the GTCNT counter starts/stops after a count clock that is selected in GTCR.TPCS[3:0]. Therefore, an event generated before the GTCNT counter actually starts is ignored, resulting in situations in which an event is accepted or an interrupt occurs after GTCR.CST is set to 0.

Before correction

(No description)

After correction

21.10.8. Counter Clear Operation in Complementary PWM Mode
During complementary PWM mode, the counter clear at the end of the trough section including the initial output section (GTCNT count value of the master channel matches the value of GTDVU register) is prohibited. When the counter is cleared in complementary PWM mode, adjust the timing so that counter clearing does not occur at the end of the trough section. By using synchronous clear operation by inter channel cooperation described in 21.3.8.3 and selecting compare match as the counter clearing source, it is possible to avoid the counter clear at the end of the trough section.

21.10.9. Setting Range of the compare match registers when GTIOR.CPSCIR=1
In complementary PWM mode, when GTIOR.CPSCIR=1 and the initial output of GTIOCnA/GTIOCnB pins after synchronization clearing is disabled, set the compare match registers (GTCCRA, GTCCRC, GTCCRD, GTCCRE, GTCCRF) to greater than twice the value of GTDVU.

21.10.10. Prohibit Invalid Register Setting
The register settings that are instructed to be invalid, such as "The setting is invalid during event counting operation", are not guaranteed. These setting is prohibited.