

# RENESAS TECHNICAL UPDATE

1753, Shimonumabe, Nakahara-ku, Kawasaki-shi, Kanagawa 211-8668 Japan  
Renesas Electronics Corporation

Product Category	MPU/MCU		Document No.	TN-SH7-A790A/E	Rev.	1.00
Title	Correction of SH7785 PCI Controller Hardware Manual (2)		Information Category	Technical Notification		
Applicable Product	SH7785 Group	Lot No.	Reference Document	SH7785 Hardware Manual Rev.1.00, Jan.10.2008 (REJ09B0261-0100)		
		All lots				

The SH7785 PCI Controller Hardware Manual has following errata (correction).

Cancellation line part is before correction (removed) and gray part is after correction (added).

[Correction]

1. Add the new section after section 13.4.5(2) as 13.4.5(3), Special Cycle Generation (page 649).

#### 13.4.5(3) Special Cycle Generation

When the PCIC operates as the host device, a special cycle is generated by setting H'8000 FF00 in the PCIPAR and writing to the PCIPDR.

2. Section number is sifted after as follows:

13.4.5(~~3~~)(4) Arbitration

13.4.5(~~4~~)(5) Interrupts

3. Table 13.6 Interrupt Priority: SH7785 Hardware Manual page 650, sifted section number 13.4.5(5)

Signal	Interrupt Source	INTEVT	Priority
:	:	:	High
<del>PCIEERR</del>	A <del>PCIC</del> PCIC error occurs. Generated by PCIIR (except for SDI) and PCIAINT. (Maskable)	H'AA0	↑ ↓
:	:	:	Low

[Note]

The SERR# interrupt must be processed by the PCISERR.

- End of Correction -