Date: Aug. 28, 2023

RENESAS TECHNICAL UPDATE

TOYOSU FORESIA, 3-2-24, Toyosu, Koto-ku, Tokyo 135-0061, Japan
Renesas Electronics Corporation

Product Category	MPU/MCU		Document No.	TN-RL*-A0126A/E	Rev.	1.00
Title	Correction for Incorrect Description Notice RL78/G16 Descriptions in the User's Manual: Hardware Rev. 1.00 Changed		Information Category	Technical Notification		
Applicable Product	RL78/G16 Group	Lot No. All lots	Reference Document	RL78/G16 User's Manual: Hardware Rev. 1.00 R01UH0980EJ0100 (Mar. 2023)		

This document describes misstatements found in the RL78/G16 User's Manual: Hardware Rev. 1.00 (R01UH0980EJ0100).

Corrections

Applicable Item	Applicable Page	Contents
1.1 Features	Page 23 to Page 24	Incorrect descriptions revised
1.3.2 16-pin products	Page 30	Incorrect descriptions revised
1.3.3 20-pin products	Page 31	Incorrect descriptions revised
1.3.4 24-pin products	Page 35	Incorrect descriptions revised
1.3.5 32-pin products	Page 38	Incorrect descriptions revised
4.5.3 Register setting examples for used port and alternate functions	Page154 to Page164	Incorrect descriptions revised
7.3 Registers Controlling Real-time Clock 2	Page 358	Incorrect descriptions revised
15.3.2 CTSU control register 0 (CTSUCR0)	Page 703 to Page 704	Incorrect descriptions revised
15.3.8 CTSU channel enable control register 0 (CTSUCHAC0)	Page 711	Incorrect descriptions revised
15.3.9 CTSU channel enable control register 1 (CTSUCHAC1)	Page 713	Incorrect descriptions revised
15.3.10 CTSU channel transmit/receive control register 0 (CTSUCHTRC0)	Page 715	Incorrect descriptions revised
15.3.11 CTSU channel transmit/receive control register 1 (CTSUCHTRC1)	Page 717	Incorrect descriptions revised
15.3.12 CTSU high-pass noise reduction control register (CTSUDCLKC)	Page 719	Incorrect descriptions revised
15.3.13 CTSU status register (CTSUST)	Page 720	Incorrect descriptions revised
15.3.21 TSCAP pin setting register (VTSEL)	Page 733	Incorrect descriptions revised
20.3.4 SFR guard function	Page 821	Incorrect descriptions revised
20.3.4.1 Invalid memory access detection control register (IAWCTL)	Page 821	Incorrect descriptions revised
20.3.5 Invalid memory access detection	Page 823	Incorrect descriptions revised
20.3.7 Testing of the A/D converter	Page 827	Incorrect descriptions revised
CHAPTER 26 ELECTRICAL SPECIFICATIONS (T_A = −40 to +85°C)	Page 892	Incorrect descriptions revised
26.3.2 Supply current characteristics	Page 898	Incorrect descriptions revised
CHAPTER 27 ELECTRICAL SPECIFICATIONS (T_A = −40 to+105°C, T_A = −40 to +125°C)	Page 916	Incorrect descriptions revised
27.3.2 Supply current characteristics	Page 922 to Page 923	Incorrect descriptions revised

Document Improvement

The above corrections will be made for the next revision of the User's Manual: Hardware.

Corrections in the User's Manual: Hardware

No.	Corrections and Applicable Items			Pages in this document for corrections
	Document No.	English	R01UH0980EJ 0100	
1	1.1 Features		Page 23 to Page 24	Page 3
2	1.3.2 16-pin products		Page 30	Page 3
3	1.3.3 20-pin products		Page 31	Page 4
4	1.3.4 24-pin products		Page 35	Page 4
5	1.3.5 32-pin products		Page 38	Page 4
6	4.5.3 Register setting examples for used port and alternate functions		Page154 to Page164	Page 5 to Page 11
7	7.3 Registers Controlling Real-time Clock 2		Page 358	Page 11
8	15.3.2 CTSU control register 0 (CTSUCR0)		Page 703 to Page 704	Page 12 to Page 13
9	15.3.8 CTSU channel enable control register 0(CTSUCHAC0)		Page 711	Page 14
10	15.3.9 CTSU channel enable control register 1 (CTSUCHAC1)		Page 713	Page 14
11	15.3.10 CTSU channel transmit/receive control register 0 (CTSUCHTRC0)		page 715	Page 14
12	15.3.11 CTSU channel transmit/receive control register 1 (CTSUCHTRC1)		Page 717	Page 15
13	15.3.12 CTSU high-pass noise reduction control register (CTSUDCLKC)		Page 719	Page 15
14	15.3.13 CTSU status register (CTSUST)		Page 720	Page 15
15	15.3.21 TSCAP pin setting register (VTSEL)		Page 733	Page 16
16	20.3.4 SFR guard function		Page 821	Page 16
17	20.3.4.1 Invalid memory access detection control register (IAWCTL)		Page 821	Page 16
18	20.3.5 Invalid memory access detection		Page 823	Page 17 to Page 18
19	20.3.7 Testing of the A/D converter		Page 827	Page 18
20	CHAPTER 26 ELECTRICAL SPECIFICATIONS (T_A = −40 to +85°C)		Page 892	Page 19
21	26.3.2 Supply current characteristics		Page 898	Page 20
22	CHAPTER 27 ELECTRICAL SPECIFICATIONS (T_A = −40 to+105°C, T_A = −40 to +125°C)		Page 916	Page 21
23	27.3.2 Supply current characteristics		Page 922 to Page 923	Page 22 to Page 23

Incorrect: Bold with underline; Correct: Gray hatched

Revision History No,

RL78/G16 Correction for incorrect description notice

Document Number	Issue Date	Description
TN-RL*-A0126A/E	Aug. 28, 2023	First edition issued Corrections No.1 to No.23 revised (this document)

1. 1.1 Features (page 23 to page 24)

Incorrect:

High-speed on-chip oscillator

- Select from 16 MHz, 8 MHz, 4 MHz, 2 MHz, and 1 MHz
- Frequency accuracy ±1.0% (VDD = 2.4 to 5.5 V, TA = −20 to +85°C)
  (G: Industrial applications, M: Industrial applications)
- Frequency accuracy ±1.5% (VDD = 2.4 to 5.5 V, TA = −40 to −20°C)
  (G: Industrial applications, M: Industrial applications)
- **Frequency accuracy ±2.0% (VDD = 2.4 to 5.5 V, TA = +85 to +125°C)**
  (G: Industrial applications, M: Industrial applications)
- Frequency accuracy ±2.0% (VDD = 2.4 to 5.5 V, TA = −40 to +85°C)
  (A: Consumer applications)

(omitted)

Capacitive touch sensing unit (CTSUb)

- 15 channels
- Self-capacitance method: A single pin configures a single key, supporting up to 15 keys
- Mutual capacitance method: **Matrix configuration with 15 pins, supporting up to 56 keys**

2. 1.3.2 16-pin products (page 30)

Incorrect:

・16-pin plastic HWQFN (3 × 3 mm, 0.5-mm pitch)

(omitted)

Remark 1. For pin identification, see 1.4 Pin Identification.

Remark 2. Functions in parentheses can be assigned via settings in the peripheral I/O redirection register (PIOR).Refer to Figure 4-6 Format of Peripheral I/O Redirection Registers 0 to 6 (PIOR0 to PIOR6).

Correct:

High-speed on-chip oscillator

- Select from 16 MHz, 8 MHz, 4 MHz, 2 MHz, and 1 MHz
- Frequency accuracy ±1.0% (VDD = 2.4 to 5.5 V, TA = −20 to +85°C)
  (G: Industrial applications, M: Industrial applications)
- Frequency accuracy ±1.5% (VDD = 2.4 to 5.5 V, TA = −40 to −20°C)
  (G: Industrial applications, M: Industrial applications)
- Frequency accuracy ±1.5% (VDD = 2.4 to 5.5 V, TA = +85 to +105°C)
  (G: Industrial applications)
- Frequency accuracy ±1.5% (VDD = 2.4 to 5.5 V, TA = +85 to +125°C)
  (M: Industrial applications)
- Frequency accuracy ±2.0% (VDD = 2.4 to 5.5 V, TA = −40 to +85°C)
  (A: Consumer applications)

(omitted)

Capacitive touch sensing unit (CTSUb)

- 15 channels
- Self-capacitance method: A single pin configures a single key, supporting up to 15 keys
- Mutual capacitance method: A key can be created with a matrix configuration by selecting transmit/receive pins from 15 pins.

Correct:

・16-pin plastic HWQFN (3 × 3 mm, 0.5-mm pitch)

(omitted)

Remark 1. For pin identification, see 1.4 Pin Identification.

Remark 2. Functions in parentheses can be assigned via settings in the peripheral I/O redirection register (PIOR).Refer to Figure 4-6 Format of Peripheral I/O Redirection Registers 0 to 6 (PIOR0 to PIOR6).

Remark 3. For the product in a QFN package, solder the exposed die pad onto a plated area of the PCB that has no electrical connections.

3. 1.3.3 20-pin products (page 31)

Incorrect:

･20-pin plastic SSOP (4.4 × 5.0 mm, 0.65-mm pitch)

Correct:

･20-pin plastic LSSOP (4.4 × 6.5 mm, 0.65-mm pitch)

4. 1.3.4 24-pin products (page 35)

Incorrect:

･24-pin plastic HWQFN (4 × 4 mm, 0.5-mm pitch)

(omitted)

Remark 1. For pin identification, see 1.4 Pin Identification.

Remark 2. Functions in parentheses can be assigned via settings in the peripheral I/O redirection register (PIOR).Refer to Figure 4-6 Format of Peripheral I/O Redirection Registers 0 to 6 (PIOR0 to PIOR6).

Correct:

･24-pin plastic HWQFN (4 × 4 mm, 0.5-mm pitch)

(omitted)

Remark 1. For pin identification, see 1.4 Pin Identification.

Remark 2. Functions in parentheses can be assigned via settings in the peripheral I/O redirection register (PIOR).Refer to Figure 4-6 Format of Peripheral I/O Redirection Registers 0 to 6 (PIOR0 to PIOR6).

Remark 3. For the product in a QFN package, solder the exposed die pad onto a plated area of the PCB that has no electrical connections.

5. 1.3.5 32-pin products (page 38)

Incorrect:

･32-pin plastic HWQFN (5 × 5 mm, 0.5-mm pitch)
･32-pin plastic LQFP (7 × 7 mm, 0.8-mm pitch)

(omitted)

Remark 1. For pin identification, see 1.4 Pin Identification.

Remark 2. Functions in parentheses can be assigned via settings in the peripheral I/O redirection register (PIOR).Refer to Figure 4-6 Format of Peripheral I/O Redirection Registers 0 to 6 (PIOR0 to PIOR6).

Correct:

･32-pin plastic HWQFN (5 × 5 mm, 0.5-mm pitch)
･32-pin plastic LQFP (7 × 7 mm, 0.8-mm pitch)

(omitted)

Remark 1. For pin identification, see 1.4 Pin Identification.

Remark 2. Functions in parentheses can be assigned via settings in the peripheral I/O redirection register (PIOR).Refer to Figure 4-6 Format of Peripheral I/O Redirection Registers 0 to 6 (PIOR0 to PIOR6).

Remark 3. For the product in a QFN package, solder the exposed die pad onto a plated area of the PCB that has no electrical connections.

6. 4.5.3 Register setting examples for used port and alternate functions (page 154 to Page 164)

Incorrect:

Table 4-8. Setting Examples of Registers and Output Latches When Using Pin Function (1/14)

Pin Name	Used Function		PIORr	POMp	PMCq	PMn	Pm	TSSELt	Alternate Function Output		32-pin	24-pin	20-pin	16-pin	10-pin
	unction Name	I/O							SAU Output Function	Other than SAU					
P00	P00	Input	—	×	—	1	×	—	×	×	✓	✓	✓	✓	✓
		Output	—	0	—	0	0/1	—	TxD0/SO00 = 1 (SCK11/SCL11) = 1 Note 1 SDA11 = 1 Note 3	(TO02) = 0 (SCLA0) = 0 (RTC1HZ) = 0 Note 1					
		N-ch open drain output	—	1	—	0	0/1	—							
	SO00	Output	PIOR21 = 0 PIOR20 = 0	0	—	0	1	—	(SCK11/SCL11) = 1 Note 1 SDA11 = 1 Note 3	(TO02) = 0 (SCLA0) = 0 (RTC1HZ) = 0 Note 1	✓	✓	✓	✓	✓
	TxD0	Output		0/1	—	0	1	—			✓	✓	✓	✓	✓
	(SCK11)	Input	PIOR24 = 0 PIOR23 = 0 PIOR22 = 1	×	—	1	×	—	×	×	✓	✓	✓	✓	—
		Output		0	—	0	1	—	TxD0/SO00 = 1 SDA11 = 1 Note 3	(TO02) = 0 (SCLA0) = 0 (RTC1HZ) = 0 Note 1					
	(SCL11)	Output		0	—	0	1	—			✓	✓	✓	✓	—
	(SCLA0)	I/O	PIOR33 = 1 PIOR32 = 0	1	—	0	0	—	TxD0/SO00 = 1 (SCK11/SCL11) = 1 Note 1 SDA11 = 1 Note 3	(TO02) = 0 (RTC1HZ) = 0 Note 1	✓	✓	✓	✓	✓
	(RTC1HZ)	Output	PIOR67 = 0 PIOR66 = 1	0	—	0	0	—	×	(TO02) = 0 (SCLA0) = 0	✓	✓	✓	✓	—

Correct:

Table 4-8. Setting Examples of Registers and Output Latches When Using Pin Function (1/14)

Pin Name	Used Function		PIORr	POMp	PMCq	PMn	Pm	TSSELt	Alternate Function Output		32-pin	24-pin	20-pin	16-pin	10-pin
	unction Name	I/O							SAU Output Function	Other than SAU					
P00	P00	Input	—	×	—	1	×	—	×	×	✓	✓	✓	✓	✓
		Output	—	0	—	0	0/1	—	TxD0/SO00 = 1 (SCK11/SCL11) = 1 Note 1 SDA11 = 1 Note 3	(TO02) = 0 (SCLA0) = 0 (RTC1HZ) = 0 Note 1					
		N-ch open drain output	—	1	—	0	0/1	—							
	SO00	Output	PIOR21 = 0 PIOR20 = 0	0/1	—	0	1	—	(SCK11/SCL11) = 1 Note 1 SDA11 = 1 Note 3	(TO02) = 0 (SCLA0) = 0 (RTC1HZ) = 0 Note 1	✓	✓	✓	✓	✓
	TxD0	Output		0/1	—	0	1	—			✓	✓	✓	✓	✓
	(SCK11)	Input	PIOR24 = 0 PIOR23 = 0 PIOR22 = 1	×	—	1	×	—	×	×	✓	✓	✓	✓	—
		Output		0/1	—	0	1	—	TxD0/SO00 = 1 SDA11 = 1 Note 3	(TO02) = 0 (SCLA0) = 0 (RTC1HZ) = 0 Note 1					
	(SCL11)	Output		0/1	—	0	1	—			✓	✓	✓	✓	—
	(SCLA0)	I/O	PIOR33 = 1 PIOR32 = 0	1	—	0	0	—	TxD0/SO00 = 1 (SCK11/SCL11) = 1 Note 1 SDA11 = 1 Note 3	(TO02) = 0 (RTC1HZ) = 0 Note 1	✓	✓	✓	✓	✓
	(RTC1HZ)	Output	PIOR67 = 0 PIOR66 = 1	0	—	0	0	—	×	(TO02) = 0 (SCLA0) = 0	✓	✓	✓	✓	—

Incorrect:

Table 4-8. Setting Examples of Registers and Output Latches When Using Pin Function (2/14)

Pin Name	Used Function		PIORr	POMp	PMCq	PMn	Pm	TSSELt	Alternate Function Output		32-pin	24-pin	20-pin	16-pin	10-pin
	unction Name	I/O							SAU Output Function	Other than SAU					
P01	P01	Input	—	×	0	1	×	0	×	×	✓	✓	✓	✓	✓
		Output	—	0	0	0	0/1	0	SDA00 = 1 (SO11) = 1 Note 3 (SDA11) = 1 Note 1	TO02 = 0 (TO01) = 0 (SDAA0) = 0					
		N-ch open drain output	—	1	0	0	0/1	0							
	ANI0	Analog input	—	×	1	1	×	0	×	×	✓	✓	✓	✓	✓
	TS00	I/O	×	0	×	1	0	1	×	×	✓	✓	✓	✓	✓
	INTP5	Input	PIOR51 = 0 PIOR50 = 0	×	≈	1	×	0	×	×	✓	✓	✓	✓	✓
	(SO11)	I/O	PIOR24 = 1 PIOR23 = 0 PIOR22 = 1	0	0	0	1	0	SDA00 = 1 (SDA11) = 1 Note 1	TO02 = 0 (TO01) = 0 (SDAA0) = 0	✓	✓	—	—	—

Correct:

Table 4-8. Setting Examples of Registers and Output Latches When Using Pin Function (2/14)

Pin Name	Used Function		PIORr	POMp	PMCq	PMn	Pm	TSSELt	Alternate Function Output		32-pin	24-pin	20-pin	16-pin	10-pin
	unction Name	I/O							SAU Output Function	Other than SAU					
P01	P01	Input	—	×	0	1	×	0	×	×	✓	✓	✓	✓	✓
		Output	—	0	0	0	0/1	0	SDA00 = 1 (SO11) = 1 Note 3 (SDA11) = 1 Note 1	TO02 = 0 (TO01) = 0 (SDAA0) = 0					
		N-ch open drain output	—	1	0	0	0/1	0							
	ANI0	Analog input	—	×	1	1	×	0	×	×	✓	✓	✓	✓	✓
	TS00	I/O	×	×	×	1	0	1	×	×	✓	✓	✓	✓	✓
	INTP5	Input	PIOR51 = 0 PIOR50 = 0	×	0	1	×	0	×	×	✓	✓	✓	✓	✓
	(SO11)	I/O	PIOR24 = 1 PIOR23 = 0 PIOR22 = 1	0/1	0	0	1	0	SDA00 = 1 (SDA11) = 1 Note 1	TO02 = 0 (TO01) = 0 (SDAA0) = 0	✓	✓	—	—	—

Incorrect:

Table 4-8. Setting Examples of Registers and Output Latches When Using Pin Function (3/14)

Pin Name	Used Function		PIORr	POMp	PMCq	PMn	Pm	TSSELt	Alternate Function Output		32-pin	24-pin	20-pin	16-pin	10-pin
	unction Name	I/O							SAU Output Function	Other than SAU					
P02	P02	Input	—	—	0	1	×	—	×	×	✓	✓	✓	✓	✓
		Output	—	—	0	0	0/1	—	SCK00/SCL00 = 1 (SCK20/SCL20) = 1 Note 4 (SO11) = 1 Note 1	PCLBUZ0 = 0 VCOUT0 = 0 TO01 = 0 (TO02) = 0 Note 1					
	INTP7	Input	PIOR55 = 0 PIOR54 = 0	—	≈	1	×	—	×	×	✓	✓	✓	✓	✓

Incorrect:

Table 4-8. Setting Examples of Registers and Output Latches When Using Pin Function (4/14)

Pin Name	Used Function		PIORr	POMp	PMCq	PMn	Pm	TSSELt	Alternate Function Output		32-pin	24-pin	20-pin	16-pin	10-pin
	unction Name	I/O							SAU Output Function	Other than SAU					
P03	P03	Input	—	×	0	1	×	0	×	×	✓	✓	✓	✓	✓
		Output	—	×	0	0	0/1	0	(SO00/TxD0) = 1 Note 1	TO00 = 0 (TO05) = 0 Note 1 SCLA0 = 0 Note 5					
		N-ch open drain output	—	1	≈	0	0/1	0							
	ANI2	Analog input	—	×	1	1	×	0	×	×	✓	✓	✓	✓	✓
	TS03	I/O	×	0	×	1	0	1	×	×	✓	✓	✓	✓	✓
	(SO00)	Output	PIOR21 = 1 PIOR20 = 0	×	0	0	1	0	×	TO00 = 0	✓	✓	✓	✓	—
	(TxD0)	Output		×	0	0	1	0	×	TO05 = 0 Note 1 SCLA0 = 0 Note 5	✓	✓	✓	✓	—
P04	P04	Input	—	×	0	1	×	0	×	×	✓	✓	✓	✓	✓
		Output	—	×	0	0	0/1	0	(SO00/TxD0) = 1 Note 1 TxD1 = 1 Note 1 (SDA00) = 1 Note 1	TO06 = 0 Note 1 (TO01) = 0 SDAA0 = 0 Note 5					
		N-ch open drain output	—	1	≈	0	0/1	0							
	ANI3	Analog input	—	×	1	1	×	0	×	×	✓	✓	✓	✓	✓
	TS04	I/O	×	0	×	1	0	1	×	×	✓	✓	✓	✓	✓
	(SO00)	Output	PIOR21 = 0 PIOR20 = 1	0	0	0	1	0	(SO00/TxD0) = 1 Note 1 TxD1 = 1 Note 1 (SDA00) = 1 Note 1	TO06 = 0 Note 1 (TO01) = 0 SDAA0 = 0 Note 5	✓	✓	✓	✓	—
	(TxD0)	Output		×	0	0	1	0			✓	✓	✓	✓	—
	TxD1	Output	PIOR31 = 0 PIOR30 = 0	0	0	0	1	0	(SO00/TxD0) = 1 Note 1 (SDA00) = 1 Note 1	TO06 = 0 Note 1 (TO01) = 0 SDAA0 = 0 Note 5	✓	✓	✓	✓	—
	SDAA0	I/O	PIOR32 = 0	1	0	0	0	0	×	TO06 = 0 Note 1 (TO01) = 0	—	—	—	—	✓

Correct:

Table 4-8. Setting Examples of Registers and Output Latches When Using Pin Function (3/14)

Pin Name	Used Function		PIORr	POMp	PMCq	PMn	Pm	TSSELt	Alternate Function Output		32-pin	24-pin	20-pin	16-pin	10-pin
	unction Name	I/O							SAU Output Function	Other than SAU					
P02	P02	Input	—	—	0	1	×	—	×	×	□	□	□	□	□
		Output	—	—	0	0	0/1	—	SCK00/SCL00 = 1 (SCK20/SCL20) = 1 Note 4 (SO11) = 1 Note 1	PCLBUZ0 = 0 VCOUT0 = 0 TO01 = 0 (TO02) = 0 Note 1					
	INTP7	Input	PIOR55 = 0 PIOR54 = 0	—	0	1	×	—	×	×	□	□	□	□	□

Correct:

Table 4-8. Setting Examples of Registers and Output Latches When Using Pin Function (4/14)

Pin Name	Used Function		PIORr	POMp	PMCq	PMn	Pm	TSSELt	Alternate Function Output		32-pin	24-pin	20-pin	16-pin	10-pin
	unction Name	I/O							SAU Output Function	Other than SAU					
P03	P03	Input	—	×	0	1	×	0	×	×	✓	✓	✓	✓	✓
		Output	—	×	0	0	0/1	0	(SO00/TxD0) = 1 Note 1	TO00 = 0 (TO05) = 0 Note 1 SCLA0 = 0 Note 5					
		N-ch open drain output	—	1	0	0	0/1	0							
	ANI2	Analog input	—	×	1	1	×	0	×	×	✓	✓	✓	✓	✓
	TS03	I/O	×	×	×	1	0	1	×	×	✓	✓	✓	✓	✓
	(SO00)	Output	PIOR21 = 1 PIOR20 = 0	0/1	0	0	1	0	×	TO00 = 0	✓	✓	✓	✓	—
	(TxD0)	Output		0/1	0	0	1	0	×	TO05 = 0 Note 1 SCLA0 = 0 Note 5	✓	✓	✓	✓	—
P04	P04	Input	—	×	0	1	×	0	×	×	✓	✓	✓	✓	✓
		Output	—	×	0	0	0/1	0	(SO00/TxD0) = 1 Note 1 TxD1 = 1 Note 1 (SDA00) = 1 Note 1	TO06 = 0 Note 1 (TO01) = 0 SDAA0 = 0 Note 5					
		N-ch open drain output	—	1	0	0	0/1	0							
	ANI3	Analog input	—	×	1	1	×	0	×	×	✓	✓	✓	✓	✓
	TS04	I/O	×	×	×	1	0	1	×	×	✓	✓	✓	✓	✓
	(SO00)	Output	PIOR21 = 0 PIOR20 = 1	0/1	0	0	1	0	(SO00/TxD0) = 1 Note 1 TxD1 = 1 Note 1 (SDA00) = 1 Note 1	TO06 = 0 Note 1 (TO01) = 0 SDAA0 = 0 Note 5	✓	✓	✓	✓	—
	(TxD0)	Output		0/1	0	0	1	0			✓	✓	✓	✓	—
	TxD1	Output	PIOR31 = 0 PIOR30 = 0	0/1	0	0	1	0	(SO00/TxD0) = 1 Note 1 (SDA00) = 1 Note 1	TO06 = 0 Note 1 (TO01) = 0 SDAA0 = 0 Note 5	✓	✓	✓	✓	—
	SDAA0	I/O	PIOR32 = 0	1	0	0	0	0	×	TO06 = 0 Note 1 (TO01) = 0	—	—	—	—	✓

Incorrect:

Table 4-8. Setting Examples of Registers and Output Latches When Using Pin Function (5/14)

Pin Name	Used Function		PIORr	POMp	PMCq	PMn	Pm	TSSELt	Alternate Function Output		32-pin	24-pin	20-pin	16-pin	10-pin
	unction Name	I/O							SAU Output Function	Other than SAU					
P05	P05	Input	—	×	0	1	×	0	×	×	✓	✓	✓	✓	—
		Output	—	0	0	0	0/1	0	SO11 = 1 (SCK00/SCL00) = 1 (SDA00) = 1	(TO02) = 0 (TO07) = 0					
		N-ch open drain output	—	1	≈	0	0/1	0							
	ANI4	Analog input	—	×	1	1	×	0	×	×	✓	✓	✓	✓	—
	TS05	I/O	×	0	×	1	0	1	×	×	✓	✓	✓	✓	—
	SO11	Output	PIOR24 = 0 PIOR23 = 0 PIOR22 = 0	0	0	0	1	0	(SCK00/SCL00) = 1 (SDA00) = 1	(TO02) = 0 (TO07) = 0	✓	✓	✓	✓	—
	(INTP6)	Input	PIOR53 = 0 PIOR52 = 1	×	0	1	×	0	×	×	✓	✓	✓	✓	—
	(SCK00)	Input	PIOR21 = 1 PIOR20 = 0	×	0	1	×	0	×	×	✓	✓	✓	✓	—
		Output		0	0	0	1	0	SO11 = 1 (SDA00) = 1	(TO02) = 0 (TO07) = 0					
	(SCL00)	Output		0	0	0	1	0			✓	✓	✓	✓	—
	(SI00)	Input	PIOR21 = 0 PIOR20 = 1	×	0	1	×	0	×	×	✓	✓	✓	✓	—
	(RxD0)	Input		×	0	1	×	0	×	×	✓	✓	✓	✓	—
	(SDA00)	I/O		1	0	0	1	0	×	×	✓	✓	✓	✓	—
P06	P06	Input	—	×	0	1	×	0	×	×	✓	✓	✓	✓	—
		Output	—	0	0	0	0/1	0	SDA11 = 1 (SCK00/SCL00) = 1	SCLA0 = 0[Note 6] (SCLA0) = 0[Note 3] (TO03) = 0 (PCLBUZ) = 0					
		N-ch open drain output	—	1	0	0	0/1	0							
	ANI5	Analog input	—	×	1	1	×	0	×	×	✓	✓	✓	✓	—
	TS06	I/O	×	0	×	1	0	1	×	×	✓	✓	✓	✓	—
	(SCK00)	Input	PIOR21 = 0 PIOR20 = 1	×	0	1	×	0	×	×	✓	✓	✓	✓	—
		Output		0	0	0	1	0	SDA11 = 1	SCLA0 = 0[Note 6] (SCLA0) = 0[Note 3] (TO03) = 0 (PCLBUZ) = 0	✓	✓	✓	✓	—
	(SCL00)	Output		0	0	0	1	0			✓	✓	✓	✓	—

Correct:

Table 4-8. Setting Examples of Registers and Output Latches When Using Pin Function (5/14)

Pin Name	Used Function		PIORr	POMp	PMCq	PMn	Pm	TSSELt	Alternate Function Output		32-pin	24-pin	20-pin	16-pin	10-pin
	unction Name	I/O							SAU Output Function	Other than SAU					
P05	P05	Input	—	×	0	1	×	0	×	×	✓	✓	✓	✓	—
		Output	—	0	0	0	0/1	0	SO11 = 1 (SCK00/SCL00) = 1 (SDA00) = 1	(TO02) = 0 (TO07) = 0					
		N-ch open drain output	—	1	0	0	0/1	0							
	ANI4	Analog input	—	×	1	1	×	0	×	×	✓	✓	✓	✓	—
	TS05	I/O	×	×	×	1	0	1	×	×	✓	✓	✓	✓	—
	SO11	Output	PIOR24 = 0 PIOR23 = 0 PIOR22 = 0	0/1	0	0	1	0	(SCK00/SCL00) = 1 (SDA00) = 1	(TO02) = 0 (TO07) = 0	✓	✓	✓	✓	—
	(INTP6)	Input	PIOR53 = 0 PIOR52 = 1	×	0	1	×	0	×	×	✓	✓	✓	✓	—
	(SCK00)	Input	PIOR21 = 1 PIOR20 = 0	×	0	1	×	0	×	×	✓	✓	✓	✓	—
		Output		0/1	0	0	1	0	SO11 = 1 (SDA00) = 1	(TO02) = 0 (TO07) = 0					
	(SCL00)	Output		0/1	0	0	1	0			✓	✓	✓	✓	—
	(SI00)	Input	PIOR21 = 0 PIOR20 = 1	×	0	1	×	0	×	×	✓	✓	✓	✓	—
	(RxD0)	Input		×	0	1	×	0	×	×	✓	✓	✓	✓	—
	(SDA00)	I/O		1	0	0	1	0	×	×	✓	✓	✓	✓	—
P06	P06	Input	—	×	0	1	×	0	×	×	✓	✓	✓	✓	—
		Output	—	0	0	0	0/1	0	SDA11 = 1 (SCK00/SCL00) = 1	SCLA0 = 0[Note 6] (SCLA0) = 0[Note 3] (TO03) = 0 (PCLBUZ) = 0					
		N-ch open drain output	—	1	0	0	0/1	0							
	ANI5	Analog input	—	×	1	1	×	0	×	×	✓	✓	✓	✓	—
	TS06	I/O	×	×	×	1	0	1	×	×	✓	✓	✓	✓	—
	(SCK00)	Input	PIOR21 = 0 PIOR20 = 1	×	0	1	×	0	×	×	✓	✓	✓	✓	—
		Output		0/1	0	0	1	0	SDA11 = 1	SCLA0 = 0[Note 6] (SCLA0) = 0[Note 3] (TO03) = 0 (PCLBUZ) = 0	✓	✓	✓	✓	—
	(SCL00)	Output		0/1	0	0	1	0			✓	✓	✓	✓	—

Incorrect:

Table 4-8. Setting Examples of Registers and Output Latches When Using Pin Function (6/14)

Pin Name	Used Function		PIORr	POMp	PMCq	PMn	Pm	TSSELt	Alternate Function Output		32-pin	24-pin	20-pin	16-pin	10-pin
	unction Name	I/O							SAU Output Function	Other than SAU					
P07	P07	Input	—	×	0	1	×	0	×	×	✓	✓	✓	✓	—
		Output	—	0	0	0	0/1	0	SCK11/SCL11 = 1	VCOUT1 = 0					
		N-ch open drain output	—	1	0	0	0/1	0		(TO03) = 0 TO04 = 0 SDAA0 = 0Note 6 (SDAA0) = 0Note 3					
	ANI6	Analog input	—	×	1	1	×	0	×	×	✓	✓	✓	✓	—
	TS07	I/O	×	0	×	1	0	1	×	×	✓	✓	✓	✓	—
	TI04	Input	PIOR14 = 0	×	0	1	×	0	×	×	✓	✓	✓	✓	—
	TO04	Output	PIOR13 = 0	×	0	0	0	0	×	VCOUT1 = 0 (TO03) = 0 SDAA0 = 0Note 6 (SDAA0) = 0Note 3	✓	✓	✓	✓	—
	(TO03)	Output	PIOR12 = 0 PIOR11 = 0 PIOR10 = 1	0	0	0	0	0	×	VCOUT1 = 0 TO04 = 0 SDAA0 = 0Note 6 (SDAA0) = 0Note 3	✓	✓	✓	✓	—
	SCK11	Input	PIOR24 = 0	×	0	1	×	0	×	×	✓	✓	✓	✓	—
		Output	PIOR23 = 0 PIOR22 = 0	0	0	0	1	0	×	VCOUT1 = 0 (TO03) = 0 TO04 = 0 SDAA0 = 0Note 6 (SDAA0) = 0Note 3					
	SCL11	Output	PIOR24 = 0 PIOR23 = 0 PIOR22 = 0	0	0	0	1	0			✓	✓	✓	✓	—
	SDAA0	I/O	PIOR32 = 0	1	0	0	0	0	×	VCOUT1 = 0 (TO03) = 0 TO04 = 0	—	—	✓	✓	—
	(SDAA0)	I/O	PIOR33 = 0 PIOR32 = 1	1	0	0	0	0	×	VCOUT1 = 0 (TO03) = 0 TO04 = 0	✓	✓	—	—	—
	VCOUT1	Output	PIOR65 = 0 PIOR64 = 0 PIOR63 = 0	×	0	0	0	0	×	(TO03) = 0 TO04 = 0 SDAA0 = 0Note 6 (SDAA0) = 0Note 3	✓	✓	✓	✓	—

Correct:

Table 4-8. Setting Examples of Registers and Output Latches When Using Pin Function (6/14)

Pin Name	Used Function		PIORr	POMp	PMCq	PMn	Pm	TSSELt	Alternate Function Output		32-pin	24-pin	20-pin	16-pin	10-pin
	unction Name	I/O							SAU Output Function	Other than SAU					
P07	P07	Input	—	×	0	1	×	0	×	×	✓	✓	✓	✓	—
		Output	—	0	0	0	0/1	0	SCK11/SCL11 = 1	VCOUT1 = 0					
		N-ch open drain output	—	1	0	0	0/1	0		(TO03) = 0 TO04 = 0 SDAA0 = 0Note 6 (SDAA0) = 0Note 3					
	ANI6	Analog input	—	×	1	1	×	0	×	×	✓	✓	✓	✓	—
	TS07	I/O	×	×	×	1	0	1	×	×	✓	✓	✓	✓	—
	TI04	Input	PIOR14 = 0	×	0	1	×	0	×	×	✓	✓	✓	✓	—
	TO04	Output	PIOR13 = 0	0	0	0	0	0	×	VCOUT1 = 0 (TO03) = 0 SDAA0 = 0Note 6 (SDAA0) = 0Note 3	✓	✓	✓	✓	—
	(TO03)	Output	PIOR12 = 0 PIOR11 = 0 PIOR10 = 1	0	0	0	0	0	×	VCOUT1 = 0 TO04 = 0 SDAA0 = 0Note 6 (SDAA0) = 0Note 3	✓	✓	✓	✓	—
	SCK11	Input	PIOR24 = 0	×	0	1	×	0	×	×	✓	✓	✓	✓	—
		Output	PIOR23 = 0 PIOR22 = 0	0/1	0	0	1	0	×	VCOUT1 = 0 (TO03) = 0 TO04 = 0 SDAA0 = 0Note 6 (SDAA0) = 0Note 3					
	SCL11	Output	PIOR24 = 0 PIOR23 = 0 PIOR22 = 0	0/1	0	0	1	0			✓	✓	✓	✓	—
	SDAA0	I/O	PIOR32 = 0	1	0	0	0	0	×	VCOUT1 = 0 (TO03) = 0 TO04 = 0	—	—	✓	✓	—
	(SDAA0)	I/O	PIOR33 = 0 PIOR32 = 1	1	0	0	0	0	×	VCOUT1 = 0 (TO03) = 0 TO04 = 0	✓	✓	—	—	—
	VCOUT1	Output	PIOR65 = 0 PIOR64 = 0 PIOR63 = 0	0	0	0	0	0	×	(TO03) = 0 TO04 = 0 SDAA0 = 0Note 6 (SDAA0) = 0Note 3	✓	✓	✓	✓	—

Incorrect:

Table 4-8. Setting Examples of Registers and Output Latches When Using Pin Function (8/14)

Pin Name	Used Function		PIORr	POMp	PMCq	PMn	Pm	TSSELt	Alternate Function Output		32-pin	24-pin	20-pin	16-pin	10-pin
	unction Name	I/O							SAU Output Function	Other than SAU					
P15	P15	Input	—	—	—	1	×	—	×	×	✓	—	—	—	—
		Output	—	—	—	0	0/1	—	(SO11) = 1 (SO20/TxD2) = 1	×					
P16	P16	Input	—	×	—	1	×	×	×	×	✓	—	—	—	—
		Output	—	0	—	0	0/1	0	(SDA20) = 1	(TO03) = 0 (SCLA0) = 0					
		N-ch open drain output	—	1	—	0	0/1	0							
	TS01	I/O	×	**0**	—	1	0	1	×	×	✓	—	—	—	—
P17	P17	Input	—	×	—	1	×	×	×	×	✓	—	—	—	—
		Output	—	0	—	0	0/1	0	(SO20/TxD2) = 1	(TO04) = 0 (SDAA0) = 0					
		N-ch open drain output	—	1	—	0	0/1	0							
	TS02	I/O	×	**0**	—	1	0	1	×	×	✓	—	—	—	—
	(TI04)	Input	PIOR14 = 1 PIOR13 = 0	×	—	1	×	0	×	×	✓	—	—	—	—
	(TO04)	Output		0	—	0	0	0	×	(SDAA0) = 0	✓	—	—	—	—
	(TxD2)	Output	PIOR26 = 0 PIOR25 = 1	**0**	—	0	1	0	×	(TO04) = 0 (SDAA0) = 0	✓	—	—	—	—
	(SO20)	Output		**×**	—	0	1	0			✓	—	—	—	—
	(SDAA0)	I/O	PIOR33 = 1 PIOR32 = 1	1	—	0	0	0	×	(TO04) = 0	✓	—	—	—	—

Correct:

Table 4-8. Setting Examples of Registers and Output Latches When Using Pin Function (8/14)

Pin Name	Used Function		PIORr	POMp	PMCq	PMn	Pm	TSSELt	Alternate Function Output		32-pin	24-pin	20-pin	16-pin	10-pin
	unction Name	I/O							SAU Output Function	Other than SAU					
P15	P15	Input	—	—	—	1	×	—	×	×	✓	—	—	—	—
		Output	—	—	—	0	0/1	—	(SO11) = 1 (SO20/TxD2) = 1	×					
P16	P16	Input	—	×	—	1	×	×	×	×	✓	—	—	—	—
		Output	—	0	—	0	0/1	0	(SDA20) = 1	(TO03) = 0 (SCLA0) = 0					
		N-ch open drain output	—	1	—	0	0/1	0							
	TS01	I/O	×	×	—	1	0	1	×	×	✓	—	—	—	—
P17	P17	Input	—	×	—	1	×	×	×	×	✓	—	—	—	—
		Output	—	0	—	0	0/1	0	(SO20/TxD2) = 1	(TO04) = 0 (SDAA0) = 0					
		N-ch open drain output	—	1	—	0	0/1	0							
	TS02	I/O	×	×	—	1	0	1	×	×	✓	—	—	—	—
	(TI04)	Input	PIOR14 = 1 PIOR13 = 0	×	—	1	×	0	×	×	✓	—	—	—	—
	(TO04)	Output		0	—	0	0	0	×	(SDAA0) = 0	✓	—	—	—	—
	(TxD2)	Output	PIOR26 = 0 PIOR25 = 1	0/1	—	0	1	0	×	(TO04) = 0 (SDAA0) = 0	✓	—	—	—	—
	(SO20)	Output		0/1	—	0	1	0			✓	—	—	—	—
	(SDAA0)	I/O	PIOR33 = 1 PIOR32 = 1	1	—	0	0	0	×	(TO04) = 0	✓	—	—	—	—

Incorrect:

Table 4-8. Setting Examples of Registers and Output Latches When Using Pin Function (9/14)

Pin Name	Used Function		PIORr	POMp	PMCq	PMn	Pm	TSSELt	Alternate Function Output		32-pin	24-pin	20-pin	16-pin	10-pin
	unction Name	I/O							SAU Output Function	Other than SAU					
P20	P20	Input	—	×	0	1	×	0	×	×	✓	✓	✓	—	—
		Output	—	0	0	0	0/1	0	(SCK11/SCL11) = 1	(TO00) = 0	✓	✓	✓	—	—
		N-ch open drain output	—	1	0	0	0/1	0	(TxD1) = 1 SDA20 = 1	(TO03) = 0	✓	✓	✓	—	—
	(SCK11)	Input	PIOR24 = 0 PIOR23 = 1 PIOR22 = 0	×	0	1	×	0	×	×	✓	✓	✓	—	—
		Output		0	0	0	1	0	×	(TO00) = 0	✓	✓	✓	—	—
	(SCL11)	Output		0	0	0	1	0		(TO03) = 0	✓	✓	✓	—	—
	(RxD1)	Input	PIOR31 = 1 PIOR30 = 1	×	0	1	×	0	×	×	✓	—	—	—	—
	(TxD1)	Output	PIOR31 = 0 PIOR30 = 1	0	0	0	1	0	(SCK11/SCL11) = 1 SDA20 = 1	(TO00) = 0 (TO03) = 0	✓	✓	✓	—	—
	TS11	I/O	×	0	×	1	0	1	×	×	✓	✓	✓	—	—
P21	P21	Input	—	—	0	1	×	0	×	×	✓	✓	✓	—	—
		Output	—	—	0	0	0/1	0	SO20/TxD2 = 1	(TO00) = 0	✓	✓	✓	—	—
	ANI9	Analog input	—	—	1	1	×	0	×	×	✓	✓	✓	—	—
	(INTP7)	Input	PIOR55 = 1 PIOR54 = 0	—	≈	1	×	0	×	×	✓	✓	✓	—	—
	(TO00)	Output	PIOR01 = 1 PIOR00 = 0	—	≈	0	0	0	×	×	✓	✓	✓	—	—
	(RxD1)	Input	PIOR31 = 0 PIOR30 = 1	—	0	1	×	0	×	×	✓	✓	✓	—	—
	SO20	Output	PIOR26 = 0 PIOR25 = 0	—	0	0	1	0	×	(TO00) = 0	✓	✓	✓	—	—
	TxD2	Output	PIOR26 = 0 PIOR25 = 0	—	≈	0	1	0	×	(TO00) = 0	✓	✓	✓	—	—
	TS10	I/O	×	—	×	1	0	1	×	×	✓	✓	✓	—	—

Incorrect:

Table 4-8. Setting Examples of Registers and Output Latches When Using Pin Function (10/14)

Pin Name	Used Function		PIORr	POMp	PMCq	PMn	Pm	TSSELt	Alternate Function Output		32-pin	24-pin	20-pin	16-pin	10-pin
	unction Name	I/O							SAU Output Function	Other than SAU					
P23	P23	Input	—	×	0	1	×	0	×	×	✓	✓	✓	—	—
		Output	—	—	0	0	0/1	0	(SCL11) = 1	(TO04) = 1	✓	✓	✓	—	—

Correct:

Table 4-8. Setting Examples of Registers and Output Latches When Using Pin Function (9/14)

Pin Name	Used Function		PIORr	POMp	PMCq	PMn	Pm	TSSELt	Alternate Function Output		32-pin	24-pin	20-pin	16-pin	10-pin
	unction Name	I/O							SAU Output Function	Other than SAU					
P20	P20	Input	—	×	0	1	×	0	×	×	✓	✓	✓	—	—
		Output	—	0	0	0	0/1	0	(SCK11/SCL11) = 1	(TO00) = 0	✓	✓	✓	—	—
		N-ch open drain output	—	1	0	0	0/1	0	(TxD1) = 1 SDA20 = 1	(TO03) = 0	✓	✓	✓	—	—
	(SCK11)	Input	PIOR24 = 0 PIOR23 = 1 PIOR22 = 0	×	0	1	×	0	×	×	✓	✓	✓	—	—
		Output		0/1	0	0	1	0	×	(TO00) = 0	✓	✓	✓	—	—
	(SCL11)	Output		0/1	0	0	1	0		(TO03) = 0	✓	✓	✓	—	—
	(RxD1)	Input	PIOR31 = 1 PIOR30 = 1	×	0	1	×	0	×	×	✓	—	—	—	—
	(TxD1)	Output	PIOR31 = 0 PIOR30 = 1	0/1	0	0	1	0	(SCK11/SCL11) = 1 SDA20 = 1	(TO00) = 0 (TO03) = 0	✓	✓	✓	—	—
	TS11	I/O	×	×	×	1	0	1	×	×	✓	✓	✓	—	—
P21	P21	Input	—	—	0	1	×	0	×	×	✓	✓	✓	—	—
		Output	—	—	0	0	0/1	0	SO20/TxD2 = 1	(TO00) = 0	✓	✓	✓	—	—
	ANI9	Analog input	—	—	1	1	×	0	×	×	✓	✓	✓	—	—
	(INTP7)	Input	PIOR55 = 1 PIOR54 = 0	—	0	1	×	0	×	×	✓	✓	✓	—	—
	(TO00)	Output	PIOR01 = 1 PIOR00 = 0	—	0	0	0	0	×	×	✓	✓	✓	—	—
	(RxD1)	Input	PIOR31 = 0 PIOR30 = 1	—	0	1	×	0	×	×	✓	✓	✓	—	—
	SO20	Output	PIOR26 = 0 PIOR25 = 0	—	0	0	1	0	×	(TO00) = 0	✓	✓	✓	—	—
	TxD2	Output	PIOR26 = 0 PIOR25 = 0	—	0	0	1	0	×	(TO00) = 0	✓	✓	✓	—	—
	TS10	I/O	×	—	×	1	0	1	×	×	✓	✓	✓	—	—

Correct:

Table 4-8. Setting Examples of Registers and Output Latches When Using Pin Function (10/14)

Pin Name	Used Function		PIORr	POMp	PMCq	PMn	Pm	TSSELt	Alternate Function Output		32-pin	24-pin	20-pin	16-pin	10-pin
	unction Name	I/O							SAU Output Function	Other than SAU					
P23	P23	Input	—	—	0	1	×	0	×	×	✓	✓	✓	—	—
		Output	—	—	0	0	0/1	0	(SCL11) = 1	(TO04) = 1	✓	✓	✓	—	—

Incorrect:

Table 4-8. Setting Examples of Registers and Output Latches When Using Pin Function (11/14)

Pin Name	Used Function		PIORr	POMp	PMCq	PMn	Pm	TSSELt	Alternate Function Output		32-pin	24-pin	20-pin	16-pin	10-pin
	unction Name	I/O							SAU Output Function	Other than SAU					
P41	P41	Input	—	×	—	1	×	0	×	×	✓	✓	✓	✓	—
		Output	—	0	—	0	0/1	0	SCK20/SCL20 = 1[Note 2] (SO11) = 1[Note 2] (SDA11) = 1[Note 2]	TO03 = 0 (TO02) = 0 RTC1HZ = 0 (VCOUT0) = 0 (VCOUT1) = 0	✓	✓	✓	✓	—
		N-ch open drain output	—	1	—	0	0/1	0			✓	✓	✓	✓	—
	(SO11)	Output	PIOR24 = 0 PIOR23 = 1 PIOR22 = 0	×	—	0	1	0	SCK20/SCL20 = 1[Note 2]	TO03 = 0 (TO02) = 0 RTC1HZ = 0 (VCOUT0) = 0 (VCOUT1) = 0	✓	✓	✓	—	—
	(SDA11)	I/O		1	—	0	1	0	SCK20/SCL20 = 1[Note 2]	TO03 = 0 (TO02) = 0 RTC1HZ = 0 (VCOUT0) = 0 (VCOUT1) = 0	✓	✓	✓	—	—
	SCK20	Input	PIOR26 = 0 PIOR25 = 0	×	—	1	×	—	×	×	✓	✓	✓	—	—
		Output		0	—	0	1	—	(SO11) = 1[Note 2] (SDA11) = 1[Note 2]	TO03 = 0 (TO02) = 0 RTC1HZ = 0 (VCOUT0) = 0 (VCOUT1) = 0	✓	✓	✓	—	—
	SCL20	Output		0	—	0	1	—			✓	✓	✓	—	—

Correct:

Table 4-8. Setting Examples of Registers and Output Latches When Using Pin Function (11/14)

Pin Name	Used Function		PIORr	POMp	PMCq	PMn	Pm	TSSELt	Alternate Function Output		32-pin	24-pin	20-pin	16-pin	10-pin
	unction Name	I/O							SAU Output Function	Other than SAU					
P41	P41	Input	—	×	—	1	×	0	×	×	✓	✓	✓	✓	—
		Output	—	0	—	0	0/1	0	SCK20/SCL20 = 1[Note 2] (SO11) = 1[Note 2] (SDA11) = 1[Note 2]	TO03 = 0 (TO02) = 0 RTC1HZ = 0 (VCOUT0) = 0 (VCOUT1) = 0	✓	✓	✓	✓	—
		N-ch open drain output	—	1	—	0	0/1	0			✓	✓	✓	✓	—
	(SO11)	Output	PIOR24 = 0 PIOR23 = 1 PIOR22 = 0	0/1	—	0	1	0	SCK20/SCL20 = 1[Note 2]	TO03 = 0 (TO02) = 0 RTC1HZ = 0 (VCOUT0) = 0 (VCOUT1) = 0	✓	✓	✓	—	—
	(SDA11)	I/O		1	—	0	1	0	SCK20/SCL20 = 1[Note 2]	TO03 = 0 (TO02) = 0 RTC1HZ = 0 (VCOUT0) = 0 (VCOUT1) = 0	✓	✓	✓	—	—
	SCK20	Input	PIOR26 = 0 PIOR25 = 0	×	—	1	×	—	×	×	✓	✓	✓	—	—
		Output		0/1	—	0	1	—	(SO11) = 1[Note 2] (SDA11) = 1[Note 2]	TO03 = 0 (TO02) = 0 RTC1HZ = 0 (VCOUT0) = 0 (VCOUT1) = 0	✓	✓	✓	—	—
	SCL20	Output		0/1	—	0	1	—			✓	✓	✓	—	—

7. 7.3 Registers Controlling Real-time Clock 2 (page 358)

Incorrect:

The following shows the register states depending on reset sources.

Reset Source	System Registers[Note 1]	Calendar Registers[Note 2]
Internal reset by data retention power supply voltage	Reset	Not reset
External reset	Retained	Retained
WDT	Retained	Retained
TRAP	Retained	Retained
LVD	Retained	Retained
Other internal reset	Retained	Retained

(omitted)

Correct:

The following shows the register states depending on reset sources.

Reset Source	System Registers[Note 1]	Calendar Registers[Note 2]
Internal reset by data retention power supply voltage	Reset	Not reset
External reset	Retained	Retained
WDT	Retained	Retained
TRAP	Retained	Retained
SPOR	Retained	Retained
Other internal reset	Retained	Retained

(omitted)

8. 15.3.2 CTSU control register 0 (CTSUCR0) (page 703 to page 704)

Incorrect:

Figure 15-5. Format of CTSU Control Register 0 (CTSUCR0) (2/3)

CTSUSNZ	CTSU suspension enable[Note 3]
0	Suspension is disabled.
1	Suspension is enabled.

This bit enables or disables suspension when the external trigger (an interval interrupt signal from the 12-bit interval timer) is selected (the CTSUCAP bit = 1). This bit can be used to suspend the CTSU, which decreases power consumption during the wait state.
The CTSU state changes as follows depending on the register setting.

CTSUPON Bit in CTSUCR1 Register	CTSUSNZ Bit	CTSUCAP Bit	CTSUSTRT Bit	External Trigger	CTSU State
0	0	0	0	—	Stopped
1	0	—	—	—	Operating
1	1	1	0	—	Suspended
1	1	1	1	Not detected	Suspended
1	1	1	1	Detection of rising edges	Operating
1	1	0	0	—	SW suspended
Other than the above					Setting prohibited

"Suspended" refers to the state in which the capacitor of the external low-pass filter connected to the TSCAP pin is not being charged.
"SW suspended" refers to the state of suspension initiated in response to the software trigger when the software trigger has been selected by setting the CTSUCAP bit to 0. To start measurement from the SW suspended state, set the CTSUSNZ bit to 0 and wait for 16 µs before setting the CTSUSTRT bit to 1. To return the CTSU to the SW suspended state again after measurement is finished, set the CTSUSNZ bit to 1.

(omitted)

Correct:

Figure 15-0. Format of CTSU Control Register 0 (CTSUCR0) (1/3)

CTSUSNZ	CTSU suspension enable[Note 3]
0	Suspension is disabled.
1	Suspension is enabled.

This bit enables or disables suspension when an external trigger (an interval interrupt signal from the 12-bit interval timer) is selected (the CTSUCAP bit = 1).
Setting this bit drives the CTSU hard macro into the suspended state, which decreases power consumption during the wait state. The suspended state refers to the state in which the capacitor of the external low-pass filter connected to the TSCAP pin is not being charged.
The CTSU state changes as follows depending on the register setting.

State control of the CTSU hard macro> VDC: CTSU measurement power

CTSUPON Bit in CTSUCR1 Register	CTSUSNZ Bit	CTSUCAP Bit	CTSUSTRT Bit	External Trigger	CTSU State
0	0	0	0	—	Stopped
1	0	0	0		Waiting for the start of measurement (VDC = ON)
1	0	0	1		Measuring in normal operating mode (VDC = ON)
1	1	1	0		Preparing for setting measurement by an external trigger (VDC = OFF)
1	1	1	1	Not detected (waiting)	Suspended (waiting for an external trigger) (VDC = OFF)
1	1	1	1	Detection of rising edges (operating)	Measuring in normal operating mode (VDC = ON)[Note 4]
1	1	0	0	—	SW suspended (VDC = OFF)
Other than the above					Setting prohibited

(1) Suspended state

While the CTSU is in the wait state for an external trigger by setting the CTSUSTRT bit to 1 after selecting an external trigger (the CTSUCAP bit = 1) and enabling suspension (the CTSUSNZ bit = 1), the CPU can be placed in STOP mode.
When a rising edge of the external trigger is detected during STOP mode, the CTSU issues a clock request to the clock generating block and makes a transition to normal operating mode to start measurement.

(2) SW suspended state

The SW suspended state refers to the state of suspension initiated when the software trigger has been selected (the CTSUCA bit = 0) and suspension has been enabled (the CTSUSNZ = 1).
This state is used when placing the CTSU hard macro in the suspended state to decrease power consumption by software. In the SW suspended state, placing the CPU in STOP mode is also possible. For return from STOP state, an interrupt is used.

To start measurement from the SW suspended state, set the CTSUSNZ bit to 0 and then wait for at least 64 cycles of the base clock (e.g.: at least 128 µs when the base clock is at 0.5 MHz) before setting the CTSUSTRT bit to 1.
To resume the SW suspended state after the end of measurement, set the CTSUSNZ bit to 1.

(omitted)

Incorrect:

Figure 15-5. Format of CTSU Control Register 0 (CTSUCR0) (3/3)

(omitted)

CTSUSTRT	CTSU measurement operation start[Note1]
0	Measurement operation stops.
1	Measurement operation starts.

When the CTSUCAP bit is 0 (software trigger), measurement is started by writing 1 to the CTSUSTRT bit, and the CTSUSTRT bit becomes 0 when measurement is finished.

When the CTSUCAP bit is 1 (external trigger), the CTSU waits for an external trigger by writing 1 to the CTSUSTRT bit, and measurement is started at the rising edge of the external trigger. When measurement is finished, the CTSU waits for the next external trigger and operation continues.

If 1 is written to the CTSUSTRT bit when it is 1, writing is ignored and operation continues.

To forcibly stop operation (forced stop) when the CTSUSTRT bit is 1, set the CTSUSTRT bit to 0 and the CTSUINIT bit to 1 simultaneously.

The CTSU states are listed below.

CTSUSTRT Bit	CTSUCAP Bit	CTSU State
0	0	Stopped
0	1	Stopped
1	0	During measurement
1	1	During measurement or wait for an external trigger[Note4]

(omitted)

Note 4. The state can be read from the CTSUSTC[2:0] flags in the CTSUST register.
During measurement: CTSUSTC[2:0] flags in the CTSUST register ≠ 000B
Wait for an external trigger: CTSUSTC[2:0] flags in the CTSUST register = 000B

Correct:

Figure 15-5. Format of CTSU Control Register 0 (CTSUCR0) (3/3)

(omitted)

CTSUSTRT	CTSU measurement operation start[Note1]
0	Measurement operation stops.
1	Measurement operation starts.

When the CTSUCAP bit is 0 (software trigger), measurement is started by writing 1 to the CTSUSTRT bit, and the CTSUSTRT bit becomes 0 when measurement is finished.

When the CTSUCAP bit is 1 (external trigger), the CTSU waits for an external trigger by writing 1 to the CTSUSTRT bit, and measurement is started at the rising edge of the external trigger. When measurement is finished, the CTSU waits for the next external trigger and operation continues.

If 1 is written to the CTSUSTRT bit when it is 1, writing is ignored and operation continues.

To forcibly stop operation (forced stop) when the CTSUSTRT bit is 1, set the CTSUSTRT bit to 0 and the CTSUINIT bit to 1 simultaneously.

The CTSU states are listed below.

CTSUSTRT Bit	CTSUCAP Bit	CTSU State
0	0	Stopped
0	1	Stopped
1	0	During measurement
1	1	During measurement or wait for an external trigger[Note5]

(omitted)

Note 4. When a trigger occurs during STOP mode, measurement is performed in normal measurement mode.

Note 5. The state can be read from the CTSUSTC[2:0] flags in the CTSUST register.
During measurement: CTSUSTC[2:0] flags in the CTSUST register ≠ 000B
Wait for an external trigger: CTSUSTC[2:0] flags in the CTSUST register = 000B

9. 15.3.8 CTSU channel enable control register 0 (CTSUCHAC0) (page 711)

Incorrect:

The CTSUCHAC0 register is used to enable or disable the TS pins (TS00 to TS07) of the CTSU.
The CTSUCHAC0 register can be set by **an 8-bit memory manipulation instruction**.
Reset signal generation clears this register to 00H.

Correct:

The CTSUCHAC0 register is used to enable or disable the TS pins (TS00 to TS07) of the CTSU.
The CTSUCHAC0 register can be set by a 1-bit or 8-bit memory manipulation instruction.
Reset signal generation clears this register to 00H.

10. 15.3.9 CTSU channel enable control register 1 (CTSUCHAC1) (page 713)

Incorrect:

The CTSUCHAC1 register is used to enable or disable the TS pins (TS08 to TS14) of the CTSU.
The CTSUCHAC1 register can be set by **an 8-bit memory manipulation instruction.**
Reset signal generation clears this register to 00H.

Correct:

The CTSUCHTRC1 register is used to set reception or transmission for the TS pins (TS08 to TS15) in mutual capacitance full scan mode.
The CTSUCHTRC1 register can be set by a 1-bit or 8-bit memory manipulation instruction .
Reset signal generation clears this register to 00H.

11. 15.3.10 CTSU channel transmit/receive control register 0 (CTSUCHTRC0) (page 715)

Incorrect:

The CTSUCHTRC0 register is used to set transmission or reception for the TS pins (TS00 to TS07) in mutual capacitance full scan mode.
The CTSUCHTRC0 register can be set by **an 8-bit memory manipulation instruction**.
Reset signal generation clears this register to 00H.

Correct:

The CTSUCHTRC0 register is used to set transmission or reception for the TS pins (TS00 to TS07) in mutual capacitance full scan mode.
The CTSUCHTRC0 register can be set by a 1-bit or 8-bit memory manipulation instruction.
Reset signal generation clears this register to 00H.

12. 15.3.11 CTSU channel transmit/receive control register 1 (CTSUCHTRC1) (page 717)

Incorrect:

The CTSUCHTRC1 register is used to set reception or transmission for the TS pins (TS08 to TS15) in mutual capacitance full scan mode.
The CTSUCHTRC1 register can be set by **an 8-bit memory manipulation instruction**.
Reset signal generation clears this register to 00H.

Correct:

The CTSUCHTRC1 register is used to set reception or transmission for the TS pins (TS08 to TS15) in mutual capacitance full scan mode.
The CTSUCHTRC1 register can be set by a 1-bit or 8-bit memory manipulation instruction .
Reset signal generation clears this register to 00H.

13. 15.3.12 CTSU high-pass noise reduction control register (CTSUDCLKC) (page 719)

Incorrect:

The CTSUDCLKC register is used to set the mode of the spectrum diffusion clock for high-pass noise reduction and control the amount of diffusion.
The CTSUDCLKC register can be set by **an 8-bit memory manipulation instruction**.
Reset signal generation clears this register to 00H.

Correct:

The CTSUDCLKC register is used to set the mode of the spectrum diffusion clock for high-pass noise reduction and control the amount of diffusion.
The CTSUDCLKC register can be set by a 1-bit or 8-bit memory manipulation instruction .
Reset signal generation clears this register to 00H.

14. 15.3.13 CTSU status register (CTSUST) (page 720)

Incorrect:

The CTSUST register is used to indicate the current measurement status, whether the measurement result stored in the counter has been read, whether the counter has overflowed, and the mutual capacitance measurement status.
The CTSUST register can be set by **an 8-bit memory manipulation instruction**.
Writing 1 to the CTSUINIT bit in the CTSUCR0 register initializes this register.
Reset signal generation clears this register to 00H.

Correct:

The CTSUST register is used to indicate the current measurement status, whether the measurement result stored in the counter has been read, whether the counter has overflowed, and the mutual capacitance measurement status.
The CTSUST register can be set by a 1-bit or 8-bit memory manipulation instruction .
Writing 1 to the CTSUINIT bit in the CTSUCR0 register initializes this register.
Reset signal generation clears this register to 00H.

15. 15.3.21 TSCAP pin setting register (VTSEL) (page 733)

Incorrect:

When the touch pin function is in use (when the TSSELxx bit is set to 1), the setting of the VTSEL register is effective. This register disables or enables input to the P02 pin.
The VTSEL register can be set by an **8-bit memory manipulation instruction**.
Reset signal generation clears this register to 00H.

Correct:

When the touch pin function is in use (when the TSSELxx bit is set to 1), the setting of the VTSEL register is effective. This register disables or enables input to the P02 pin.
The VTSEL register can be set by a 1-bit or 8-bit memory manipulation instruction .
Reset signal generation clears this register to 00H.

16. 20.3.4 SFR guard function (page 821)

Incorrect:

To guarantee safe operation, the IEC61508 standard requires important data stored in the SFRs to be protected even if a CPU malfunction occurs.
The RL78/G16 provides functionality to protect the data in the control registers for use with the ports, interrupts, clock control, **voltage detection**, and RAM parity error detection.
Enabling this function disables writing to the protected area of the SFRs. Reading from the protected area is possible as usual.

Correct:

To guarantee safe operation, the IEC61508 standard requires important data stored in the SFRs to be protected even if a CPU malfunction occurs.
The RL78/G16 provides functionality to protect the data in the control registers for use with the ports, interrupts, clock control, and RAM parity error detection.
Enabling this function disables writing to the protected area of the SFRs. Reading from the protected area is possible as usual.

17. 20.3.4.1 Invalid memory access detection control register (IAWCTL) (page 821)

Incorrect:

Figure 20-7. Format of Invalid Memory Access Detection Control Register (IAWCTL)

(omitted)

GCSC	Protection of clock, **voltage detector,** and RAM parity error detection control registers
0	Disabled. Reading from and writing to the clock, **voltage detector,** and RAM parity error detection control registers are allowed.
1	Enabled. Writing to the clock, **voltage detector,** and RAM parity error detection control registers is not allowed. Reading is possible. [Protected SFRs] CMC, CSC, OSTS, CKC, PERx, OSMC, RPECTL

Correct:

Figure 20-7. Format of Invalid Memory Access Detection Control Register (IAWCTL)

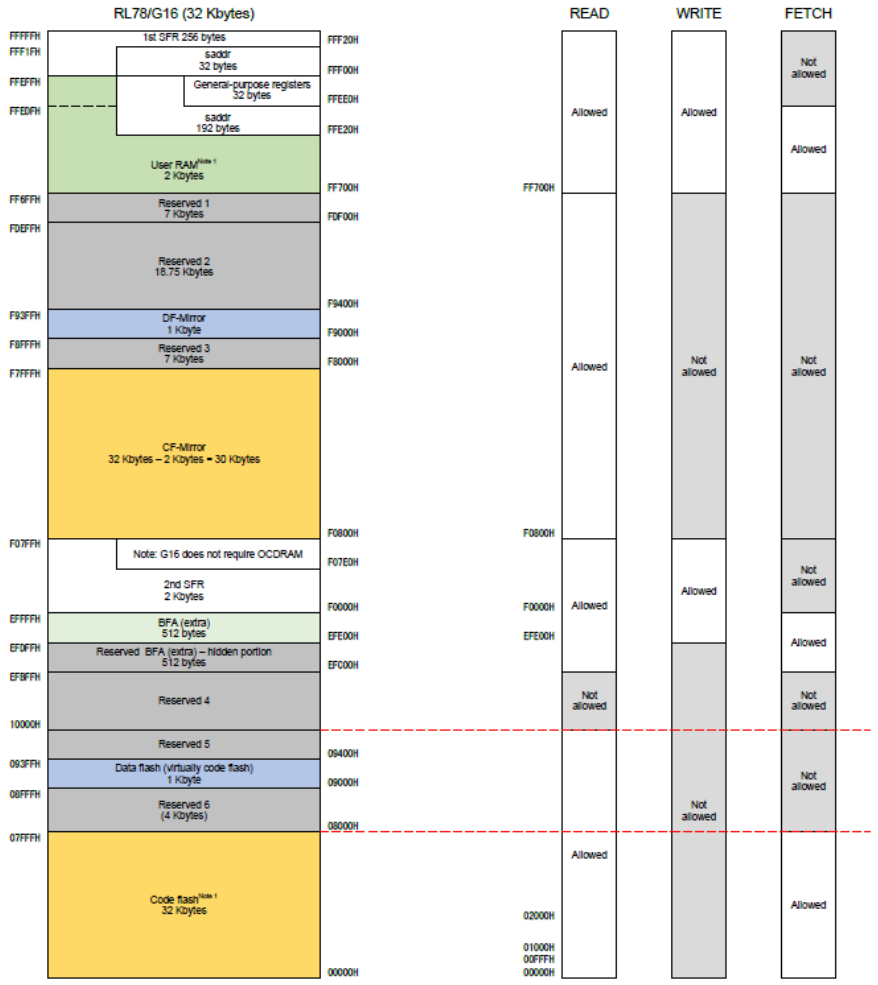
(omitted)

GCSC	Protection of clock and RAM parity error detection control registers
0	Disabled. Reading from and writing to the clock and RAM parity error detection control registers are allowed.
1	Enabled. Writing to the clock and RAM parity error detection control registers is not allowed. Reading is possible. [Protected SFRs] CMC, CSC, OSTS, CKC, PERx, OSMC, RPECTL

18. 20.3.5 Invalid memory access detection (page 823)

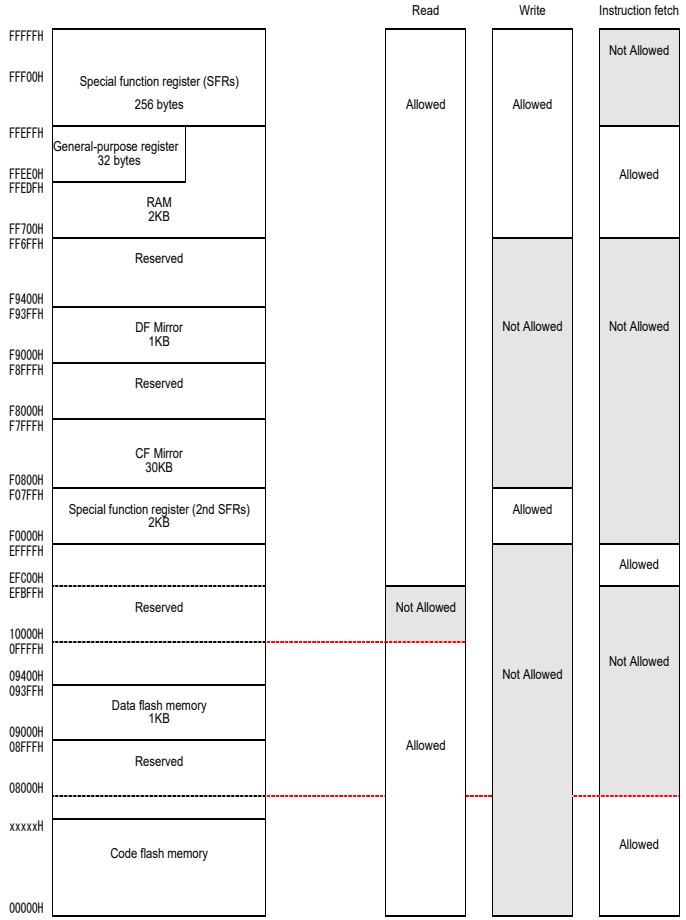
Incorrect:

Figure 20-8. Invalid Access Areas **Complete change of figure**



Correct:

Figure 20-8. Invalid Access Areas



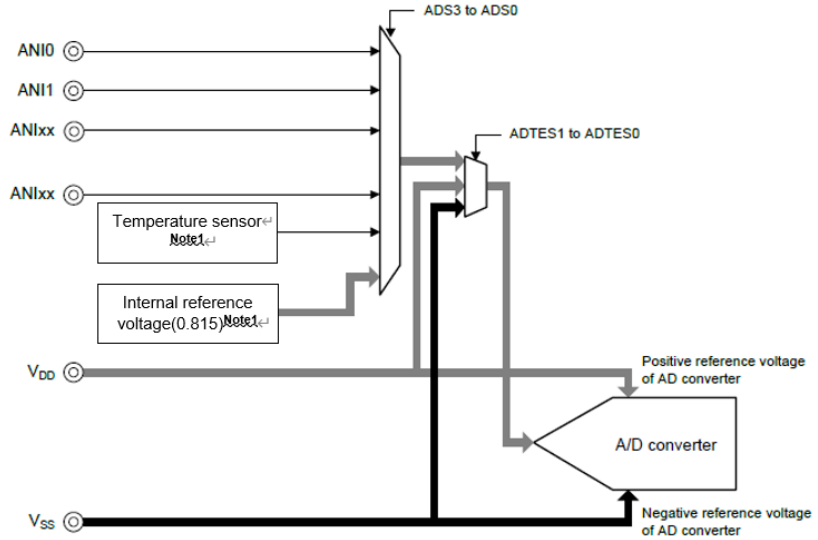
Note 1. The following table lists the capacity and address of the code flash memory and RAM, and the lowest address of the area to be detected as invalid when accessed of each product.

Products	Code flash memory (00000H to xxxxxH)	RAM (zzzzzH to FFEFFH)	Lowest address of the area to be detected as invalid when accessed for reading or instruction fetching (yyyyyH)
R5F121xA (x = 1, 4, 6, 7, B)	16384 × 8 bits (00000H to 03FFFH)	2048 × 8 bits (FF700H to FFEFFH)	10000H
R5F121xC (x = 1, 4, 6, 7, B)	32768 × 8 bits (00000H to 07FFFH)	2048 × 8 bits (FF700H to FFEFFH)	10000H

19. 20.3.7 Testing of the A/D converter (page 827)

Incorrect:

Figure 20-11. Configuration of Testing of A/D Converter



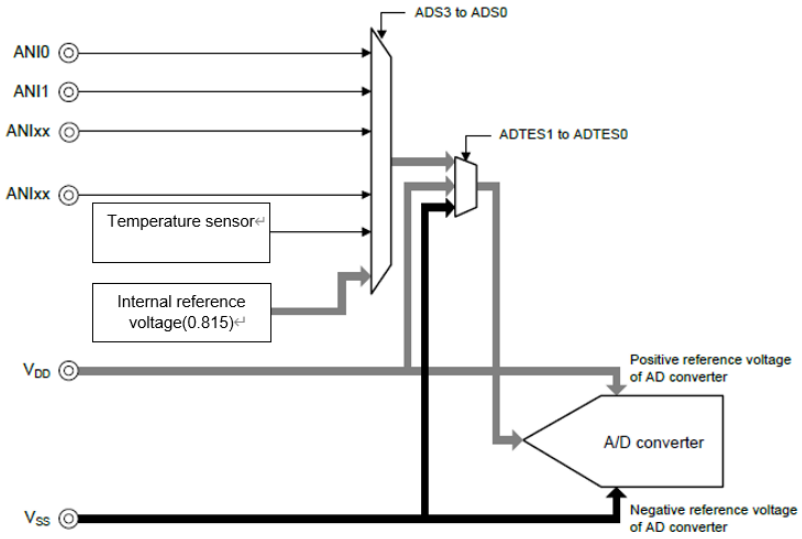
Note 1. This is only selectable in HS (high-speed main) mode.

Note 1. The following table lists the capacity and address of the code flash memory and RAM, and the lowest address of the area to be detected as invalid when accessed of each product.

Products	Code flash memory (00000H to xxxxxH)	Lowest address of the area to be detected as invalid when accessed for reading	Lowest address of the area to be detected as invalid when accessed for instruction fetching
R5F121xA (x = 1, 4, 6, 7, B)	16384 × 8 bits (00000H to 03FFFH)	10000H	08000H
R5F121xC (x = 1, 4, 6, 7, B)	32768 × 8 bits (00000H to 07FFFH)	10000H	08000H

Correct:

Figure 20-11. Configuration of Testing of A/D Converter



Note Deleted

20. CHAPTER 26 ELECTRICAL SPECIFICATIONS (TA = −40 to +85°C) (page 892)

Incorrect:

This chapter describes the electrical specifications of A: Consumer applications (T_A = −40 to +85°C).

(omitted)

Correct:

This chapter describes the electrical specifications of A: Consumer applications (T_A = −40 to +85°C), G: Industrial applications (T_A = −40 to +105°C), and M: Industrial applications (T_A = −40 to +125°C) when they are used in the range of T_A = −40 to +85°C.

(omitted)

Remark There are differences in the high-speed on-chip oscillator clock accuracy between G: Industrial applications and M: Industrial applications, and A: Consumer applications.

Classification	A: Consumer applications	G: Industrial applications	M: Industrial applications
High-speed on-chip oscillator clock accuracy	±2.0% when T_A = −40 to +85°C	±1.5% when T_A = +85 to +105°C ±1.0% when T_A = −20 to +85°C ±1.5% when T_A = −40 to −20°C	±1.5% when T_A = +85 to +125°C ±1.0% when T_A = −20 to +85°C ±1.5% when T_A = −40 to −20°C

21. 26.3.2 Supply current characteristics (page 898)

Incorrect:

[T_A = −40 to +85°C, 2.4 V ≤ VDD ≤ 5.5 V, VSS = 0 V]

Item	Symbol	Condition				MIN.	TYP.	MAX.	Unit
Supply current[Note 1]	I_{DD1}	Operating mode	Basic operation	f_{IH} = 16 MHz[Note 4]	V_{DD} = 3.0 V, 5.0 V		0.97		mA
			Normal operation	f_{SUB} = 32.768 kHz[Note 7] T_A = −40°C	Square wave input		3.65	5.80	mA
					Resonator connection		3.70	6.00	mA
				f_{SUB} = 32.768 kHz[Note 7] T_A = +25°C	Square wave input		3.90	5.80	mA
					Resonator connection		4.18	6.00	mA
				f_{SUB} = 32.768 kHz[Note 7] T_A = +50°C	Square wave input		4.04	6.20	mA
					Resonator connection		4.37	6.40	mA
				f_{SUB} = 32.768 kHz[Note 7] T_A = +70°C	Square wave input		4.20	6.50	mA
					Resonator connection		4.56	6.70	mA
				f_{SUB} = 32.768 kHz[Note 7] T_A = +85°C	Square wave input		4.40	7.80	mA
					Resonator connection		4.80	8.00	mA
	I_{DD2}[Note 2]	HALT mode		f_{IH} = 16 MHz[Note 4]	V_{DD} = 3.0 V, 5.0 V		385	800	µA
				f_{SUB} = 32.768 kHz[Note 8] T_A = −40°C	Square wave input		0.69	1.45	mA
					Resonator connection		0.75	1.65	mA
				f_{SUB} = 32.768 kHz[Note 8] T_A = +25°C	Square wave input		0.75	1.45	mA
					Resonator connection		1.04	1.65	mA
				f_{SUB} = 32.768 kHz[Note 8] T_A = +50°C	Square wave input		0.84	1.74	mA
					Resonator connection		1.20	1.94	mA
				f_{SUB} = 32.768 kHz[Note 8] T_A = +70°C	Square wave input		0.97	2.20	mA
					Resonator connection		1.33	2.40	mA
				f_{SUB} = 32.768 kHz[Note 8] T_A = +85°C	Square wave input		1.13	3.10	mA
					Resonator connection		1.51	3.30	mA
	I_{DD3}[Note 3]	STOP mode[Note 9]		V_{DD} = 3.0 V			0.62	2.80	µA

Correct:

[T_A = −40 to +85°C, 2.4 V ≤ VDD ≤ 5.5 V, VSS = 0 V]

Item	Symbol	Condition				MIN.	TYP.	MAX.	Unit
Supply current[Note 1]	I_{DD1}	Operating mode	Basic operation	f_{IH} = 16 MHz[Note 4]	V_{DD} = 3.0 V, 5.0 V		0.97		mA
			Normal operation	f_{SUB} = 32.768 kHz[Note 7] T_A = −40°C	Square wave input		3.65	5.80	µA
					Resonator connection		3.70	6.00	µA
				f_{SUB} = 32.768 kHz[Note 7] T_A = +25°C	Square wave input		3.90	5.80	µA
					Resonator connection		4.18	6.00	µA
				f_{SUB} = 32.768 kHz[Note 7] T_A = +50°C	Square wave input		4.04	6.20	µA
					Resonator connection		4.37	6.40	µA
				f_{SUB} = 32.768 kHz[Note 7] T_A = +70°C	Square wave input		4.20	6.50	µA
					Resonator connection		4.56	6.70	µA
				f_{SUB} = 32.768 kHz[Note 7] T_A = +85°C	Square wave input		4.40	7.80	µA
					Resonator connection		4.80	8.00	µA
	I_{DD2}[Note 2]	HALT mode		f_{IH} = 16 MHz[Note 4]	V_{DD} = 3.0 V, 5.0 V		385	800	µA
				f_{SUB} = 32.768 kHz[Note 8] T_A = −40°C	Square wave input		0.69	1.45	µA
					Resonator connection		0.75	1.65	µA
				f_{SUB} = 32.768 kHz[Note 8] T_A = +25°C	Square wave input		0.75	1.45	µA
					Resonator connection		1.04	1.65	µA
				f_{SUB} = 32.768 kHz[Note 8] T_A = +50°C	Square wave input		0.84	1.74	µA
					Resonator connection		1.20	1.94	µA
				f_{SUB} = 32.768 kHz[Note 8] T_A = +70°C	Square wave input		0.97	2.20	µA
					Resonator connection		1.33	2.40	µA
				f_{SUB} = 32.768 kHz[Note 8] T_A = +85°C	Square wave input		1.13	3.10	µA
					Resonator connection		1.51	3.30	µA
	I_{DD3}[Note 3]	STOP mode[Note 9]		V_{DD} = 3.0 V			0.62	2.80	µA

22. CHAPTER 27 ELECTRICAL SPECIFICATIONS (T_A = −40 to+105°C, T_A = −40 to +125°C) (page 916)

Incorrect:

This chapter describes the electrical specifications of the following target products.
Target product G: Industrial applications T_A = −40 to +105°C
Target product M: Industrial applications T_A = −40 to +125°C
(omitted)

Correct:

This chapter describes the electrical specifications of the following target products.
Target product G: Industrial applications T_A = −40 to +105°C
Target product M: Industrial applications T_A = −40 to +125°C
(omitted)

Remark When the products are used in the range of T_A = −40 to +85°C, refer to **CHAPTER 26 Electrical Specifications (T_A = −40 to +85°C)**. However, there are differences in the high-speed on-chip oscillator clock accuracy between G: Industrial applications and M: Industrial applications, and A: Consumer applications.

Classification	A: Consumer applications	G: Industrial applications	M: Industrial applications
High-speed on-chip oscillator clock accuracy	±2.0% when T_A = −40 to +85°C	±1.5% when T_A = +85 to +105°C ±1.0% when T_A = −20 to +85°C ±1.5% when T_A = −40 to −20°C	±1.5% when T_A = +85 to +125°C ±1.0% when T_A = −20 to +85°C ±1.5% when T_A = −40 to −20°C

23. 27.3.2 Supply current characteristics (page 922 to page 923)

Incorrect:

[T_A = −40 to +105°C: G products, T_A = −40 to +125°C: M products, 2.4 V ≤ VDD ≤ 5.5 V, VSS = 0 V]

Item	Symbol	Condition				MIN.	TYP.	MAX.	Unit
Supply current[Note 1]	I_{DD1}	Operating mode	Basic operation	f_{IH} = 16 MHz[Note 4]	V_{DD} = 3.0 V, 5.0 V		0.97		mA
			Normal operation	f_{SUB} = 32.768 kHz[Note 7] T_A = −40°C	Square wave input		3.65	5.80	mA
					Resonator connection		3.70	6.00	mA
				f_{SUB} = 32.768 kHz[Note 7] T_A = +25°C	Square wave input		3.90	5.80	mA
					Resonator connection		4.18	6.00	mA
				f_{SUB} = 32.768 kHz[Note 7] T_A = +50°C	Square wave input		4.04	6.20	mA
					Resonator connection		4.37	6.40	mA
				f_{SUB} = 32.768 kHz[Note 7] T_A = +70°C	Square wave input		4.20	6.50	mA
					Resonator connection		4.56	6.70	mA
				f_{SUB} = 32.768 kHz[Note 7] T_A = +85°C	Square wave input		4.40	7.80	mA
					Resonator connection		4.80	8.00	mA
				f_{SUB} = 32.768 kHz[Note 7] T_A = +105°C	Square wave input		4.92	9.12	mA
					Resonator connection		5.36	9.32	mA
				f_{SUB} = 32.768 kHz[Note 7] T_A = +125°C	Square wave input		6.14	15.37	mA
					Resonator connection		6.60	15.57	mA

Correct:

[T_A = −40 to +105°C: G products, T_A = −40 to +125°C: M products, 2.4 V ≤ VDD ≤ 5.5 V, VSS = 0 V

Item	Symbol	Condition				MIN.	TYP.	MAX.	Unit
Supply current[Note 1]	I_{DD1}	Operating mode	Basic operation	f_{IH} = 16 MHz[Note 4]	V_{DD} = 3.0 V, 5.0 V		0.97		mA
			Normal operation	f_{SUB} = 32.768 kHz[Note 7] T_A = −40°C	Square wave input		3.65	5.80	µA
					Resonator connection		3.70	6.00	µA
				f_{SUB} = 32.768 kHz[Note 7] T_A = +25°C	Square wave input		3.90	5.80	µA
					Resonator connection		4.18	6.00	µA
				f_{SUB} = 32.768 kHz[Note 7] T_A = +50°C	Square wave input		4.04	6.20	µA
					Resonator connection		4.37	6.40	µA
				f_{SUB} = 32.768 kHz[Note 7] T_A = +70°C	Square wave input		4.20	6.50	µA
					Resonator connection		4.56	6.70	µA
				f_{SUB} = 32.768 kHz[Note 7] T_A = +85°C	Square wave input		4.40	7.80	µA
					Resonator connection		4.80	8.00	µA
				f_{SUB} = 32.768 kHz[Note 7] T_A = +105°C	Square wave input		4.92	9.12	µA
					Resonator connection		5.36	9.32	µA
				f_{SUB} = 32.768 kHz[Note 7] T_A = +125°C	Square wave input		6.14	15.37	µA
					Resonator connection		6.60	15.57	µA

Incorrect:

Item	Symbol	Condition			MIN.	TYP.	MAX.	Unit
Supply current[Note 1]	I_{DD2}[Note 2]	HALT mode	f_{IH} = 16 MHz[Note 4]	V_{DD} = 3.0 V, 5.0 V		385	824	μA
			f_{SUB} = 32.768 kHz[Note 8] T_A = −40°C	Square wave input		0.69	1.45	mA
				Resonator connection		0.75	1.65	mA
			f_{SUB} = 32.768 kHz[Note 8] T_A = +25°C	Square wave input		0.75	1.45	mA
				Resonator connection		1.04	1.65	mA
			f_{SUB} = 32.768 kHz[Note 8] T_A = +50°C	Square wave input		0.84	1.74	mA
				Resonator connection		1.20	1.94	mA
			f_{SUB} = 32.768 kHz[Note 8] T_A = +70°C	Square wave input		0.97	2.20	mA
				Resonator connection		1.33	2.40	mA
			f_{SUB} = 32.768 kHz[Note 8] T_A = +85°C	Square wave input		1.13	3.10	mA
				Resonator connection		1.51	3.30	mA
			f_{SUB} = 32.768 kHz[Note 8] T_A = +105°C	Square wave input		1.58	8.92	mA
				Resonator connection		1.99	9.12	mA
			f_{SUB} = 32.768 kHz[Note 8] T_A = +125°C	Square wave input		2.68	10.67	mA
				Resonator connection		3.12	10.87	mA
	I_{DD3}[Note 3]	STOP mode[Note 9]	V_{DD} = 3.0 V	T_A = +105°C		0.62	4.12	μA
				T_A = +125°C		0.62	10.37	μA

Correct:

Item	Symbol	Condition			MIN.	TYP.	MAX.	Unit
Supply current[Note 1]	I_{DD2}[Note 2]	HALT mode	f_{IH} = 16 MHz[Note 4]	V_{DD} = 3.0 V, 5.0 V		385	824	μA
			f_{SUB} = 32.768 kHz[Note 8] T_A = −40°C	Square wave input		0.69	1.45	μA
				Resonator connection		0.75	1.65	μA
			f_{SUB} = 32.768 kHz[Note 8] T_A = +25°C	Square wave input		0.75	1.45	μA
				Resonator connection		1.04	1.65	μA
			f_{SUB} = 32.768 kHz[Note 8] T_A = +50°C	Square wave input		0.84	1.74	μA
				Resonator connection		1.20	1.94	μA
			f_{SUB} = 32.768 kHz[Note 8] T_A = +70°C	Square wave input		0.97	2.20	μA
				Resonator connection		1.33	2.40	μA
			f_{SUB} = 32.768 kHz[Note 8] T_A = +85°C	Square wave input		1.13	3.10	μA
				Resonator connection		1.51	3.30	μA
			f_{SUB} = 32.768 kHz[Note 8] T_A = +105°C	Square wave input		1.58	8.92	μA
				Resonator connection		1.99	9.12	μA
			f_{SUB} = 32.768 kHz[Note 8] T_A = +125°C	Square wave input		2.68	10.67	μA
				Resonator connection		3.12	10.87	μA
	I_{DD3}[Note 3]	STOP mode[Note 9]	V_{DD} = 3.0 V	T_A = +105°C		0.62	4.12	μA
				T_A = +125°C		0.62	10.37	μA