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RENESAS TECHNICAL UPDATE

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Product Category	MPU/MCU		Document No.	TN-RL*-A023A/E	Rev.	1.00
Title	Correction for Incorrect Description Notice RL78/G10 Descriptions in the Hardware User's Manual Rev. 1.00 Changed		Information Category	Technical Notification		
Applicable Product	RL78/G10 R5F10Yxxx	Lot No. All lots	Reference Document	RL78/G10 User's Manual: Hardware Rev.1.00 R01UH0384EJ0100 (Jun. 2013)		

This document describes misstatements found in the RL78/G10 User's Manual: Hardware Rev.1.00 (R01UH0384EJ0100).

Corrections

Applicable Item	Applicable Page	Contents
Flash ROM: 4 KB of 10-pin products, and 16-pin products	Page 7	Specifications added
3. 1 Address Space	Pages 22 to 24	Incorrect descriptions revised
6. 3. 5 Timer channel enable status register 0 (TE0, TEH0 (8-bit mode))	Page 121	Incorrect descriptions revised
6. 3. 8 Timer output enable register 0 (TOE0)	Page 124	Incorrect descriptions revised
6. 4. 2 Basic rules of 8-bit timer operation function (only channels 1 and 3)	Page 132	Specifications added
Figure 10-13. Conversion Operation of A/D Converter	Page 235	Incorrect descriptions revised
10. 9. 3 Conflicting operations	Page 242	Descriptions added
24. 3. 1 Pin characteristics	Page 556	Specifications extended
24. 6. 1 A/D converter characteristics	Page 567	Specifications added
24. 6. 4 Data retention power supply voltage characteristics	Page 568	Descriptions added

Document Improvement

The above corrections will be made for the next revision of the User's Manual: Hardware.

Corrections in the User's Manual: Hardware

No.	Corrections and Applicable Items			Pages in this document for corrections
		Document No. English	R01UH0384EJ0100	
1	Flash ROM: 4 KB of 10-pin products, and 16-pin products		Page 7	Page 3
2	3. 1 Address Space		Pages 22 to 24	Pages 4 to 6
3	6. 3. 5 Timer channel enable status register 0 (TE0, TEH0 (8-bit mode))		Page 121	Page 7
4	6. 3. 8 Timer output enable register 0 (TOE0)		Page 124	Page 7
5	6. 4. 2 Basic rules of 8-bit timer operation function (only channels 1 and 3)		Page 132	Page 7
6	Figure 10-13. Conversion Operation of A/D Converter		Page 235	Page 8
7	10. 9. 3 Conflicting operations		Page 242	Page 9
8	24. 3. 1 Pin characteristics		Page 556	Page 10
9	24. 6. 1 A/D converter characteristics		Page 567	Pages 11 and 12
10	24. 6. 4 Data retention power supply voltage characteristics		Page 568	Page 13

Incorrect: Bold with underline; Correct: Gray hatched

Revision History

RL78/G10 User's Manual: Hardware Rev.1.00 Correction for Incorrect Description Notice

Document Number	Date	Description
TN-RL*-A023A/E	Feb. 6, 2014	First edition issued No.1 to 10 in corrections (This notice)

1. Flash ROM: 4 KB of 10-pin products, and 16-pin products (Page 7)

Flash ROM: 4 KB of 10-pin products and 16-pin products will be added to line-up in the group of RL78/G10.

The details of functions of 16-pin products will be made for the next revision of the User's Manual: Hardware.

This outline describes the function at the time when Peripheral I/O redirection register (PIOR) is set to 00H.

Item			10-pin			16-pin		
			R5F10Y14ASP	R5F10Y16ASP	R5F10Y17ASP	R5F10Y44ASP	R5F10Y46ASP	R5F10Y47ASP
Code flash memory			1 KB	2 KB	4 KB	1 KB	2 KB	4 KB
RAM			128 B	256 B	512 B	128 B	256 B	512 B
Main system clock	High-speed system clock		—			X1, X2 (crystal/ceramic) oscillation, external main system clock input (EXCLK): 1 to 20 MHz: V_{DD} = 2.7 to 5.5 V 1 to 5 MHz: V_{DD} = 2.0 to 5.5 V Note 3		
	High-speed on-chip oscillator clock		• 1.25 to 20 MHz (V_{DD} = 2.7 to 5.5 V) • 1.25 to 5 MHz (V_{DD} = 2.0 to 5.5 V Note 3)					
Low-speed on-chip oscillator clock			15 kHz (TYP)					
General-purpose register			8-bit register × 8					
Minimum instruction execution time			0.05 μs (20 MHz operation)					
Instruction set			• Data transfer (8 bits) • Adder and subtractor/logical operation (8 bits) • Multiplication (8 bits × 8 bits) • Rotate, barrel shift, and bit manipulation (set, reset, test, and Boolean operation), etc.					
I/O port	Total		8			14		
	CMOS I/O		6 (N-ch open-drain output (V_{DD} tolerance): 2)			10 (N-ch open-drain output (V_{DD} tolerance): 4)		
	CMOS input		2			4		
Timer	16-bit timer		2 channels			4 channels		
	Watchdog timer		1 channel					
	12-bit interval timer		—			1 channel		
	Timer output		2 channels (PWM output: 1)			4 channels (PWM outputs: 3 Note 1)		
Clock output/buzzer output			1					
			2.44 kHz to 10 MHz: (Peripheral hardware clock: f_{MAIN} = 20 MHz operation)					
Comparator			—			1		
8-/10-bit resolution A/D converter			4 channels			7 channels		
Serial interface			[10-pin products] CSI: 1 channel/simplified I^2C: 1 channel/UART: 1 channel [16-pin products] CSI: 2 channels/simplified I^2C: 1 channel/UART: 1 channel					
	I^2C bus		—			1 channel		
Vectored interrupt sources	Internal		8			14		
	External		3			5		
Key interrupt			6					
Reset			• Reset by $\overline{\text{RESET}}$ pin • Internal reset by watchdog timer • Internal reset by selectable power-on-reset • Internal reset by illegal instruction execution Note 2 • Internal reset by data retention lower limit voltage					
Selectable power-on-reset circuit			• Detection voltage Rising edge (V_{SPOR}): 2.25 V/2.68 V/3.02 V/4.45 V (max.) Falling edge (V_{SPDR}): 2.20 V/2.62 V/2.96 V/4.37 V (max.)					
On-chip debug function			Provided					
Power supply voltage			V_{DD} = 2.0 to 5.5 V Note 3					
Operating ambient temperature			T_A = - 40 to + 85 °C					

Notes 1. The number of outputs varies, depending on the setting of channels in use and the number of the master (see **6.9.4 Operation as multiple PWM output function**).

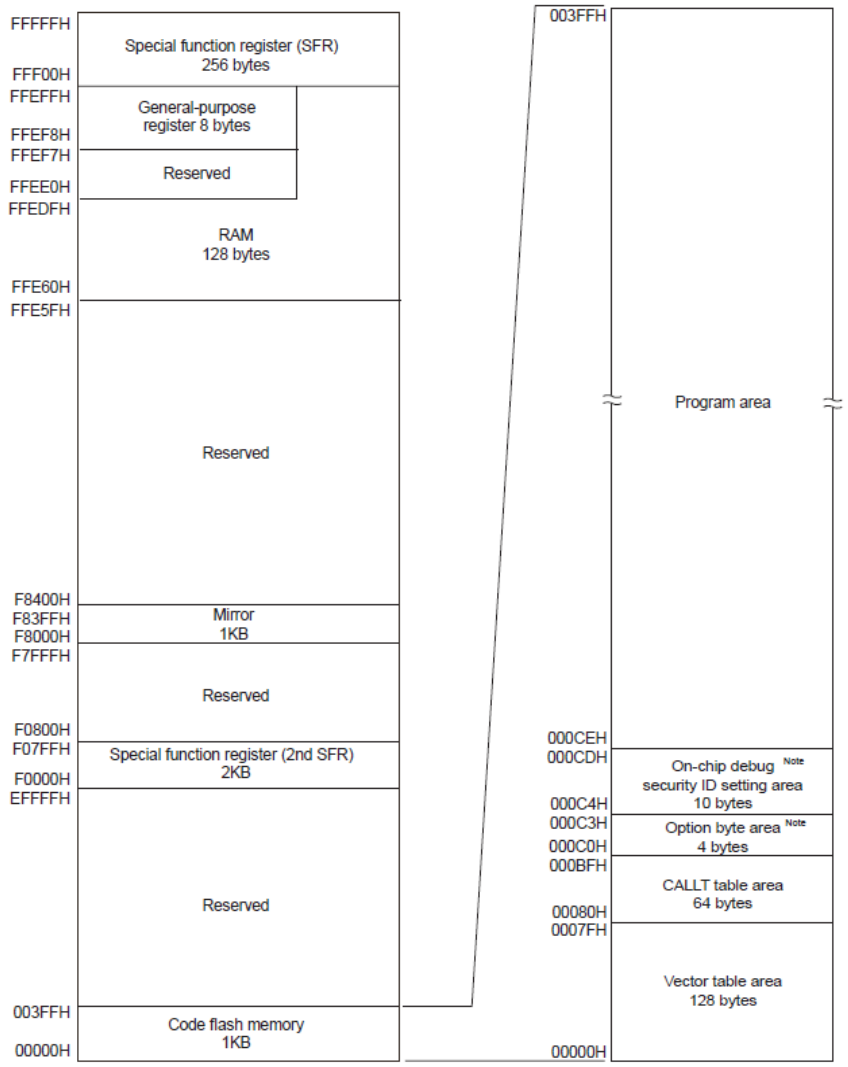
2. The illegal instruction is generated when instruction code FFH is executed. Reset by the illegal instruction execution not issued by emulation with the on-chip debug emulator.

3. Use this product within the voltage range from 2.25 to 5.5 V because the detection voltage (V_{SPOR}) of the selectable power-on-reset (SPOR) circuit should also be considered.

2. 3. 1 Address Space (Pages 22 to 24)

Incorrect:

Figure 3-1. Memory Map for the R5F10Y14ASP and R5F10Y44ASP

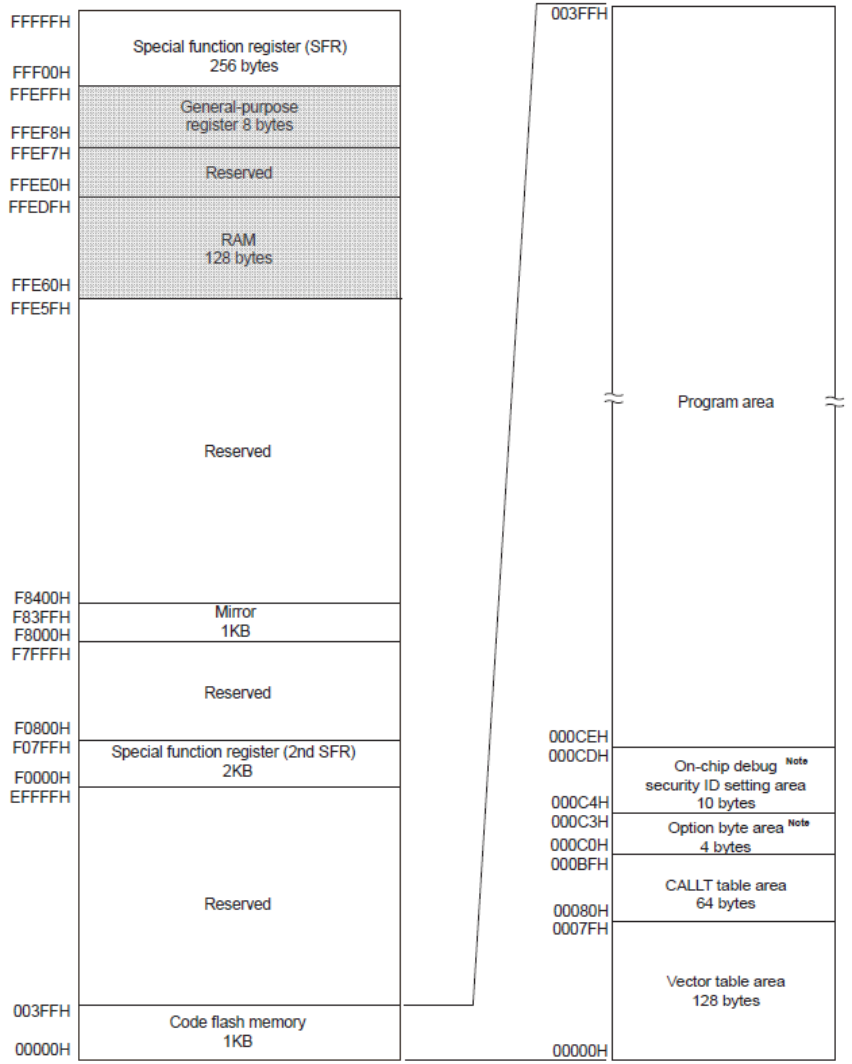


Note Set the option bytes to 000C0H to 000C3H, and the on-chip debug security IDs to 000C4H to 000CDH.

Caution Access to the reserved area is prohibited.

Correct:

Figure 3-1. Memory Map for the R5F10Y14ASP and R5F10Y44ASP

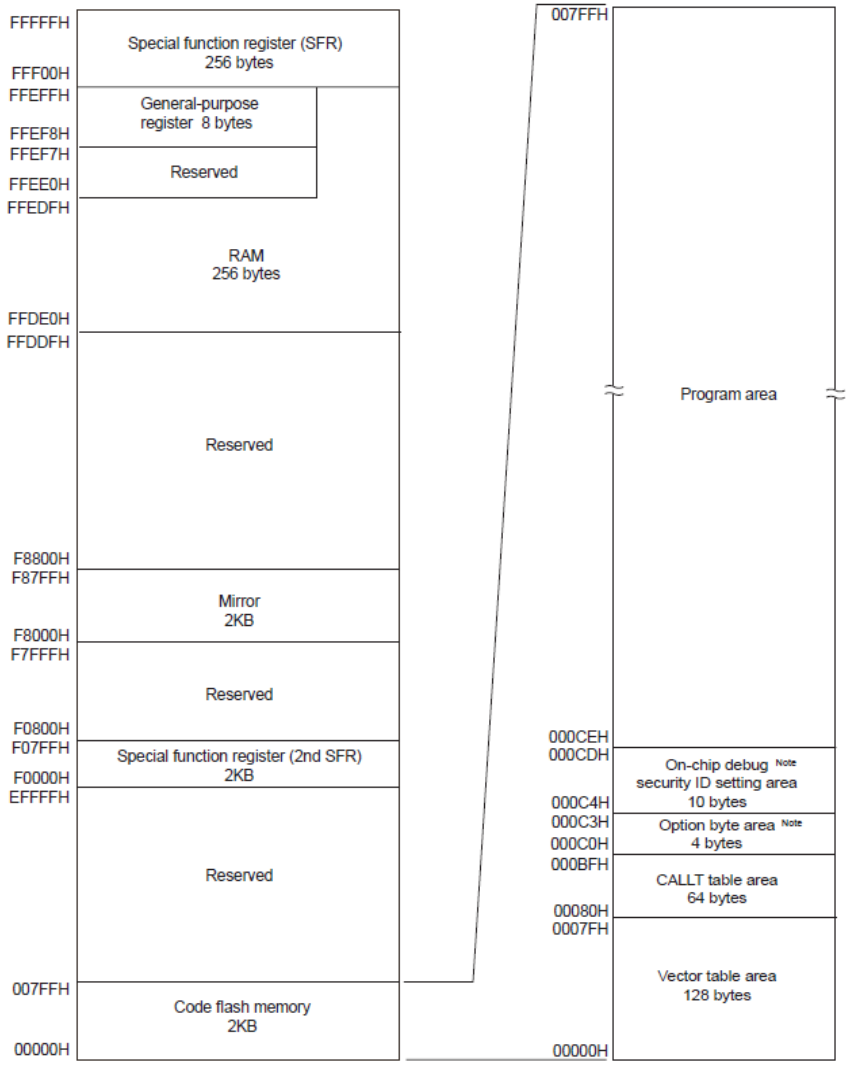


Note Set the option bytes to 000C0H to 000C3H, and the on-chip debug security IDs to 000C4H to 000CDH.

Caution Access to the reserved area is prohibited.

Incorrect:

Figure 3-2. Memory Map for the R5F10Y16ASP and R5F10Y46ASP

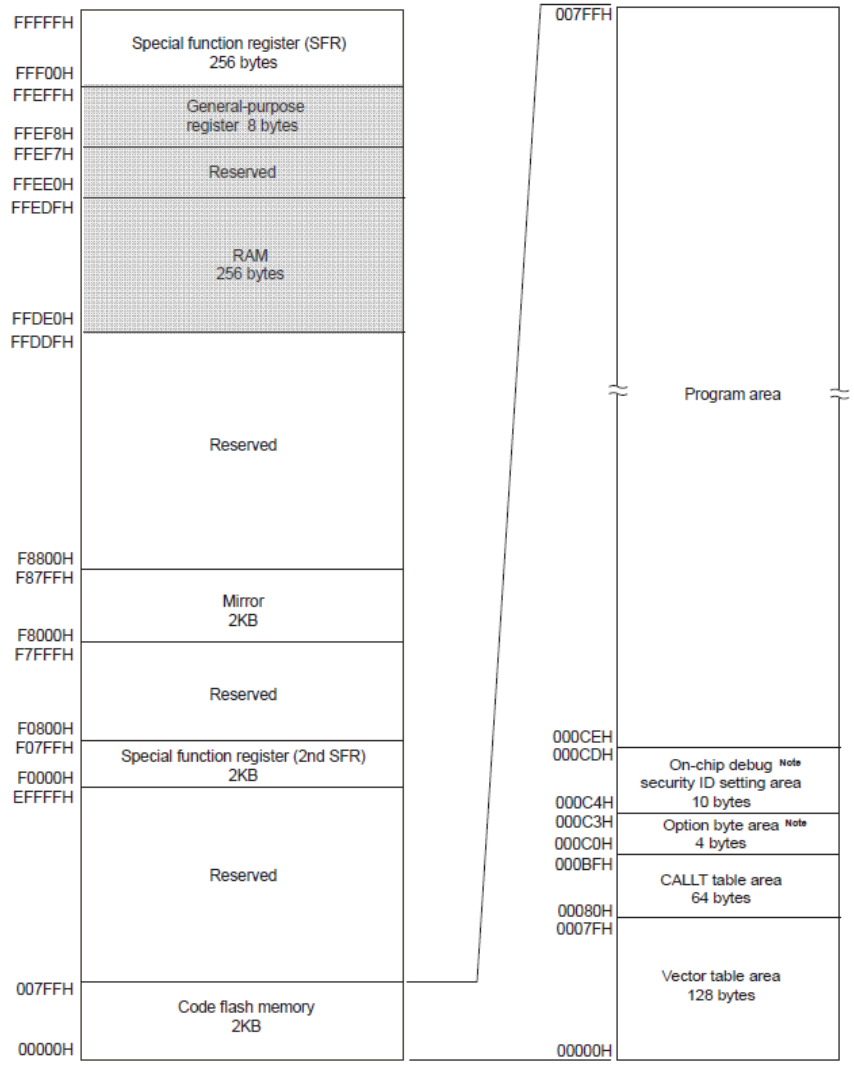


Note Set the option bytes to 000C0H to 000C3H, and the on-chip debug security IDs to 000C4H to 000CDH.

Caution Access to the reserved area is prohibited.

Correct:

Figure 3-2. Memory Map for the R5F10Y16ASP and R5F10Y46ASP

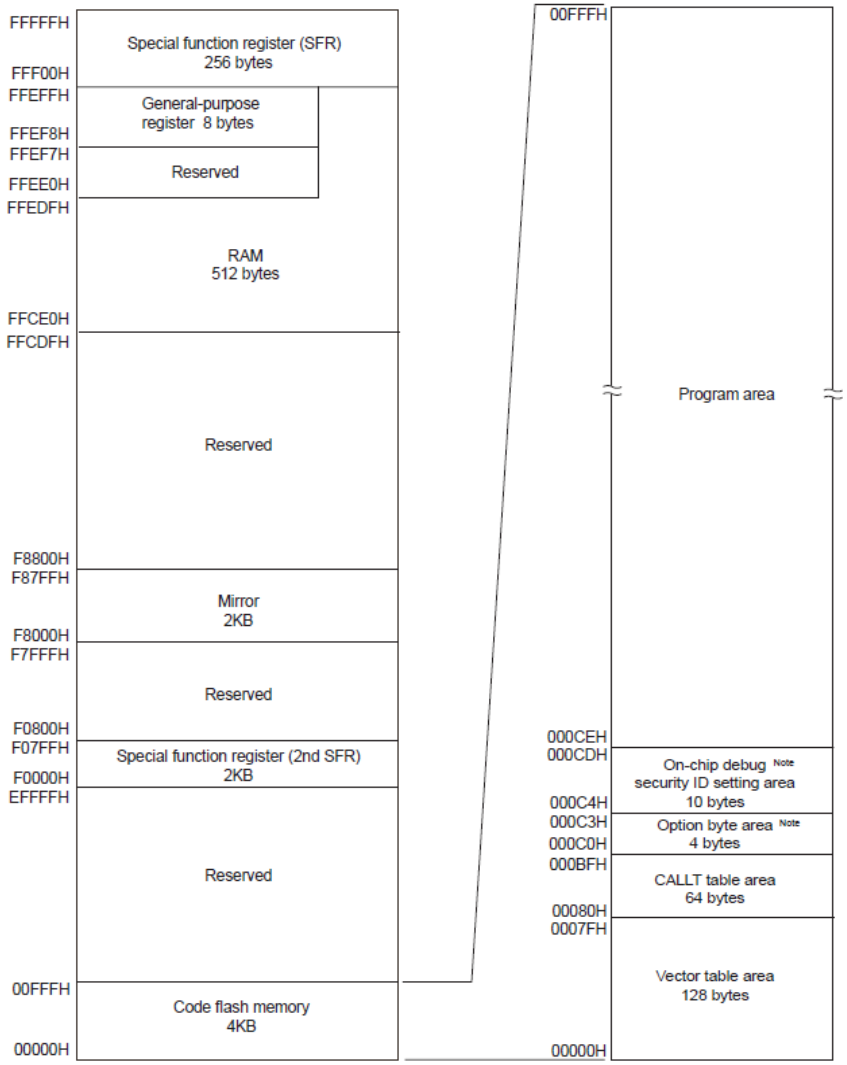


Note Set the option bytes to 000C0H to 000C3H, and the on-chip debug security IDs to 000C4H to 000CDH.

Caution Access to the reserved area is prohibited.

Incorrect:

Figure 3-3. Memory Map for the R5F10Y47ASP

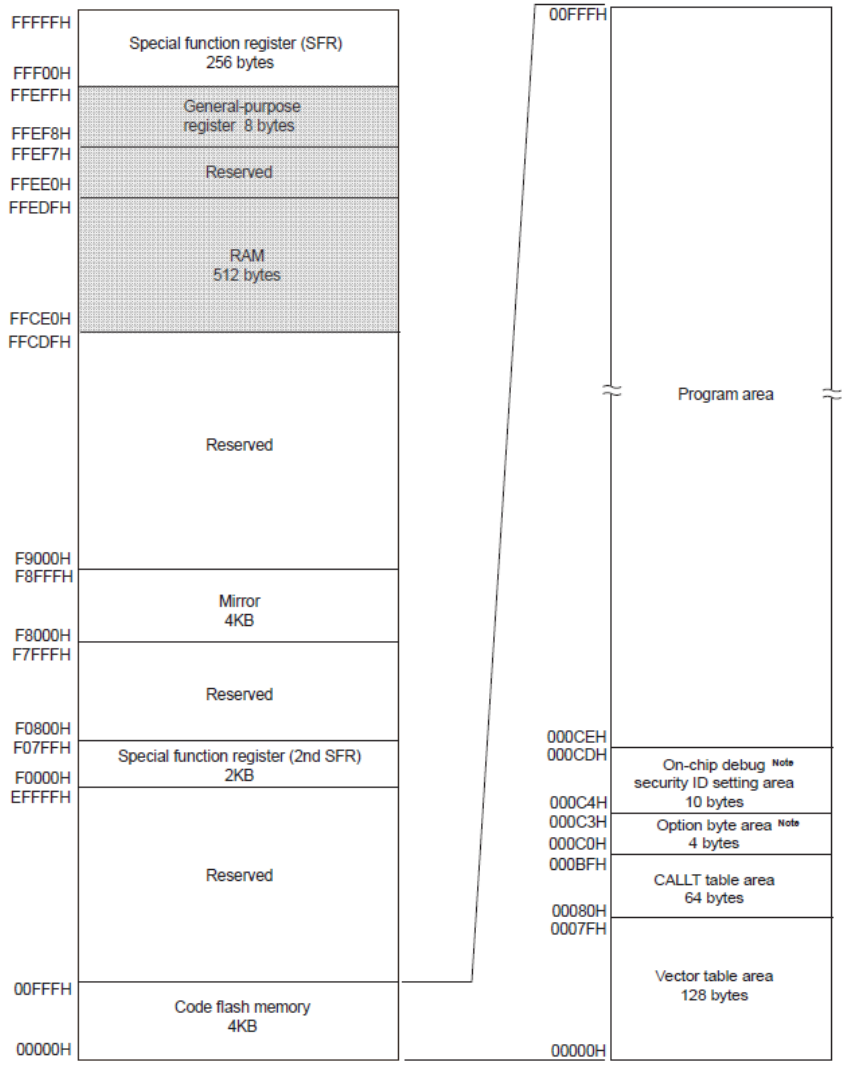


Note Set the option bytes to 000C0H to 000C3H, and the on-chip debug security IDs to 000C4H to 000CDH.

Caution Access to the reserved area is prohibited.

Correct:

Figure 3-3. Memory Map for the R5F10Y17ASP and R5F10Y47ASP



Note Set the option bytes to 000C0H to 000C3H, and the on-chip debug security IDs to 000C4H to 000CDH.

Caution Access to the reserved area is prohibited.

3. **6. 3. 5 Timer channel enable status register 0 (TE0, TEH0 (8-bit mode)) (Page 121)**

Incorrect:

The TE0 and TEH0 registers are used to enable or stop the timer operation of each channel.

Each bit of the TE0 and TEH0 registers correspond to each bit of the timer channel start register 0 (TS0, TSH0) and the timer channel stop register 0 (TT0, TTH0). When a bit of the TS0 and TSH0 registers is set to 1, the corresponding bit of TE0 and TEH0 is set to 1. When a bit of the TT0 and TTH0 registers is set to 1, the corresponding bit of TE0 and TEH0 is cleared to 0.

The TE0 and TEH0 registers can be read by an 8-bit memory manipulation instruction.

Reset signal generation clears TE0 and TEH0 registers to 00H.

Correct:

The TE0 and TEH0 registers are used to enable or stop the timer operation of each channel.

Each bit of the TE0 and TEH0 registers correspond to each bit of the timer channel start register 0 (TS0, TSH0) and the timer channel stop register 0 (TT0, TTH0). When a bit of the TS0 and TSH0 registers is set to 1, the corresponding bit of TE0 and TEH0 is set to 1. When a bit of the TT0 and TTH0 registers is set to 1, the corresponding bit of TE0 and TEH0 is cleared to 0.

The TE0 and TEH0 registers can be read by a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation clears TE0 and TEH0 registers to 00H.

4. **6. 3. 8 Timer output enable register 0 (TOE0) (Page 124)**

Incorrect:

The TOE0 register is used to enable or disable timer output of each channel.

Channel n for which timer output has been enabled becomes unable to rewrite the value of the TO0n bit of timer output register 0 (TO0) described later by software, and the value reflecting the setting of the timer output function through the count operation is output from the timer output pin (TO0n).

The TOE0 register can be set by an 8-bit memory manipulation instruction.

Reset signal generation clears this register to 00H.

Correct:

The TOE0 register is used to enable or disable timer output of each channel.

Channel n for which timer output has been enabled becomes unable to rewrite the value of the TO0n bit of timer output register 0 (TO0) described later by software, and the value reflecting the setting of the timer output function through the count operation is output from the timer output pin (TO0n).

The TOE0 register can be set by a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation clears this register to 00H.

5. **6. 4. 2 Basic rules of 8-bit timer operation function (only channels 1 and 3) (Page 132)**

Old:

The 8-bit timer operation function makes it possible to use a 16-bit timer channel in a configuration consisting of two 8-bit timer channels.

This function can only be used for channels 1 and 3, and there are several rules for using it.

The basic rules for this function are as follows:

(omitted)

(7) The lower 8 bits operate according to the settings of TMR0nH and TMR0nL registers. The following four functions support operation of the lower 8 bits:

- Interval timer function
- External event counter function
- Delay count function
- PWM output

New:

The 8-bit timer operation function makes it possible to use a 16-bit timer channel in a configuration consisting of two 8-bit timer channels.

This function can only be used for channels 1 and 3, and there are several rules for using it.

The basic rules for this function are as follows:

(omitted)

(7) The lower 8 bits operate according to the settings of TMR0nH and TMR0nL registers. The lower 8-bit timer supports the following functions:

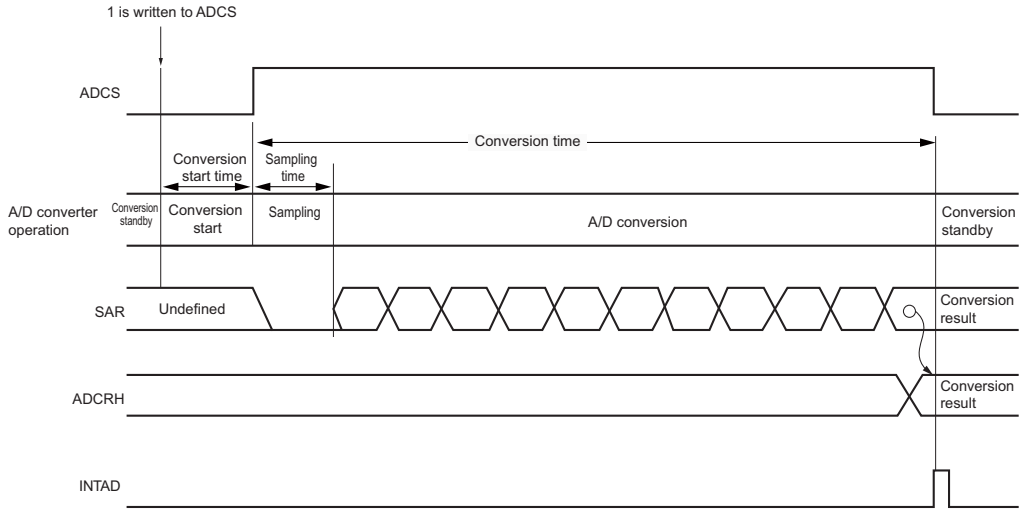
- Interval timer
- Square wave output
- External event counter
- Delay counter
- PWM output function
- Multiple PWM output function (16-pin products only)

6. Figure 10-13. Conversion Operation of A/D Converter (Page 235)

Incorrect:

<R>

Figure 10-13. Conversion Operation of A/D Converter

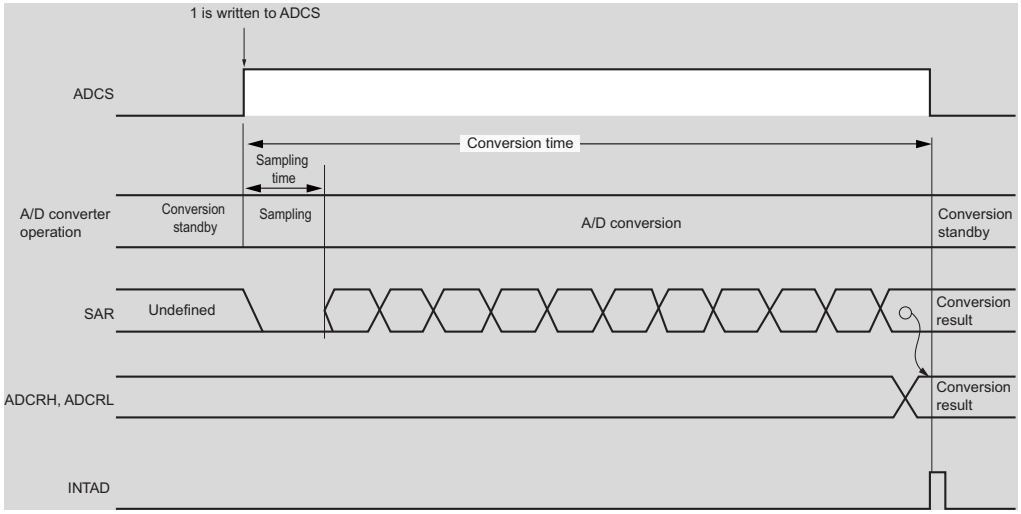


A/D conversion is performed once when the bit 7 (ADCS) of the A/D converter mode register 0 (ADM0) is set to 1 by software.

Reset signal generation clears the A/D conversion result register (ADCRL, ADCRH) to 00H.

Correct:

Figure 10-12. Conversion Operation of A/D Converter



A/D conversion is performed once when the bit 7 (ADCS) of the A/D converter mode register 0 (ADM0) is set to 1 by software. The ADCS bit is automatically cleared to 0 after A/D conversion ends.

Reset signal generation clears the A/D conversion result register (ADCRH, ADCRL) to 00H.

7. 10. 9. 3 Conflicting operations (Page 242)

Old:

10.9.3 Conflicting operations

Writing to the ADM0 register has priority if conflict between writing to the ADCRH or ADCRL register and writing 0 to the A/D converter mode register 0 (ADM0) occurs at the end of conversion. Writing to the ADCRH or ADCRL register is not performed, nor is the conversion end interrupt signal (INTAD) generated.

New:

10.9.3 Conflicting operations

<1> Reading from the ADCRH or ADCRL register has priority if conflict between writing to the A/D conversion result register (ADCRH, ADCRL) and reading from ADCRH or ADCRL register by software operation occurs at the end of conversion. After the read operation, the new conversion result is written to the ADCRH or ADCRH register.

<2> Writing to the ADM0 register has priority if conflict between writing to the ADCRH or ADCRL register and writing to the A/D converter mode register 0 (ADM0) occurs at the end of conversion. Writing to the ADCRH or ADCRL register is not performed, nor is the A/D conversion end interrupt signal (INTAD) generated.

8. 24. 3. 1 Pin characteristics (Page 556)

This shows the specifications changed in the ELECTRICAL SPECIFICATIONS of 10-pin products. The ELECTRICAL SPECIFICATIONS of “Flash ROM: 4 KB of 10-pin products and 16-pin products” will be made for the next revision of the User’s Manual: Hardware.

Old:

24.3.1 Pin characteristics

(T_A = –40 to +85°C, 2.0 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions			MIN.	TYP.	MAX.	Unit
Output current, high Note 1	I_{OH1}	P00, P01, P02 to P04, P40	Per pin				-10.0 Note 2	mA
		P40	Total Note 3	4.0 V ≤ V_{DD} ≤ 5.5 V			-10.0	mA
				2.7 V ≤ V_{DD} < 4.0 V			-2.0	mA
				2.0 V ≤ V_{DD} < 2.7 V			-1.5	mA
		P00, P01, P02 to P04	Total Note 3	4.0 V ≤ V_{DD} ≤ 5.5 V			-50.0	mA
				2.7 V ≤ V_{DD} < 4.0 V			-10.0	mA
				2.0 V ≤ V_{DD} < 2.7 V			-7.5	mA
		Total of all pins Note 3					-60.0	mA
Output current, low Note 4	I_{OL1}	P00 to P04, P40	Per pin				20.0 Note 2	mA
		P40	Total Note 3	4.0 V ≤ V_{DD} ≤ 5.5 V			20.0	mA
				2.7 V ≤ V_{DD} < 4.0 V			3.0	mA
				2.0 V ≤ V_{DD} < 2.7 V			0.6	mA
		P00 to P04	Total Note 3	4.0 V ≤ V_{DD} ≤ 5.5 V			80.0	mA
				2.7 V ≤ V_{DD} < 4.0 V			12.0	mA
				2.0 V ≤ V_{DD} < 2.7 V			2.4	mA
		Total of all pins Note 3					100.0	mA

(omitted)

New:

24.3.1 Pin characteristics

(T_A = –40 to +85°C, 2.0 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Output current, high Note 1	I_{OH1}	Per pin for 10-pin products: P00 to P04, P40 16-pin products: P00 to P07, P40, P41				-10.0 Note 2	mA
		Total of 10-pin products: P40 16-pin products: P40, P41 (When duty ≤ 70% Note 3)	4.0 V ≤ V_{DD} ≤ 5.5 V			-20.0	mA
			2.7 V ≤ V_{DD} < 4.0 V			-4.0	mA
			2.0 V ≤ V_{DD} < 2.7 V			-3.0	mA
		Total of 10-pin products: P00 to P04 16-pin products: P00 to P07 (When duty ≤ 70% Note 3)	4.0 V ≤ V_{DD} ≤ 5.5 V			-60.0	mA
			2.7 V ≤ V_{DD} < 4.0 V			-12.0	mA
			2.0 V ≤ V_{DD} < 2.7 V			-9.0	mA
		Total of all pins (When duty ≤ 70% Note 3)				-80.0	mA
Output current, low Note 4	I_{OL1}	Per pin for 10-pin products: P00 to P04, P40 16-pin products: P00 to P07, P40, P41				20.0 Note 2	mA
		Total of 10-pin products: P40 16-pin products: P40, P41 (When duty ≤ 70% Note 3)	4.0 V ≤ V_{DD} ≤ 5.5 V			40.0	mA
			2.7 V ≤ V_{DD} < 4.0 V			6.0	mA
			2.0 V ≤ V_{DD} < 2.7 V			1.2	mA
		Total of 10-pin products: P00 to P04 16-pin products: P00 to P07 (When duty ≤ 70% Note 3)	4.0 V ≤ V_{DD} ≤ 5.5 V			80.0	mA
			2.7 V ≤ V_{DD} < 4.0 V			12.0	mA
			2.0 V ≤ V_{DD} < 2.7 V			2.4	mA
		Total of all pins (When duty ≤ 70% Note 3)				120.0	mA

(omitted)

9. 24. 6. 1 A/D converter characteristics (Page 567)

This shows the specifications changed in the ELECTRICAL SPECIFICATIONS of 10-pin products. The ELECTRICAL SPECIFICATIONS of “Flash ROM: 4 KB of 10-pin products and 16-pin products” will be made for the next revision of the User’s Manual: Hardware.

Old:

24.6.1 A/D converter characteristics

(Target ANI pin : ANI0 to ANI3)

(T_A = –40 to +85°C, 2.4 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Resolution	RES			8		10	bit
Overall error Note 1	AINL	10-bit resolution	V_{DD} = 5 V		±1.7	±3.1 Note 2	LSB
			V_{DD} = 3 V		±2.3	±4.5 Note 2	LSB
Conversion time	tCONV	10-bit resolution	2.7 V ≤ V_{DD} ≤ 5.5 V	3.4		18.4	µs
			2.4 V ≤ V_{DD} ≤ 5.5 V	4.6		18.4	µs
Zero-scale error Note 1	EZS	10-bit resolution	V_{DD} = 5 V			±0.19 Note 2	%FSR
			V_{DD} = 3 V			±0.39 Note 2	%FSR
Full-scale error Note 1	EFS	10-bit resolution	V_{DD} = 5 V			±0.29 Note 2	%FSR
			V_{DD} = 3 V			±0.42 Note 2	%FSR
Integral linearity error Note 1	ILE	10-bit resolution	V_{DD} = 5 V			±1.8 Note 2	LSB
			V_{DD} = 3 V			±1.7 Note 2	LSB
Differential linearity error Note 1	DLE	10-bit resolution	V_{DD} = 5 V			±1.4 Note 2	LSB
			V_{DD} = 3 V			±1.5 Note 2	LSB
Analog input voltage	VAIN			0		V_{DD}	V

Notes 1. Excludes quantization error (±1/2 LSB).

2. This is the characteristic evaluation value plus or minus 3. These values are not used in the shipping inspection.

New:

24.6.1 A/D converter characteristics

(Target pin: ANI0 to ANI6, internal reference voltage)

(T_A = –40 to +85°C, 2.4 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Resolution	RES			8		10	bit
Overall error Notes 1, 2, 3	AINL	10-bit resolution	V_{DD} = 5 V		±1.7	±3.1	LSB
			V_{DD} = 3 V		±2.3	±4.5	LSB
Conversion time	tCONV	10-bit resolution Target pin: ANI0 to ANI6	2.7 V ≤ V_{DD} ≤ 5.5 V	3.4		18.4	µs
			2.4 V ≤ V_{DD} ≤ 5.5 V Note 5	4.6		18.4	µs
		10-bit resolution Target pin: internal reference voltage Note 6	2.4 V ≤ V_{DD} ≤ 5.5 V	4.6		18.4	µs
Zero-scale error Notes 1, 2, 3, 4	EZS	10-bit resolution	V_{DD} = 5 V			±0.19	%FSR
			V_{DD} = 3 V			±0.39	%FSR
Full-scale error Notes 1, 2, 3, 4	EFS	10-bit resolution	V_{DD} = 5 V			±0.29	%FSR
			V_{DD} = 3 V			±0.42	%FSR
Integral linearity error Notes 1, 2, 3	ILE	10-bit resolution	V_{DD} = 5 V			±1.8	LSB
			V_{DD} = 3 V			±1.7	LSB
Differential linearity error Notes 1, 2, 3	DLE	10-bit resolution	V_{DD} = 5 V			±1.4	LSB
			V_{DD} = 3 V			±1.5	LSB
Analog input voltage	VAIN	Target pin: ANI0 to ANI6		0		V_{DD}	V
		Target pin: internal reference voltage Note 6		V_{REG} Note 7			V

(**Notes** are listed on the next page.)

Notes 1. TYP. Value is the average value at T_A = 25°C. MAX. value is the average value ±3σ at normal distribution.

2. These values are the results of characteristic evaluation and are not checked for shipment.

3. Excludes quantization error (±1/2 LSB).

4. This value is indicated as a ratio (%FSR) to the full-scale value.

5. Set the LV0 bit in the A/D converter mode register 0 (ADM0) to 0 when conversion is done in the operating voltage range of 2.4 V ≤ V_{DD} < 2.7 V.

6. Set the LV0 bit in the A/D converter mode register 0 (ADM0) to 0 when the internal reference voltage is selected as the target for conversion.

7. Refer to **24.6.3 Internal reference voltage characteristics**.

Cautions 1. Arrange wiring and insert the capacitor so that no noise appears on the power supply/ground line.

2. Do not allow any pulses that rapidly change such as digital signals to be input/output to/from the pins adjacent to the conversion pin during A/D conversion.

3. Note that the internal reference voltage cannot be used as the reference voltage of the comparator when the internal reference voltage is selected as the target for A/D conversion.

10. 24. 6. 4 Data retention power supply voltage characteristics (Page 568)

This shows the specifications changed in the ELECTRICAL SPECIFICATIONS of 10-pin products. The ELECTRICAL SPECIFICATIONS of “Flash ROM: 4 KB of 10-pin products and 16-pin products” will be made for the next revision of the User’s Manual: Hardware.

Old:

24.6.4 Data retention power supply voltage characteristics

(T_A = –40 to +85°C, Vss = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Data retention power supply voltage range	V_{DDDR}		1.9		5.5	V

Caution Data is retained until the power supply voltage becomes under the minimum value of the data retention power supply voltage range. Note that data in the RAM and RESF registers might not be cleared even if the power supply voltage becomes under the minimum value of the data retention power supply voltage range.

New:

24.6.6 Data retention power supply voltage characteristics

(T_A = –40 to +85°C, V_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Data retention power supply voltage	V_{DDDR}		1.9		5.5	V

Caution Data in the RESF register is retained until the power supply voltage becomes under the minimum value of the data retention power supply voltage (V_{DDDR}). Note that data in the RESF register might not be cleared even if the power supply voltage becomes under the minimum value of the data retention power supply voltage (V_{DDDR}).