Date: Feb. 1, 2017

RENESAS TECHNICAL UPDATE

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Product Category	MPU/MCU		Document No.	TN-78K-A011A/E	Rev.	1.00
Title	Correction for Incorrect Description Notice 78K0R/Lx3-M Descriptions in the User's Manual: Hardware Rev. 1.00 Changed		Information Category	Technical Notification		
Applicable Product	78K0R/Lx3-M Group	Lot No. All lots	Reference Document	78K0R/Lx3-M User's Manual: Hardware Rev. 1.00 (R01UH0182EJ0100)		

This document describes misstatements found in the 78K0R/Lx3-M User's Manual: Hardware Rev. 1.00 (R01UH0182EJ0100)

Corrections

Applicable Item	Applicable Page	Contents
15.2 Configuration of LCD Controller/Driver Figure 15-1. Block Diagram of LCD Controller/Driver	Page 619	Incorrect descriptions revised
15.3 Registers Controlling LCD Controller/Driver Figure 15-4. Format of LCD Clock Control Register (LCDC0)	Page 622	Incorrect descriptions revised

Document Improvement

The above corrections will be made for the next revision of the User's Manual: Hardware.

Corrections in the User's Manual: Hardware

No.	Corrections and Applicable Items			Pages in this document for corrections
	Document No.	English	R01UH0182EJ0100	
1	15.2 Configuration of LCD Controller/Driver Figure 15-1. Block Diagram of LCD Controller/Driver		Page 619	Page 3
2	15.3 Registers Controlling LCD Controller/Driver Figure 15-4. Format of LCD Clock Control Register (LCDC0)		Page 622	Page 4

Incorrect: Bold with underline; Correct: Gray hatched

Revision History

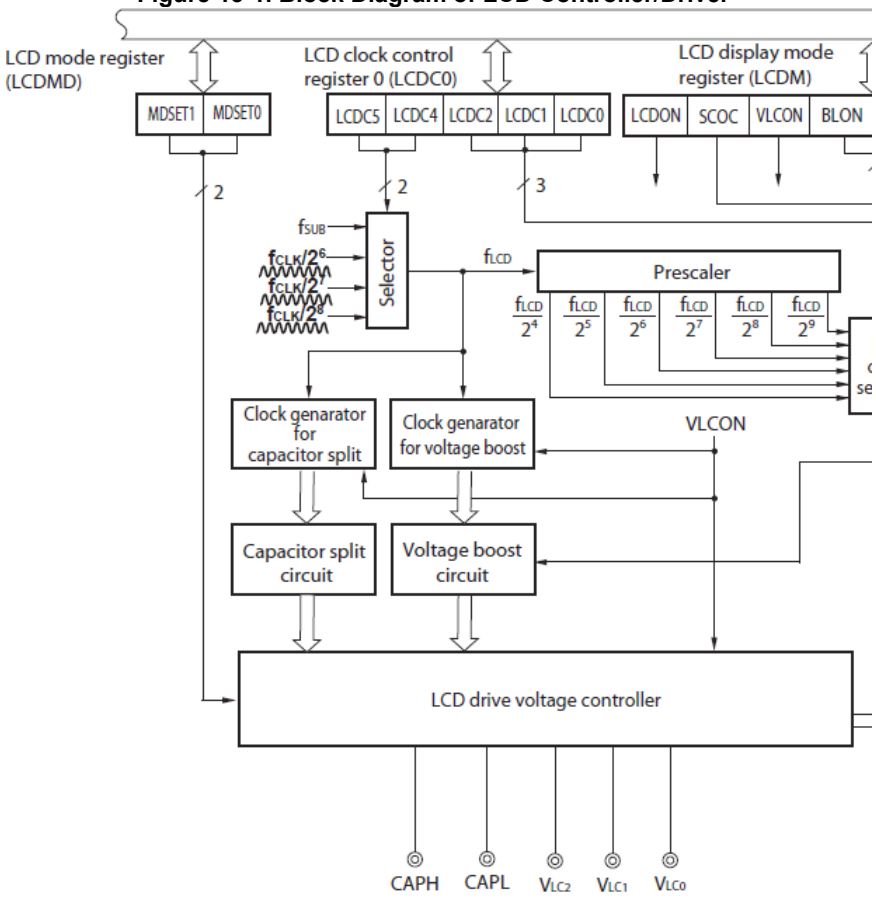
78K0R/Lx3 Correction for incorrect description notice

Document Number	Issue Date	Description
TN-78K-A011A/E	Feb. 1, 2017	First edition issued Corrections No.1 to No.2 revised (this document)

1. 15.2 Configuration of LCD Controller/Driver
   Figure 15-1. Block Diagram of LCD Controller/Driver (Page 619)

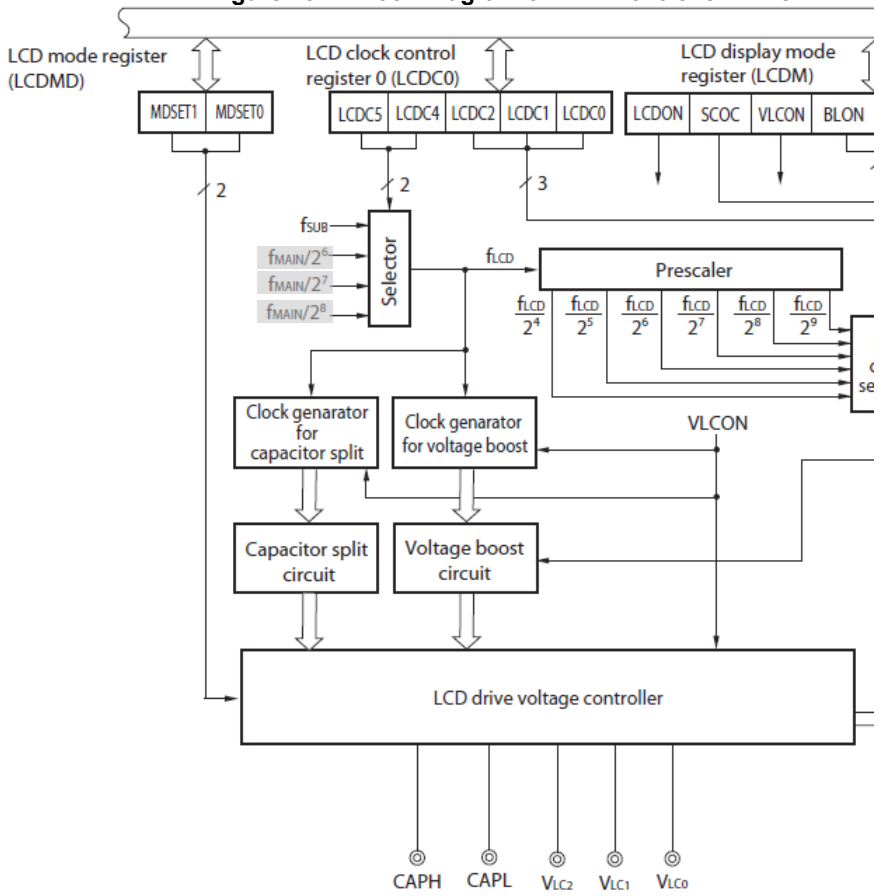
Incorrect:

Figure 15-1. Block Diagram of LCD Controller/Driver



Correct:

Figure 15-1. Block Diagram of LCD Controller/Driver



2. 15.3 Registers Controlling LCD Controller/Driver Figure 15-4. Format of LCD Clock Control Register (LCDC0) (Page 622)

Incorrect:

Figure 15-4. Format of LCD Clock Control Register (LCDC0)

Address : FFF42 H After reset : 00H R/W

Symbol	7	6	5	4	3	2	1	0
LCDC0	0	0	LCDC05	LCDC04	0	LCDC02	LCDC01	LCDC00

LCDC05	LCDC04	LCD source clock (fLCD) selection
0	0	f_{SUB}
0	1	$f_{CLK}/2^6$
1	0	$f_{CLK}/2^7$
1	1	$f_{CLK}/2^8$

LCDC02	LCDC01	LCDC00	LCD clock (LCDCL) selection
0	0	0	$f_{LCD}/2^4$
0	0	1	$f_{LCD}/2^5$
0	1	0	$f_{LCD}/2^6$
0	1	1	$f_{LCD}/2^7$
1	0	0	$f_{LCD}/2^8$
1	0	1	$f_{LCD}/2^9$
Other than above			Setting prohibited

Cautions 1. Bits 3, 6, and 7 must be set to 0.
2. Set the LCD clock (LCDCL) to no more than 512 Hz when the internal voltage boost method has been set.

Remark f_{CLK}: CPU/Peripheral hardware clock frequency
f_{SUB}: Subsystem clock frequency

Correct:

Figure 15-4. Format of LCD Clock Control Register (LCDC0)

Address : FFF42 H After reset : 00H R/W

Symbol	7	6	5	4	3	2	1	0
LCDC0	0	0	LCDC05	LCDC04	0	LCDC02	LCDC01	LCDC00

LCDC05	LCDC04	LCD source clock (fLCD) selection
0	0	f_{SUB}
0	1	$f_{MAIN}/2^6$
1	0	$f_{MAIN}/2^7$
1	1	$f_{MAIN}/2^8$

LCDC02	LCDC01	LCDC00	LCD clock (LCDCL) selection
0	0	0	$f_{LCD}/2^4$
0	0	1	$f_{LCD}/2^5$
0	1	0	$f_{LCD}/2^6$
0	1	1	$f_{LCD}/2^7$
1	0	0	$f_{LCD}/2^8$
1	0	1	$f_{LCD}/2^9$
Other than above			Setting prohibited

Cautions 1. Bits 3, 6, and 7 must be set to 0.
2. Set the LCD clock (LCDCL) to no more than 512 Hz when the internal voltage boost method has been set.

Remark f_{MAIN}: Main system clock frequency
f_{SUB}: Subsystem clock frequency