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RENESAS TECHNICAL UPDATE

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Product Category	MPU/MCU		Document No.	TN-RA*-A0062A/E	Rev.	1.00
Title	Correction for CoreSight ROM Table in RA2L1/RA2E1/RA2E2 User's Manual		Information Category	Technical Notification		
Applicable Product	RA2L1/RA2E1/RA2E2 Group	Lot No. All	Reference Document	Renesas RA2L1 Group User's Manual : Hardware Rev1.20 Renesas RA2E1 Group User's Manual : Hardware Rev1.20 Renesas RA2E2 Group User's Manual : Hardware Rev.1.10		

Chapter 2.5.4.2 CoreSight component registers

Table 2.8 CireSight component resgisters in the CoreSight ROM Table (2 of 2)

Initial value of PID0 should be corrected.

[Before]

Table 2.8 CoreSight component registers in the CoreSight ROM Table (2 of 2)

Name	Address	Access size	R/W	Initial value
PID7	0xE00F_FFDC	32 bits	R	0x00000000
PID0	0xE00F_FFE0	32 bits	R	0x0000001B
PID1	0xE00F_FFE4	32 bits	R	0x00000030
PID2	0xE00F_FFE8	32 bits	R	0x0000000A
PID3	0xE00F_FFEC	32 bits	R	0x00000000
CID0	0xE00F_FFF0	32 bits	R	0x0000000D
CID1	0xE00F_FFF4	32 bits	R	0x00000010
CID2	0xE00F_FFF8	32 bits	R	0x00000005
CID3	0xE00F_FFFC	32 bits	R	0x000000B1

[After]

1. Renesas RA2L1 Group User's Manual: Hardware Rev1.20

   Initial value of PID0 should be corrected to 0x000000**2F.**

Table 2.8 CoreSight component registers in the CoreSight ROM Table (2 of 2)

Name	Address	Access size	R/W	Initial value
PID7	0xE00F_FFDC	32 bits	R	0x00000000
PID0	0xE00F_FFE0	32 bits	R	0x0000002F
PID1	0xE00F_FFE4	32 bits	R	0x00000030
PID2	0xE00F_FFE8	32 bits	R	0x0000000A
PID3	0xE00F_FFEC	32 bits	R	0x00000000
CID0	0xE00F_FFF0	32 bits	R	0x0000000D
CID1	0xE00F_FFF4	32 bits	R	0x00000010
CID2	0xE00F_FFF8	32 bits	R	0x00000005
CID3	0xE00F_FFFC	32 bits	R	0x000000B1

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2. Renesas RA2E1 Group User's Manual: Hardware Rev1.20
   Initial value of PID0 should be corrected to 0x00000**39**.

Table 2.8 CoreSight component registers in the CoreSight ROM Table (2 of 2)

Name	Address	Access size	R/W	Initial value
PID7	0xE00F_FFDC	32 bits	R	0x00000000
PID0	0xE00F_FFE0	32 bits	R	0x00000**39**
PID1	0xE00F_FFE4	32 bits	R	0x00000030
PID2	0xE00F_FFE8	32 bits	R	0x0000000A
PID3	0xE00F_FFEC	32 bits	R	0x00000000
CID0	0xE00F_FFF0	32 bits	R	0x0000000D
CID1	0xE00F_FFF4	32 bits	R	0x00000010
CID2	0xE00F_FFF8	32 bits	R	0x00000005
CID3	0xE00F_FFFC	32 bits	R	0x000000B1

3. Renesas RA2E2 Group User's Manual: Hardware Rev1.10
   Initial value of PID0 should be corrected to 0x000000**3D**.

Table 2.8 CoreSight component registers in the CoreSight ROM Table (2 of 2)

Name	Address	Access size	R/W	Initial value
PID7	0xE00F_FFDC	32 bits	R	0x00000000
PID0	0xE00F_FFE0	32 bits	R	0x000000**3D**
PID1	0xE00F_FFE4	32 bits	R	0x00000030
PID2	0xE00F_FFE8	32 bits	R	0x0000000A
PID3	0xE00F_FFEC	32 bits	R	0x00000000
CID0	0xE00F_FFF0	32 bits	R	0x0000000D
CID1	0xE00F_FFF4	32 bits	R	0x00000010
CID2	0xE00F_FFF8	32 bits	R	0x00000005
CID3	0xE00F_FFFC	32 bits	R	0x000000B1