To our customers,

Old Company Name in Catalogs and Other Documents

On April 1st, 2010, NEC Electronics Corporation merged with Renesas Technology Corporation, and Renesas Electronics Corporation took over all the business of both companies. Therefore, although the old company name remains in this document, it is a valid Renesas Electronics document. We appreciate your understanding.

Renesas Electronics website: http://www.renesas.com

April 1st, 2010
Renesas Electronics Corporation

Issued by: Renesas Electronics Corporation (http://www.renesas.com)

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RENESAS TECHNICAL UPDATE

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Renesas Technology Corp.

Product Category	MPU&MCU		Document No.	TN-SH7-A586A/E	Rev.	1.00
Title	Amendment of SH7720 Hardware manual(3)		Information Category	Technical Notification		
Applicable Product	HD6417720	Lot No. All	Reference Document	SH7720 hardware manual Rev2.00 (REJ09B0033-0200)		

There are the amendments of a Bus State Controller (BSC).

1. Page 280 of 1382 9.4.1 Common Control Register (CMNCR) "Bit15 WAITSEL" deleted.
   This bit is always read as 0. The write value should always be 0.
   Samples the $\overline{\text{WAIT}}$ signal at the falling edge of the CKIO and can be input asynchronously.

2. Page 315 of 1382 9.4.4 SDRAM Control Register (SDCR) "Bit12 SLOW" deleted.
   This bit is always read as 0. The write value should always be 0.
   Command, address, and write data for SDRAM is output at the rising edge of CKIO. Read data from SDRAM is latched at the rising edge of CKIO.

As related to No.1 and No.2, the following descriptions are also modified.

3. Page 367 of 1382 9.5.5 SDRAM Interface "Low-Frequency Mode" deleted.
4. Page 367 of 1382 "Figure 9.27 Access Timing in Low-Frequency Mode" deleted.
5. Page 1222 of 1382 37.2 Register Bits CMNCR "Bit15 WAITSEL" deleted.
6. Page 1225 of 1382 37.2 Register Bits SDCR "Bit12 SLOW" deleted.
7. Page 1313 of 1382
   "Figure 38.37 Access Timing in Low-Frequency Mode of SDRAM (Auto Precharge Mode, TRWL = 1 Cycle)" deleted.
8. Page 1314 of 1382
   "Figure 38.38 Auto Refresh Timing in Low-Frequency Mode of SDRAM (TRP = 2 Cycles)" deleted.
9. Page 1315 of 1382
   "Figure 38.39 Self Refresh Timing in Low-Frequency Mode of SDRAM (TRP = 2 Cycles)" deleted.
10. Page 1316 of 1382
    "Figure 38.40 Power-On Sequence in Low-Frequency Mode of SDRAM (Mode Write Timing, TRP = 2 Cycles)" deleted.