Date: Aug. 7, 2015

# RENESAS TECHNICAL UPDATE

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| Product Category | System LSI | | Document No. | TN-RIN-A006A/E | Rev. | 1.00 |
|---|---|---|---|---|---|---|
| Title | AC characteristics update for external microcomputer interface | | Information Category | Technical Notification | | |
| Applicable Product | See following | Lot No.<br>All lots | Reference Document | R-IN32M3 Series Datasheet (R18DS0008EJ0204)<br>R-IN32M3 Series User's Manual Peripheral Functions R-IN32M3-CL R-IN32M3-EC (R18UZ0005EJ0601) | | |

AC characteristics in R-IN32 Series Datasheet is updated and a note is added in User's Manual as below.

1. Applicable Product

| Product Type | Model Marking | Product Code |
|---|---|---|
| R-IN32M3-EC | MC-10287F1 | MC-10287F1-HN4-A |
| | | MC-10287F1-HN4-M1-A |
| R-IN32M3-CL | D60510F1 | UPD60510F1-HN4-A |
| | | UPD60510F1-HN4-M1-A |

2. Documentation update

A) R-IN32M3 Series Datasheet

AC timing definitions for external microcomputer interface are missing in the datasheet. The following specification and timing chart are revised.

And the specification of wait active time for asynchronous mode, $t_{WRWAITF}$ and $t_{RDWAITF}$, is changed.

– 4.7.4 External microcomputer interface signal

(1) Synchronous mode

Regarding added timing definitions, this TU will be update as soon as symbol and value are decided.

| | # | Parameter | Symbol | MIN | MAX | Unit |
|---|---|---|---|---|---|---|
| | 1 | HBUSCLK high level width | $t_{HBHIGH}$ | $0.5t_{HBCYC}$-2.1 | $0.5t_{HBCYC}$+2.1 | ns |
| | 2 | HBUSCLK low level width | $t_{HBLOW}$ | $0.5t_{HBCYC}$-2.1 | $0.5t_{HBCYC}$+2.1 | ns |
| | 3 | HBUSCLK input cycle | $t_{HBUSCLK}$ | 20.0 | - | ns |
| | 4 | Address, HCSZ/HPGCSZ input setup time | $t_{SKHA}$ | 4.0 | - | ns |
| | 5 | HBENZ0-HBENZ3 (HWRZ0-HWRZ3), HWRSTZ input setup time | $t_{SKHWR}$ | 4.0 | - | ns |
| | 6 | Address, HCSZ/HPGCSZ input hold time | $t_{HKHA}$ | 1.0 | - | ns |
| | 7 | HBENZ0-HBENZ3 (HWRZ0-HWRZ3), HWRSTBZ input hold time | $t_{HKHWR}$ | 1.0 | - | ns |
| Added | 8 | HWRZ0-HWRZ3, HWRSTBZ recovery time (high width) | | | | ns |
| | 9 | Data setup time | $t_{SKIHD}$ | 4.0 | - | ns |
| | 10 | Data hold time | $t_{HKIHD}$ | 1.0 | - | ns |
| Added | 11 | Data, HWAITZ output delay time | | | | |
| Added | 12 | HWAITZ output delay time | | | | ns |
| Added | 13 | HWAITZ valid data output delay time | | | | ns |
| Added | 14 | HWAITZ valid data hold time | | | | ns |
| Added | 15 | HWIATZ output hold time | | | | ns |
| Added | 16 | Data, HWAITZ output hold time | | | | ns |
| Added | 17 | Address, HCSZ, HPGCSZ input setup time (HRDZ fall edge) | | | | ns |
| Added | 18 | Address, HCSZ/HPGCSZ input hold time (HRDZ rise edge) | | | | ns |
| Added | 19 | HRDZ recovery time (high width) | | | | ns |
| Added | 20 | Data, HWAITZ output delay time (HRDZ fall edge) | | | | ns |
| Added | 21 | HWAITZ valid data output delay time (HRDZ fall edge) | | | | ns |
| Added | 22 | Data setup time | | | | ns |
| Added | 23 | Data, HWAITZ valid data output hold time | | | | ns |
| | 24 | Data, HWAITZ output delay time (HRDZ rise edge) | $t_{HKOHD}$ | 2.0 | 10.0 | ns |
| Added | 25 | Data, HWAITZ output delay time when on-page access | | | | ns |
| Added | 26 | Data, HWAITZ output delay time when off-page access | | | | ns |
| Added | 27 | HWAITZ valid data output delay time | | | | ns |

(a) SRAM and Page ROM write timing

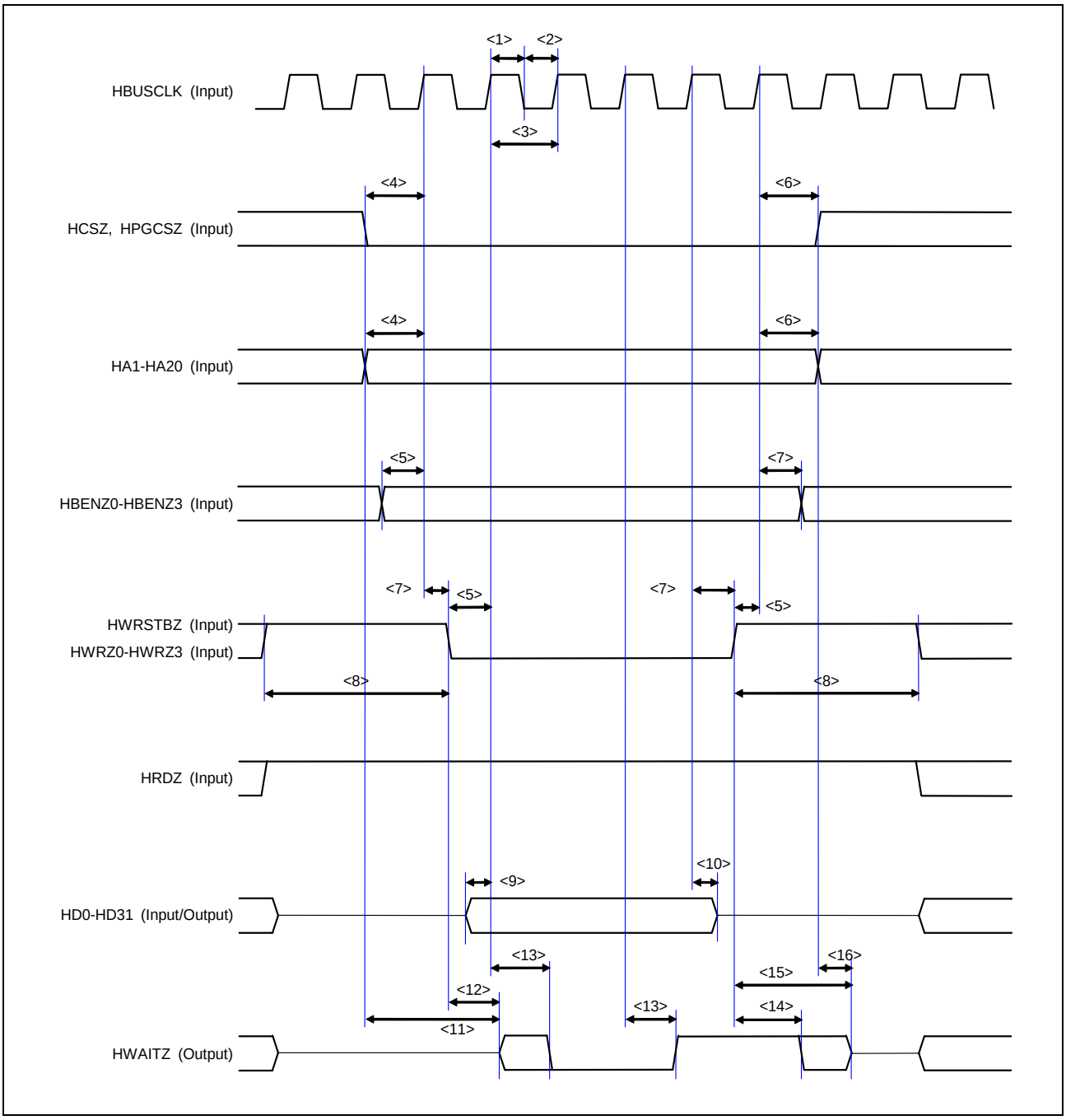


Figure External microcomputer interface write timing (SRAM and Page ROM)

(b) SRAM read timing

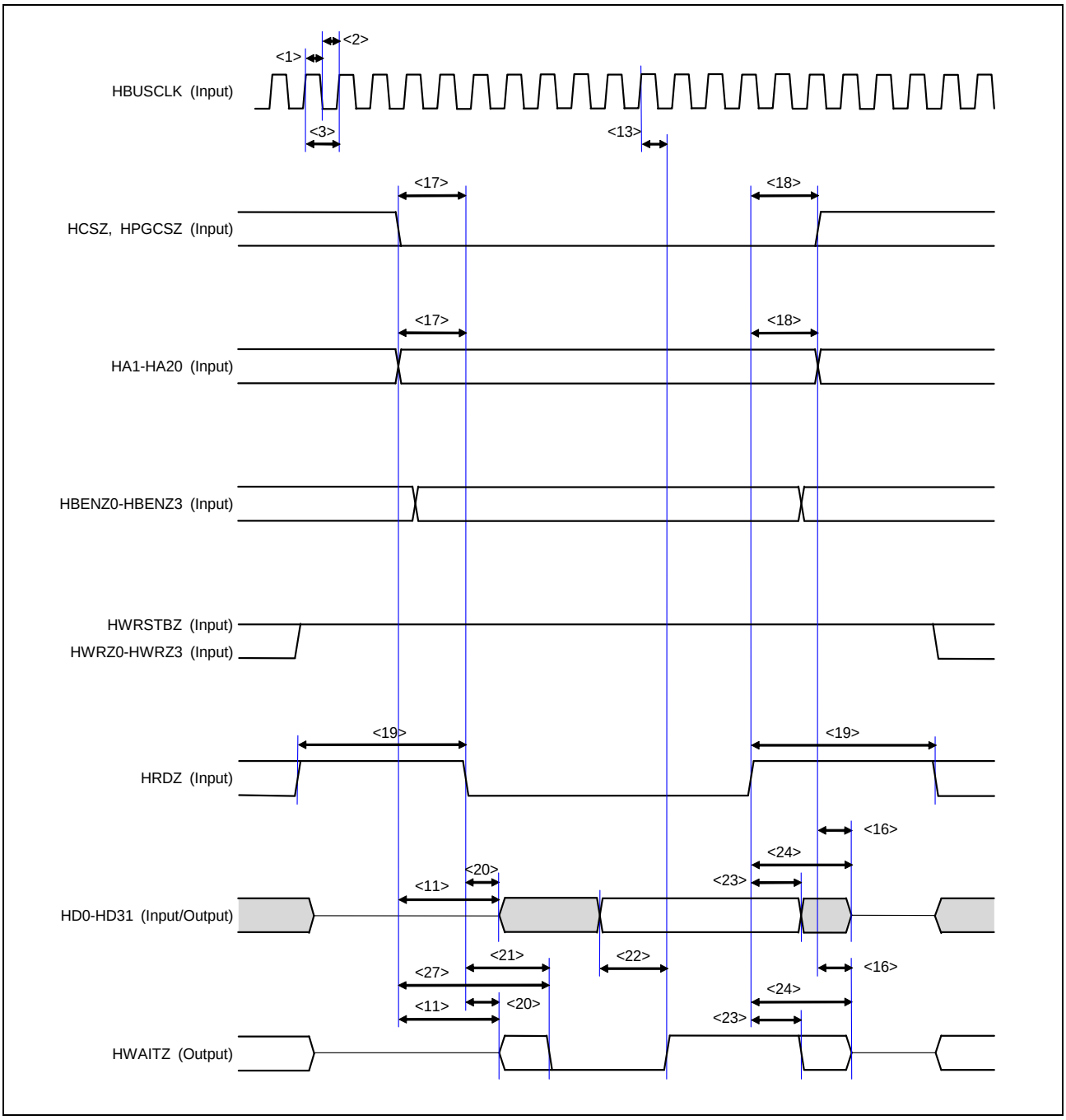


Figure External microcomputer interface read timing (SRAM)

(c) Page ROM read timing

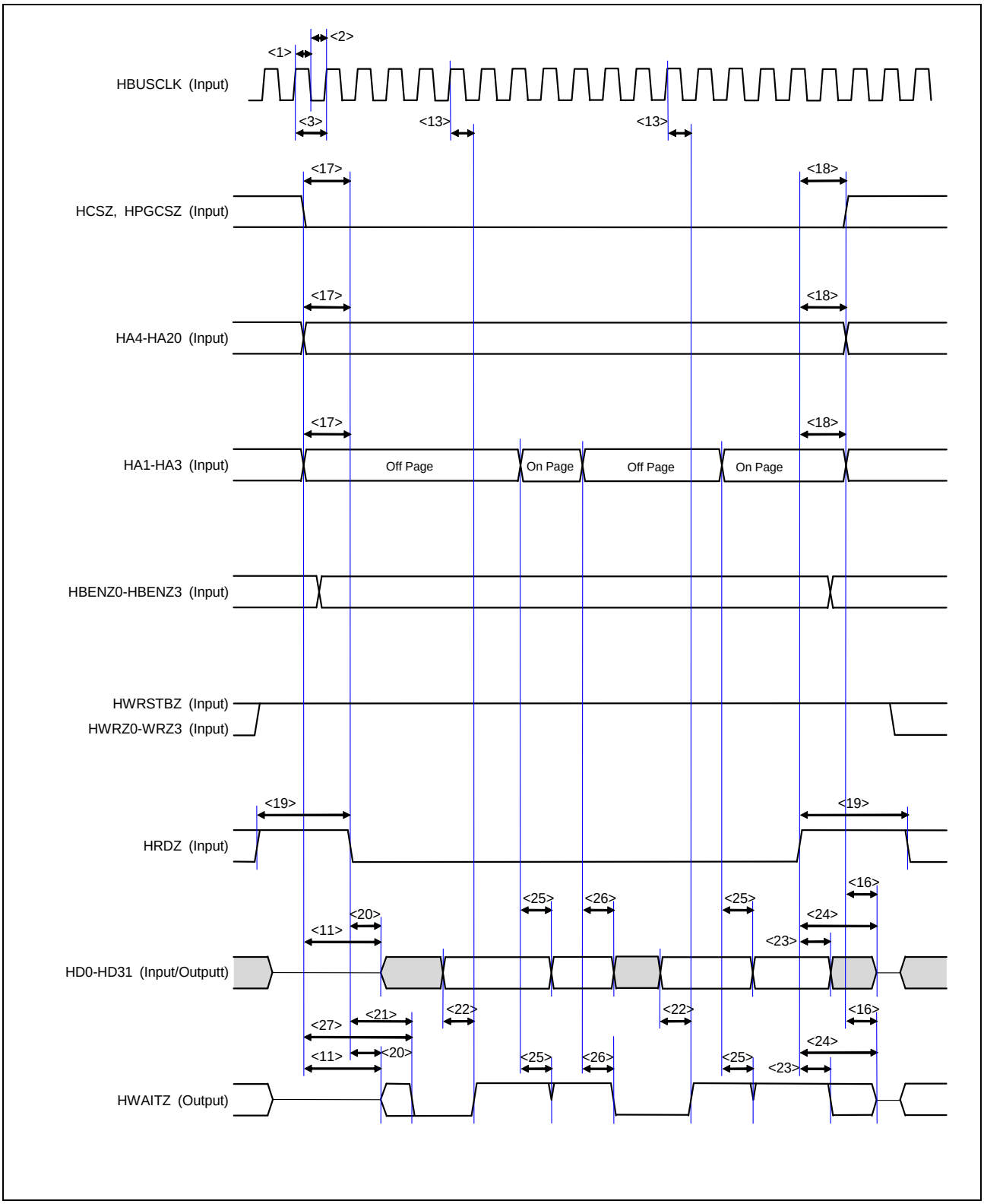


Figure External microcomputer interface read timing (Page ROM)

(2) Asynchronous mode

Regarding added timing definitions, this TU will be update as soon as symbol and value are decided.

Wait active time, $t_{WRWAITF}$ and $t_{RDWAITF}$, was changed from 10.0ns to 40.0ns.

| | # | Parameter | Symbol | MIN | MAX | Unit |
|---|---|---|---|---|---|---|
| Added | 1 | Address, HCSZ/HPGCSZ, HBENZ0-HBENZ3 input setup time | | | | ns |
| Added | 2 | Address, HCSZ/HPGCSZ, HBENZ0-HBENZ3 input hold time | | | | ns |
| Added | 3 | HWRZ0-HWRZ3, HWRSTBZ recovery time (high width) | | | | ns |
| | 4 | HWRZ0-3, HWRSTBZ to data setup | $t_{WRS}$ | 1.0 *2 | - | ns |
| Added | 5 | HWRZ0-3, HWRSTBZ to data hold | | | | ns |
| Added | 6 | HWAITZ output delay time (Address, HCSZ/HPGCSZ) | | | | ns |
| Added | 7 | HWAITZ output delay time (HWRSTBZ, HWRZ0-HWRZ3) | | | | ns |
| Revised | 8 | HWRZ0-3, HWRSTBZ to wait active | $t_{WRWAITF}$ | - | **40.0** | ns |
| Added | 9 | HWRZ0-3, HWRSTBZ to wait hold | | | | ns |
| Added | 10 | Data, HWAITZ output hold time (HWRZ0-HWRZ3, HERSTBZ) | | | | ns |
| Added | 11 | Data, HWAITZ output hold time (Address, HCSZ/HPGCSZ) | | | | ns |
| Added | 12 | HRDZ to Address, HCSZ/HPGCSZ setup time | | | | ns |
| Added | 13 | HRDZ to Address, HCSZ/HPGCSZ hold time | | | | ns |
| Added | 14 | HRDZ recovery time (high width) | | | | ns |
| | 15 | Data, HWAITZ output delay time | $t_{RDLZ}$ | - | 10.0 | ns |
| Revised | 16 | HRDZ to wait active | $t_{RDWAITF}$ | - | **40.0** | ns |
| | 17 | Data valid to wait inactive | $t_{WAITR}$ | 10.0 *1 | - | ns |
| Added | 18 | Data, HWAITZ valid data output hold time | | | | ns |
| | 19 | Data, HWAITZ output hold time | $t_{RDHZ}$ | 3.0 | - | ns |
| Added | 20 | Data, HWAITZ output delay time when on-page access | | | | ns |
| Added | 21 | Data, HWAITZ output delay time when off-page access | | | | ns |
| Added | 22 | Data hold time when on-page access | | | | ns |
| Added | 23 | Data hold time when off-page access | | | | ns |
| Added | 24 | HWAITZ valid data output delay time | | | | ns |

Note: *1 At the case RDDTS1-0 bits on HIFBTC register is set to 01B. This value can be changed between 10ns and 30ns by register setting

*2 At the case WRSTD1-0 bits on HIFBTC register is set to 01B. This value can be changed between -70ns and +1ns by register setting.

(a) SRAM and Page ROM write timing

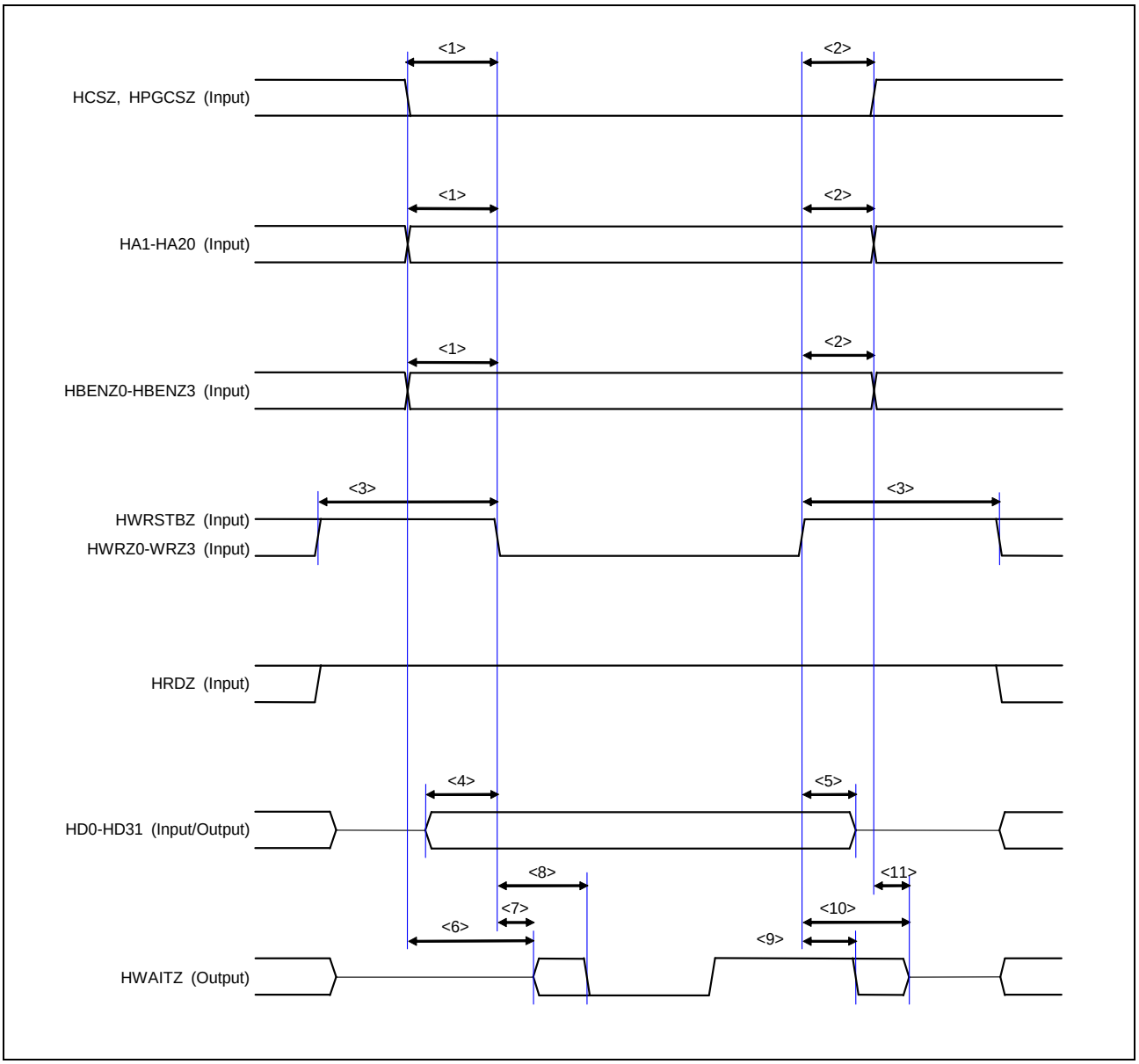


Figure External microcomputer interface write timing (SRAM and Page ROM)

(b) SRAM read timing

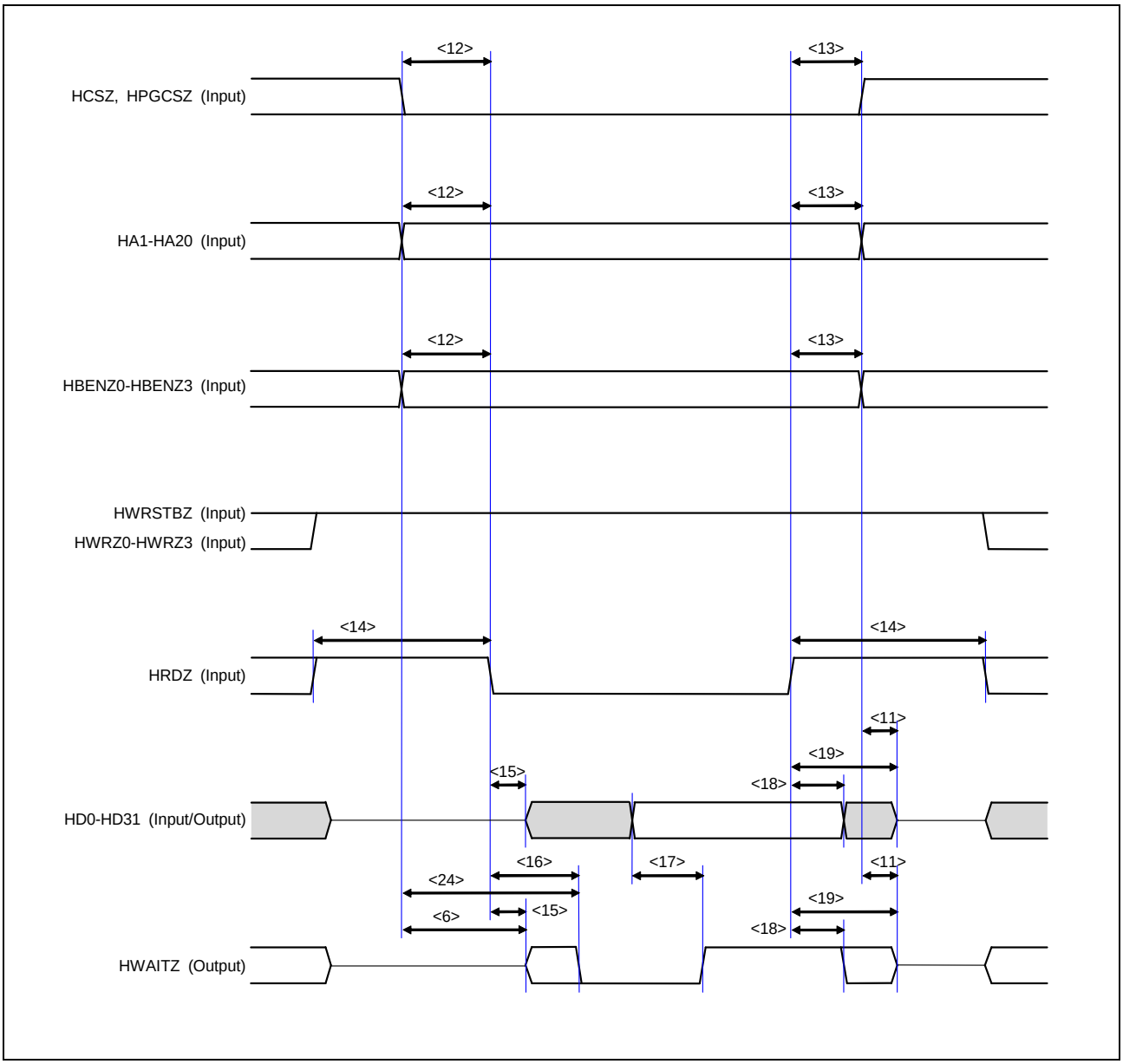


Figure External microcomputer interface read timing (SRAM)

(c) Page ROM read timing

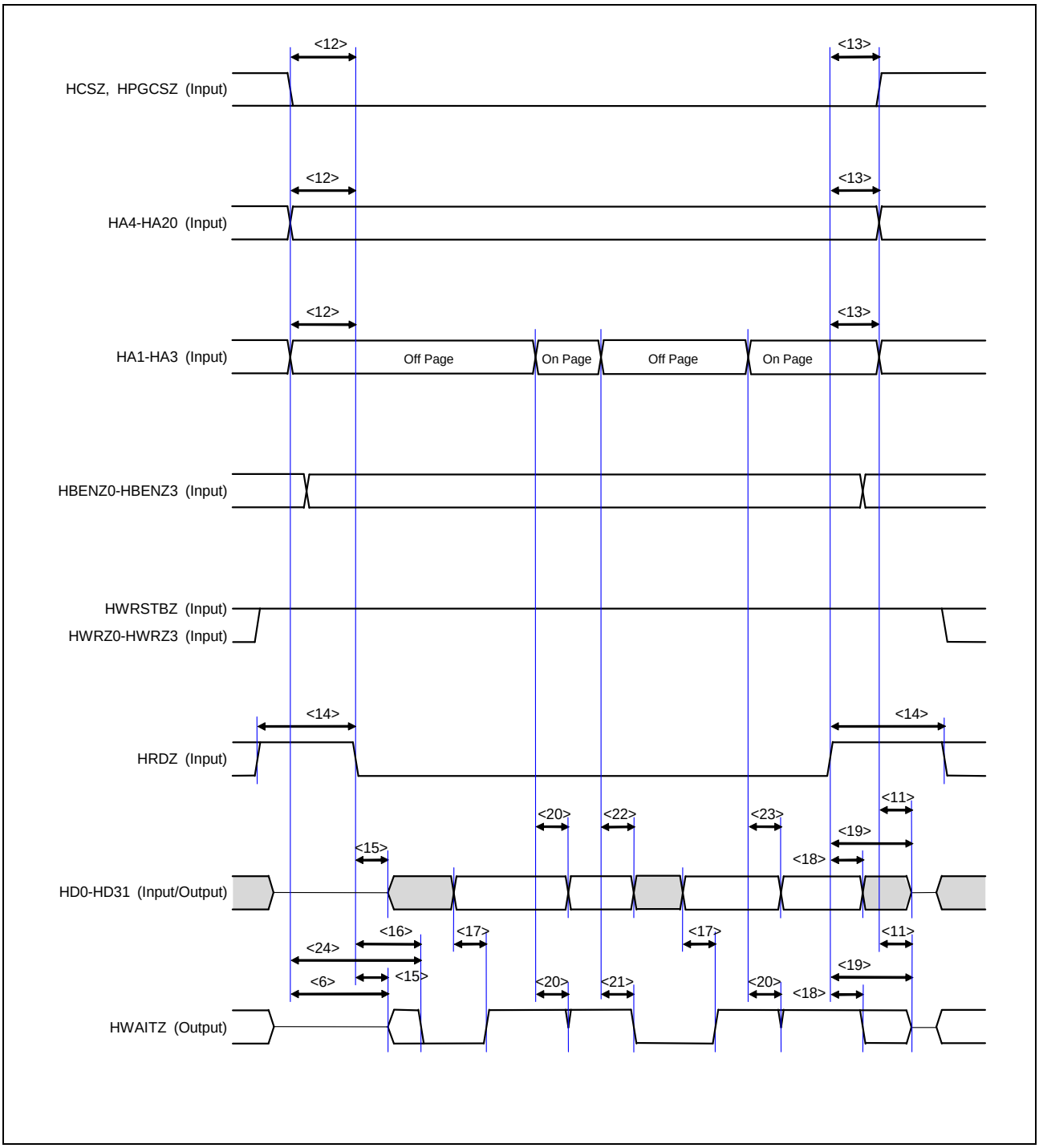


Figure External microcomputer interface read timing (Page ROM)

(3) Synchronous SRAM type transmission mode

All timing definitions are newly added. This TU will be update as soon as symbol and value are decided.

| # | Parameter | Symbol | MIN | MAX | Unit |
|---|---|---|---|---|---|
| 1 | HBUSCLK input cycle | | | - | ns |
| 2 | HBUSCLK high level width | | | | ns |
| 3 | HBUSCLK low level width | | | | ns |
| 4 | Address, HCSZ/HPGCSZ input setup time (HBUSCLK rise edge) | | | | ns |
| 5 | Address, HCSZ/HPGCSZ input hold time (HBUSCLK rise edge) | | | | ns |
| 6 | Address, HCSZ/HPGCSZ input setup time (HBUSCLK fall edge) | | | | ns |
| 7 | Address, HCSZ/HPGCSZ input hold time (HBUSCLK fall edge) | | | | ns |
| 8 | HWRZ0-HWRZ3 input setup time (HBUSCLK rise edge) | | | | ns |
| 9 | HWRZ0-HWRZ3 input hold time (HBUSCLK rise edge) | | | | ns |
| 10 | HWRZ0-HWRZ3 input setup time (HBUSCLK fall edge) | | | | ns |
| 11 | HWRZ0-HWRZ3 input hold time (HBUSCLK fall edge) | | | | ns |
| 12 | HBCYSTZ, HWRSTBZ input setup time (HBUSCLK rise edge) | | | | ns |
| 13 | HBCYSTZ, HWRSTBZ input hold time (HBUSCLK rise edge) | | | | ns |
| 14 | HBCYSTZ, HWRSTBZ input setup time (HBUSCLK fall edge) | | | | ns |
| 15 | HBCYSTZ, HWRSTBZ input hold time (HBUSCLK fall edge) | | | | ns |
| 16 | HRDZ input setup time (HBUSCLK rise edge) | | | | ns |
| 17 | HRDZ input hold time (HBUSCLK rise edge) | | | | ns |
| 18 | HRDZ input setup time (HBUSCLK fall edge) | | | | ns |
| 19 | HRDZ input hold time (HBUSCLK fall edge) | | | | ns |
| 20 | Data input setup time (HBUSCLK rise edge) | | | | ns |
| 21 | Data input hold time (HBUSCLK rise edge) | | | | ns |
| 22 | Data input setup time (HBUSCLK fall edge) | | | | ns |
| 23 | Data input hold time (HBUSCLK fall edge) | | | | ns |
| 24 | Data output delay time (HBUSCLK rise edge) | | | | ns |
| 25 | Data output float time (HBUSCLK rise edge) | | | | ns |
| 26 | Data output delay time (HBUSCLK fall edge) | | | | ns |
| 27 | Data output float time (HBUSCLK fall edge) | | | | ns |
| 28 | HWAITZ output delay time (HBUS rise edge) | | | | ns |
| 29 | HWAITZ output delay time (HBUS fall edge) | | | | ns |
| 30 | Data output hold time (HCSZ/HPGCSZ rise edge) | | | | ns |

(a) Write timing

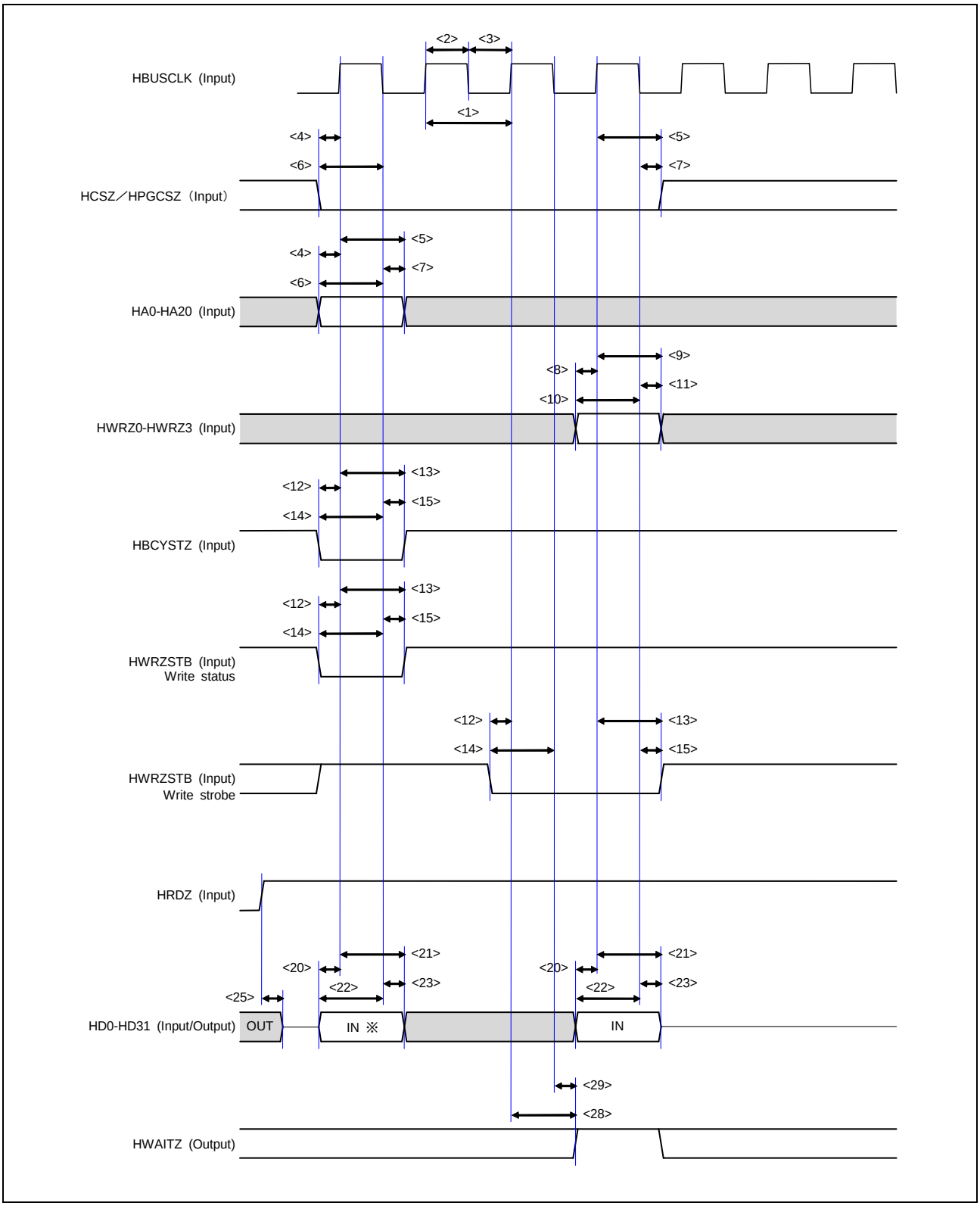


Figure External microcomputer interface write timing (Address/Data Multiplex)

(b) Read timing

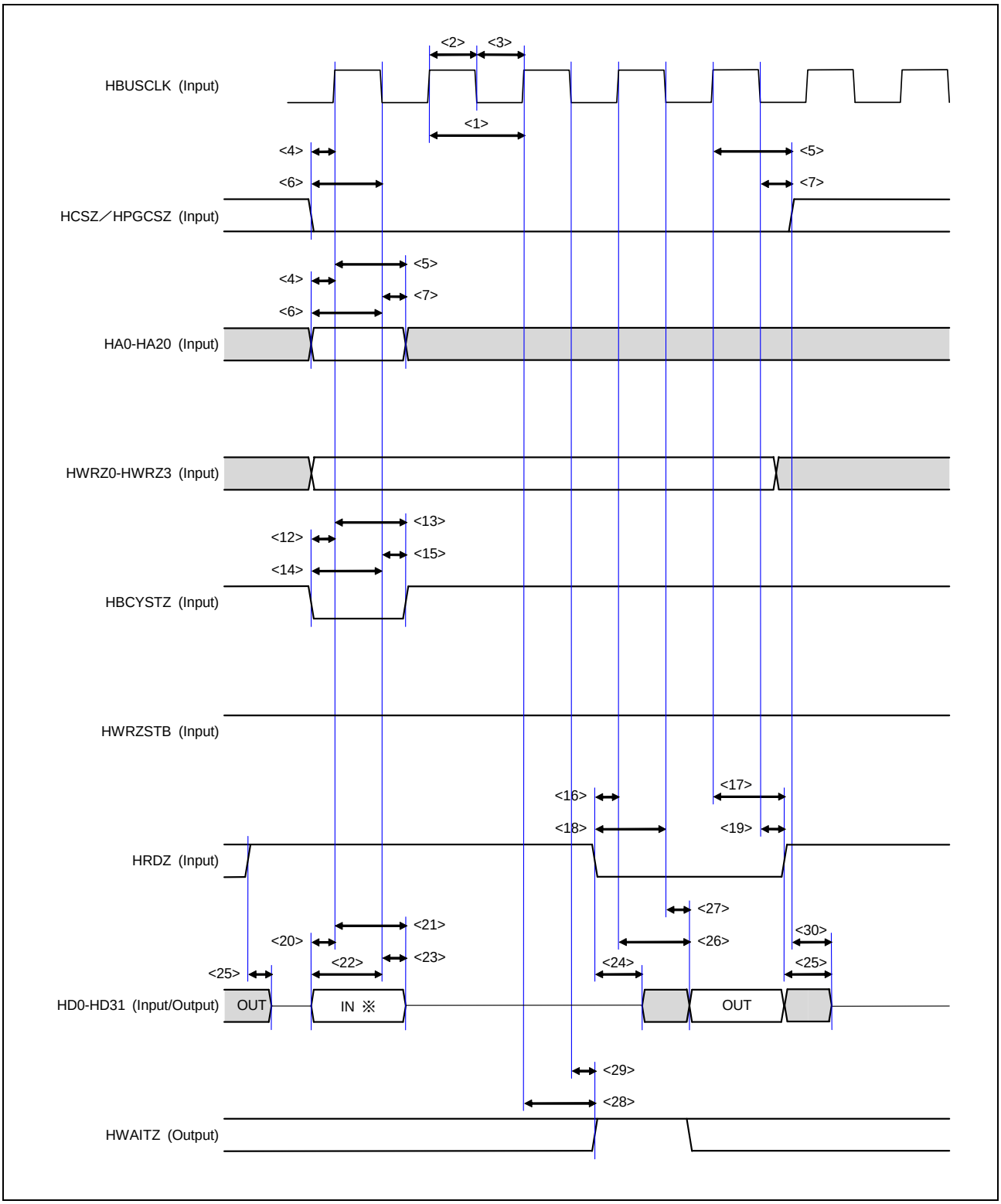


Figure External microcomputer interface read timing (Address/Data Multiplex)

B) R-IN32M3 Series User's Manual Peripheral Functions R-IN32M3-CL R-IN32M3-EC

The following note is added in 11. External Microcomputer Interface.

"Note: During a bus request for external microcomputer interface, address value must not vary. If address is changed during read access, it causes that incorrect data is returned and HWAITZ signal is NOT de-asserted."

3. Release schedule

| Document Title | Issue Date |
|---|---|
| R-IN32M3 Series Datasheet | Aug 7, 2015 |
| R-IN32M3 Series User's Manual Peripheral Functions R-IN32M3-CL R-IN32M3-EC | Aug 31, 2015 |