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RENESAS TECHNICAL UPDATE

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Product Category	MPU/MCU		Document No.	TN-450-A012A/E	Rev.	1.00
Title	4571 Group Corrections for Timer Control Register PA		Information Category	Technical Notification		
Applicable Product	M34571G4FP M34571G4-XXXFP M34571G6FP M34571G6-XXXFP M34571GDFP M34571GD-XXXFP	Lot No. ——	Reference Document	4571 Group Datasheet		

Please be advised that the 4571 Group datasheet (REJ03B0179-0102, Rev.1.02) has been revised as corrections have been made to timer control register PA.

1. Corrections

Timer control register PA is not initialized in RAM back-up mode (00_2) and the setting value is retained. When the MCU enters RAM back-up mode while bit 1 (prescaler count source selection bit) in register PA is set to 1, the MCU does not exit RAM back-up mode even if a return signal is input. When using RAM back-up mode, set bit 1 in register PA to 0 by a program and enter RAM back-up mode.

Program Example

```
        ; Processing to set prescaler
LA   3  ; 11₂
TPAA    ; Set 11₂ to the register PA
        ; Operate prescaler and select INSTCK divided by 4.

    ⋮
    ⋮   ; Use the prescaler.

        ; Processing to enter RAM back-up mode
LA   0  ; 00₂ or 01₂
TPAA    ; Set 0 to the register PA1.
        ; Select prescaler count source INSTCK.

    ⋮
DI
EPOF
POF
    ⋮
    ⋮
```

When bit 0 in register PA is 1, the MCU exits RAM back-up mode and the prescaler operates when the program starts operating. However, since the prescaler value becomes undefined, execute the TPSAB instruction and set the value to the prescaler after stopping the count.

2. Revisions in the Datasheet (4571 Group, REJ03B0179-0102, Rev.1.02)

2.1 Control Registers (pages 30 and 64)

Before (Incorrect)

Timer control register PA		at reset : 00_2	at RAM back-up : **00_2**	W TPAA
PA1	Prescaler count source selection bit	0	Instruction clock (INSTCK)	
		1	Instruction clock divided by 4 (INSTCK/4)	
PA0	Prescaler control bit	0	Stop (**state initialized**) *	
		1	Operating	

After (Correct)

Timer control register PA		at reset : 00_2	at RAM back-up : **state retained** (1)	W TPAA
PA1	Prescaler count source selection bit	0	Instruction clock (INSTCK)	
		1	Instruction clock divided by 4 (INSTCK)/4	
PA0	Prescaler control bit	0	Stop (**state retained**) *	
		1	Operating	

Note 1. When using RAM back-up mode, set the value in PA1 to 0 by a program and enter RAM back-up mode.

* The description of 0 for PA0 (prescaler control bit) has also been revised.

2.2 Functions and States Retained at RAM Back-Up (page 44)

Before (incorrect)

Functions	RAM back-up
Timer control registers **PA**, W3	x
Timer control registers W1, W2, W5	O

"O" represents that the function can be retained, and "x" represents that the function is initialized.

After (correct)

Functions	RAM back-up
Timer control registers W3	x
Timer control registers W1, W2, W5, **PA**	O

"O" represents that the function can be retained, and "x" represents that the function is initialized.

3. Revisions for Datasheet and Customer Standard Specification

Revisions will be made to the 4571 Group Datasheet Rev. 1.02 and issued as Rev.1.03. Please note that issued customer standard specifications will be changed to warranty information according to this technical notification. Contact a Renesas Electronics sales department when the customer standard specifications needs to be issued after these revisions are made.