RENESAS TECHNICAL UPDATE

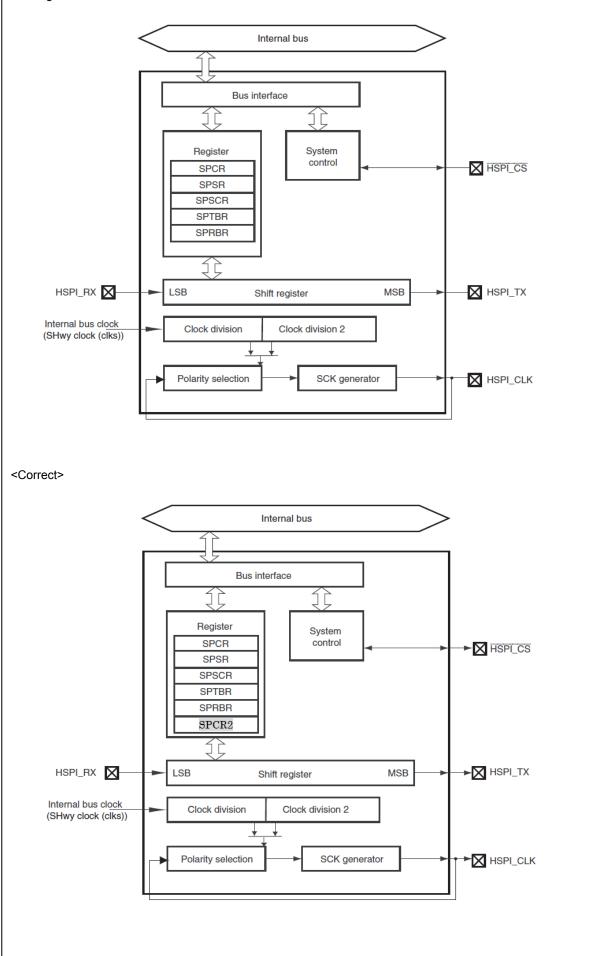
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Product Category	MPU/MCU	Document No.	TN-SH7-A857A/E	Rev.	1.00				
Title	Correct SH7734 User's Manual:Hardware(HSPI)		Information Category	Technical Notification					
Applicable Product	SH7734 Lot No.		Reference Document	SH7734 User's Manual: Hardware Rev.1.00 (R01UH0233EJ0100)					
There is correction and addition to explanation of "18.Serial Peripheral Interface (HSPI)" in SH7734 User's Manual. The correction is shown by shading.									
1. Correct t <wrong></wrong>	o "18.1.1 Features" in page 1567								
-	DMA transfer of data for transmission and rece	eived data is	possible throug	h two DMA channels.					
<correct> Independent</correct>	DMA transfer of data for transmission and rece DMA transfer of dat a for transmission and re in master mode are supported as high-speed	ceived data	is possible thro	bugh two DMA channel	s. Transm	iission			



2. Correct to "Figure 18.1 Block Diagram of HSPI" in page 1568

<Wrong>





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<wrong></wrong>	00000		1.114.0	22		
Receive buffer register	SPRBR	R	H'10	32		
<correct></correct>						
Receive buffer register	SPRBR	R	H'10	32		
Control register 2	SPCR2	R/W	H'14	32		
4. Correct to "Table 18.2(2)) Register State in E	ach Opera	ting Mode"	in page 1570		
<wrong></wrong>						
SPRBR Initializ	zed Initialize	d F	Retained	Retained	Retained	Initialized
<correct></correct>				D / I / I	D <i>i i</i> i	
SPRBR Initializ			Retained	Retained	Retained	Initialized
SPCR2 Initializ	zed Initialize	a F	Retained	Retained	Retained	Initialized
18.2.6 Control Register 2 (\$ SPCR2 is a 32-bit readable a	and writable register	that is use	ed to set the c	clock frequency fo	or data transfer v	when transfer is to b
18.2.6 Control Register 2 (SPCR2 is a 32-bit readable a at a higher rate than that set	and writable register in the SPCR. in master mode are 1 30 29 28 - - - - - - - - - - - - - - - - - - - - - - - - - - - - - 5 14 13 12 E - - - - - - - - -	supported 27 26 — — — R R 11 10 — скнр4 с — 0	as high-spee 25 24 2 — — — — R R F 9 8 7	d modes for use v 3 22 21 20 3 R R R 7 6 5 4 HP1 CKHP0ckcycs ckcy 0 0 0 0	vith DMA transfe 19 18 1' — — — — R R F 3 2 1 ^{C4} cксүсэ cксүс2 cкс 0 0 0 0	Pr. 7 16 7 R 8 R 0 YC1 CKCYC0 0 0
Initial value: — R/W: R Bit: 15 HF Initial value: 0 R/W: R/V	and writable register in the SPCR. in master mode are $\frac{1}{10}$ $\frac{30}{29}$ $\frac{28}{28}$ $\frac{1}{28}$ $\frac{1}{28}$ $\frac{29}{28}$ $\frac{1}{28}$ $\frac{1}{29}$ $\frac{28}{28}$ $\frac{1}{28}$ $\frac{1}{29}$ $\frac{28}{28}$ $\frac{1}{28}$ $\frac{1}{29}$ $\frac{28}{28}$ $\frac{1}{28}$ $\frac{1}{29}$ $\frac{28}{28}$ $\frac{1}{28}$ $\frac{1}{29}$ $\frac{28}{28}$ $\frac{1}{29}$ $\frac{1}{29}$ $\frac{28}{28}$ $\frac{1}{29}$ $\frac{1}{29}$ $\frac{1}{29}$ $\frac{1}{29}$ $\frac{1}{29}$ $\frac{1}{29}$ 1	supported <u>27</u> <u>26</u> <u>—</u> — R R 11 10 <u>—</u> СКНР4 СКНР4 СКНР4	25 24 22 — — — — — — R R F 9 8 7 СКНРЗ СКНР2 СКНР2 0 0 С	d modes for use v 3 22 21 20 3 R R R 7 6 5 4 HP1 CKHP0ckcycs ckcy 0 0 0 0	vith DMA transfe <u>19</u> 18 1 [°] <u>—</u> ——— R R F <u>3</u> 2 1 ^{С4} сксусз <mark>сксус2</mark> скс 0 0 с	Pr. 7 16 7 R 8 R 0 YC1 CKCYC0 0 0
18.2.6 Control Register 2 (SPCR2 is a 32-bit readable at a higher rate than that set Transmission and reception in Initial value: R/W: R Bit: Initial value: R/W: R/ Initial value: R/W: R/ Initial value: R/W: R/ Initial value: R/W: R/ Value	and writable register in the SPCR. in master mode are 1 30 29 28 R R R 5 14 13 12 E N R R R N R R N R R	supported 27 26 — — — R R 11 10 — СКНР4 (— 0 R R/W iption	25 24 22 — — — — — — R R F 9 8 7 СКНРЗ СКНР2 СКНР2 0 0 С	d modes for use v 3 22 21 20 3 R R R 7 6 5 4 HP1 CKHP0ckcycs ckcy 0 0 0 0	vith DMA transfe <u>19</u> 18 1 [°] <u>—</u> ——— R R F <u>3</u> 2 1 ^{С4} сксусз <mark>сксус2</mark> скс 0 0 с	Pr. 7 16 7 R 8 R 0 YC1 CKCYC0 0 0
18.2.6 Control Register 2 (SPCR2 is a 32-bit readable at a higher rate than that set at a higher rate than that set Transmission and reception in Initial value: R/W: Bit: 15 Initial value: 0 R/W: Bit Bit Bit Bit	and writable register in the SPCR. in master mode are 30 29 28 - - - - - - - - - -	supported <u>27</u> <u>26</u> <u>—</u> <u>—</u> R R <u>11</u> <u>10</u> <u>—</u> СКНР4 с <u>—</u> 0 R R/W iption	as high-spee 25 24 2 — — — — R R F 9 8 7 СКНРЗ СКНР2 СКН 0 0 С R/W R/W R/	d modes for use w 3 22 21 20 3 R R R 7 6 5 4 HP1 CKHP0ckcycs ckcy 0 0 0 0 W R/W R/W R/W	19 18 1' R R F 3 2 1 C4 ckcvcs]ckcvc2[ckc' 0 0 0 C // R/W R/W R/Y	Pr. 7 16 7 R 8 R 0 YC1 CKCYC0 0 0
18.2.6 Control Register 2 (SPCR2 is a 32-bit readable at a higher rate than that set at a higher rate than that set Transmission and reception in Bit: 31 Initial value: — R/W: R Bit: 15 Initial value: 0 R/W: R Initial value: 0 R/W: R Initial value: 0 R/W: R	and writable register in the SPCR. in master mode are 30 29 28 - - - - - - - - - -	supported <u>27</u> <u>26</u> <u>—</u> <u>—</u> R R <u>11</u> <u>10</u> <u>—</u> СКНР4 <u>0</u> R R/W iption ved bits are al	as high-spee 25 24 2 — — — — R R F 9 8 7 СКНРЗ СКНР2 СКН 0 0 С R/W R/W R/	d modes for use v 3 22 21 20 3 R R R 7 6 5 4 HP1 CKHP0 ckcycs ckcy 0 0 0 0 W R/W R/W R/W 	19 18 1' R R F 3 2 1 C4 ckcvcs]ckcvc2[ckc' 0 0 0 C // R/W R/W R/Y	Pr. 7 16 7 R 8 R 0 YC1 CKCYC0 0 0
18.2.6 Control Register 2 (SPCR2 is a 32-bit readable at a higher rate than that set SPCR2 is a 32-bit readable at a higher rate than that set Transmission and reception in Initial value: Initial value: R/W: Bit: 15 Initial value: R/W: Bit: 15 Initial value: 0 R/W: Bit: 15 Initial value: 0 R/W: Bit	and writable register in the SPCR. in master mode are <u>30 29 28</u> <u></u> R R R <u>5 14 13 12</u> <u>6 R/W Descr</u> R Reser These These The w	Supported 27 26 R R 11 10 - CKHP4 0 R R/W iption ved bits are all rite value s	as high-spee	d modes for use v 3 22 21 20 3 R R R 7 6 5 4 HP1 CKHP0 cKCYCS CKCY 0 0 0 0 W R/W R/W R/W 3 W R/W R/W R/W 4 R/W R/W R/W 4 R/W R/W R/W	vith DMA transfe	Pr. 7 16 7 R 8 R 0 YC1 CKCYC0 0 0
8.2.6 Control Register 2 (SPCR2 is a 32-bit readable at a higher rate than that set at a higher rate than that set Transmission and reception in Initial value: R/W: Bit: 15 Initial value: 0 R/W: Bit Bit No Bit	and writable register in the SPCR. in master mode are <u>30 29 28</u> <u></u> R R R <u>5 14 13 12</u> <u>6 R/W Descr</u> R Reser These These These Enable	Supported 27 26 R R 11 10 - CKHP4 - 0 R R/W iption ved bits are al rite value s speed trans es or disab	as high-spee	d modes for use v 3 22 21 20 3 R R R 7 6 5 4 HP1 CKHP0 CKCYCS CKCY 0 0 0 0 W R/W R/W R/W 3 W R/W R/W R/W 5 an undefined val 5 be 0.	vith DMA transfe	Pr. 7 16 7 R 8 R 0 YC1 CKCYC0 0 0
18.2.6 Control Register 2 (SPCR2 is a 32-bit readable at a higher rate than that set SPCR2 is a 32-bit readable at a higher rate than that set Transmission and reception in the image of the	and writable register in the SPCR. in master mode are and and writable register in the SPCR. and and and and and and and and and and	Supported 27 26 R R 11 10 - CKHP4 0 R R/W iption ved bits are al rite value s speed trans es or disab te division	as high-spee	d modes for use v 3 22 21 20 	vith DMA transfe	Pr. 7 16 7 R 8 R 0 YC1 CKCYC0 0 0
18.2.6 Control Register 2 (SPCR2 is a 32-bit readable at a higher rate than that set SPCR2 is a 32-bit readable at a higher rate than that set Transmission and reception in Initial value: Initial value: R/W: Bit: 15 Initial value: R/W: Bit: 15 Initial value: 0 R/W: Bit: 15 Initial value: 0 R/W: Bit	and writable register in the SPCR. in master mode are <u>30 29 28</u> <u></u> R R R <u>5 14 13 12</u> <u>E</u> N R R R I e R/W Descr These These These These With th 0: The	Supported 27 26 R R 11 10 - CKHP4 0 R R/W iption ved bits are all rite value s speed trans es or disable te division	as high-spee	d modes for use v 3 22 21 20 3 R R R 7 6 5 4 4P1 CKHP0 CKCYC5 CKCY 0 0 0 0 W R/W R/W R/W 3 be 0. n of a serial clock PCR2. t is disabled.	vith DMA transfe	Pr. 7 16 7 R 8 R 0 YC1 CKCYC0 0 0
18.2.6 Control Register 2 (SPCR2 is a 32-bit readable at a higher rate than that set at a higher rate than that set Transmission and reception in Initial value: R/W: Bit: 15 Initial value: R/W: Bit: 15 Initial value: 0 R/W: Bit: 15 Initial value: 0 R/W: Bit: 15 Initial value: 0 R/W: Bit Bit Name 11 to 16	and writable register in the SPCR. in master mode are <u>30 29 28</u> <u></u> R R R <u>5 14 13 12</u> <u>E</u> N R R R I e R/W Descr These These These These With th 0: The	Supported 27 26 R R 11 10 - CKHP4 0 R R/W iption ved bits are al rite value s speed trans es or disab te division clock sett clock sett	as high-spee	d modes for use v 3 22 21 20 3 R R R 7 6 5 4 4P1 CKHP0 CKCYC5 CKCY 0 0 0 0 W R/W R/W R/W 3 be 0. n of a serial clock PCR2. t is disabled.	vith DMA transfe	Pr. 7 16 7 R 8 R 0 YC1 CKCYC0 0 0



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Bit	Bit Name	Initial Value	R/W	Description
10 to 6	CKHP[4:0]	0	R/W	Serial clock high period
				The width at high level of the serial bit clock is set to (this setting) cycles of the SuperHyway clock (clks). If the width at high level is not set to half of the period setting in CKCYC, the duty cycle will greatly diverge from 50:50.
5 to 0	CKCYS[5:0]	0	R/W	Serial clock period
				The period of the serial bit clock is set to (this setting - 1) cycles of the SuperHyway clock (clks). The maximum frequency of the serial bit clock is 20 MHz. In accord with the formula for calculation given below, the CKCYC value should be no less than 9.

The serial bit clock frequency can be computed using the following formula:

Serial bit clock frequency = _____SuperHyway (Internal bus) clock frequency

CKCYC + 1

If any bit (FBS, CLKP, IDIV or CLKC) of SPCR is changed or any bit of SPCR2 is changed, the HSPI is soft reset.

Register settings and serial bit-clock frequencies are indicated below.						
CKCYC[5:0]	CKHP[4:0]	Serial bit clock frequency	Duty			
D'9	D'5	SuperHyway clock frequency/10	50%			
D'11	D'6	SuperHyway clock frequency/12	50%			
D'13	D'7	SuperHyway clock frequency/14	50%			
D'15	D'8	SuperHyway clock frequency/16	50%			
D'17	D'9	SuperHyway clock frequency/18	50%			
D'63	D'32	SuperHyway clock frequency/64	50%			

6. Correct "18.3.5 HSPI Software Reset" to page 1587

<Wrong>

The HSPI software reset is generated when the control bits except SPCR, the interrupt/DMA enable bits and the chip select value bit (CSV) of SPSCR are modified.

<Correct>

The HSPI software reset is generated when the control bits except SPCR/SPCR2, the interrupt/DMA enable bits and the chip select value bit (CSV) of SPSCR are modified.

- End of report -

