Date: Jun. 27, 2018

RENESAS TECHNICAL UPDATE

TOYOSU FORESIA, 3-2-24, Toyosu, Koto-ku, Tokyo 135-0061, Japan
Renesas Electronics Corporation

Product Category	MPU/MCU		Document No.	TN-RX*-A195A/E	Rev.	1.00
Title	Disclosure of the Electrical Characteristics for SD Host Interface (SDHI) in RX64M Group and RX71M Group		Information Category	Technical Notification		
Applicable Product	RX64M Group RX71M Group	Lot No. All	Reference Document	RX64M Group User's Manual: Hardware Rev.1.10 (R01UH0377EJ0110) RX71M Group User's Manual: Hardware Rev.1.10 (R01UH0493EJ0110)		

This document discloses the AC characteristics for the SD host interface (SDHI) in the RX64M and RX71M groups. The disclosed details are as follows.

Table 1. SDHI Timing

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = V_{BATT} = 2.7 to 3.6 V, 2.7 V ≤ VREFH0 ≤ AVCC0,
VCC_USBA = AVCC_USBA = 3.0 to 3.6 V,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = VSS1_USBA = VSS2_USBA = PVSS_USBA = AVSS_USBA = 0 V,
PCLKA = 8 to 120 MHz, PCLKB = 8 to 60 MHz, $T_a = T_{opr}$,
Output load conditions: V_{OH} = VCC × 0.5, V_{OL} = VCC × 0.5, C = 30 pF,
High-drive output is selected by the drive capacity control register.

Item		Symbol	Min.	Max.	Unit	Test Conditions*1
SDHI	SDHI_CLK pin output cycle time	$t_{PP(SD)}$	2 × t_{PBcyc}*2	—	ns	Figure 1
	SDHI_CLK pin output high pulse width	$t_{WH(SD)}$	0.4 × $t_{PP(SD)}$	—	ns	
	SDHI_CLK pin output low pulse width	$t_{WL(SD)}$	0.4 × $t_{PP(SD)}$	—	ns	
	SDHI_CLK pin output rise time	$t_{TLH(SD)}$	—	5	ns	
	SDHI_CLK pin output fall time	$t_{THL(SD)}$	—	5	ns	
	Output data delay time (data transfer mode) for SDHI_CMD and SDHI_D0 to SDHI_D3 pins	$t_{ODLY(SD)}$	–6.5	4	ns	
	Input data setup time for SDHI_CMD and SDHI_D0 to SDHI_D3 pins	$t_{ISU(SD)}$	7	—	ns	
	Input data hold time for SDHI_CMD and SDHI_D0 to SDHI_D3 pins	$t_{IH(SD)}$	2	—	ns	

Note 1. We recommend using pins that have a letter ("-A", "-B", etc.) to indicate group membership appended to their names as groups. For the SDHI interface, the AC portion of the electrical characteristics is measured for each group.
Note 2. t_{PBcyc}: PCLKB cycle

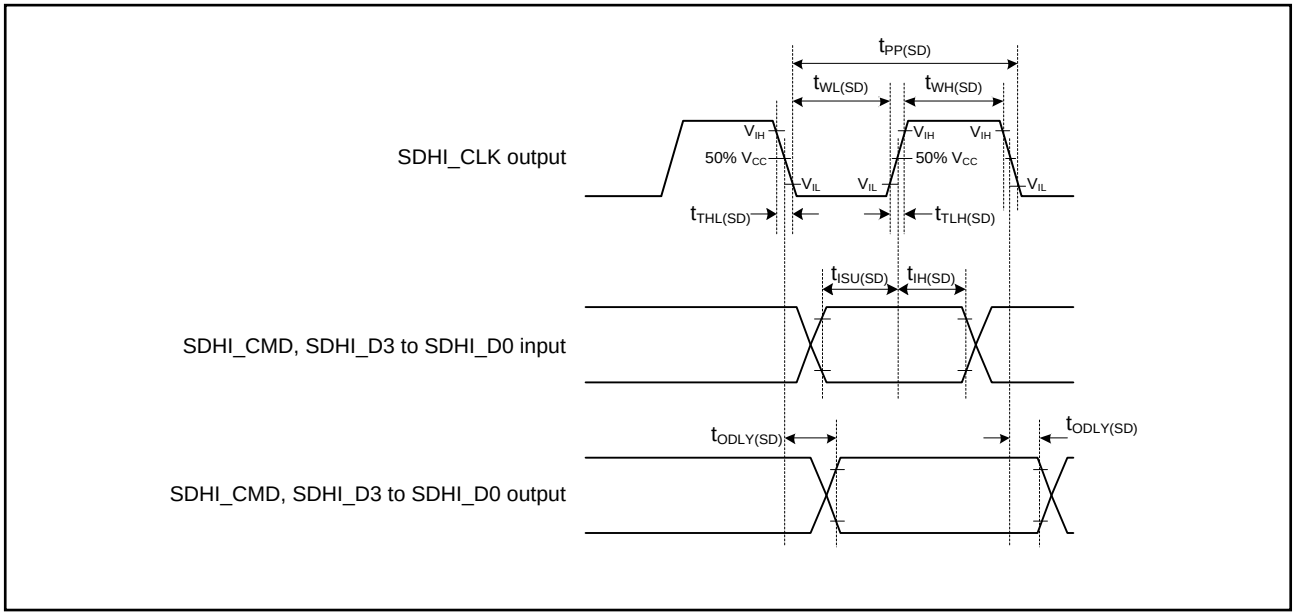

Figure 1. SD Host Interface Input/Output Signal Timing