

RENESAS TECHNICAL UPDATE

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Product Category	MPU/MCU		Document No.	TN-RX*-A049A/E	Rev.	1.00
Title	Notes on Using the PWM Delay Generation Circuit of the General PWM Timer (GPTa)		Information Category	Technical Notification		
Applicable Product	RX62G Group	Lot No.	Reference Document	RX62G Group User's Manual: Hardware		
		All lots				

Thank you for your valued patronage and best wishes for your continued success in business.

This notification is an update consisting of notes on timing of the delay value to be set when using the PWM delay generation circuit of the general PWM timer (GPTa). The related hardware manuals will be revised based on the information in these notes.

1.1 Notes on Setting of the Delay Value in the PWM Delay Generation Circuit

When a PWM output waveform is delayed in the PWM delay generation circuit by a toggled PWM output operation at a compare match, do not change the delay value to be set while the compare match value falls in the range shown in the following table. The registers subject to the timing restriction of change to the setting value are the GTDLYFA, GTDLYRA, GTDLYFB, and GTDLYRB registers.

Mode	Counting Direction	Compare Match Value
Saw wave	Counting up	"GTPR - 2" or more
	Counting down	"2" or less
Triangle wave	Counting down	"2" or less

Figure 1 shows an example of the timing restriction of change to the setting in the GTDLYFA register in saw-wave one-shot pulse mode (counting up). When $GTCCRD \geq GTPR - 2$, do not change the setting in the GTDLYFA register.

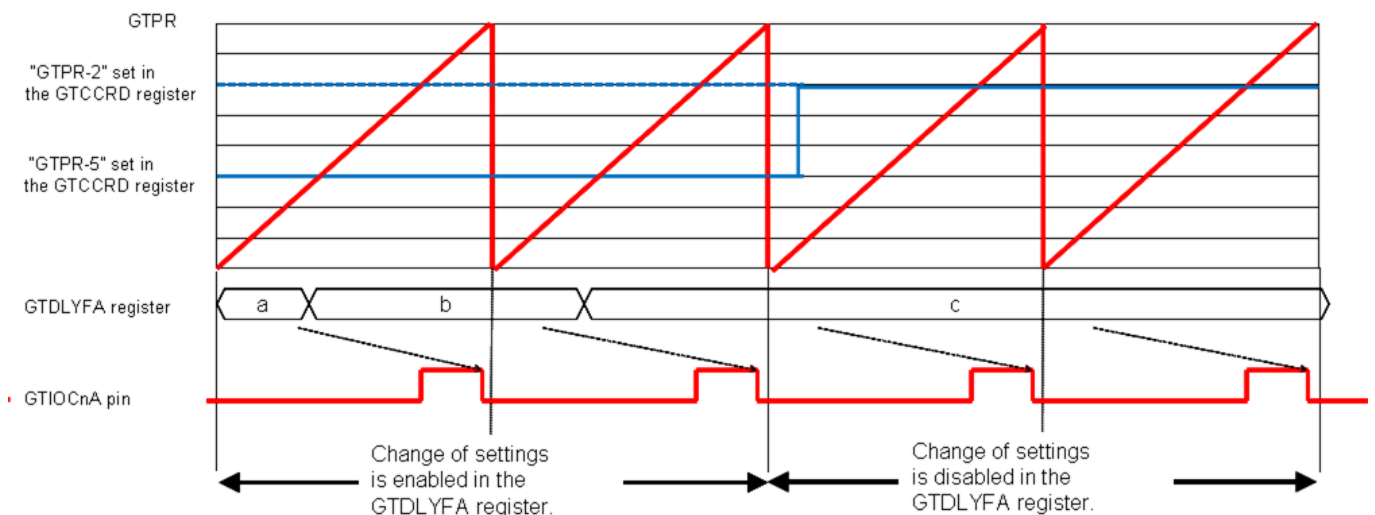


Figure 1 Timing Restriction of Change to the Setting in the GTDLYFA Register

When a setting in the GTDLYFA, GTDLYRA, GTDLYFB, or GTDLYRB register is changed when changes in register settings is disabled, it may cause an abnormal output waveform. For example, the timing of the change in an output waveform may deviate from the specified one. Do not change the setting value of these registers.

1.2 Notes on Setting of GPT Operation When Using the PWM Delay Generation Circuit

When the PWM delay generation circuit is used, set an interval longer than five cycles ICLK between the setting of the GTIOC pin function and the enabling of GTIOC pin output. Unless the GTIOC pin output is enabled after the setting of the GTIOC pin function has been reflected in the actual circuit, an unintended glitch is output from the GTIOC pin.

In addition to setting an interval between the setting of the GTIOC pin function and the enabling of GTIOC pin output, modification of the setting procedure can be used to obtain the same results. To achieve this, a compare match value should be set after the GTIOC pin function is set or the GTIOC pin output should be enabled after buffer operation or buffer values are set. Figure 2 shows an example of the modified setting procedures.

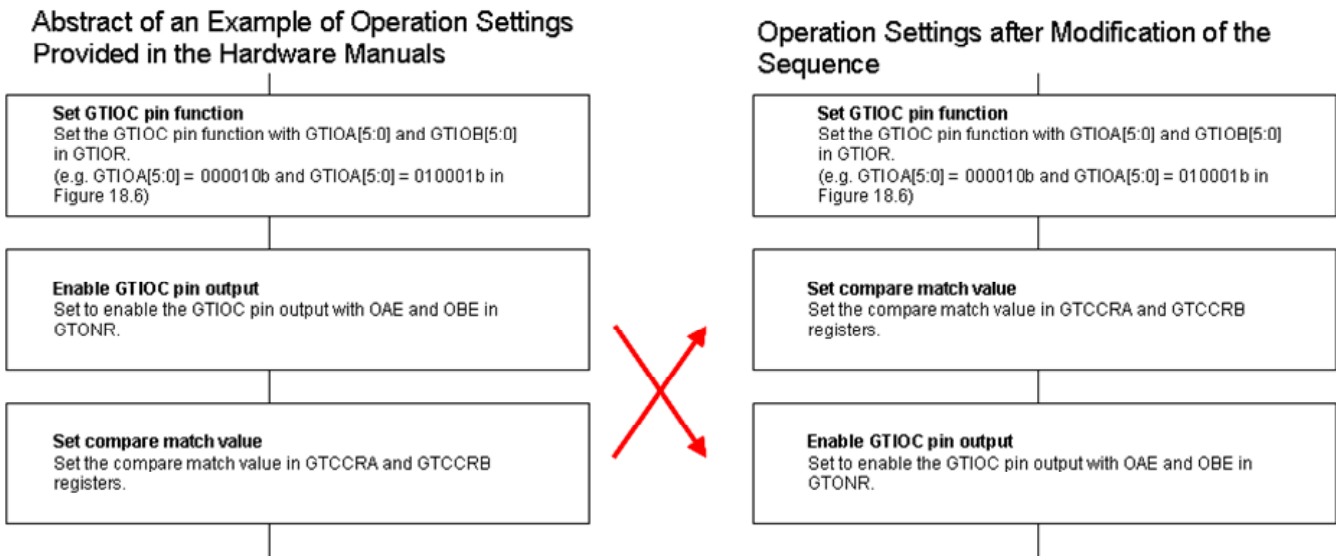


Figure 2 Example of Modified Procedures for Register Operation Setting

In the following examples, an interval longer than five cycles of ICLK should be set between the setting of the GTIOC pin function and the enabling of GTIOC pin output:

-18.3.1.2 Waveform Output by Compare Match

Figure 18.7 Example for Setting Low Output and High Output Operation and

Figure 18.10 Example for Setting Toggled Output Operation

-18.3.2.2 Buffer Operation for GTCCRA and GTCCRB

Figure 18.20 Example for Setting GTCCRA and GTCCRB Buffer Operation (for Output Compare)

-18.3.3 PWM Output Operating Mode

Figure 18.29 Example for Setting Saw-Wave PWM Mode,

Figure 18.31 Example for Setting Saw-Wave One-Shot Pulse Mode,

Figure 18.33 Example for Setting Triangle-Wave PWM Mode 1,

Figure 18.35 Example for Setting Triangle-Wave PWM Mode 2,

Figure 18.37 Example for Setting Triangle-Wave PWM Mode 3,

Figure 18.41 Example for Setting Automatic Dead Time Setting Function (Saw-Wave One-Shot Pulse Mode,

Triangle-Wave PWM Mode 3), and

Figure 18.42 Example for Setting Automatic Dead Time Setting Function (Triangle-Wave PWM Mode 1 or 2)

1.3 Correction to the Hardware Manuals

The content of this update is going to be added as an addendum to the RX62G Group Hardware Manuals in the next version.