ISL70001SEH, ISL70001SRH VOUT Power-Up/Down Glitch Problem Report

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## Abstract

This technical brief explains the GIDEP Problem Advisory BP6-P-16-01 issued for the ISL70001SEH, ISL70001SRH devices.

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# Description of Problem

The ISL70001SRH and ISL70001SEH can exhibit a $V_{OUT}$ response during a power-up or power-down period when $V_{IN}$ is between 1.3V and 1.8V. This range of $V_{IN}$ is below the nominal $V_{IN}$ POR threshold of approximately 2.65V for PORSEL set to ground and 4.1V for PORSEL set to $V_{IN}$. For $V_{IN}$ ramps of faster than 10V/ms this anomalous output activity is not possible, however, for slower $V_{IN}$ ramps there is the possibility of output activity. During power-up, $V_{OUT}$ follows a normal soft-start behavior, which will not exceed the $V_{OUT}$ set-point voltage. During power-down $V_{IN}$ ramp the activity again will not exceed the set-point voltage. The size of the anomalous $V_{OUT}$ response is inversely related to the ramp rate of $V_{IN}$ as this sets how long the part is in the anomalous activity range. See Figure 1 for an illustration of the issue. This problem has been fixed on the ISL70001ASEH.

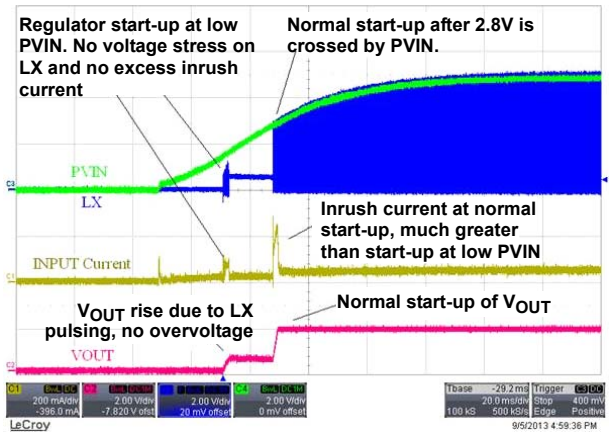



FIGURE 1. $V_{OUT}$ RESPONSE DURING A POWER-UP

# Summary of Simulation Results

Transistor level simulations indicate that the ISL70001SEH, ISL70001SRH $V_{OUT}$ glitch during power-up and power-down is limited by the soft-start voltage and ultimately by the selected $V_{OUT}$ setting (e.g., 1.2V). The glitch is a normal soft-start event terminated when POR lockout becomes active by 1.8V. That is, the glitch will follow soft-start and not exceed the programmed output voltage setting, even if the $V_{IN}$ stalls in the window of the anomalous switching activity. In the ramped power-up situation, the glitch is dominated by the soft-start voltage so the resulting glitch is substantially smaller than the selected output voltage. During power-down the soft-start voltage can cause the $V_{OUT}$ to discharge if it is precharged to a non-zero value.

## Discussion of Simulation Results

Simulations were run for the anomalous $V_{OUT}$ activity (glitch) during power-up and power-down for $0V < V_{IN} < 2V$. Simulations used the schematic shown in Figure 2 on page 4. Note that the VIN ramp rate was set to 0.2V/ms for both power-up and power-down. The results from the sequence of simulations run are summarized in Table 1. The largest power-up glitch in a $V_{OUT}$ of 426mV occurred for process corner 4 run at a temperature of +125°C. This is well below the output set point of 1.2V. Slower ramps will lead to larger glitches, however, the set-point voltage is never exceeded as indicated by the DC $V_{IN}$ case at the bottom of Table 1.

TABLE 1. SIMULATION RESULTS FOR POWER-UP/DOWN ANOMALOUS $V_{OUT}$ GLITCH FOR $V_{IN}$ RAMPING BETWEEN 0V AND 2V AT 0.2V/ms.

| SIMULATION CONDITIONS | (Note 1) | VOUT GLITCH (V) |
|---|---|---|
| Power-up, Nominal Process, -55°C | Figure 3 | 0 |
| Power-up, Nominal Process, +25°C | Figure 3 | 0.058 |
| Power-up, Nominal Process, **+125°C (Worst temp)** | Figure 3 | 0.236 |
| Power-up, Process Corner 1, +125°C | Figure 4 | 0.103 |
| Power-up, Process Corner 3, +125°C | Figure 4 | 0 |
| Power-up, Process Corner 2, +125°C | Figure 5 | 0.368 |
| Power-up, Process **Corner 4, +125°C (Worst case)** | Figure 5 | 0.426 |
| Power-down, Process **Corner 4, +125°C** | Figure 7 | Discharges from 0.7V |
| Power-up, Post 100krad, Nominal process, +25°C | Figure 8 | 0.236 |
| DC VIN = 1.796V for Process Corner 4, +125°C | Figure 9 | 1.178 for 1.200 set |

NOTE:

1. Simulation plots are in the called out Figures.

The first three simulations of Table 1 are depicted in Figure 3 on page 5. For the -55°C case the oscillator (SyncIO) never goes active so that the switching node (Phase1) never activates and consequently the output ($V_{OUT}$) never charges. The fall of Dfeet activates the POR circuitry and blocks further switching until POR is released at about $V_{IN}$ = 2.65V (for PORSEL set to ground). The +25°C case shows both SyncIO and Phase1 activity before Dfeet goes low. This short activity results in a $V_{OUT}$ glitch of 58mV. At +125°C the SyncIO and Phase1 activity starts at a lower $V_{IN}$ and proceeds to allow $V_{OUT}$ to track the soft-start voltage (SS_cap) with the selected feedback gain of 2x applied. In this case the $V_{OUT}$ glitch reaches 236mV. The +125°C case is the worst temperature for the glitch.

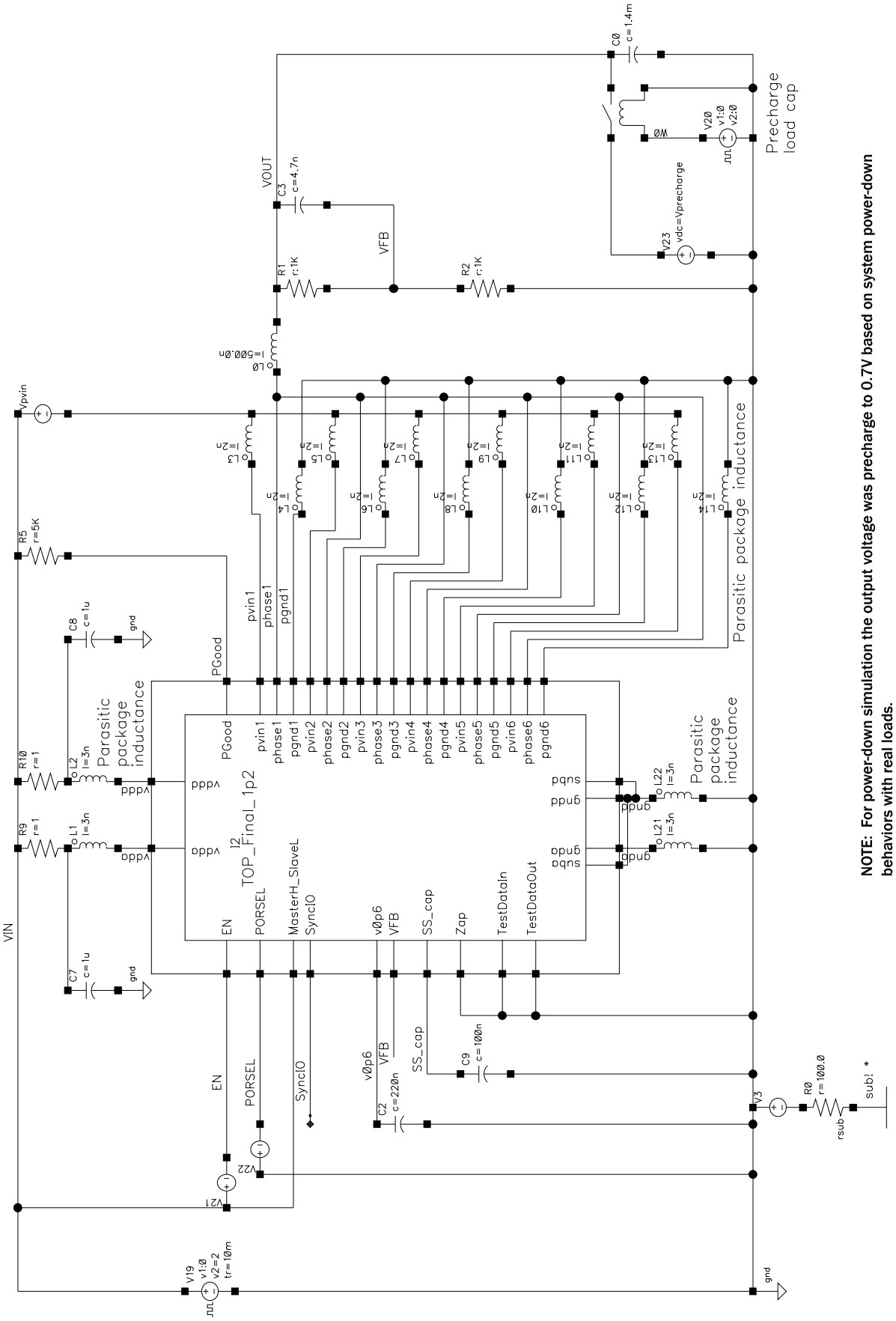
The four process corners were run at +125°C and are the next four entries in Table 1. The 1st and 3rd process corners are depicted in Figure 4 in the same fashion as in Figure 3. Corner 1 had a short episode of Phase1 activity that yielded an output glitch of 103mV. Corner 3 exhibited no Phase1 activity and consequently had no glitch on $V_{OUT}$. Figure 5 depicts the results from the 2nd and 4th process corners. Both cases resulted in appreciable $V_{OUT}$ glitches of 368mV and 426mV respectively. So the worst case power-up glitch of 426mV was seen for process corner 4 and a temperature of +125°C.

Figure 6 on page 8 shows the four process cases of power-up simulations at +125°C comparing the $V_{OUT}$ signal to 2x the soft-start voltage. The factor of 2 comes from the set-point voltage being set to 1.2V and the reference voltage being 0.6V. These plots highlight the fact that the soft-start voltage is in control of the glitch ramp. This indicates that the voltage control loop is functioning and in control of $V_{OUT}$ and that a normal

soft-start has been initiated. This assertion is further supported by simulation results in Figure 9 on page 11. This simulation allows the anomalous switching condition to continue by holding $V_{IN}$ = 1.796V. The resulting $V_{OUT}$ response ramps up to approximately the set-point voltage of 1.200V (1.178V) and then holds at that level. Again the voltage loop is seen to be active and in control of $V_{OUT}$.

A power-down ramp was simulated for process corner 4 at +150°C and the results are presented in Figure 7 on page 9. In this case the $V_{OUT}$ was precharged to 0.7V to emulate the load discharging $V_{OUT}$ to a diode drop indicative of an active load. The most interesting fact is that the anomalous switching activity leads to the $V_{OUT}$ being discharged.

Figure 8 on page 10 presents simulations to represent the effects of radiation. The pre-radiation case shown (on the left) is again the nominal process at +25°C. The post-radiation (100krad(Si), on the right) is the process corner representing the nominal process post-radiation at +25°C. The radiation has increased the glitch from 58mV to 236mV, but the form of the glitch in that it follows the soft-start voltage remains intact.




**NOTE: For power-down simulation the output voltage was precharge to 0.7V based on system power-down behaviors with real loads.**

**FIGURE 2. $V_{OUT}$ POWER-UP/DOWN ANOMALOUS GLITCH SIMULATION SCHEMATIC**

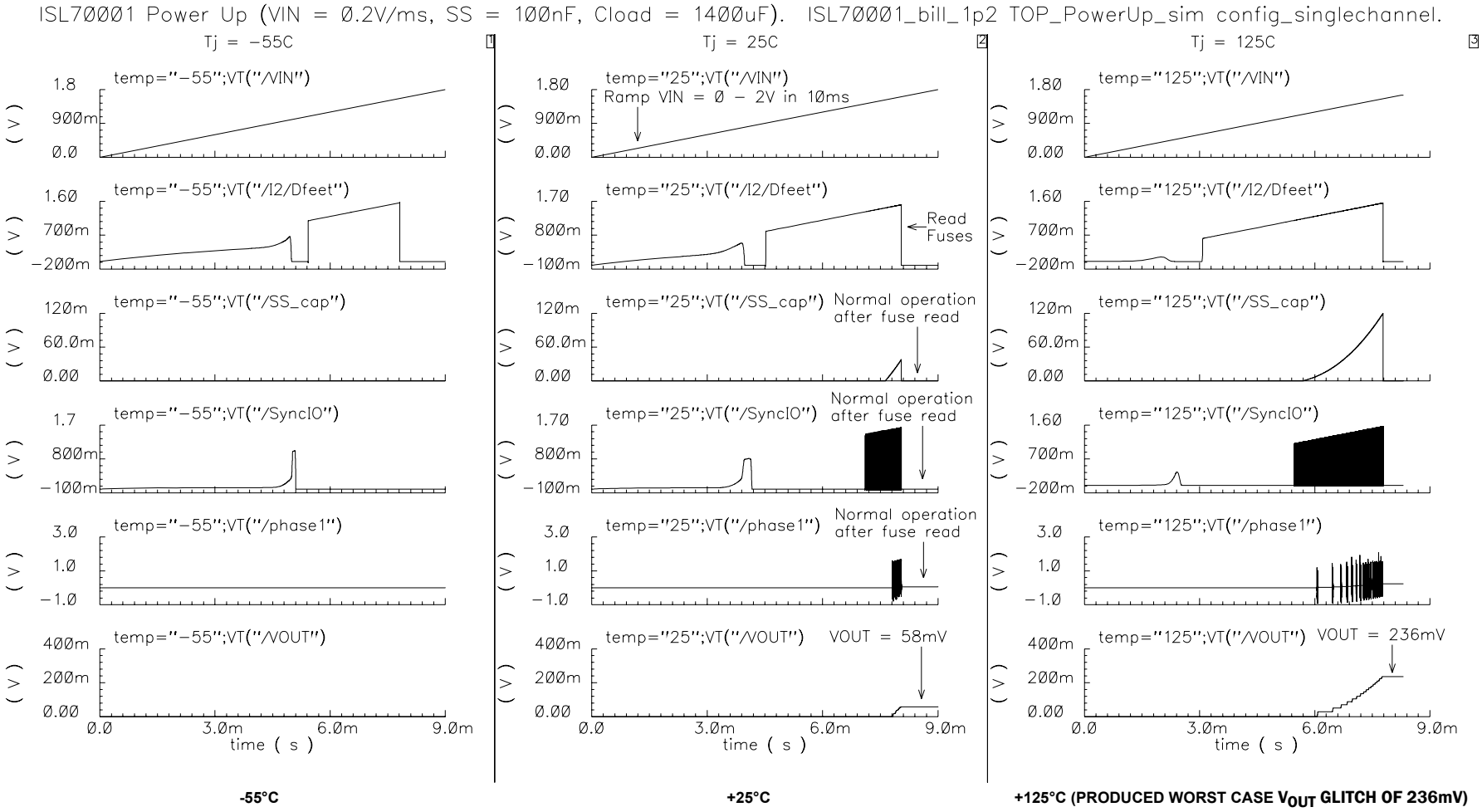
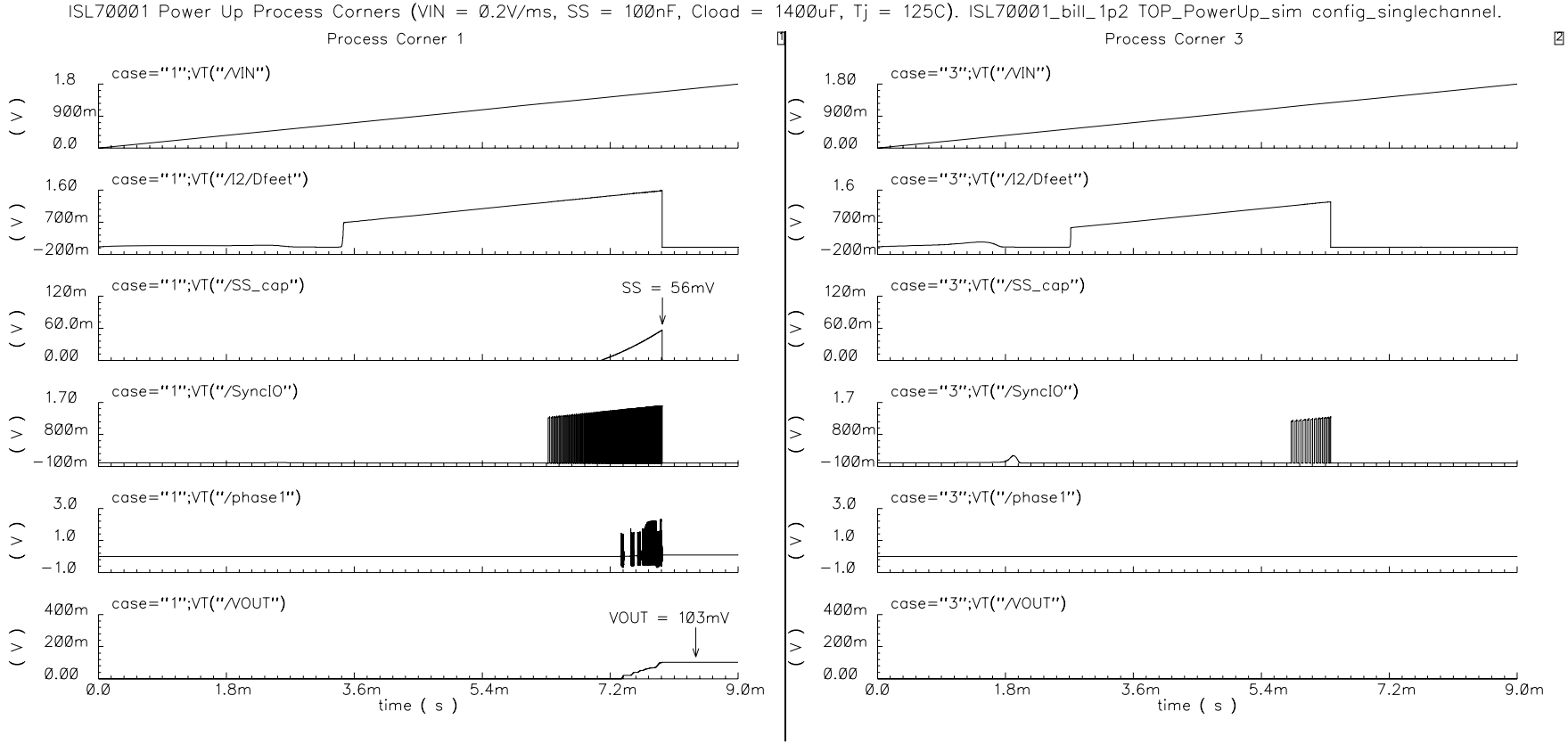
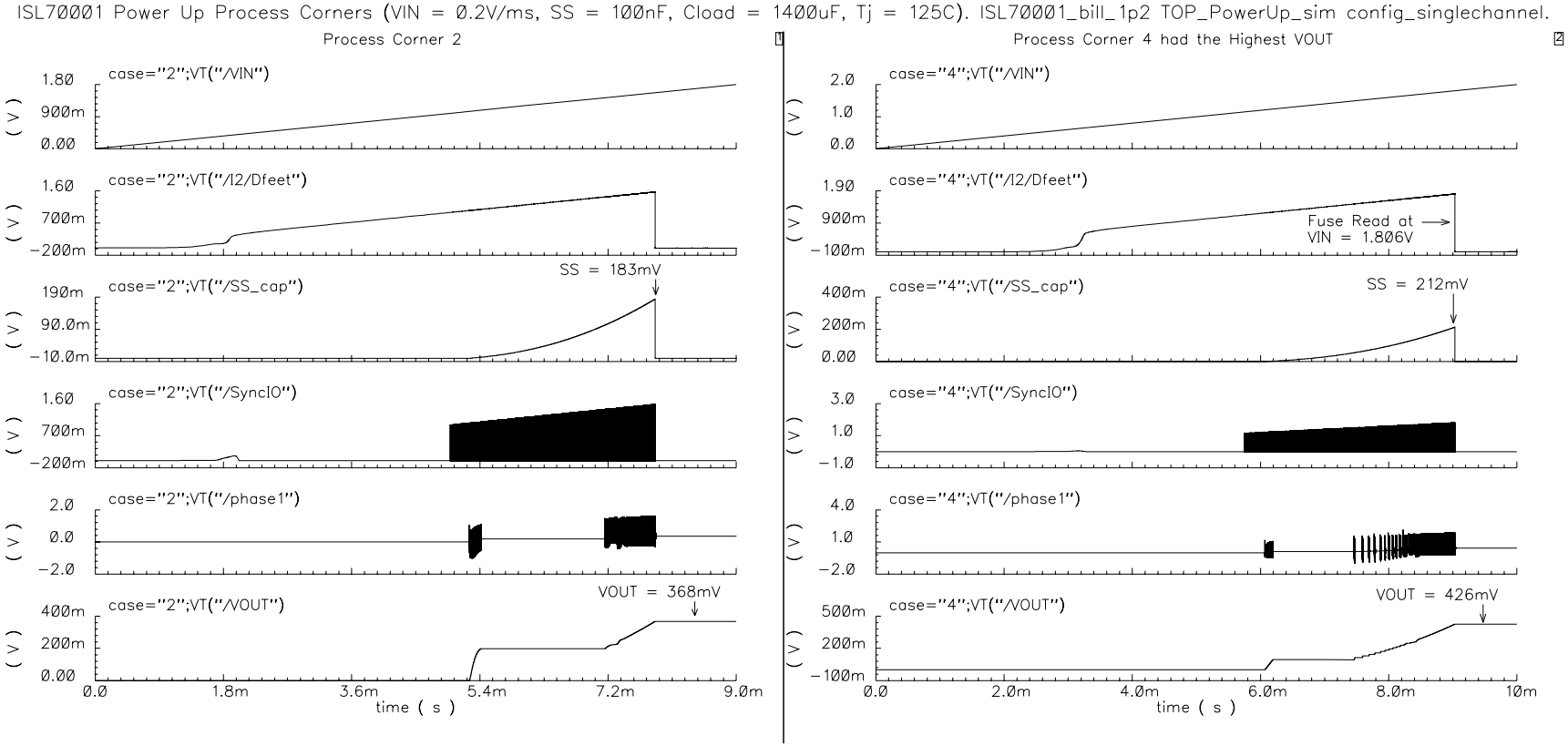



**FIGURE 3. POWER-UP SIMULATIONS OF NOMINAL PROCESSING AT THREE TEMPERATURES**



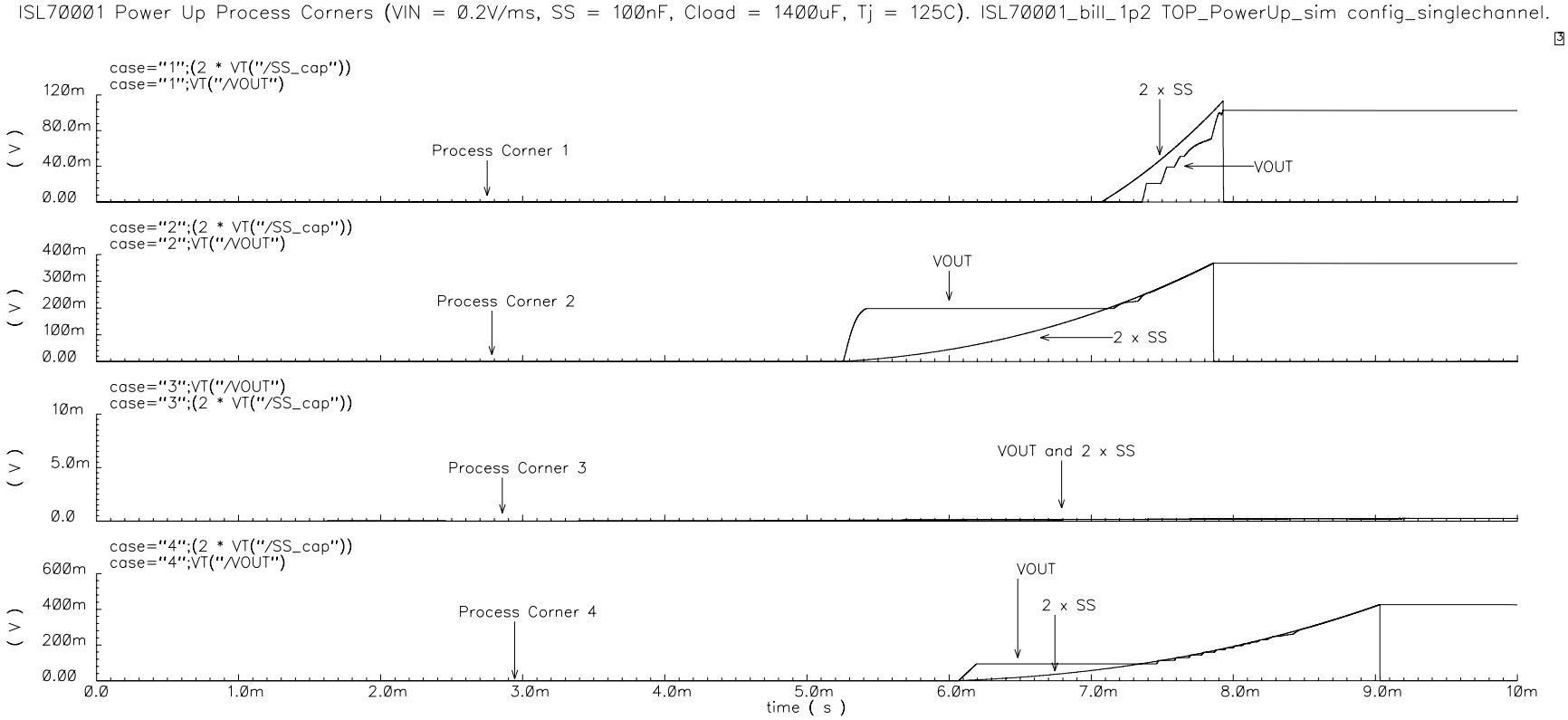

NOTE: Only corner 1 generated a $V_{OUT}$ glitch at 103mV.

**FIGURE 4. POWER-UP SIMULATIONS OF PROCESS CORNERS 1 AND 3 AT +125°C**



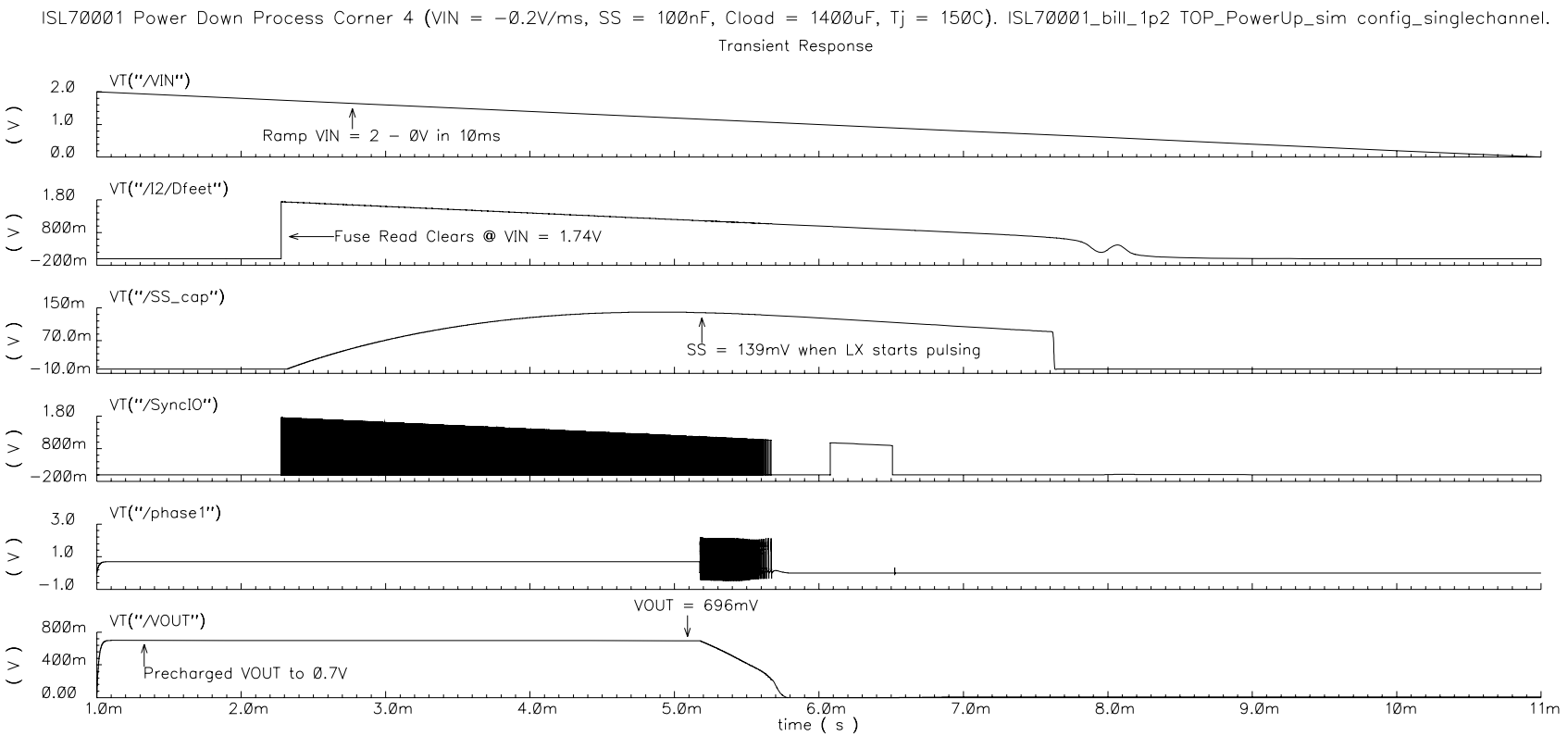

NOTE: Corner 4 exhibited the worst case glitch Of 426mV.

**FIGURE 5. POWER-UP SIMULATIONS OF PROCESS CORNERS 2 AND 4 AT +125°C**




NOTE: These show that the glitch is limited by the soft-start voltage as the part follows a normal soft-start progression.

**FIGURE 6. SIMULATIONS CLOSE-UP VIEW OF PROCESS CORNERS $V_{OUT}$ GLITCH AS COMPARED TO 2x ($V_{OUT}$ = 2xVREF) THE SOFT-START VOLTAGE.**




NOTE: Starting from a precharge of 0.7V to emulate power-down ramps of actual loads. The switching activity actually causes the $V_{OUT}$ to discharge under soft-start voltage control.

**FIGURE 7. PROCESS CORNER 4 RAMP DOWN AT +150°C**

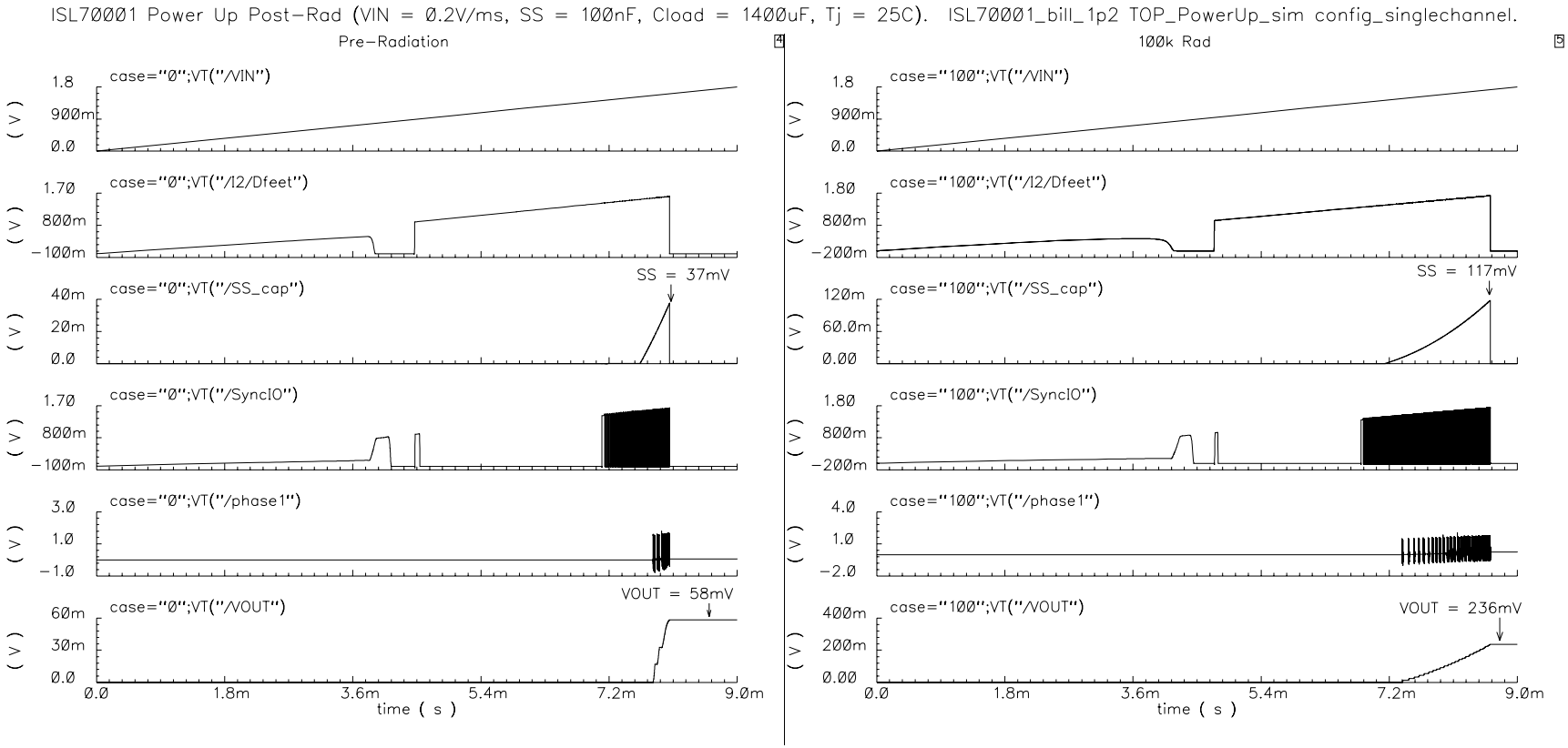
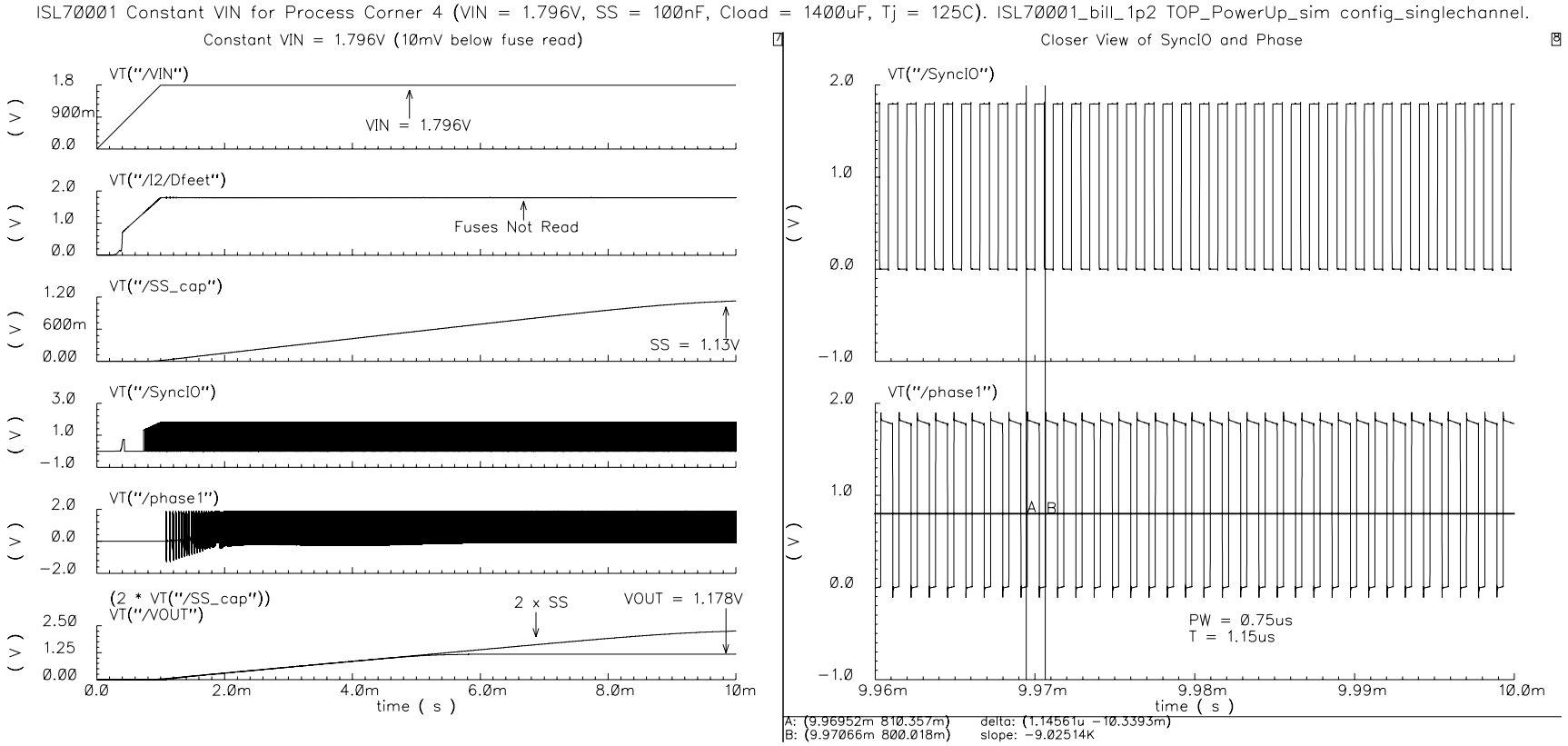



**FIGURE 8. PRE AND POST 100krad(Si) POWER-UP RAMP FOR NOMINAL PROCESS AT +25°C**




NOTE: Conditions were process corner 4 and +125°C. $V_{OUT}$ stops rising at approximately the set-point voltage of 1.200V (1.178V untrimmed).

**FIGURE 9. $V_{OUT}$ SIMULATION FOR CONSTANT $V_{IN}$ = 1.796V TO PRODUCE A STEADY-STATE RESPONSE**

# Summary of Bench Testing Results Summary

Bench testing the ISL70001SEH, ISL70001SRH for the anomalous $V_{OUT}$ response on power-up and power-down demonstrated that the glitch never exceeded 1V when the set voltage was 1.2V. This was true of all 40 units from five different production lots tested at +25°C as well as for the four units selected for testing at +125°C and the six units tested post irradiation to 100krad(Si) at 50-300rad(Si)/s. The pertinent parameters for the bench testing are listed in Table 2.

**TABLE 2. PERTINENT PARAMETERS FOR BENCH TESTING ISL70001SEH, ISL70001SRH FOR POWER-UP AND POWER-DOWN ANOMALOUS $V_{OUT}$ GLITCH.**

| PARAMETER | VALUE |
|---|---|
| Input Capacitance | 200µF |
| Output Inductor | 1µH |
| Output Capacitance | 500µF |
| Soft-Start Capacitance | 100nF |
| VREF Capacitance | 220nF |
| Output Set Voltage | 1.2V |
| Power-Up Supply Ramp | Between 0.1 and 0.2V/ms |
| Power-Down Supply Ramp | Between -0.1 and -0.2V/ms |
| VIN Sweep Limits | 0V to 2V |

NOTE: Testing was done on a socketed ISL70001SEH, ISL70001SRH evaluation board.

The worst power-up glitch for all testing conditions was 627mV for irradiated LOT-3-1, which also registered the worst case +25°C power-up glitch at 296mV. The pre- and post-irradiation power-up glitches are presented in Figures 10 and 11 respectively. It should be noted that both responses follow normal soft-start charging behavior until termination of the anomalous switching at about $V_{IN}$ = 1.8V. In the post-irradiation case, Figure 11, the $V_{IN}$ ramp barely extended beyond the termination of the anomalous switching period leading to a result indicative of a much slower power-up ramp than intended. A faster ramp would have terminated the switching event sooner and led to a smaller glitch.

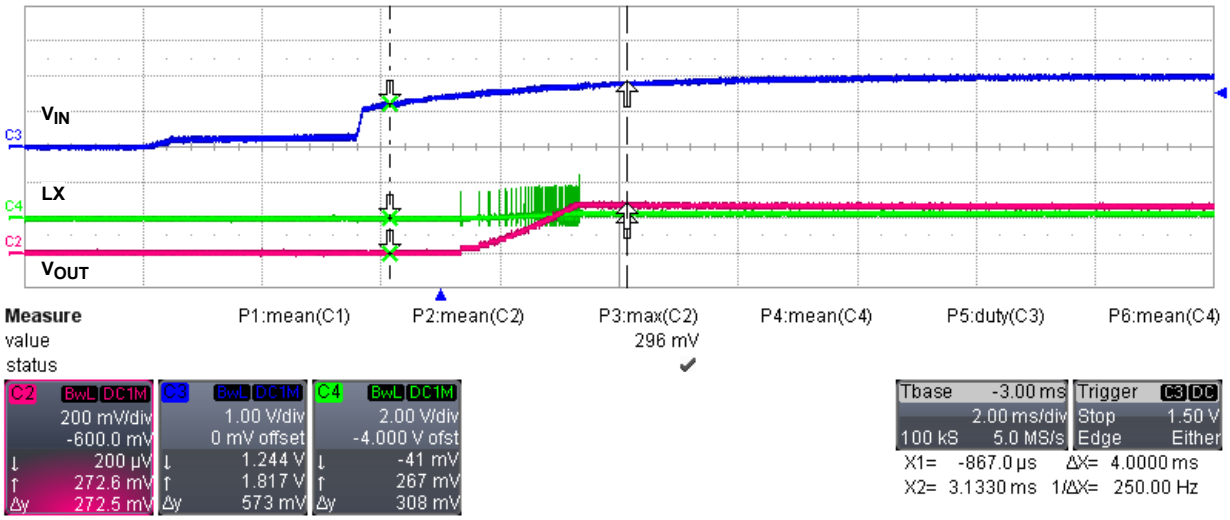



**FIGURE 10. POWER-UP GLITCH FOR UNIT LOT-3-1 AT +25°C PRIOR TO IRRADIATION**

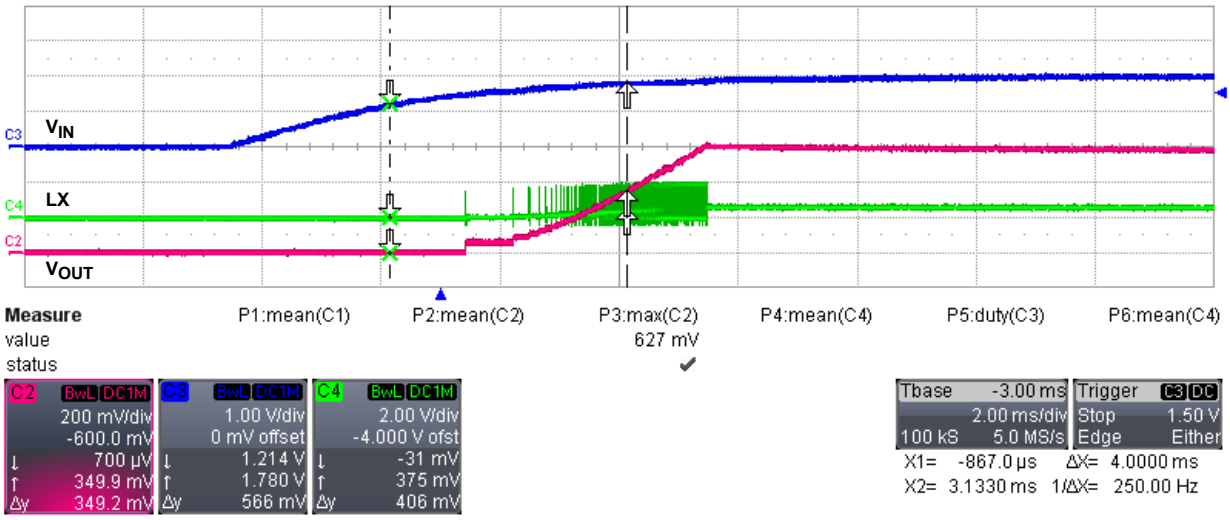



**FIGURE 11. POWER-UP GLITCH FOR UNIT LOT-3-1 AT +25°C AFTER BIASED IRRADIATION TO 100krad(Si) AND 50-300rad(Si)/S**

The worst case power-down glitch of 467mV was seen on unit LOT-1-2684 at +25°C and is represented in Figure 12. The rapid $V_{OUT}$ charging at the end of switching activity was anomalous among the parts tested. The next worst power-down event was registered by unit LOT-3-1 after irradiation and is shown in Figure 13. The final discharge phase of the glitch was typical behavior.

Units were also tested for the DC condition of $V_{IN}$ held at the top of the region of anomalous switching. Of all the units tested in this fashion, LOT-3-1 exhibited the highest $V_{OUT}$ level at 905mV as is represented in Figure 14 on page 15.

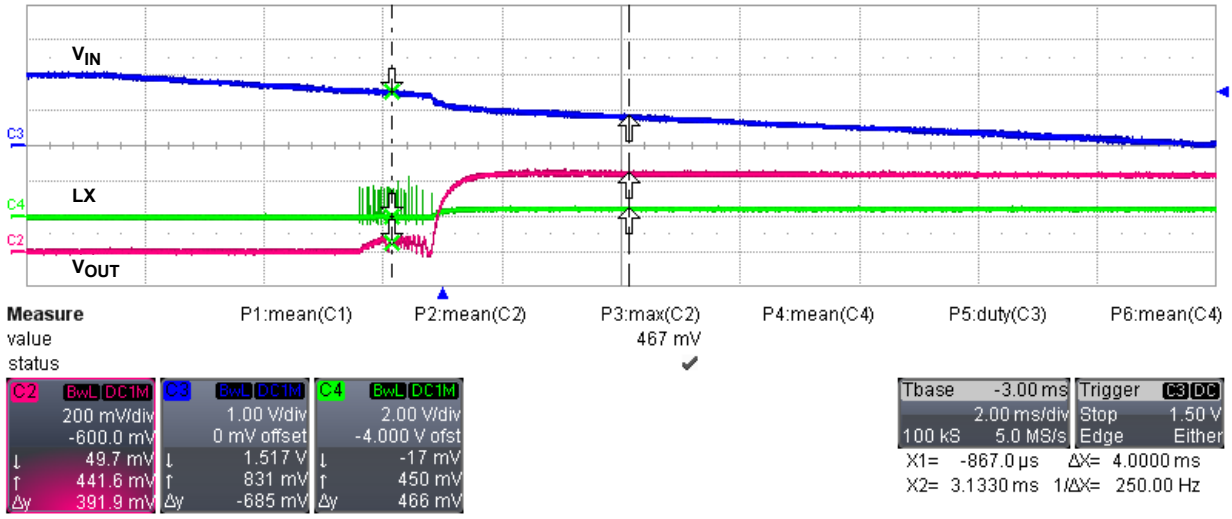



FIGURE 12. POWER-DOWN GLITCH FOR UNIT LOT-1-2684 AT +25°C

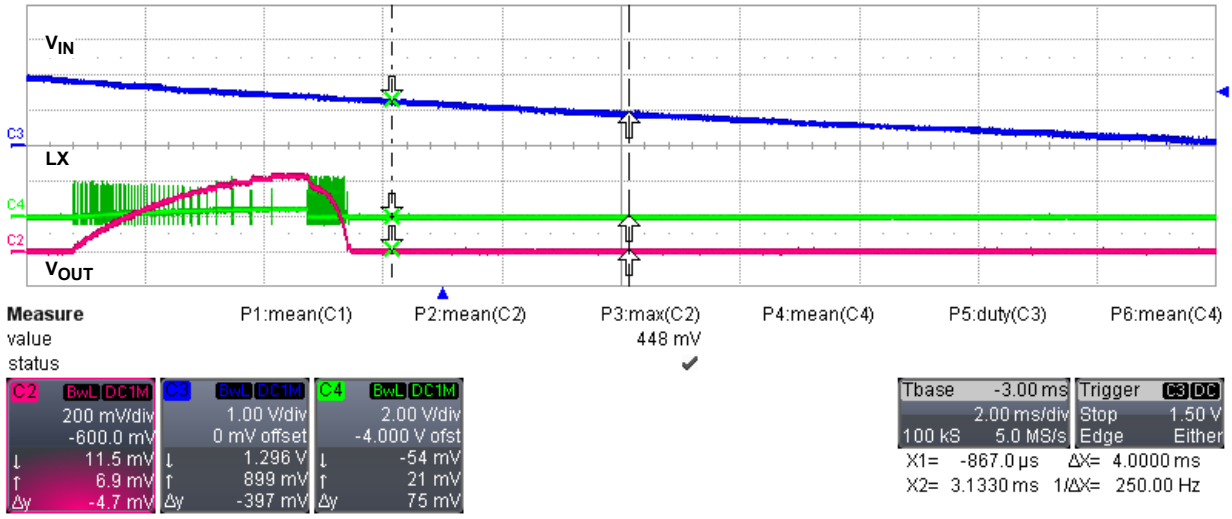



FIGURE 13. POWER-DOWN GLITCH FOR UNIT LOT-3-1 AT +25°C AFTER BIASED IRRADIATION TO 100krad(Si) AND 50-300rad(Si)/S

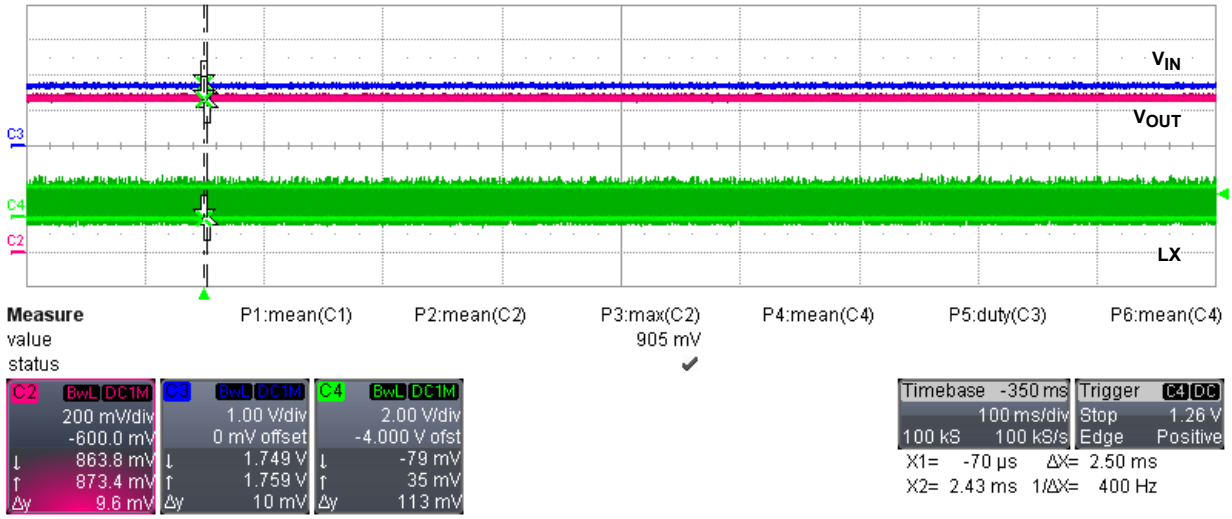



**FIGURE 14. DC BEHAVIOR OF UNIT LOT-3-1 AT +25°C**

## Discussion of Bench Testing Results

Testing began with all 40 units tested at +25°C for power-up, power-down, and DC anomalous $V_{OUT}$. Then four units were selected for testing at temperature (+85°C and +125°C), based on simulation results and bench testing indicating the worst case condition to be high temperature. Finally six units were selected for biased irradiation and these parts were again tested at +25°C. The tabular results of all this testing is presented in Table 3.

TABLE 3. RESULTS OF BENCH TESTING UNITS FOR ANOMALOUS $V_{OUT}$ RESPONSES FOR $V_{IN}$ RISING, FALLING AND DC OPERATION.

| LOT | SN | TEMP (°C) | krad(Si) | RISING (mV) | FALLING (mV) | DC (mV) |
|---|---|---|---|---|---|---|
| LOT-1 | 2621 | +25 | 0 | 109 | 192 | 683 |
| LOT-1 | 2625 | +25 | 0 | 25 | 70 | 289 |
| LOT-1 | 2626 | +25 | 0 | 134 | 92 | 218 |
| LOT-1 | 2634 | +25 | 0 | 147 | 219 | 814 |
| LOT-1 | 2660 | +25 | 0 | 109 | 122 | 212 |
| LOT-1 | 2661 | +25 | 0 | 102 | 109 | 166 |
| LOT-1 | 2662 | +25 | 0 | 25 | 154 | 492 |
| LOT-1 | 2664 | +25 | 0 | 128 | 141 | 134 |
| LOT-1 | 2665 | +25 | 0 | 122 | 116 | 406 |
| LOT-1 | 2666 | +25 | 0 | 113 | 192 | 801 |
| LOT-1 | 2667 | +25 | 0 | 70 | 128 | 387 |
| LOT-1 | 2668 | +25 | 0 | 78 | 147 | 567 |
| LOT-1 | 2669 | +25 | 0 | 89 | 179 | 498 |
| LOT-1 | 2670 | +25 | 0 | 83 | 76 | 317 |
| LOT-1 | 2684 | +25 | 0 | 70 | 467 | 595 |
| LOT-1 | 2684 | +85 | 0 | 184 | 261 | 907 |
| LOT-1 | 2684 | +125 | 0 | 184 | 286 | 920 |
| LOT-1 | 2688 | +25 | 0 | 116 | 206 | 620 |
| LOT-1 | 2691 | +25 | 0 | 154 | 160 | 548 |
| LOT-2 | 2859 | +25 | 0 | 70 | 89 | 418 |
| LOT-2 | 2860 | +25 | 0 | 116 | 179 | 580 |
| LOT-2 | 2862 | +25 | 0 | 63 | | 454 |
| LOT-2 | 2864 | +25 | 0 | 166 | 141 | 762 |
| LOT-2 | 2865 | +25 | 0 | 141 | 173 | 729 |
| LOT-2 | 2866 | +25 | 0 | 106 | 166 | 498 |
| LOT-2 | 2868 | +25 | 0 | 141 | 193 | 814 |
| LOT-2 | 2874 | +25 | 0 | 128 | 173 | 801 |
| LOT-3 | 1 | +25 | 0 | 296 | 297 | 905 |
| LOT-3 | 1 | +25 | 100 | 627 | 448 | |
| LOT-3 | 2 | +25 | 0 | 219 | 222 | 867 |
| LOT-3 | 3 | +25 | 0 | 212 | 265 | 867 |
| LOT-3 | 3 | +85 | 0 | 280 | 344 | 952 |
| LOT-3 | 3 | +125 | 0 | 280 | 389 | 1016 |
| LOT-3 | 4 | +25 | 0 | 212 | 232 | 873 |
| LOT-3 | 4 | +25 | 100 | 425 | 387 | |

TABLE 3. RESULTS OF BENCH TESTING UNITS FOR ANOMALOUS $V_{OUT}$ RESPONSES FOR $V_{IN}$ RISING, FALLING AND DC OPERATION. (Continued)

| LOT | SN | TEMP (°C) | krad(Si) | RISING (mV) | FALLING (mV) | DC (mV) |
|---|---|---|---|---|---|---|
| LOT-3 | 5 | +25 | 0 | 199 | 263 | 880 |
| LOT-4 | 0 | +25 | 0 | 219 | 303 | 867 |
| LOT-4 | 0 | +25 | 100 | 406 | 393 | |
| LOT-4 | 1 | +25 | 0 | 193 | 283 | 847 |
| LOT-4 | 2 | +25 | 0 | 238 | 296 | 873 |
| LOT-4 | 2 | +85 | 0 | 306 | 395 | 965 |
| LOT-4 | 2 | +125 | 0 | 325 | 408 | 978 |
| LOT-4 | 7 | +25 | 0 | 231 | 237 | 873 |
| LOT-4 | 7 | +25 | 100 | 436 | 399 | |
| LOT-4 | 8 | +25 | 0 | 219 | 375 | 867 |
| LOT-5 | 5 | +25 | 0 | 63 | 76 | 115 |
| LOT-5 | 6 | +25 | 0 | 26 | 86 | 179 |
| LOT-5 | 7 | +25 | 0 | 134 | 224 | 542 |
| LOT-5 | 7 | +85 | 0 | 235 | 325 | 920 |
| LOT-5 | 7 | +125 | 0 | 242 | 363 | 971 |
| LOT-5 | 8 | +25 | 0 | 128 | 147 | 215 |
| LOT-5 | 8 | +25 | 100 | 296 | 399 | |
| LOT-5 | 9 | +25 | 0 | 96 | 237 | 606 |
| LOT-5 | 9 | +25 | 100 | 406 | 356 | |

The power-up glitch results at +25°C are graphically presented in Figure 15 on page 18. The extreme point correlates to unit LOT-3-1 and is represented in Figure 10 on page 13.

The power-down glitches at +25°C are graphically represented in Figure 16 on page 18. The extreme value of 467mV corresponds to LOT-1-2684 and is represented in Figure 12 on page 14. This case is an outlier in its form and magnitude. All other parts exhibited a discharge to zero as is the case in Figure 13 on page 14.

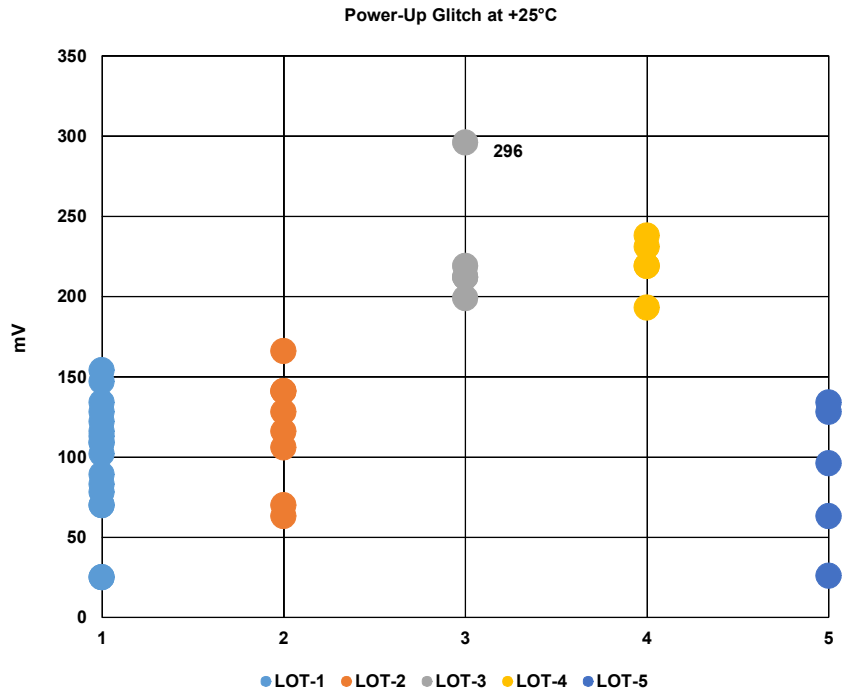



FIGURE 15. POWER-UP GLITCH MAGNITUDES AT +25°C PLOTTED BY PRODUCT LOT GROUPINGS

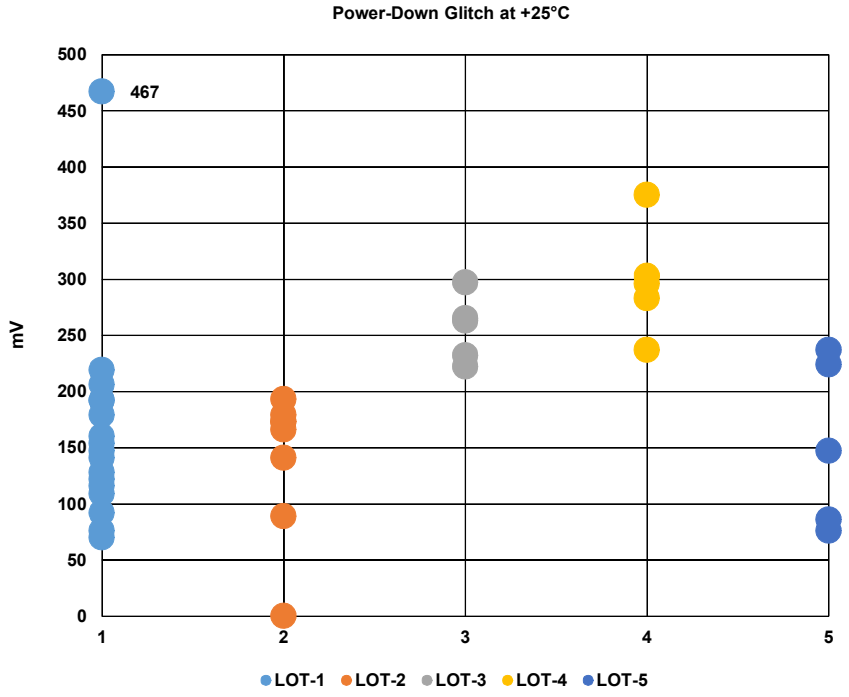



FIGURE 16. POWER-DOWN GLITCH MAGNITUDES AT +25°C PLOTTED BY PRODUCT LOT GROUPINGS

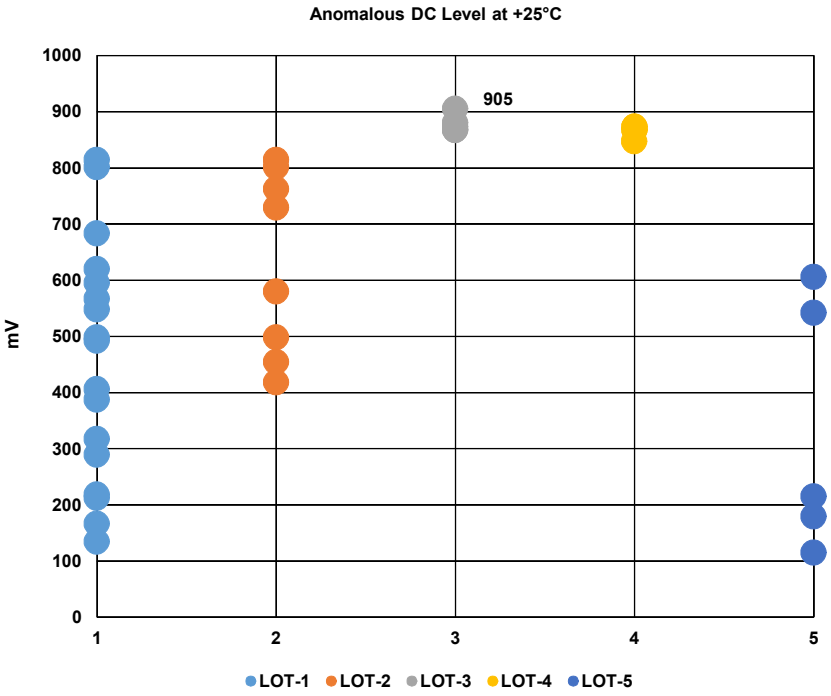



FIGURE 17. ANOMALOUS DC $V_{OUT}$ MAGNITUDES AT +25°C PLOTTED BY PRODUCT LOT GROUPINGS

The parts were also operated with $V_{IN}$ being a DC level and adjusted to give the maximum $V_{OUT}$ output. The results are graphically represented in Figure 17. All parts tested exhibited output voltages less than the set-point at 1.2V.

Four units were selected to test at elevated temperature. As represented in Figure 18 on page 20 all four units tended toward larger power-up glitches as temperature increased. The maximum delta from +25°C was only 114mV at +125°C and the resulting maximum glitch at +125°C was only 325mV. The power-down glitch magnitudes are shown in Figure 19 on page 20. Unit LOT-1-2684 showed more typical behavior at the elevated temperatures than it did at +25°C. The +125°C behavior is depicted in Figure 20 on page 21. This behavior lacks the abrupt rise in $V_{OUT}$ seen in Figure 12 on page 14 and is responsible for the reduced glitch magnitude.

Another six units were selected for post radiation testing. The units were irradiated in the standard biased configuration at 50-300rad(Si)/s to a dose of 100krad(Si). Then, the parts were again tested for glitches at +25°C. Figure 21 on page 21 shows the pre- and post-irradiation power-up glitch magnitudes measured at +25°C. The irradiation led to larger glitch magnitudes with the largest one being LOT-3-1 as already shown in Figure 11 on page 13. The power-down glitch behavior over radiation is shown in Figure 22 on page 22. Again the extreme case is that of LOT-3-1 and has already been shown in Figure 11 on page 13.

Nothing in all the testing done implies that the power-up or power-down behavior of the part will result in the $V_{OUT}$ exceeding the set point (1.2V in the bench cases here). This is consistent with the simulation results.

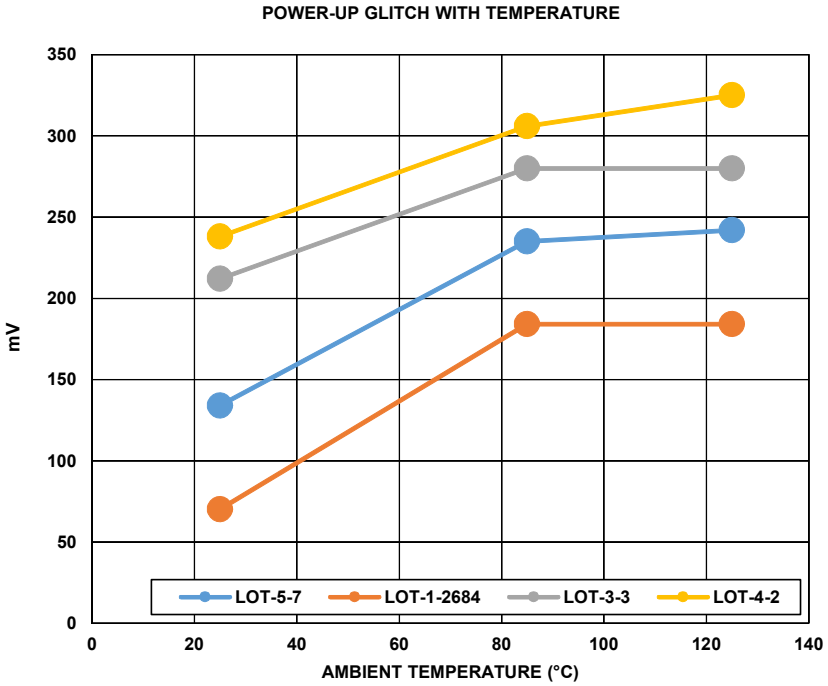



FIGURE 18. POWER-UP GLITCH MAGNITUDES AT TEMPERATURES +25°C, +85°C, AND +125°C FOR FOUR SAMPLED UNITS

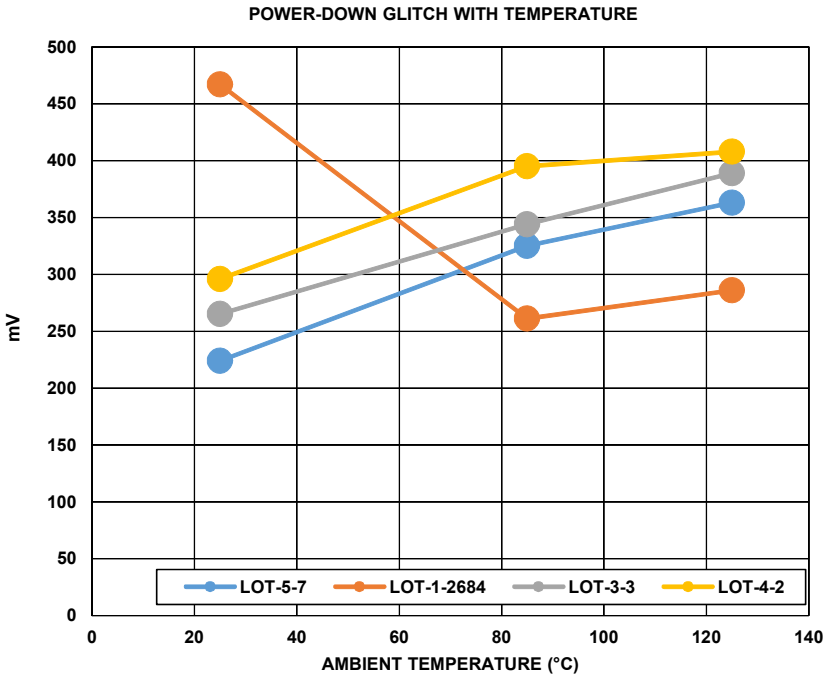



FIGURE 19. POWER-DOWN GLITCH MAGNITUDES AT TEMPERATURES +25°C, +85°C, AND +125°C FOR FOUR SAMPLED UNITS

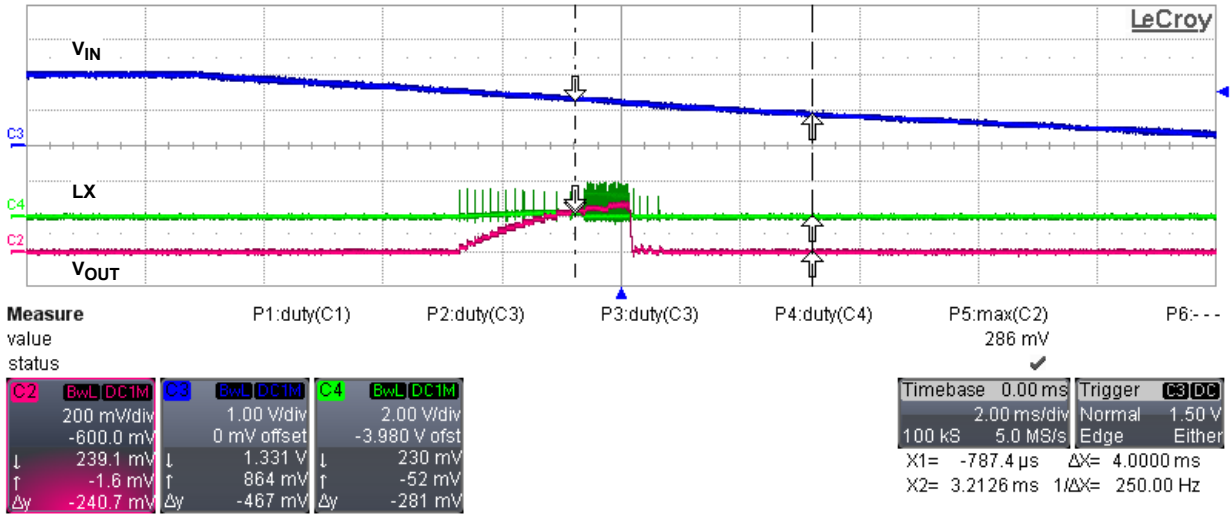



FIGURE 20. LOT-1-2684 POWER-DOWN GLITCH AT +125°C

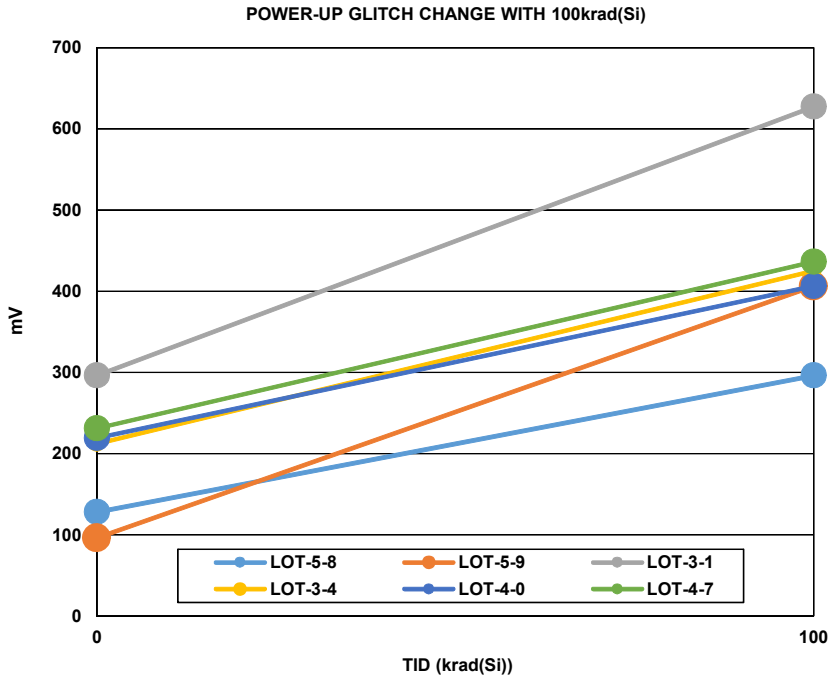



FIGURE 21. PRE- AND POST-RADIATION (100krad(Si)) +25°C POWER-UP GLITCH MAGNITUDES

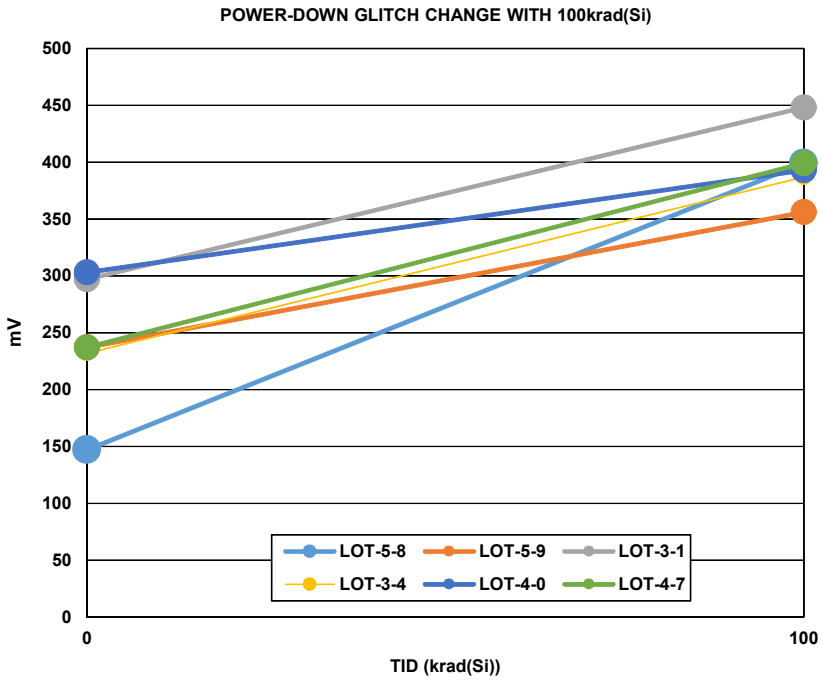



FIGURE 22. PRE- AND POST-RADIATION (100krad(Si)) +25°C POWER-DOWN GLITCH MAGNITUDES

# ISL70001SEH, ISL70001SRH Implemented as Clock Slave or Externally Clocked Device

The ISL70001SEH, ISL70001SRH, when set as a master, the control signal path that controls output activity is such that LX activity starts at ~1.5V prior to it being inhibited by a fuse read at ~1.7V. This design weakness was corrected on the ISL70001A and all subsequent ISL7000x devices.

In the ISL70001SEH, ISL70001SRH when in slave mode, the control signal path from the SYNC input to the output and LX activity is inhibited until the PORSEL selected UVLO threshold is satisfied. This is a different signal path than exists when the ISL70001SEH, ISL70001SRH is in master mode.

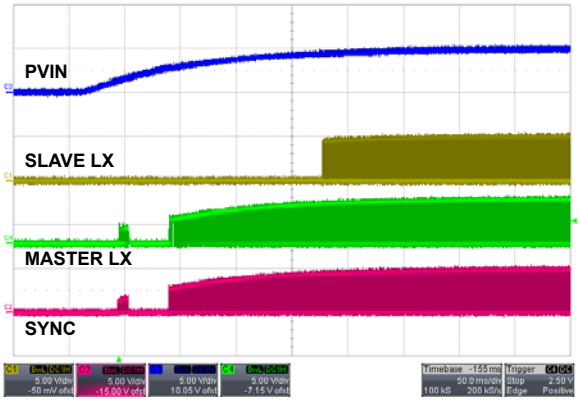



FIGURE 23. SLOW PVIN RISE, RESULTING IN EARLY MASTER LX AND SYNC ACTIVITY WITH NO CLOCKED SLAVE LX ACTIVITY

Figure 23 illustrates the expected behavior when a master and a SYNC clocked slave or externally clocked slave device is powered up slowly. The clocked slave device has its PORSEL = high and the master PORSEL = low. The slow rising PVIN (BLUE) results in the master LX activity (GREEN)) accompanied by SYNC (RED) activity, however, no slave LX (YELLOW) activity until the clocked slave UVLO is satisfied.

# Summary

The conditions where ISL70001SEH, ISL70001SRH do not exhibit LX activity below UVLO.

There are several ways to avoid the possibility of ISL70001SEH, ISL70001SRH LX pin pulsing. Any 1 of these 3 conditions will inhibit the LX pin pulsing below UVLO.

1. External Clock
   a. If the M/S pin is tied low and an external clock is applied to SYNC, the LX pulsing will not occur until UVLO is satisfied.
2. Enable
   a. If the EN pin is held at <0.5 V until $V_{IN}$ > 1.6V, the LX pin pulsing will not occur.
   b. Using a suitable external resistor divider between $V_{IN}$ and EN will prevent LX pin pulsing.
3. PVIN Ramp
   a. A 10V/ms minimum PVIN ramp will prevent the LX pin pulsing.

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