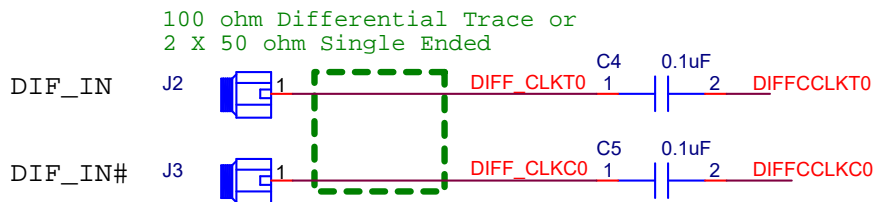
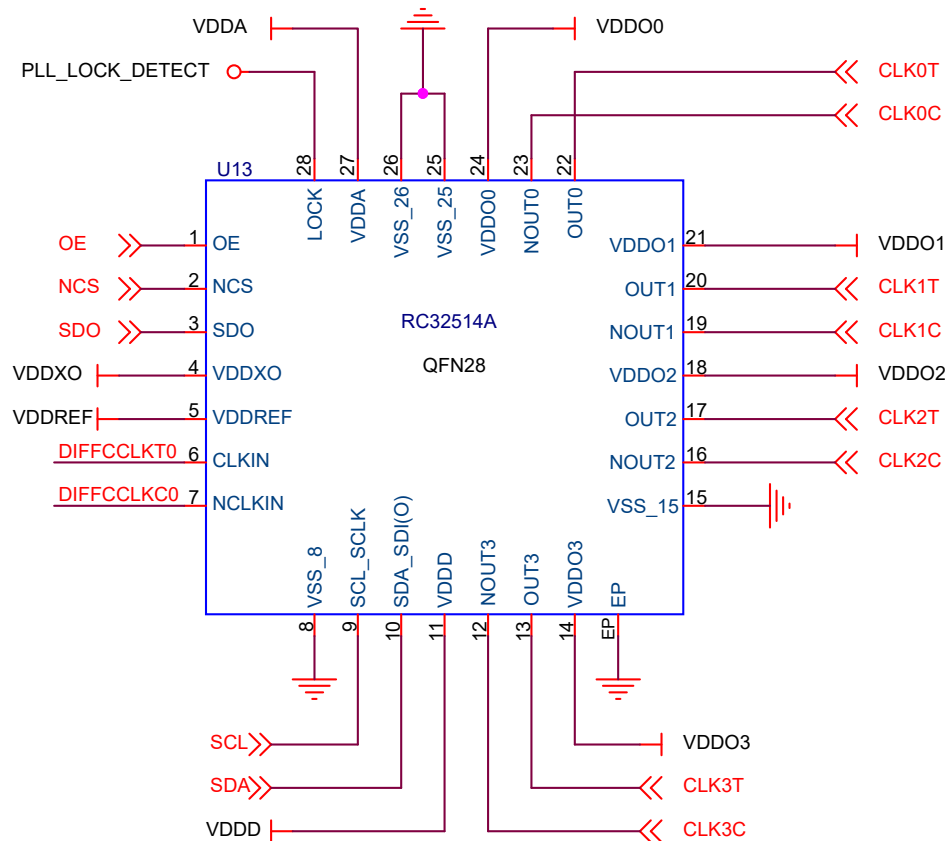


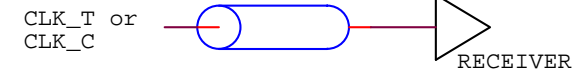
RC32514A with 4 output pairs



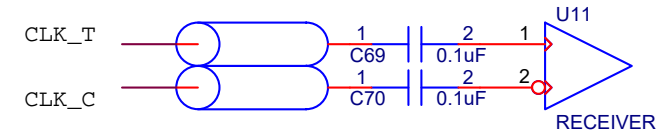
The RC32514A CLKIN input has on-chip termination and DC bias. The CLKIN input is customizable with two types of terminations or the termination disabled. It is also possible to configure CLKIN for single ended CMOS (1.8V swing).

OUTPUT TERMINATION

LVC MOS TERMINATION

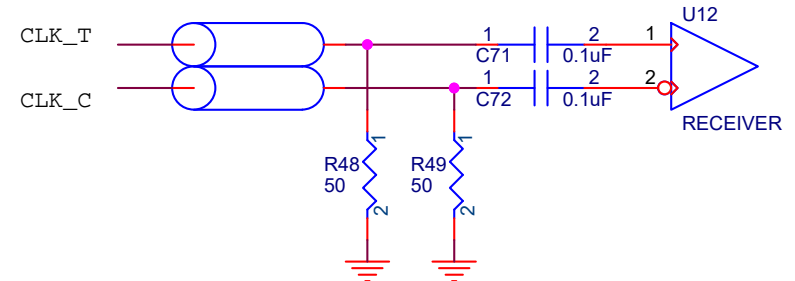


HCSL TERMINATION* using Internal Termination



When internal termination of Merlin output driver is enabled. AC coupling is optional.

HCSL TERMINATION* using External Termination

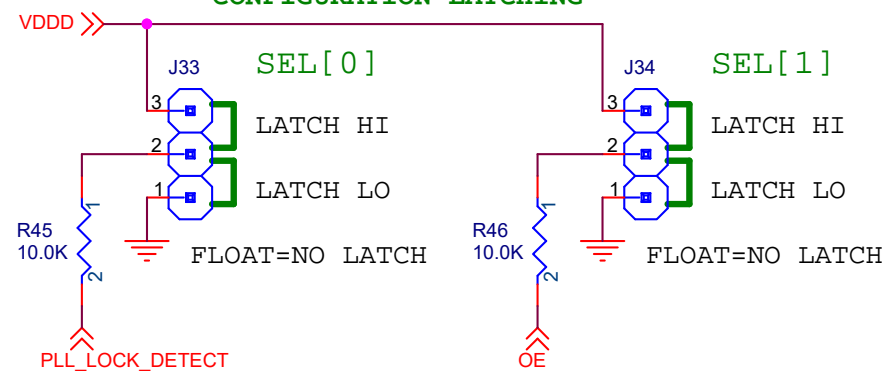


When internal termination is disabled. AC coupling is optional after the external termination with R48 and R49.

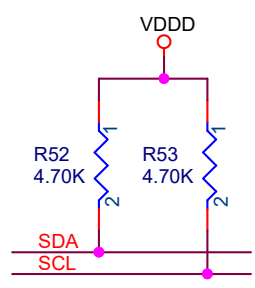
* When AC coupling, the Common Mode Voltage is removed and the differential signal will be compatible with most generic differential clock inputs.

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CONFIGURATION LATCHING



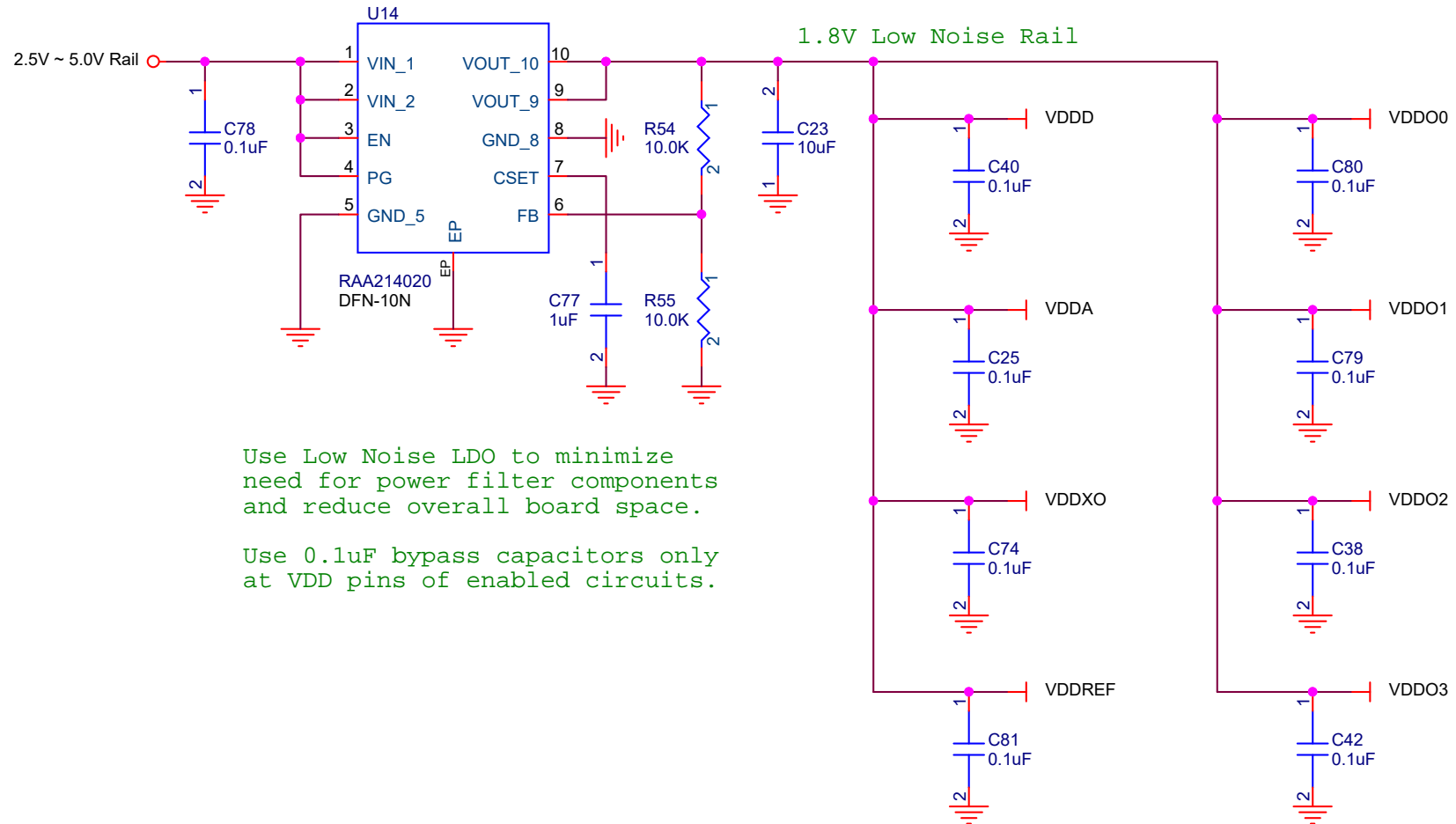
The PLL_LOCK_DETECT and OE pins can be used to latch a pre-programmed configuration. Pull either high or low through a 10K resistor to latch either "1" or "0" for the Select bit. Two bits for selecting one of 4 pre-programmed configurations.



I2C lines SCL and SDA cannot rise above VDDD. Please use Level Shifter when I2C host uses higher than VDDD voltage levels. VDDD can be up to 3.3V to connect to an I2C host without level shifter.

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FemtoClock 2 Reference Schematic		
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POWER SUPPLY FILTERING, USING A REGULATOR



Use Low Noise LDO to minimize need for power filter components and reduce overall board space.

Use 0.1uF bypass capacitors only at VDD pins of enabled circuits.

Title
FemtoClock 2 Reference Schematic

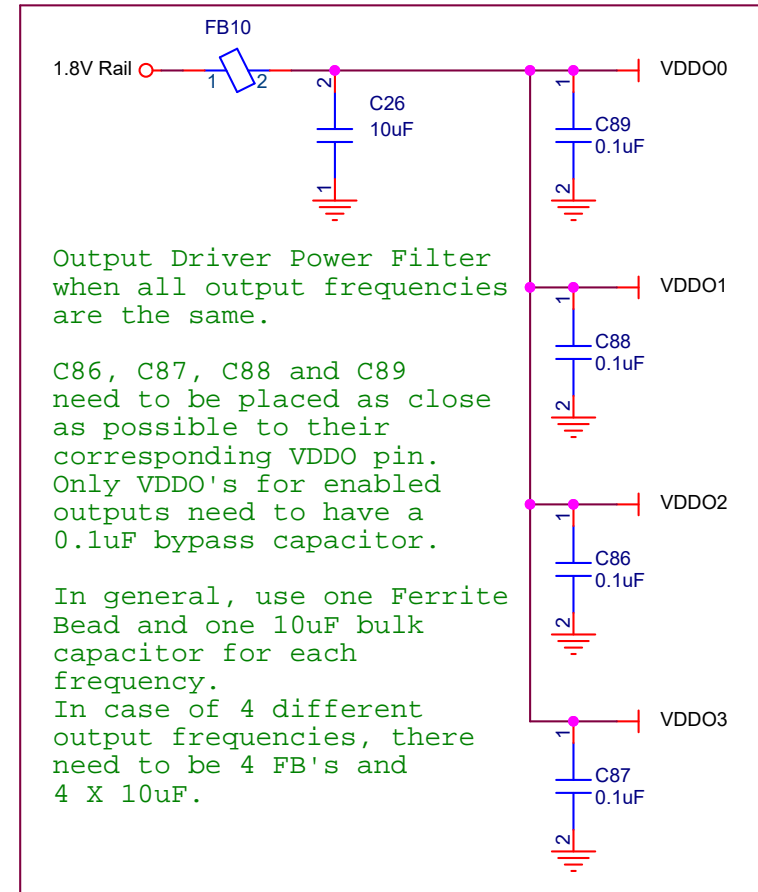
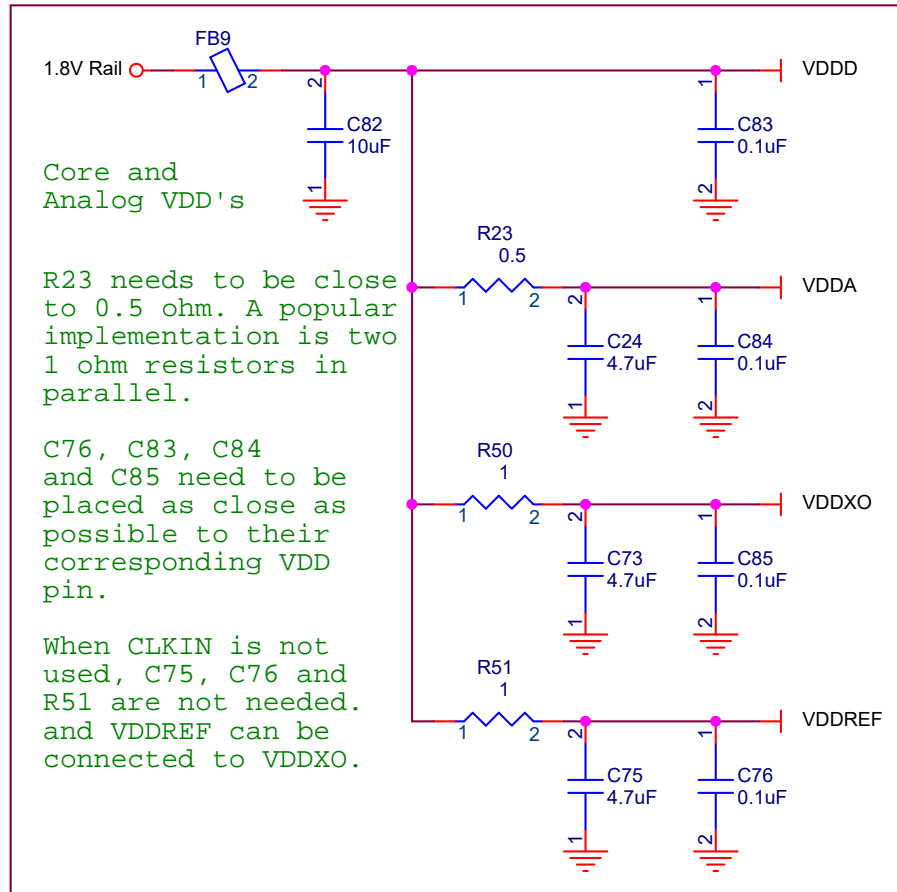
Size A Document Number
RC32514A_FC2_REF-SCHEM

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POWER SUPPLY FILTERING, USING FERRITE BEADS



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