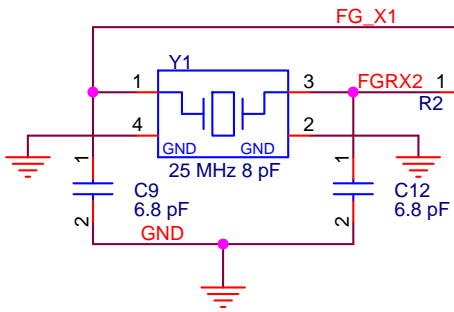
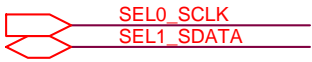
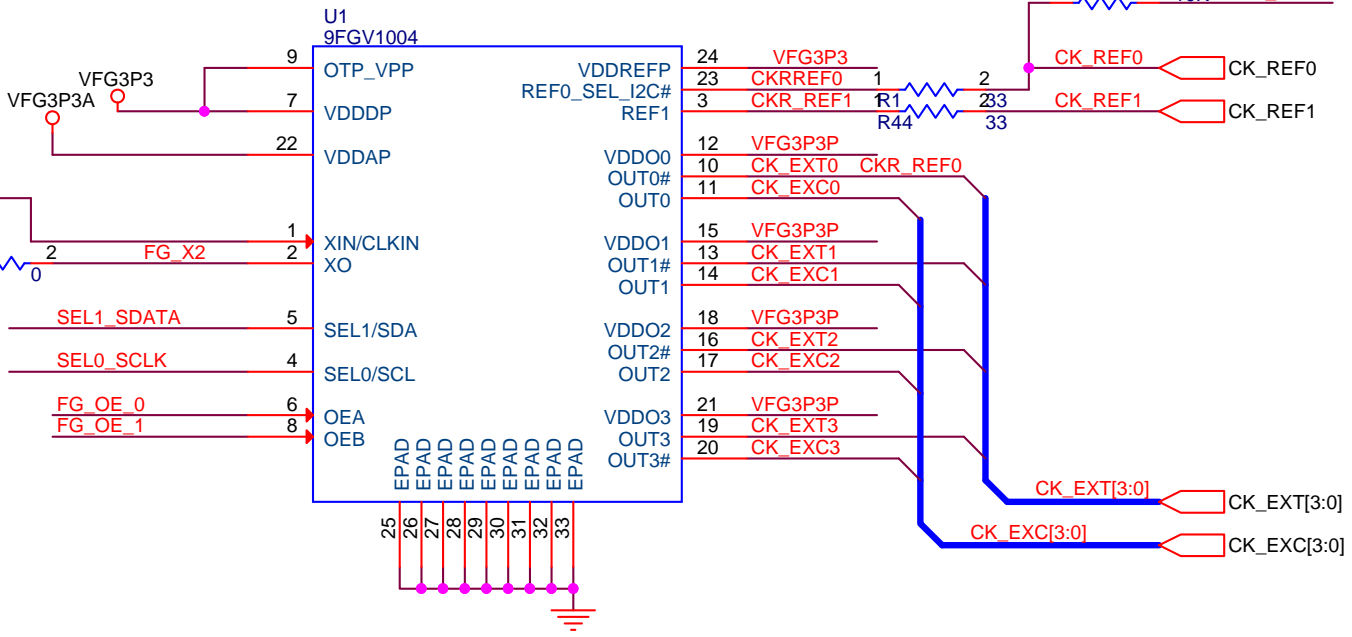
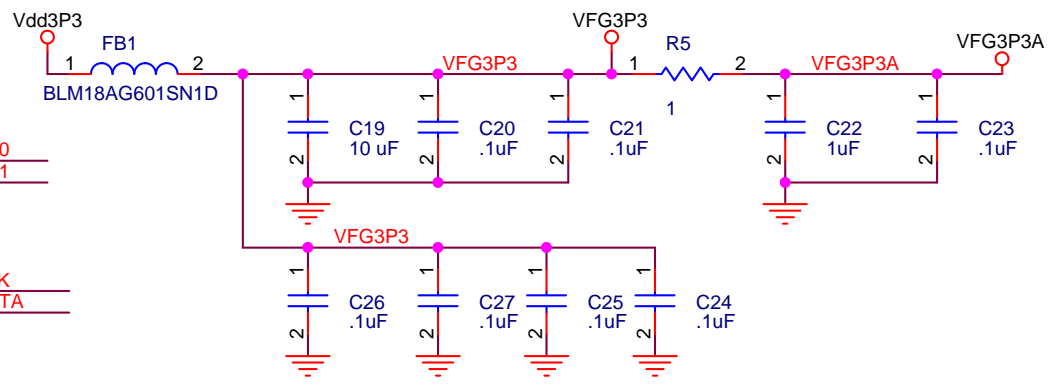
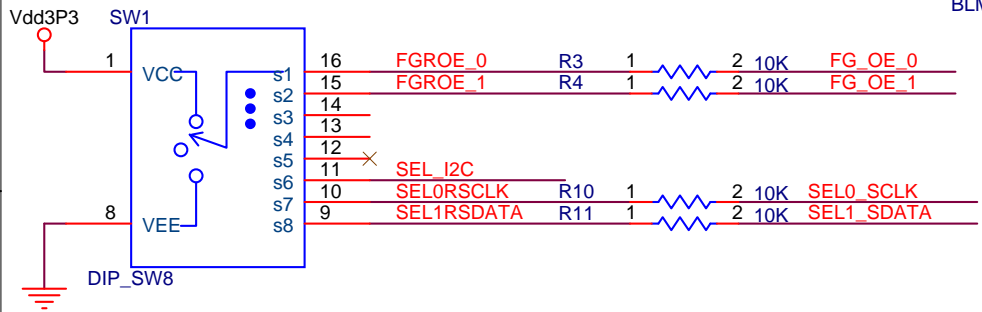


SEL0_SCLK
SEL1_SDAT



Layout notes.

1. Separate Xout and Xin traces by at least 3 x the trace width.
2. Do not share crystal load capacitor ground via with other components.
3. Route power from bead through bulk capacitor pad then through 0.1uF capacitor pad then to clock chip Vdd pad.
4. Do not share ground vias. One ground pin one ground via.
5. Exposed pad should be grounded but is not required.



Integrated Device Technology		
San Jose, CA		
Size A	Document Number 9FGV1004_EVB	Rev 0.2
Date:	Thursday, December 15, 2016	Sheet 1 of 3