

RENESAS SEMICONDUCTOR RELIABILITY REPORT

GROUP : S5D5
DEVICE : R7FS5D5XXX
APPLICATION : Consumer / Industry

Quality Assurance Div.
Renesas Electronics Corporation

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Table. Reliability test results (QFP)

Test Items	Reference	Test Conditions	Results Failure/Size	Comment
High Temperature Operating Life (HTOL)	JESD22-A108	Ta=125 °C, Vccmax, 1000 hrs	0/22	
High Temperature Storage Life (HTSL)	JESD22-A103	Ta=150 °C, 1000 hrs	0/22	
Temperature Humidity bias (THB) (*1)	JESD22-A101	Ta=85 °C, RH=85 %, Vccmax, 1000 hrs	0/22	
Temperature Cycling (TC) (*1)	JESD22-A104	Ta=-65 °C to 150 °C , 300 cycles	0/22	
Latch-Up (LU)	JESD78	Pulse Current Injection, I=+/-150 mA	0/3	
Electrostatic discharge (ESD-HBM)	JS-001	1.5 kΩ, 100 pF, +/-2000 V, 1 time	0/3	Class: 2
Electrostatic discharge (ESD-CDM)	JESD22-C101	+/-500V,1time	0/3	Class: C2
Solderability (SD)	J-STD-002	245 °C, 5 s, Solder coverage ≥95 %	0/5	
Resistance to Soldering Heat (PC)	JESD22-A113, J-STD-020	MSL3(Moisture Sensitivity Level 3)	0/22	

*1) With preconditioning per JESD22-A113, MSL 3

•It is tested to confirm that all the samples are satisfied with an individual product specification.

Note :

Basically qualification tests were performed using a representative product with the same wafer process and the same package structure .

Table. Reliability test results (LGA)

Test Items	Reference	Test Conditions	Results Failure/Size	Comment
High Temperature Operating Life (HTOL)	JESD22-A108	Ta=125 °C, Vccmax, 1000 hrs	0/22	
High Temperature Storage Life (HTSL)	JESD22-A103	Ta=150 °C, 1000 hrs	0/22	
Temperature Humidity bias (THB) (*1)	JESD22-A101	Ta=85 °C, RH=85 %, Vccmax, 1000 hrs	0/22	
Temperature Cycling (TC) (*1)	JESD22-A104	Ta=-55 °C to 125 °C , 500 cycles	0/22	
Latch-Up (LU)	JESD78	Pulse Current Injection, I=+/-150 mA	0/3	
Electrostatic discharge (ESD-HBM)	JS-001	1.5 kΩ, 100 pF, +/-2000 V, 1 time	0/3	Class: 2
Electrostatic discharge (ESD-CDM)	JESD22-C101	+/-500V,1time	0/3	Class: C2
Resistance to Soldering Heat (PC)	JESD22-A113, J-STD-020	MSL3(Moisture Sensitivity Level 3)	0/22	

*1) With preconditioning per JESD22-A113, MSL 3

·It is tested to confirm that all the samples are satisfied with an individual product specification.

Note :

Basically qualification tests were performed using a representative product with the same wafer process and the same package structure .

The failure rate of the device in an actual use condition can be estimated by the below procedure.

•Equation for the failure rate estimation (λ)

$$\lambda = \lambda_b \times \pi T \text{ (FIT)}$$

① Unique failure rate (λ_b)

$$\lambda_b = 0.08 \text{ FIT}$$

Unique failure rate at $T_a = 55^\circ\text{C}$ using 60 % confidence level.

② Temperature term (πT)

$$\pi T = \exp\{11600 \times E_a \times (1/(273+55) - 1/(273+T_a))\}$$

E_a : Activation energy (eV)

T_a : Ambient temperature ($^\circ\text{C}$)

πT simplified chart as $E_a = 0.7 \text{ eV}$												
T_a ($^\circ\text{C}$)	40	50	55	60	65	70	75	80	85	90	100	110
πT	0.31	0.68	1	1.45	2.08	2.95	4.15	5.77	7.96	10.88	19.82	34.99

•MTTF (Mean Time To Failure)

$$MTTF = 1/\lambda$$

Reference about Renesas package code

Package type		Package code *1
Lead type plastic package	QFP	PxQP
Non-lead type plastic package	QFN	PxQN
Grid array type plastic package	BGA	PxBG
	LGA	PxLG

*1. First four digit

Table. Product list

No	Group	Product part number	Package code	No	Group	Product part number	Package code
1	S5D5	R7FS5D57A3A01CFB	PLQP0144K*	51			
2	S5D5	R7FS5D57C3A01CFB	PLQP0144K*	52			
3	S5D5	R7FS5D57A3A01CFP	PLQP0100K*	53			
4	S5D5	R7FS5D57C3A01CFP	PLQP0100K*	54			
5	S5D5	R7FS5D57A2A01CLK	PTLG0145K*	55			
6	S5D5	R7FS5D57A3A01CLK	PTLG0145K*	56			
7	S5D5	R7FS5D57C2A01CLK	PTLG0145K*	57			
8	S5D5	R7FS5D57C3A01CLK	PTLG0145K*	58			
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48				98			
49				99			
50				100			