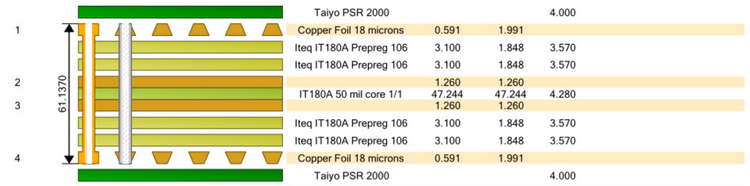
AVS MASTER DONGLE ALPHA SCHEMATICS

SCHEMATIC PAGE DISCRIPTION

PAGE01 : COVER SHEET
PAGE02 : SYSTEM BLOCK DIAGRAM
PAGE03 : USB, MCU, SPI, AVS CONNECTOR
PAGE04 : REVISION HISTORY

PCB LAYER STACKUP



Layer	Stack up	Description	Base Thickness	Processed Thickness	er
		Taiyo PSR 2000			4.000
1		Copper Foil 18 microns	0.591	1.991	
		Iteq IT180A Prepreg 106	3.100	1.848	3.570
		Iteq IT180A Prepreg 106	3.100	1.848	3.570
2			1.260	1.260	
		IT180A 50 mil core 1/1	47.244	47.244	4.280
3			1.260	1.260	
		Iteq IT180A Prepreg 106	3.100	1.848	3.570
		Iteq IT180A Prepreg 106	3.100	1.848	3.570
4		Copper Foil 18 microns	0.591	1.991	
		Taiyo PSR 2000			4.000

Copper Thickness = 6.501 |Dielectric Thickness = 54.636 |Solder Mask Thickness = 4.000

Impedance Signal Layer	Structure Name	Ref. Plane 1 in Layer	Ref. Plane 2 in Layer	Lower Trace Width (W1)	Trace Separation (S1)	Ground Strip Separation (D1)	Calculated Impedance	Target Impedance	Tol (+/- %)
1	Coated Microstrip 1B	2	0	5.990	0.000	0.000	49.990	50.000	10.000
1	Edge Coupled Coated Microstrip 1B	2	0	5.000	5.648	0.000	90.000	90.000	10.000
4	Coated Microstrip 1B	3	0	5.990	0.000	0.000	49.990	50.000	10.000
4	Edge Coupled Coated Microstrip 1B	3	0	5.000	5.648	0.000	90.000	90.000	10.000

1. PCB MATERIAL: IT180A

2. NUMBER OF LAYERS: 4

Layer 1 - Signal
Layer 2 - GND
Layer 3 - Power
Layer 4 - Signal

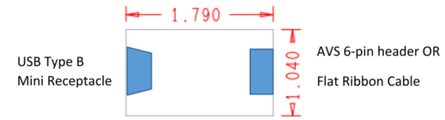
3. IMPEDANCE CONTROL: YES

a. 90 ohm Differential for USB
b. 50 ohm single ended for other signals

MAJOR REVISION HISTORY

REV	PCB Part No	PCA Part No	DATE	Remark
1.0	ISLAVSEVAL1Z		12-MAY-2015	Alpha PCB released for fabrication
2.0	ISLAVSEVAL1Z Rev B		18-AUG-2015	Beta PCB released for fabrication

PCB MECHANICAL DETAILS



1. PCB SIZE: 1.790 X 1.040 in (+/-TBD)

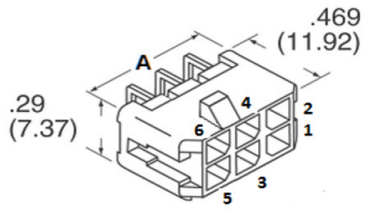
2. PCB THICKNESS: 0.062 in (+/-TBD)

I2C ADDRESS TABLE

MCU REF	VOLTAGE	REFERENCE DESIGNATOR	DESCRIPTION	8 BIT ADDRESS
I2C0	3.3V	U8	D TO A CONVERTER INTERFACE	1100000R/Wb
I2C0	3.3V	U11	DIGITAL POTENTIOMETER	1010000R/Wb

Note: LSB of 8 bit I2C address is 0 for write operation and is 1 for read operation.

AVS CONNECTOR PINOUT



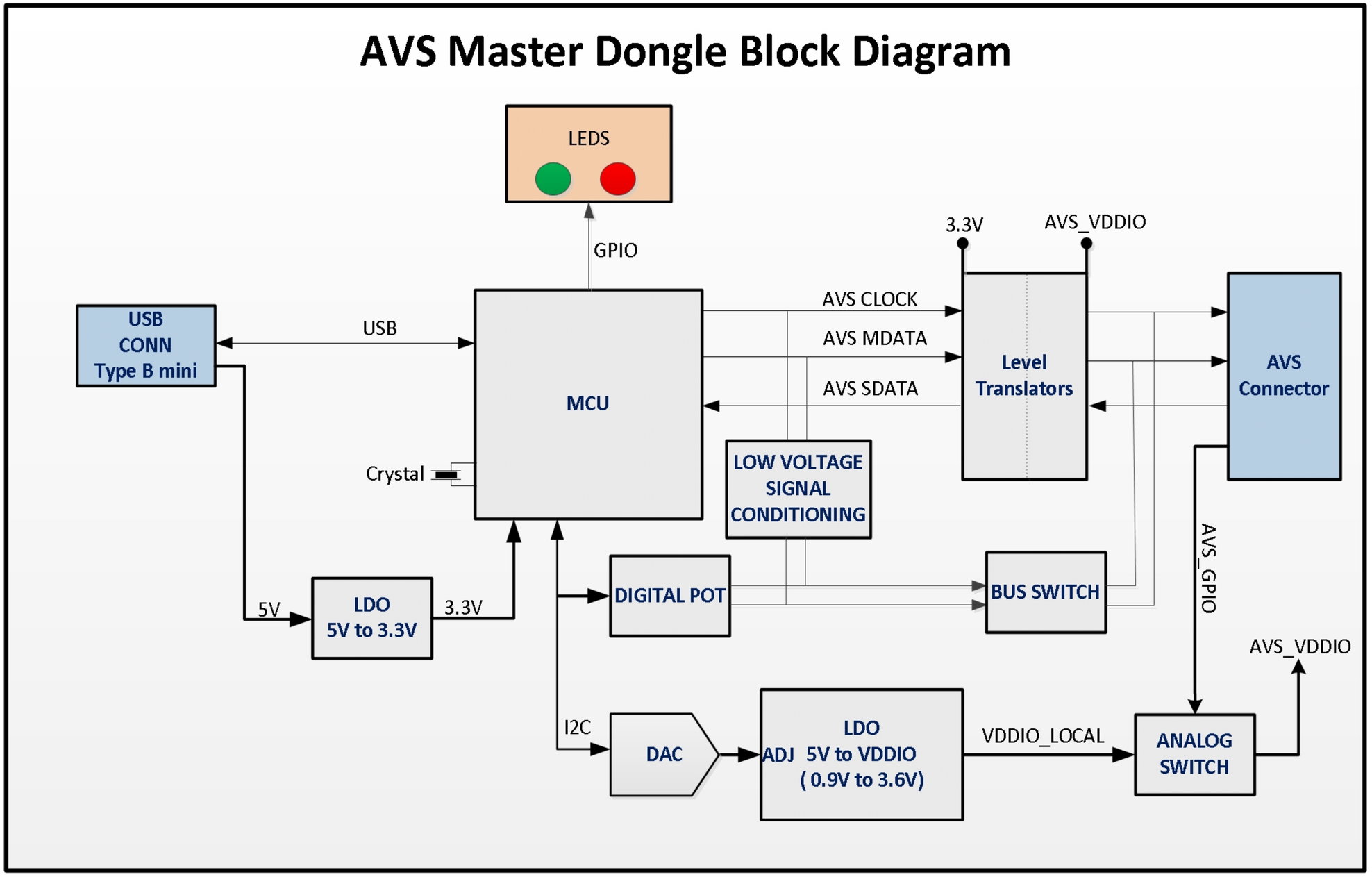
Pin Number	Pin Name	Description
1	AVSCLK	AVS Clock (From Master to Slave)
2	AVSSDATA	AVS Slave Data (From Slave to Master)
3	AVSMDATA	AVS Master Data (From Master to Slave)
4	GND	Ground
5	VDDIO	Communication Voltage (From Master to Slave)
6	GPIO	Configurable Input/Output (Functionality to be decided later)

SCHEMATIC NOTES

1. PARTS NOT INSTALLED ARE INDICATED WITH 'DNP'
2. SIGNAL NET NAMES WITH "_N" SUFFIX, ARE ACTIVE LOW SIGNALS

Project	AVS_Master_Dongle	Designed for Intersil by eInfochips
Title	COVER SHEET	intersil eInfochips The Solutions People
Size D	eInfochips#: 16_00258_02	Rev 2.0
Date: Tuesday, August 18, 2015	Sheet 1 of 4	

SYSTEM BLOCK DIAGRAM



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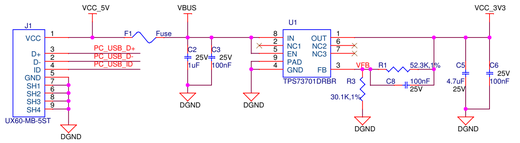
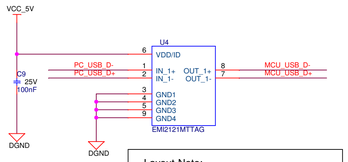
USB, MCU, SPI, AVS CONNECTOR

USB 2.0 HIGH SPEED INTERFACE

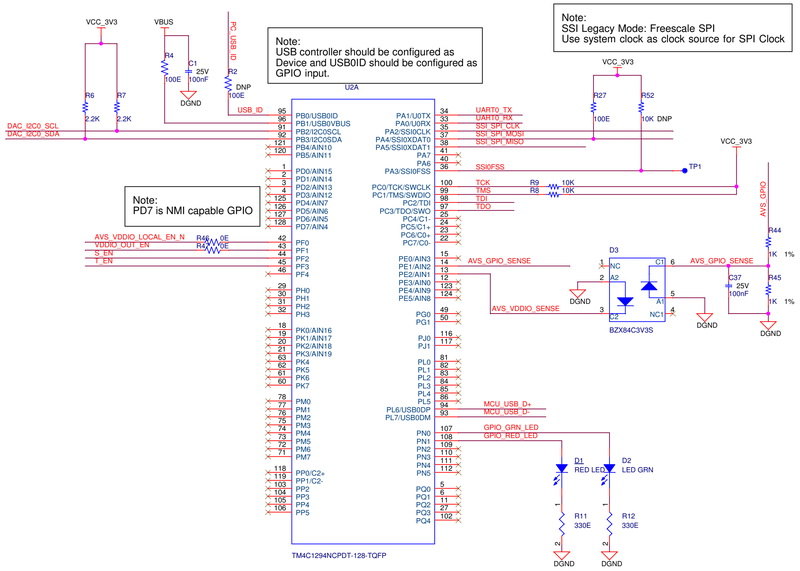




Layout Note:
Place EMI2121 close to USB Mini-B connector without via.

For better routing IN_1+/OUT_1+ and IN_1-/OUT_1- are connected to DM and DP respectively.

MCU



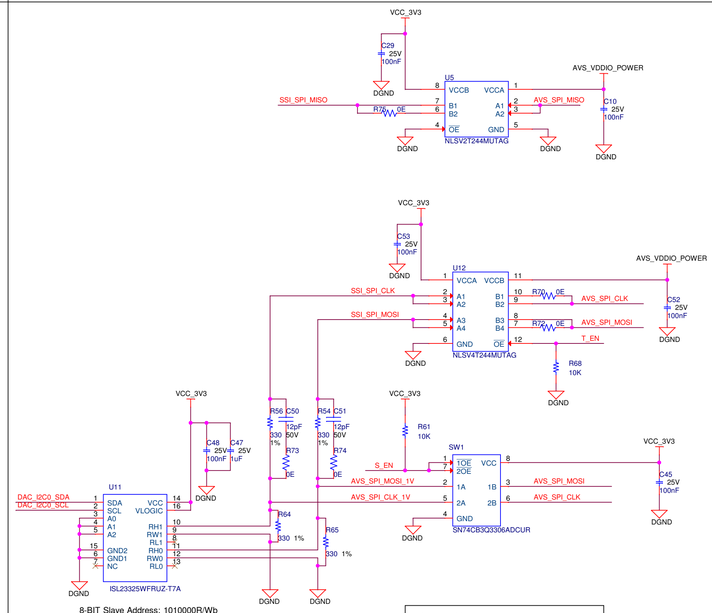
Note:
USB controller should be configured as Device and USB0ID should be configured as GPIO input.

Note:
SSI Legacy Mode: Freescale SPI
Use system clock as clock source for SPI Clock

Note:
PD7 is NMI capable GPIO

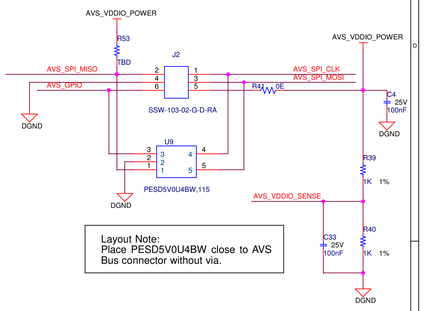
LED Indicators:
State: Green blink, Red off---good traffic
State: Green on, Red off---power good, no traffic
State: Green off, Red blink---bad traffic (SlaveAck is not good)

AVS BUS LEVEL TRANSLATOR

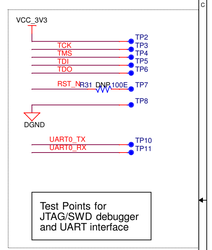


Layout Note:
Place level translators close to AVS Bus connector.

AVS BUS INTERFACE

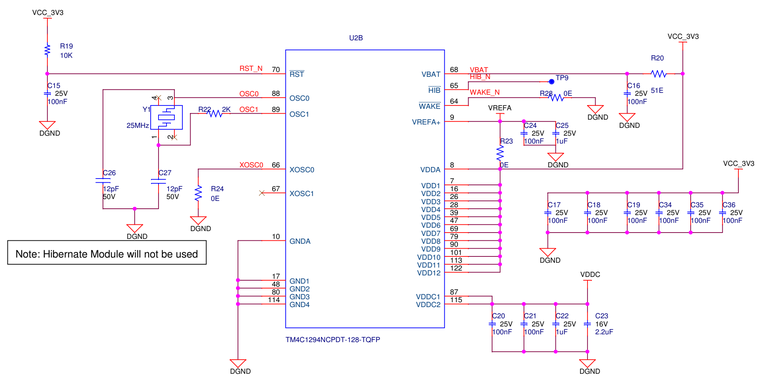


Layout Note:
Place PESD5V0U4BW close to AVS Bus connector without via.



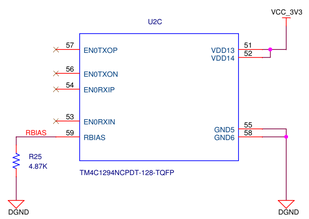
Test Points for JTAG/SWD debugger and UART interface

MCU POWER, RESET & CLOCK



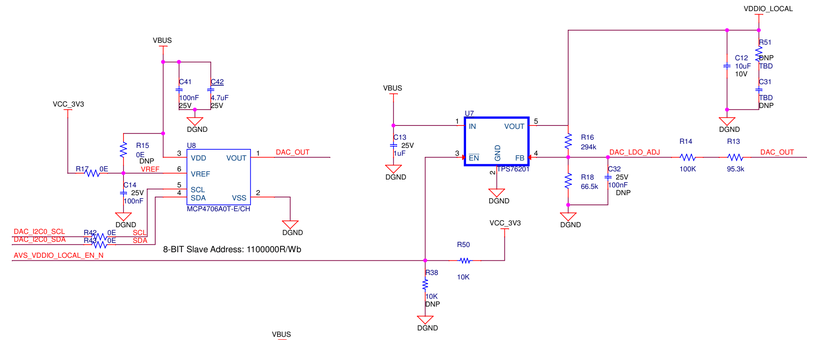
Note: Hibernate Module will not be used

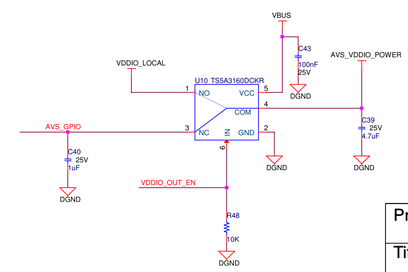
Layout Note:
Place C23,C22 and, C21/C20 close to Pin 115 and C20/C21 at Pin 87.



Note: Ethernate Module will not be used

VDDIO GENERATION





Note:
Analog switch (2X1 mux/demux) provided to select VDDIO_LOCAL / AVS_GPIO.

MOUNTING HOLE

MT1 MT2 MT3 MT4
163MIL NPTH HOLE

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Title USB,MCU,SPI,AVS CONN		
Size D	eInfochips#: 16_00258_02	Rev 2.0
Date: Tuesday, August 18, 2015	Sheet 3 of 4	

PCB Rev.	SCH Rev.	DESCRIPTION	DATE
1.0	0.01	1.Create Initial Draft schematic.	23APR2015
	0.02	1.Added R32,R33 and R34 for future option during alpha. 2.Changed U3 connection and swapped CLK and MISO line for better placement. 3. Changed U4 connection and swapped D+ and D- connection for better placement and to avoid line crossover. 4. Changed U9 connection for better placement 5. Added testpoints on UART0 Tx (TP10) and UART0 Rx (TP11) line for debugging during software development. 6. Added R35, R36 and R37 are added in schematic for series termination. 7. R38 pull up added in schematic for VDDIO LDO enable line control. 8. C32 decoupling capacitor is added on DAC output voltage for transient improvement. 9. C31 added on VDDIO for decoupling.	28APR2016
	0.03	1.Added R39, R40 and C33 for sensing AVS_VDDIO using ADC of microcontroller. 2. C34, C35 and, C36 decoupling capacitor are added in schematic.	02MAY2015
	0.04	1. Support circuit for bidirectional AVS_VDDIO added in scheamic following are the changes in schematic -ADC CH-2 is used to sense external VDDIO & zener protection. -Added U10 load switch in schematic to provide supply to slave.	04MAY2015
	0.05	1. Added Analog Mux/demux (2X1) switch to select power source for translator either from VDDIO_LOCAL or AVS_GPIO/ AVS_VDDIO. 2. Removed Load switch from schematic. 3. ADC CH-2 is used to sense AVS_GPIO instead of AVS_VDDIO_LOCAL.	06MAY2015
	0.06	1. R49 removed from schematic and direct AVS_GPIO is connected to analog switch for ease of routing. 2. VDDC net name given to internal LDO filter net. 3. eI_Part# property updated for procurement purpose.	11MAY2015
	1.0	Released Alpha schematic for PCB fabrication.	12MAY2015

PCB Rev.	SCH Rev.	DESCRIPTION	DATE
2.0	1.01	1. R39, R40 and R44, R45 value changed to 1K from 10K. 2. R51 added in series with C12 to minimize ripple by stabilizing control loop of LDO (U7). 3. C12 type changed to tantalum capacitor and C32 made DNP in schematic.	01JULY2015
	1.02	1. ADC Module R39, R40,C33,R44, R45,C37 and D3 made DNP in schematic. 2. Added R52 pull up on SSI0FSS. 3. Added R53 pull up on AVS_SPI_MISO line.	20JULY2015
	1.03	1. ADC Module R39, R40,C33,R44, R45,C37 and D3 changed to mount from DNP. 2. C39 value changed to 4.7uF from 1uF.	24JULY2015
	1.04	1. Programmable Resistor divider option added to support low voltage communication at higher speed.	17AUG2015
	2.0	Beta Release	18AUG2015

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