PRODUCT CHANGE NOTICE

Data Sheet Specification Change for Intersil Product ISL78600ANZ*

Refer to:
PCN15003

Date: January 19, 2015

intersil™

January 19, 2015

To: Our Valued Intersil Customers

Subject: **Data Sheet Specification Change for Intersil Product ISL78600ANZ***

This notice is to inform you that Intersil has changed the data sheet specification for the ISL78600ANZ* products. The change involves multiple changes to the electrical table along with additional clarification of product operation on this complex device. The change aligns the data sheet with the product characteristics and is necessary to maintain product manufacturability in support of customer delivery requirements. Details regarding the change are contained on the following pages. The updated data sheet is available upon request, please send your request by email to: Automotive@intersil.com.

Products affected: ISL78600ANZ ISL78600ANZ-T

There have been no changes to the die/silicon or product itself. There will be no change in the external marking of the packaged parts.

Intersil will take all necessary actions to conform to agreed upon customer requirements and to ensure the continued high quality and reliability of Intersil products being supplied. Customers may expect to receive product electrically screened to the revised data sheet beginning *ninety* days from the date of this notification or earlier with approval.

If you have concerns with this advisory, Intersil must hear from you promptly. Please contact the nearest Intersil Sales Office or call the Intersil Corporate line at 1-888-468-3774, in the United States, or 1-321-724-7143 outside of the United States.

Regards,

Jeffrey Touvell

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Intersil Corporation PCN15003

CC: W. Choroco C. Martinez G. MacDonald N. Lyne

PCN15003 Data Sheet Change

Original:

ESD Rating
- Human Body Model (Tested per JESD22-A114F) 2kV
- Machine Model (Tested per JESD22A115-A) 200V
- Capacitive Discharge Model (Tested per JESD22-C101D) 750V

Latch Up (Tested per JESD-78B; Class 2, Level A) 100mA

Recommended Operating Conditions

T_A, Ambient Temperature Range . . . . . -40°C to +105°C
V_{BAT} . . . . . 6V to 60V
V_{BAT} (Daisy Chain Operation) . . . . . 10V to 60V
VCn (for n = 1 to 12) . . . . . V(VCn-1) to V(VCn-1) + 5V
VCO . . . . . -0.1V to 0.1V
CBn (for n = 1 to 9) . . . . . V(VCn-1) to V(VCn-1) + 9V
CBn (for n = 10 to 12) . . . . . V(VCn) -9V to V(VCn)
DIN, SCLK, $\overline{CS}$, DOUT, $\overline{Data\ Ready}$, Comms Select 1, Comms Select 2, ExT1, ExT2, ExT3, ExT4, TEMPREG, REF, V3P3, VCC, $\overline{Fault}$, Comms Rate 0, Comms Rate 1, EN, VDDEXT . . . . . 0V to 3.6V

New:

Recommended Operating Conditions

T_A, Ambient Temperature Range . . . . . -40°C to +105°C
V_{BAT} . . . . . 6V to 60V
V_{BAT} (Daisy Chain Operation) . . . . . 10V to 60V
VCn (for n = 1 to 12) . . . . . V(VCn-1) to V(VCn-1) + 5V
VCO . . . . . -0.1V to 0.1V
CBn (for n = 1 to 9) . . . . . V(VCn-1) to V(VCn-1) + 9V
CBn (for n = 10 to 12) . . . . . V(VCn) -9V to V(VCn)
DIN, SCLK, $\overline{CS}$, COMMS SELECT 1, COMMS SELECT 2, V3P3, VCC, COMMS RATE 0, COMMS RATE 1, EN . . . . . 0V to 3.6V
ExT1, ExT2, ExT3, ExT4 . . . . . 0V to 2.5V

ESD Rating
- Human Body Model (Tested per JESD22-A114F) 2kV
- Capacitive Discharge Model (Tested per JESD22-C101D) 500V

Latch-up (Tested per JESD-78B; Class 2, Level A) 100mA

Electrical Specifications V_{BAT} = 6 to 60V, T_A = -20°C to +60°C, unless otherwise specified. Biasing setup as in Figure 56 on page 84 or equivalent.

				New				Original			
PARAMETER	SYMBOL	TEST CONDITIONS		MIN (Note 7)	TYP	MAX (Note 7)	UNIT	MIN (Note 7)	TYP	MAX (Note 7)	UNIT
V_{BAT} Supply Current	I_{VBAT}	Non Daisy Chain configuration. Device enabled. No communications, ADC, measurement, balancing or open wire detection activity.	6V	7	35	80	µA	15	35	60	µA
			39.6V	0	64	241	µA	15	64	150	µA
			60V	0	90	250	µA	15	90	160	µA
		-40°C to +105°C (Note 9)		0		280	µA			200	µA
	$I_{VBATMID}$	Daisy Chain configuration – mid stack device. Enabled. No communications, ADC, measurement, balancing or open wire detection activity.	6V	700	1020	1210	µA	700	1020	1200	µA
			39.6V	900	1250	1560	µA	900	1250	1500	µA
			60V	1000	1400	1700	µA	1000	1400	1700	µA
		-40°C to +105°C (Note 9)				1850	µA			1850	µA
		Peak current when Daisy Chain transmitting			18		mA		18		mA
	$I_{VBATSLEEP2}$ (Note 9)	Sleep mode (EN = 1, Stand-alone, non-Daisy Chain)		3.5	8	16	µA	5	8	14	µA
		40°C to +105°C		3		70	µA	5		23	µA
	$I_{VBATSHDN}$ (Note 9)	Shutdown. device “off” (EN = 0) (Daisy Chain and Non-Daisy Chain configurations)	6V	1.5	7	15.5	µA	5	7	14	µA
			39.6V	3	7	18	µA	N/A	N/A	N/A	µA
			60V	5	7	23	µA	N/A	N/A	N/A	µA
		-40°C to +105°C		1		77	µA	5		23	µA
VCC Supply Current	I_{VCC}	Device enabled (EN = 1). Stand-Alone or Daisy Configuration. No ADC or Daisy Chain communications active.		2.0	3.25	4.5	mA	2.0	3.25	4.5	mA
		-40°C to +105°C (Note 9)		2.0		5.0	mA	2.0		5.0	mA
	$I_{VCCSHDN}$	Device disabled (EN = 0). Shutdown mode.		0	1.2	4.1	µA	0	1.2	3.5	µA
		-40°C to +105°C (Note 9)				9.0	µA			9.0	µA

			New				Original			
PARAMETER	SYMBOL	TEST CONDITIONS	MIN (Note 7)	TYP	MAX (Note 7)	UNIT	MIN (Note 7)	TYP	MAX (Note 7)	UNIT
MEASUREMENT SPECIFICATIONS										
Cell Input Current. Note: Cell accuracy figures assume a fixed 1kΩ resistor is placed in series with each VCn pin (n = 0 to 12)	I_{VCELL}	VC0 input VC0 ≥ 0.5 and VC0 ≤ 4.0V	-1.5	-1	-0.5	µA	-1.5	-1	-0.5	µA
		VC0 > 4.0V	-1.75		-0.5	µA	-1.75		-0.5	µA
		-40°C to +105°C (Note 9)	-2.0	-1	-0.5	µA	-2.0	-1	-0.5	µA
		VC1, VC2, VC3 inputs VCn - VC(n-1) ≥ 0.5 and VCn-VC(n-1) ≤ 4.0V	-2.7	-2	-1.3	µA	-2.7	-2	-1.3	µA
		VCn - VC(n-1) > 4.0V	-2.85		-1.0	µA	-2.85		-1.0	µA
		-40°C to +105°C (Note 9)	-3.0	-2	-0.84	µA	-3.0	-2	-1.0	µA
		VC4 input VCn - VC(n-1) ≥ 0.5 and VCn-VC(n-1) ≤ 4.0V	-0.6	0	0.71	µA	-0.6	0	0.6	µA
		VCn - VC(n-1) > 4.0V	-0.8		1.15	µA	-0.7		0.85	µA
		-40°C to +105°C (Note 9)	- 0.84	0	1.31	µA	- 0.8	0	0.95	µA
		VC5, VC6, VC7, VC8, VC9, VC10, VC11 inputs VCn - VC(n-1) < 2.6V	0.5	2	2.7	µA	0.5	2	2.7	µA
		VCn - VC(n-1) ≥ 2.6V and VCn-VC(n-1) ≤ 4.0V	1.32	2	2.89	µA	1.5	2	2.7	µA
		VCn - VC(n-1) > 4.0V	1.16	2	3.33	µA	1.5	2	3.1	µA
		-40°C to +105°C (Note 9)	0.5	2	3.43	µA	0.5	2	3.25	µA
		VC12 input VC12 - VC11 ≥ 0.5 and VC12-VC11 ≤ 4.0V	0.37	1	1.85	µA	0.6	1	1.7	µA
		VC12 - VC11 > 4.0V	0.19		2.3	µA	0.6		2.05	µA
		-40°C to +105°C (Note 9)	0.15	1	2.47	µA	0.6	1	2.3	µA
Initial V_{BAT} monitor Voltage Error (Note 10)	ΔV_{BAT}	Measured at V_{BAT} = 36V to 43.2V	-100		100	mV	-100		100	mV
		Measured at V_{BAT} = 31.2V to 48V	-125		125	mV	-125		125	mV
		Measured at V_{BAT} = 31.2V to 59.4V	-250		250	mV	-250		250	mV
		Measured at V_{BAT} = 6V to 59.4V	-320		332	mV	-300		300	mV
		Measured at V_{BAT} = 6V to 59.4V -40°C to +105°C (Note 9)	-490		490	mV	-490		490	mV

			New				Original			
PARAMETER	SYMBOL	TEST CONDITIONS	MIN (Note 7)	TYP	MAX (Note 7)	UNIT	MIN (Note 7)	TYP	MAX (Note 7)	UNIT
External Temperature Input Gain Error	V_{EXTG}	Error at 2.5V input	-7.5		11	mV	-7.5		11.0	mV
		-40°C to +105°C (Note 9)	-13.4		19.3	mV	-8		18.5	mV
FAULT DETECTION SYSTEM SPECIFICATIONS										
V2P5 Power-good Window	V_{2PH}	2.5V power-good window high threshold. V_{BAT} = 39.6V	2.62	2.7	2.766	V	2.55	2.7	2.9	V
		-40°C to +105°C (These MIN and/or MAX values are based on characterization data and are not 100% tested.)	2.616		2.77	V	2.55		2.9	V
V_{REF} Power-Good Window	V_{RPH}	V_{REF} Power-good window high threshold. V_{BAT} = 39.6V	2.525	2.7	2.9	V	2.525	2.7	2.9	V
		V_{BAT} = 39.6V; -40°C to +105°C (Note 9)	2.525		2.9	V	2.525		2.9	V
	V_{RPL}	V_{REF} Power-good window low threshold. V_{BAT} = 39.6V	2.15	2.30	2.465	V	2.15	2.30	2.46	V
		V_{BAT} = 39.6V; -40°C to +105°C (Note 9)	2.0		2.5	V	2.0		2.5	V
V_{REF} Reference Accuracy Test	V_{RACC}	V_{REF} value calculated using stored coefficients. V_{BAT} = 39.6V (See "Voltage Reference Check Calculation" on page 88.)		2.500		V	2.488	2.500	2.512	V
		~~V_{BAT} = 39.6V; -40°C (Note 9)~~					2.488		2.512	V
		~~V_{BAT} = 39.6V; +85°C (Note 9)~~					2.4849		2.5172	V
		~~V_{BAT} = 39.6V; +105°C (Note 9)~~					2.4692		2.5273	V
CELL BALANCE OUTPUT SPECIFICATIONS										
Internal Cell Balance Output Clamp	VCBCL	I_{CB} = 100µA.	8.94			V	9.0			V

Notes:

7. Compliance to datasheet limits is assured by one or more methods: production test, characterization and/or design.
8. Scan and Measurement start times are synchronised by the receiver to the falling edge of the 24th clock pulse (Daisy Chain systems) or to the falling edge of the 16th clock pulse (non-Daisy Chain, single device systems) of the Scan or *Measure* command. Clock pulses are at the SCLK pin for Master and Stand-alone devices, and at the DHi/DLo1 pins for middle and Top Daisy Chain devices. Max values are based on characterization of the internal clock and are not 100% tested.
9. These MIN and/or MAX values are based on characterization data and are not 100% tested.
10. ~~Biasing setup as in Figure 55 on page 84 or equivalent.~~
10. Stresses may be induced in the ISL78600 during soldering or other high temperature events that affect measurement accuracy. Initial accuracy does not include effects due to this. See Figure 4B for cell reading accuracy obtained after soldering to Intersil evaluation boards. When soldering the ISL78600 to a customized circuit board with a layout or construction significantly differing from the Intersil evaluation board, design verification tests should be applied to determine drift due to soldering and over lifetime.