Integrated Device Technology, Inc.
6024 Silver Creek Valley Road, San Jose, CA - 95138

PRODUCT/PROCESS CHANGE NOTICE (PCN)

PCN #: **Q1403-01** DATE: **April 9, 2014**

Product Affected: F1240NBGI
F1240NBGI8

Date Effective: **April 9, 2014**

MEANS OF DISTINGUISHING CHANGED DEVICES:

- ☐ Product Mark
- ☐ Back Mark
- ☐ Date Code
- ■ Other — Shipment after PCN Effective

Contact: IDT PCN DESK

E-mail: pcndesk@idt.com

Attachment: ■ Yes ☐ No

Samples: Contact your local sales representative for sample and datasheet requests.

DESCRIPTION AND PURPOSE OF CHANGE:

- ☐ Die Technology
- ☐ Wafer Fabrication Process
- ☐ Assembly Process
- ☐ Equipment
- ☐ Material
- ☐ Testing
- ☐ Manufacturing Site
- ■ Data Sheet
- ☐ Other

This notice is to advise our customers that Data Sheet is changed from Rev 0 to Rev 1 to clarify F1240 safe use condidtions to help customers not damage F1240 in their applications. Refer to Attachment I for details of the changes.

RELIABILITY/QUALIFICATION SUMMARY:

There is no expected change in quality or reliability.

CUSTOMER ACKNOWLEDGMENT OF RECEIPT:

IDT records indicate that you require written notification of this change. Please use the acknowledgement below or E-Mail to grant approval or request additional information. If IDT does not receive acknowledgement within 30 days of this notice it will be assumed that this change is acceptable.
IDT reserves the right to ship either version manufactured after the process change effective date.

Customer: _____ ☐ ***Approval for shipments prior to effective date.***

Name/Date: _____ E-Mail Address: _____

Title: _____ Phone# /Fax# : _____

CUSTOMER COMMENTS: _____

IDT ACKNOWLEDGMENT OF RECEIPT:

RECD. BY: _____ DATE: _____

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PRODUCT/PROCESS CHANGE NOTICE (PCN)

ATTACHMENT I - PCN # : Q1403-01

PCN Type: Data Sheet

Data Sheet Change: Yes

Details Of Change:

This notice is to advise our customers that Data Sheet is changed from Rev 0 to Rev 1 to clarify F1240 safe use condidtions to help customers not damage F1240 in their applications.

Table 1: Datasheet Changes

From:

(i) Absolute Maximum Ratings: changes marked in red box.

ABSOLUTE MAXIMUM RATINGS

V_{CC} to GND	-0.3V to +5.5V
GA[5-0], GB[5-0], DATA, CSb, CLK, V_{MODE}, $STBY_A$, $STBY_B$	-0.3V to (VCC_ + 0.25V)
OUT_A-, OUT_A+, OUT_B-, OUT_B+	-0.3V to (VCC_ + 0.25V)
IN_A-, IN_A+, IN_B-, IN_B+	-0.3V to +2.2V
ISET_A, ISET_B to GND	-0.3V to +2.2V
RF Input Power (IN_A-, IN_A+, IN_B-, IN_B+) @ G_{MAX}	+15 dBm
Continuous Power Dissipation	1.5W
θ_{JA} (Junction – Ambient)	+40°C/W
θ_{JC} (Junction – Case) The Case is defined as the exposed paddle	+3°C/W
Operating Temperature Range (Case Temperature)	T_C = -40°C to +100°C
Maximum Junction Temperature	150°C
Storage Temperature Range	-65°C to +150°C
Lead Temperature (soldering, 10s) .	+260°C

To:

ABSOLUTE MAXIMUM RATINGS

V_{CC} to GND	-0.3V to +5.5V
GA[5-0], GB[5-0], DATA, CSb, CLK, V_{MODE}, $STBY_A$, $STBY_B$	-0.6V to (VCC_ + 0.25V)
OUT_A-, OUT_A+, OUT_B-, OUT_B+	+2.5V to (VCC_ + 0.25V)
IN_A-, IN_A+, IN_B-, IN_B+	-0.3V to +2.2V
ISET_A, ISET_B current sink to GND	0 to +1.25mA
RF Input Power (IN_A-, IN_A+, IN_B-, IN_B+) @ G_{MAX}	+15 dBm
Continuous Power Dissipation	1.5W
θ_{JA} (Junction – Ambient)	+40°C/W
θ_{JC} (Junction – Case) The Case is defined as the exposed paddle	+3°C/W
Operating Temperature Range (Case Temperature)	T_C = -40°C to +100°C
Maximum Junction Temperature	150°C
Storage Temperature Range	-65°C to +150°C
Lead Temperature (soldering, 10s)	+260°C

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ATTACHMENT I - PCN # : Q1403-01

From:

(ii) Pin Descriptions: changes marked in red box.

PIN DESCRIPTIONS

Pin #	Pin Name	Pin Function
1	GA3 / DATA	4 dB ATTN ctrl bit for Channel A (Parallel Mode) OR DATA (Serial Mode)
2	GA4 / CLK	8 dB ATTN ctrl bit for Channel A(Parallel Mode) OR CLK (Serial Mode)
3	GA5	16 dB Attenuation ctrl bit for Channel A
4	VMODE	Pull low for serial mode. Float or pull high for parallel mode. Has internal Pullup
5	NC	This pin is internally grounded
6	GB5	16 dB Attenuation ctrl bit for Channel B: 1 or high = 16 dB ATTN
7	GB4	8 dB Attenuation ctrl bit for Channel B: 1 or high = 8 dB ATTN
8	GB3	4 dB Attenuation ctrl bit for Channel B: 1 or high = 4 dB ATTN
9	GB2	2 dB Attenuation ctrl bit for Channel B: 1 or high = 2 dB ATTN
10	GB1	1 dB Attenuation ctrl bit for Channel B: 1 or high = 1 dB ATTN
11	IN_B+	Channel B Differential Input +. AC couple
12	IN_B-	Channel B Differential Input -. AC couple
13	GND	Connect this pin to Ground
14	VCC	Connect this pin to the 5V DC Power Bus
15	ISET_B	ChB Icc set: Use the recommended value from the BOM section
16	GB0	0.5 dB Attenuation ctrl bit for Channel B: 1 or high = 0.5 dB ATTN
17	OUT_B+	Channel B Differential Output +. Pull up to Vcc through an inductor
18	OUT_B-	Channel B Differential Output-. Pull up to Vcc through an inductor
19	STYB_B	Pull low to Power Down ChB. Float or Pull high to enable ChB
20	GND	Connect this pin to Ground
21	GND	Connect this pin to Ground
22	STYB_A	Pull low to Power Down ChA. Float or Pull high to enable ChA
23	OUT_A-	Channel A Differential Output -. Pull up to Vcc through an inductor
24	OUT_A+	Channel A Differential Output +. Pull up to Vcc through an inductor
25	GA0	0.5 dB Attenuation ctrl bit for Channel A
26	ISET_A	ChA Icc set: Use the recommended value from the BOM section
27	VCC	Connect this pin to the 5V DC Power Bus
28	GND	Connect this pin to Ground
29	IN_A-	Channel A Differential Input -. AC couple
30	IN_A+	Channel B Differential Input +. AC couple
31	GA1	1 dB Attenuation ctrl bit for Channel A
32	GA2 / CSb	2 dB ATTN ctrl bit for Channel A (Parallel Mode) OR chip select (Serial Mode)
EP	Exposed Paddle	Connect to Ground with multiple vias for good thermal relief

To:

PIN DESCRIPTIONS

Pin #	Pin Name	Pin Function
1	GA3 / DATA	4 dB ATTN ctrl bit for Channel A (Parallel Mode) OR DATA (Serial Mode)
2	GA4 / CLK	8 dB ATTN ctrl bit for Channel A(Parallel Mode) OR CLK (Serial Mode)
3	GA5	16 dB Attenuation ctrl bit for Channel A
4	VMODE	Pull low for serial mode. Float or pull high for parallel mode. Has internal Pullup
5	NC	This pin is internally grounded
6	GB5	16 dB Attenuation ctrl bit for Channel B: 1 or high = 16 dB ATTN
7	GB4	8 dB Attenuation ctrl bit for Channel B: 1 or high = 8 dB ATTN
8	GB3	4 dB Attenuation ctrl bit for Channel B: 1 or high = 4 dB ATTN
9	GB2	2 dB Attenuation ctrl bit for Channel B: 1 or high = 2 dB ATTN
10	GB1	1 dB Attenuation ctrl bit for Channel B: 1 or high = 1 dB ATTN
11	IN_B+	Channel B Differential Input +. AC couple
12	IN_B-	Channel B Differential Input -. AC couple
13	GND	Connect this pin to Ground
14	VCC	Connect this pin to the 5V DC Power Bus. Bypass capacitor is required.
15	ISET_B	ChB Icc set: Use the recommended value from the BOM section
16	GB0	0.5 dB Attenuation ctrl bit for Channel B: 1 or high = 0.5 dB ATTN
17	OUT_B+	Channel B Differential Output +. Pull up to Vcc through an inductor
18	OUT_B-	Channel B Differential Output-. Pull up to Vcc through an inductor
19	STBY_B	Pull low to Power Down ChB. Float or Pull high to enable ChB
20	GND	Connect this pin to Ground
21	GND	Connect this pin to Ground
22	STBY_A	Pull low to Power Down ChA. Float or Pull high to enable ChA
23	OUT_A-	Channel A Differential Output -. Pull up to Vcc through an inductor
24	OUT_A+	Channel A Differential Output +. Pull up to Vcc through an inductor
25	GA0	0.5 dB Attenuation ctrl bit for Channel A
26	ISET_A	ChA Icc set: Use the recommended value from the BOM section
27	VCC	Connect this pin to the 5V DC Power Bus. Bypass capacitor is required.
28	GND	Connect this pin to Ground
29	IN_A-	Channel A Differential Input -. AC couple
30	IN_A+	Channel B Differential Input +. AC couple
31	GA1	1 dB Attenuation ctrl bit for Channel A
32	GA2 / CSb	2 dB ATTN ctrl bit for Channel A (Parallel Mode) OR chip select (Serial Mode)
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(iii) Applications Information: Added section "Power Supplies" and "Control Pin Interface".

APPLICATIONS INFORMATION

The F1240 has been optimized for use in high performance IF sub-sampling applications. They have unique features that make them ideal for these very demanding applications.

Power Supplies

A common VCC power supply should be used for all pins requiring DC power. All supply pins should be bypassed with external capacitors to minimize noise and fast transients. Supply noise can degrade noise figure and fast transients can trigger ESD clamps and cause them to fail. Supply voltage change or transients should have a slew rate smaller than 1V/20uS. In addition, all control pins should remain at 0V (+/-0.3V) while the supply voltage ramps or while it returns to zero.

Control Pin Interface

If control signal integrity is a concern and clean signals cannot be guaranteed due to overshoot, undershoot, ringing, etc., the following circuit at the input of each control pin is recommended. This applies to control pins 1, 2, 3, 4, 6, 7, 8, 9, 10, 16, 19, 22, 25, 31, and 32 as shown below.