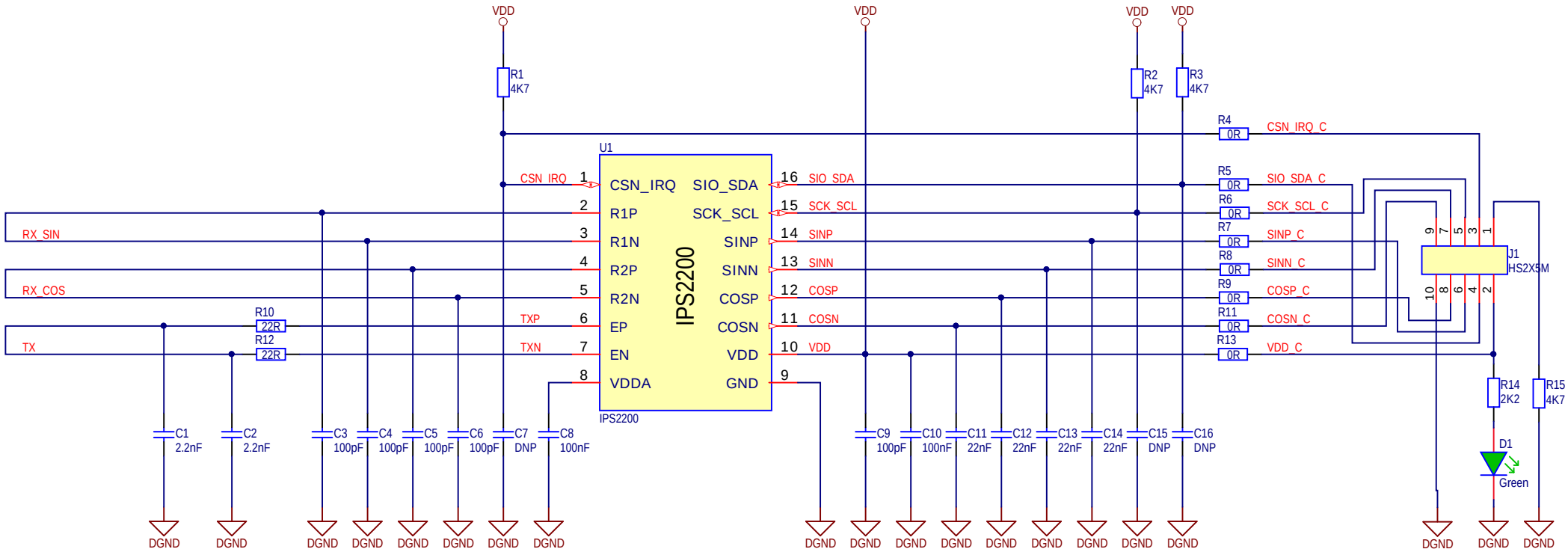
IPS2200MROT09004

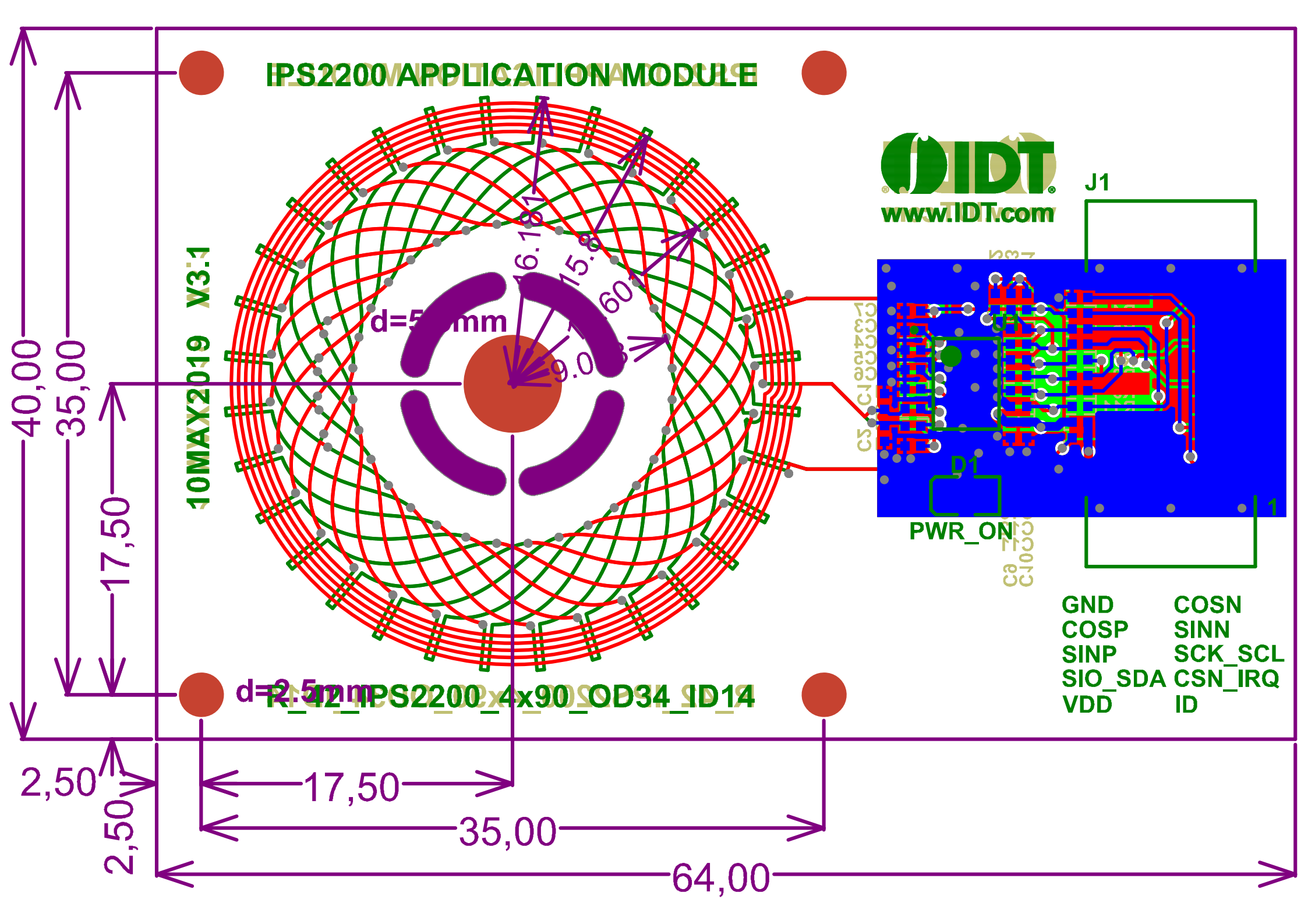
Date:	10MAY2019
Project:	IPS2200MROT09004
Version	3.1
Content:	Schematic
	Coil PCB Layout
	Coil PCB 3D Model
	Bill of Materials
	PCB Manifacture Requirements
	Coil Layer Stack
	Target PCB Layout
	Target PCB 3D Model



DNP = EMC placeholder, populate if needed

0R = EMC placeholder, adjust if needed

Title: IPS2200MROT9004			IDT www.IDT.com
Project: IPS2200MROT09004.PrjPCB			
Size: A4	Sheet: 1 of 1	Drawn by: B.Gombor	Version: 3.1
File: IPS2200MROT09004.SCHDOC			Date: 27.05.2019

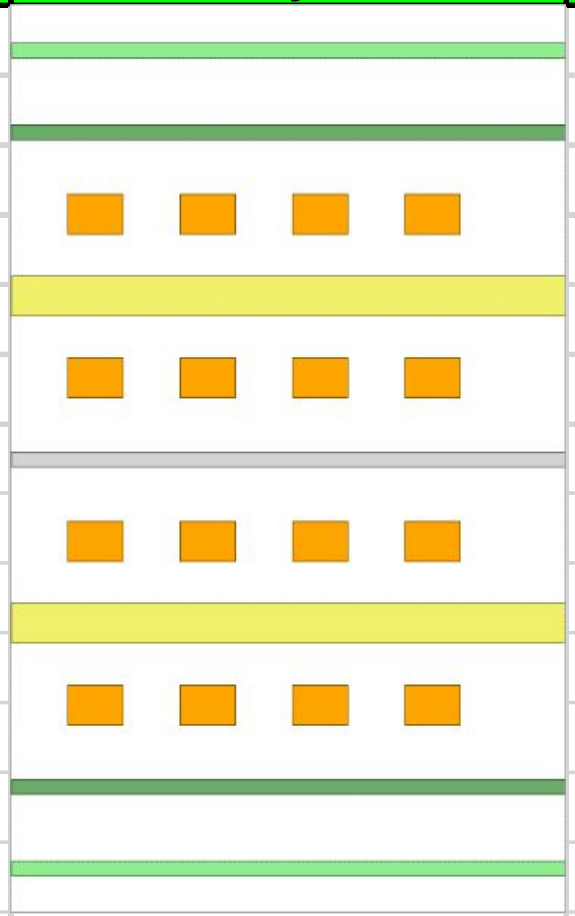

IPS2200 APPLICATION MODULE
10MAY2019 V3.1
www.IDT.com
J1
PWR_ON
D1
GND
COSP
SINP
SIO_SDA
VDD
COSN
SINN
SCK_SCL
CSN_IRQ
ID
d=5,0mm
d=2,5mm
R_42_IPS2200_4x90_OD34_ID14
40,00
35,00
17,50
2,50
2,50
17,50
35,00
64,00

Designator	Footprint	Value	Quantity
C1, C2	C0402 3D	2.2nF	2
C3, C4, C5, C6, C9	C0402 3D	100pF	5
C7, C15, C16	C0402 3D	DNP	3
C8, C10	C0402 3D	100nF	2
C11, C12, C13, C14	C0402 3D	22nF	4
D1	LED0805 G 3D	Green	1
J1	T821M110A1S100CEU-B	HS2X5M	1
R1, R2, R3, R15	R0402 3D	4K7	4
R4, R5, R6, R7, R8, R9, R11, R13	R0402 3D	0R	8
R10, R12	R0402 3D	22R	2
R14	R0402 3D	2K2	1
U1	TSSOP16_NVT02006	IPS2200	1

Manufacturing requirements

Name	IPS2200MROT09004_GERBER
Number of layers	4
Base material	FR-4
Thickness	1.0 mm +/- 10%
Thickness of copper coating	35 µm
Final cover	ENIG
Minimal copper width	0.2 mm
Minimal copper to copper distance	0.15 mm
Via hole/pad diameter	0.2/0.5 mm
Slotted holes	no
Panel dimensions	64 x 40 mm
Silk screen color	white on both sides
Solder mask color	green

Board Stack Report

Stack Up		Layer Stack			
Layer	Board Layer Stack	Name	Material	Thickness	Constant
1		Top Paste			
2		Top Overlay			
3		Top Solder	Solder Resist	0,030mm	3,5
4		Top Layer	Copper	0,035mm	
5		Dielectric 1	FR-4	0,200mm	4,2
6		Inner Layer 1	Copper	0,035mm	
7		Dielectric 3		0,400mm	4,2
8		InnerLayer 2	Copper	0,035mm	
9		Dielectric 2		0,200mm	4,2
10		Bottom Layer	Copper	0,035mm	
11		Bottom Solder	Solder Resist	0,030mm	3,5
12		Bottom Overlay			
13		Bottom Paste			
	Height : 1,000mm				

17.5
18
6.5
5,50
18JAN2019
V1.0
IPSC200 TARGET