IDT®
PEB383™
QFN
Board Design Guidelines

60E2080_AN001_02

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Contents

About this Document

This section discusses the following topics:

Scope

The *PEB383 QFN Board Design Guidelines* provides hardware reference information for the PEB383 QFN, such as layout guidelines and schematic review information. It is intended for hardware designers who are designing system interconnect applications with the PEB383 QFN.

The PEB383 is available in two package variants: QFP and QFN. While both variants have identical functionalities, they are of different physical packages and therefore require different attentions for board layouts. This document intends to be used for the QFN package. For designs that use the QFP variant, refer to the "*IDT PEB383 QFP Board Design Guidelines*".

For the remaining of this document, "PEB383 QFN" will be simply called "PEB383".

Document Conventions

This document uses the following conventions.

Non-differential Signal Notation

Non-differential signals are either active-low or active-high. An active-low signal has an active state of logic 0 (or the lower voltage level), and is denoted by a lowercase "n". An active-high signal has an active state of logic 1 (or the higher voltage level), and is not denoted by a special character. The following table illustrates the non-differential signal naming convention.

State	Single-line signal	Multi-line signal
Active low	NAMEn	NAMEn[3]
Active high	NAME	NAME[3]

Differential Signal Notation

Differential signals consist of pairs of complement positive and negative signals that are measured at the same time to determine a signal's active or inactive state (they are denoted by "_p" and "_n", respectively). The following table illustrates the differential signal naming convention.

State	Single-line signal	Multi-line signal
Inactive	NAME_p = 0 NAME_n = 1	NAME_p[3] = 0 NAME_n[3] =1
Active	NAME_p = 1 NAME_n = 0	NAME_p[3] is 1 NAME_n[3] is 0

Numeric Notation

- Hexadecimal numbers are denoted by the prefix *0x* (for example, 0x04).
- Binary numbers are denoted by the prefix *0b* (for example, 0b010).

Dimensions in this document are given in British imperial units. Use this conversion ratio for Metric units:

- 1 inch = 25.4 mm
- 1 mil = 0.0254 mm

Symbols

This symbol indicates a basic design concept or information considered helpful.

This symbol indicates important configuration information or suggestions.

This symbol indicates procedures or operating levels that may result in misuse or damage to the device.

Revision History

60E2080_AN001_01, Formal, April 2010

.Corrected nominal power supply voltages for VDD_PCIE and VDDA_PLL to 1.05V.

60E2080_AN001_01, Formal, April 2010

This is the first version of the *PEB383 QFN Board Design Guidelines*.

1. Designing a PCB for PCIe Signals

Topics discussed include the following:

1.1 PCIe Signals

The following table lists the PEB383's PCIe signals that are subject to the layout guidelines.

Table 1: PEB383 PCIe Signals

Signal Name	Pin Number
PCIE_TXD_p	A69
PCIE_TXD_n	B59
PCIE_RXD_p	A68
PCIE_RXD_n	B57
PCIE_REFCLK_P	B55
PCIE_REFCLK_n	A66

1.2 Transmission Line Terms

- Microstrips – Traces that are adjacent to a continuous reference plane. In a PCB stackup, the micro strips are on the primary and secondary layers.
- Striplines – Traces routed in inner layers and have two reference planes. In a PCB stack-up, str iplines are on internal layers.

1.3 Trace Geometry

The PCIe protocol uses differential pair routing, which requires greater care to meet the impedance tar gets on these signals versus other single-ended interfaces. Variations in the impedance of these signals will impact the overall jitter and loss within the system.

The main areas of concern for board trace routing of PCIe data and clock signals include:

- Spacing within the differential pair
- Coupling to an adjacent reference plane
- Thickness of the traces within the pair

Close coupling or relatively close physical spacing within the differential pairs, along with increased spacing to unrelated differential pairs and other signals, help to minimize crosstalk and EMI effects.

The width and spacing guidelines of the PCIe differential signals determines the impedance of the trace s and helps to insure that interconnect loss and jitter budgets are met. Signal integrity within the system is also impacted by whether or not appropriate spacing exists between differential pairs and adjacent tr aces.

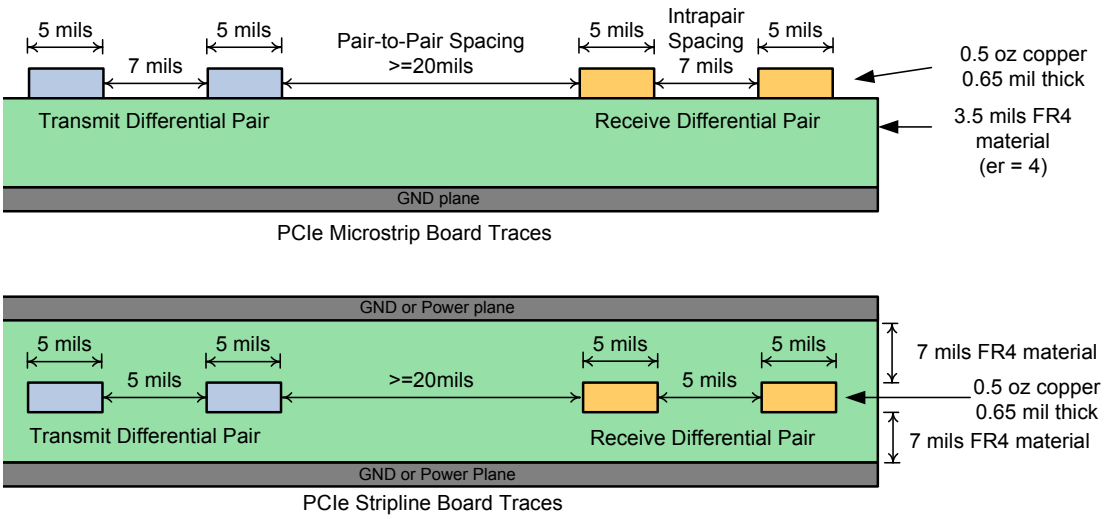
Edge-coupled microstrip traces of each differential pair within the PCIe Interface should have a differe ntial impedance of 100 Ohms. When using common PCB material, the target impedance can be achie ved with trace widths of 5-mils with a 7-mil space within the pair. This 5/7/5 routing method provides t he best compromise between impedance targets, loss impacts, crosstalk immunity, and routing flexibilit y. If stripline traces are used, they should maintain a 5/5/5 routing geometry with 5-mil trace widths co mbined with a 5-mil spacing within the pair.

A 20-mil edge-to-edge spacing should be used between traces of adjacent differential pairs in order to minimize negative crosstalk effects. A 20-mil spacing should also be maintained between differential pairs and non-PCIe signals. If unrelated signals have significantly higher voltage levels or edge rates when compared to PCIe, then a minimum 30-mil spacing should be used to avoid coupling issues.

Figure 1 displays an example of the width and spacing recommendations for PCIe differential pairs.

If board constraints require routing sections of a differential pair uncoupled where the intrapair spacing exceeds the 7-mil requirement, then the width of the uncoupled section of trace can be increased to 7-mils, as displayed in the figure. This applies to uncoupled sections that exceed 100 mils in distance. Using a 7-mil trace versus 5-mils within the uncoupled sections helps to maintain the correct different ial impedance across the uncoupled region.

Figure 1: PCIe Board Trace Width and Spacings Example



Note: PCB parameter examples are approximate. Use PCB parameters as provided by your PCB manufacturer.

1.4 Trace Length Matching

PCIe signals have constraints with respect to trace lengths and matching in order to meet jitter and loss budgets within a system. Each inch of board trace within a differential pair can add 1ps of jitter and up to 0.35dB of loss. Typically, the PCIe specification can be met with a chip-to-chip routing length up to 15 inches. When routing differential pairs connecting the finger connector pad to a PEB383 pin on an a dd-in card, traces can be routed up to 3.5 inches.

Pair-to-pair length matching within the PCIe Interface is normally not required due to the large skew a llowed at the receiver; however, it should be minimized in order to reduce the overall latency of the system. Intrapair skew is much more important and requires that the length of the traces within a differ ential pair be matched to within 5-mils of one another. Length matching within a differential pair shou ld be performed on a segment-by-segment basis rather than only as an overall measurement.

1.5 Reference Planes

High quality reference planes within the PCIe Interface improve signal integrity, reduce EMI effects, a nd minimize AC common-mode noise within the differential pairs. It is recommended that the different ial signal pairs reference the main ground plane within the PCB stackup, and reference only a single pla ne along the entire routing path. Differential traces should not be routed across or near any discontinuit ies in the reference plane. A 20-mil spacing should be maintained when routing near and parallel to the edge of a reference plane.

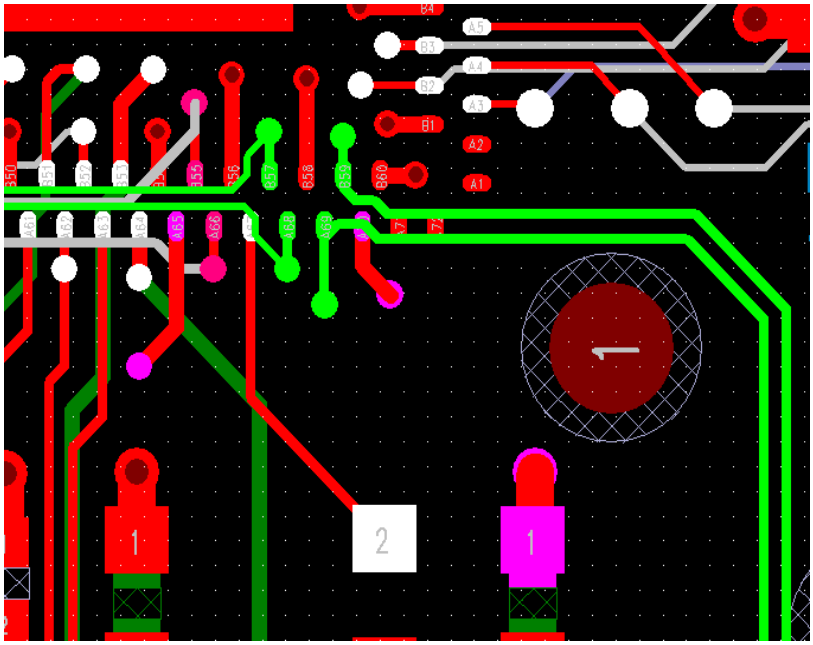
1.6 Bends in PCIe Differential Pairs

Bends or turns within the PCIe differential pairs should be kept to a minimum. The angles between tra ces should be greater than or equal to 135 degrees, and there should never be any 90 degree turns or be nds along a trace. The inner spacing within a bend of a differential pair should equal or exceed the minimum pair-to-pair spacing of 20-mils in order to minimize the introduction of common-mode noise within the system (see Figure 1). Segments within a bend should have a length equal to or greater than 1.5x the width of the trace, and if possible the number of left- and right-hand bends should be matched as closely as possible to minimize length skew differences within a differential pair.

1.7 Device Breakout Area

Within the breakout areas of the PEB383, the PCIe signal pairs should maximize the differential rout ing while minimizing any discontinuities or trace length skew (see Figure 2). Length matching of the differential traces should occur as close as possible to the pad or pin while avoiding the addition of “t ight” bends within the traces. The breakout areas should not exceed 250-mils in length for the PCIe Int erface. Within the breakout areas, the trace routing guidelines of the differential pairs can be slightly re laxed — if absolutely necessary — to facilitate successful breakout of the signals. A width and spacing geometry of 5/5/5 can be used with a minimum spacing to other signals of 7-mils.

Figure 2: PEB383 PCIe Differential Trace Breakout (green)

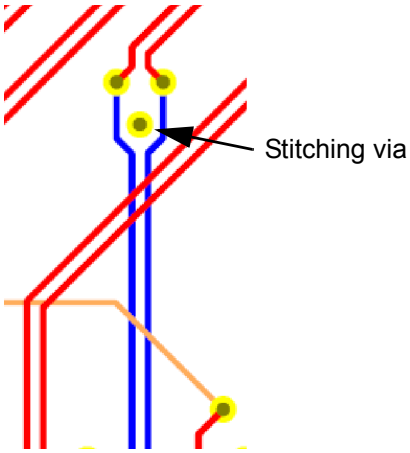


1.8 Vias in Differential Traces

Use of vias within the differential traces of the PCIe signals can have an adverse effect on system perfo rmance. If vias must be used, they should have a pad size of less than 25-mils with a finished hole size of less than 14-mils. Vias should always be placed in pairs at the same relative location and should be symmetrical between the differential traces. A maximum of four via pairs can be used within each tra nsmit differential pair of the PCIe link. Each receive differential pair can have a maximum of two vias along its path. A maximum of six via pairs are allowed along the entire PCIe interconnect path.

When traces change layers in a PCB, the reference plane for the differential traces also changes. It is re commended to introduce a stitching via close to the differential trace vias (see Figure 3). The stitching via connects all the ground planes together, and allows return current to flow easily from one ground plane to another.

Figure 3: Differential Pair Vias and Stitching Via



1.9 Routing Guidelines Summary

The routing guidelines should be used for board routing of the transmit and receive data. The guideline s are summarized in Table 2.

Table 2: PCIe Interface Routing Guidelines

Parameter	Main Route System Board	Special Breakout Area
Differential Impedance Target	100 ohms ±15 %	
Single-ended Impedance Target	60 ohms ±15 %	
Trace Width	5 mils	7 mils if uncoupled length ≥ 100 mils
Differential Pair (within pair) Spa cing	7 mils Microstrips 5 mils Striplines	5-mil spacing is acceptable
Pair-to-Pair Spacing	≥ 20 mils	7-mil spacing is acceptable

Table 2: PCIe Interface Routing Guidelines *(Continued)*

Parameter	Main Route System Board	Special Breakout Area
Trace Length Restrictions	≤ 15 ” chip-to-chip ≤ 3.5 ” chip-to-add-in card edge Connectors	Breakout is limited to ≤ 250 mils (included in overall trace length re commendations for main routes)
Length Matching within Pair	5 mils	
Length Matching Pair-to-Pair	Keep moderate for latency. 1.25ns maximum lane-to-lane skew.	
Reference Plane	GND plane recommended. Use st itching vias when changing layers. If a power plane is used as a refer ence plane, place decoupling capa citors close to the vias where the tr aces change layers.	GND islands on PWR layer are a cceptable as long as the connectio n to the main ground planes is loca l.
Splits/Voids	No routing over splits or voids.	No more than half the trace width should be over via anti-pad.
Via Usage (maximum) (6 total, entire path)	Four vias per Tx trace. Two vias per Rx trace.	Acceptable to include one via in br eakout area.
Bends	Match left and right turn bends where possible. No 90-degree or “t ight” bends.	Avoid “tight” bends when routing in breakout area.

1.10 PCIe Tx Capacitors

The PCIe specification requires that each lane of the link be AC coupled between its corresponding tra nsmitter and receiver. The AC coupling capacitors for the PEB383 are discrete components located alo ng each transmitter link on the PCB. These AC coupling capacitors allow the transmitter and receiver o n a link to be biased at separate voltages. Table 3 summarizes the guidelines for implementing the PCIe AC coupling capacitors on a system board. Recommended capacitor layout and placement are provide d in Figures 4 and 5.

Table 3: PCIe Interface AC Coupling Capacitor Guidelines

Parameter	Implementation Guideline
AC Coupling	AC coupling capacitors are required on the Tx pairs originating from the PEB383.
Capacitor Value	75nF ≤ $C_{AC\text{-}COUPLING}$ ≤ 200nF
Capacitor Tolerance	Specified minimum/maximum range must be met when capacitor tolera nce is considered along with effects due to temperature and voltage.

Table 3: PCIe Interface AC Coupling Capacitor Guidelines *(Continued)*

Parameter	Implementation Guideline
Capacitor Type	Size 603 ceramic capacitors are acceptable; however, size 402 capacitors are strongly encouraged. The smaller the package size, the less ESL is introduced into the topology. The same package and capacitor size should be used for each signal in a differential pair. Do not use capacitor packs for PCIe AC coupling.
Capacitor Pad Size	To minimize parasitic impacts, pad sizes for each capacitor should be the minimum allowed per PCB manufacturer.
Capacitor Placement	AC coupling capacitors should be located at the same place within the differential pair. They should not be staggered in distance from one trace of the differential pair to the other. Capacitors should be placed as close to each other as possible to avoid creating large uncoupled sections within the differential pair traces. Relative location from one differential pair to another is not important.
Capacitor Location – Chip-to-Connector Routing	Capacitors should be placed such that they are not located in the center point of a trace route (for example, capacitors should be placed next to the connector or 1/3 the distance between the connector and the PEB383).
Capacitor Location – Chip-to-Chip Routing	Capacitors should be located off-center within the interconnect (for example, placing the capacitors next to the Rx pins of one device is generally better than locating the capacitors in the midpoint of the interconnect).

Figure 4: PCIe AC Coupling Capacitor Symmetric Layout

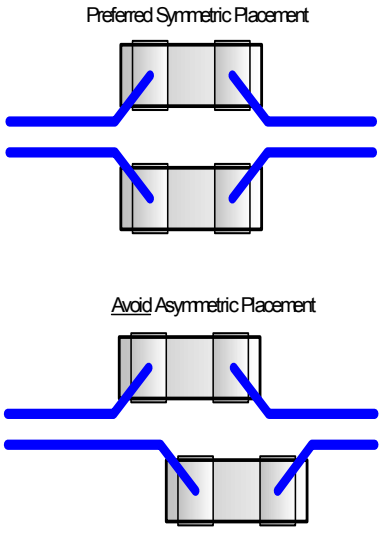
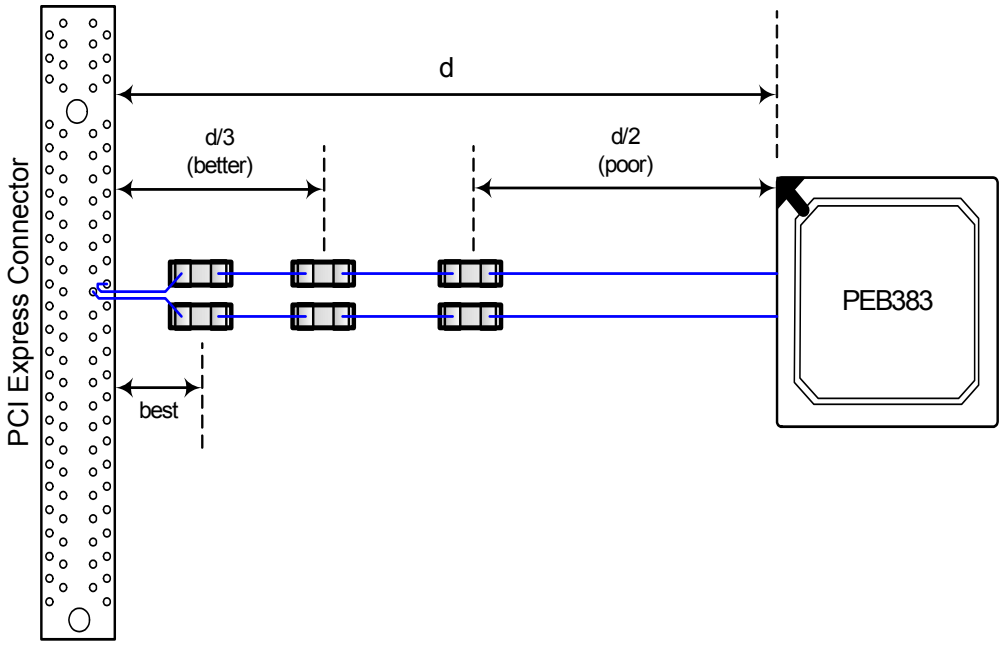


Figure 5: PCIe AC Coupling Capacitor Recommended Board Placement



1.11 PCIe_REFCLK

The PEB383 must receive a 100-MHz differential reference clock on its PCIE_REFCLK_p/n input pins. This clock can be generated from an on-board oscillator if a PCIe system clock is not available. The clock generator should provide an HCSL output-level clock that meets the PCIE_REFCLK duty cycle and jitter requirement, as specified in the *PEB383 User Manual*. Figure 6 shows a simplified schematic of an HCSL PCIE_REFCLK circuit. The HCSL source termination is specified by the HCSL clock device vendor.

Figure 6: Simplified PCIE_REFCLK Circuit

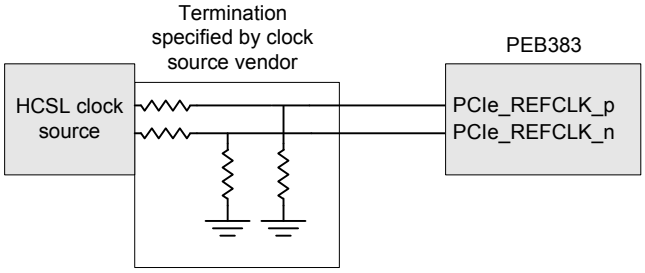


Table 4: PCIE_REFCLK Layout Guidelines

Parameter	Implementation Guidelines
PCIE_REFCLK Differential Trace Impedance	100 Ohms
PCIE_REFCLK Length Restriction for Add-in Card	From finger connector to PEB383 (or any other device): 4 inches
Length Matching within Pair	≤ 10 mils

1.12 Polarity Reversal

Lane polarity reversal support is required as per the *PCI Express Specification*. This feature can be use d to ease routing of differential pairs of the express link to and from the PEB383. As such, the follo wing are recommended:

- To connect the _p to the _n of a differential pair instead of crossing the _p and _n traces through an extra PCB layer
- To connect the _p to the _n of a differential pair instead of un-crossing traces around vias or throu gh-holes in a break-out are

2. Power Supply Filtering and Decoupling

Topics discussed include the following:

- "Analog Power Supply Filtering"
- "Decoupling Capacitors"

2.1 Analog Power Supply Filtering

2.1.1 VDDA_PCIE

The VDDA_PCIE power pin is noise sensitive. Noise on this pin may translate into unwanted jitter on the serial bit streams. The VDDA_PCIE pin should be connected to a filtered 3.3V supply (for an exa mple filter circuit, see Figure 7).

Based on the circuit in the figure, the VDDA_PCIE net can be implemented as a local plane located under the QFP (see Figure 8). Ideally, the 0.1uF capacitor is located under the QFP within the breakout vias. If this is not possible, the capacitor should be very close to the edge of the package. The net from the ferrite bead to the VDDA_PCIE pins can be implemented as a trace from the ferrite bead to the VDDA_PCIE pin breakout via, as long as the decoupling capacitor is located under the QFP and connected to the breakout via with short traces.

Figure 7: Supply Filter Circuit for VDDA_PCIE

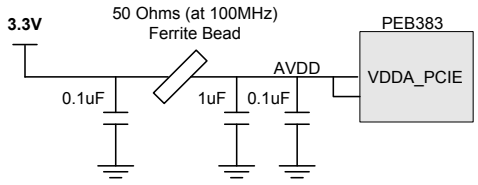
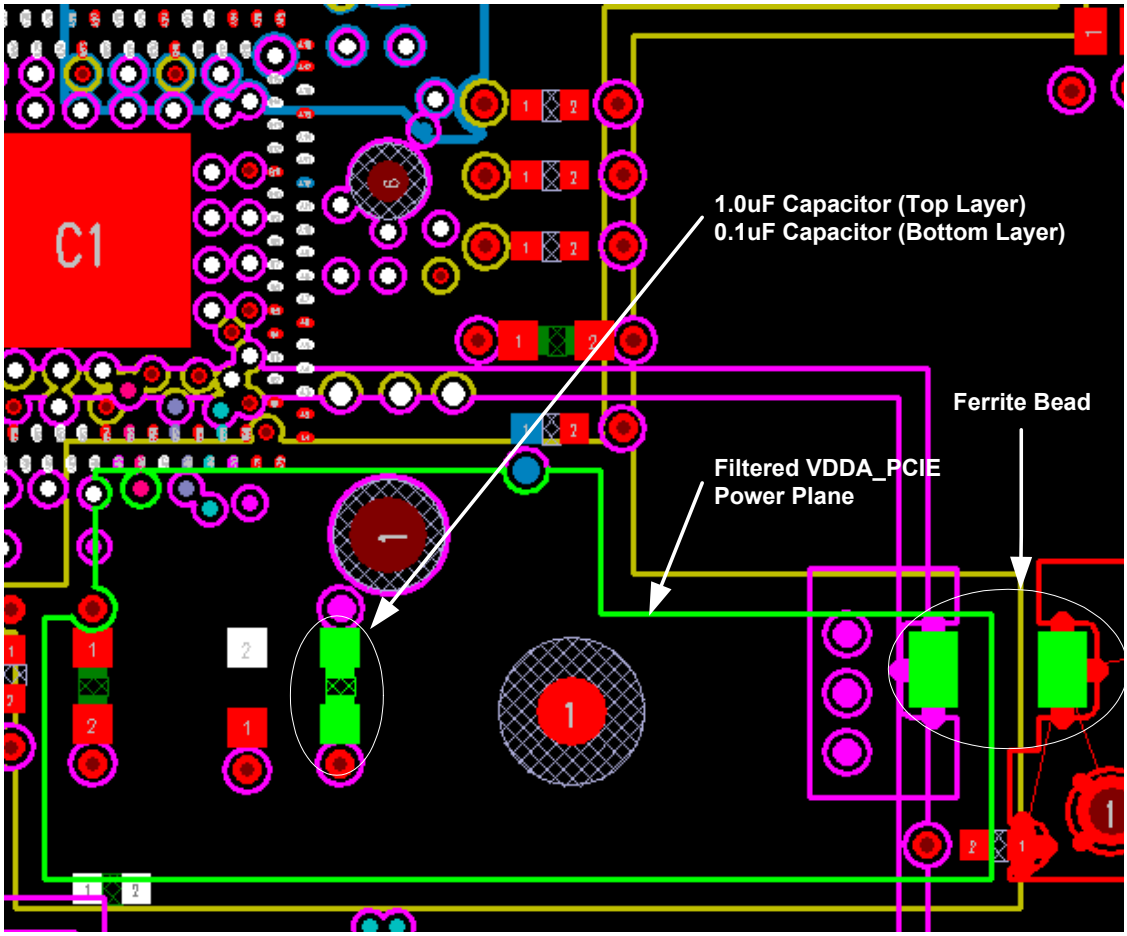


Figure 8: 1.05V VDDA_PCIE Filter Layout Example



2.1.2 VDD_PCIE

VDD_PCIE pins supply 1.05V to the SerDes circuit internal to the PEB383. The noise restriction on VDD_PCIE is 50mV peak-to-peak. A filter circuit, as displayed in Figure 9, can be used to reduce the noise from the main 1.05V supply. Ideally, the 0.1uF capacitors are located under the QFP within the breakout vias. If this is not possible, the capacitors should be very close to the edge of the package. Pref erably, the VDD_PCIE net is implemented as a local power plane under the QFP. Figure 10 shows the VDD_PCIE net implemented with a local power plane.

Figure 9: Supply Filter Circuit for VDD_PCIE

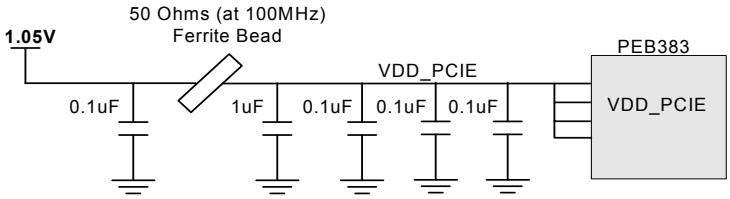
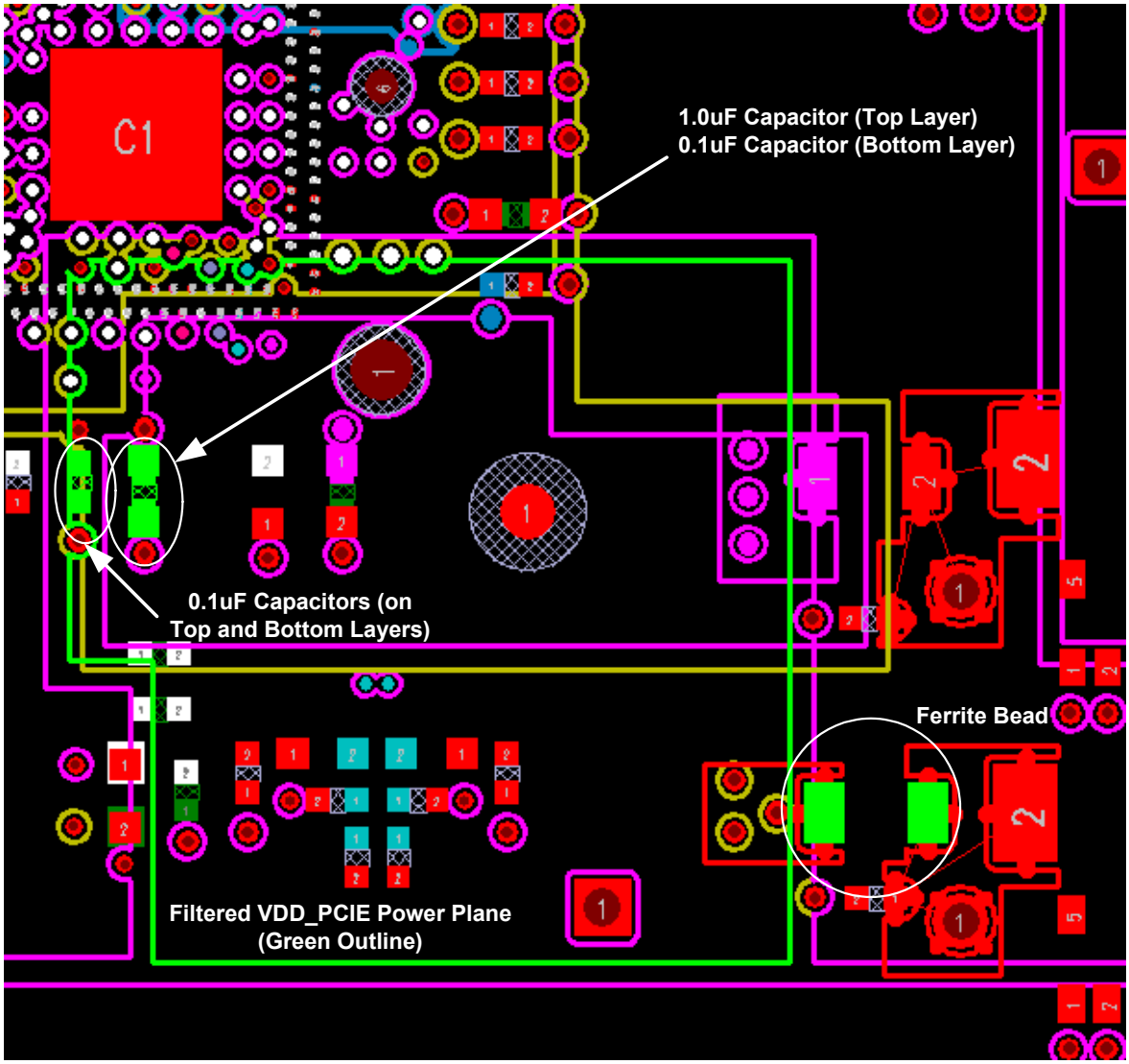


Figure 10: VDD_PCIE Filter Layout Example



2.1.3 VDDA_PLL

The VDDA_PLL supply pin provides power to the internal clock PLL circuit inside the PEB383. Use a filter circuit similar to the one in Figure 11. Place the 0.1uF and 0.01uF capacitors in the via breakout under the QFP.

Figure 11: Supply Filter Circuit for VDDA_PLL

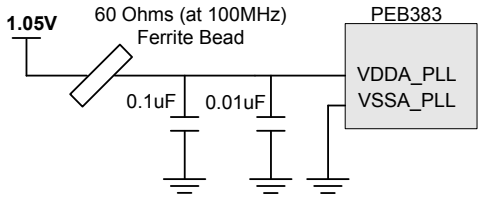
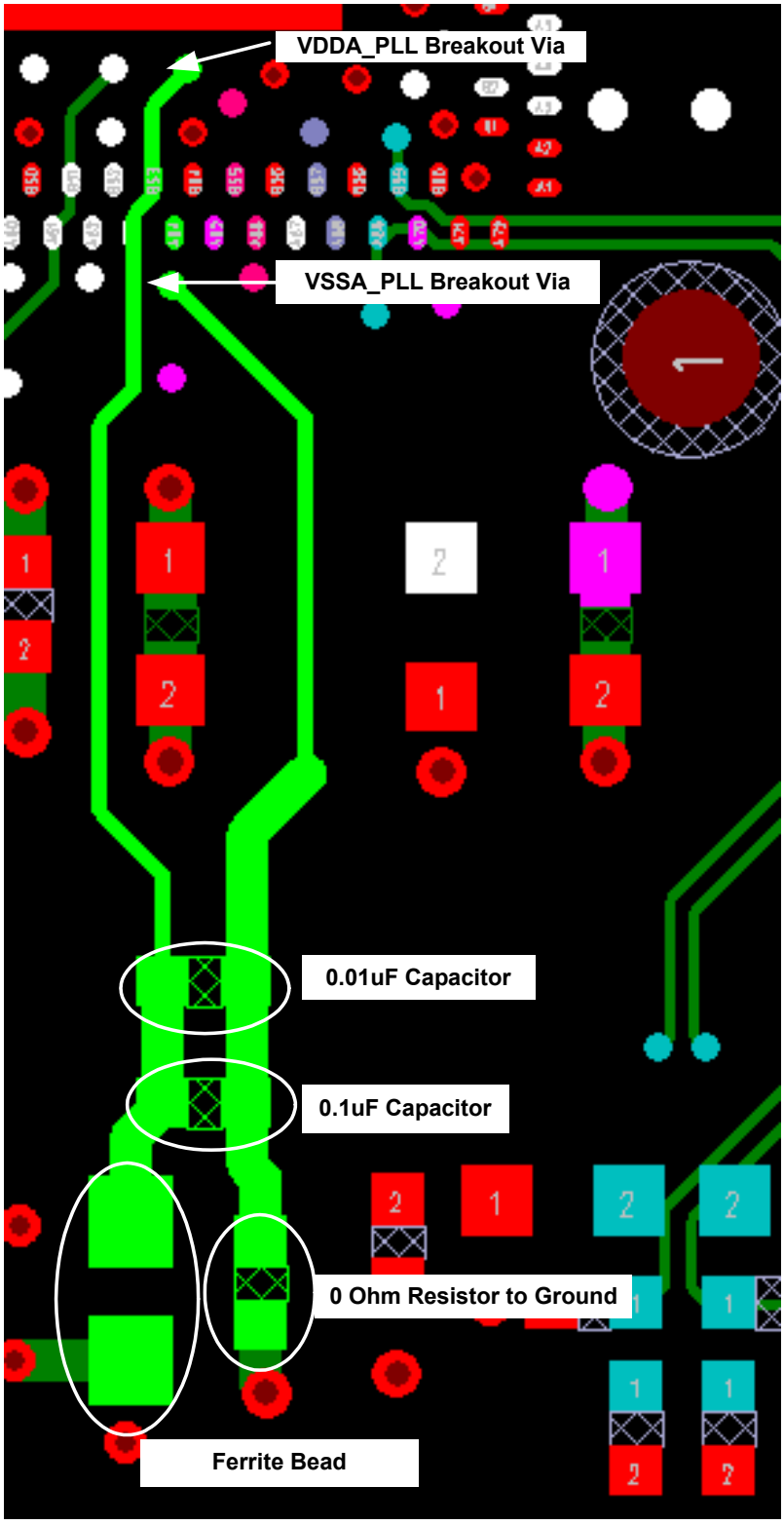


Figure 12: VDDA_PLL Filter Layout Example



2.2 Decoupling Capacitors

The PEB383 decoupling recommendation is provided in Table 5. Other components, including PCI connectors, must also be adequately decoupled.

Table 5: Decoupling Capacitor Recommendations

Rail	Capacitor value	Quantity	Placement	Description
VDD	0.1uF	6	Ideally several are placed within the QFP breakout. Others are pla ced close to the QFP.	Ceramic (X5R or X7R) Surface mount Case size 0402 or 0603
VDD	1uF	1	Close to PEB383	
VDD_PCI	0.1uF	7	Close to PEB383	
VDD_PCI	1uF	7	Close to PEB383	
VIO_PCI	0.1uF	3	Close to PEB383	

The layout example in Figure 13, Figure 14 and Figure 15show one method for inserting decoupling ca pacitors within the QFP breakout.

Figure 13: Top View of Bottom Layer, Decoupling Capacitors for VDD

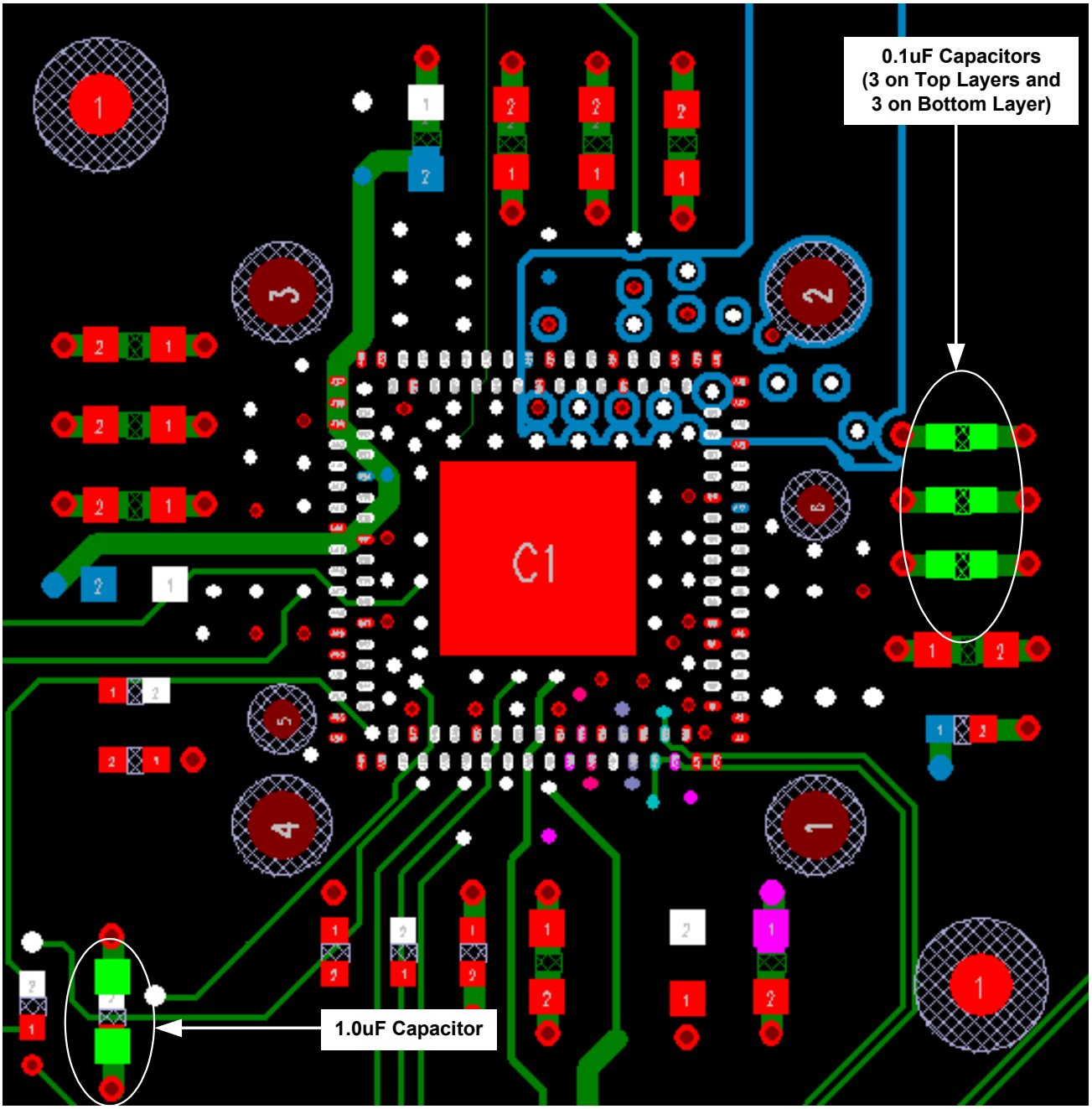
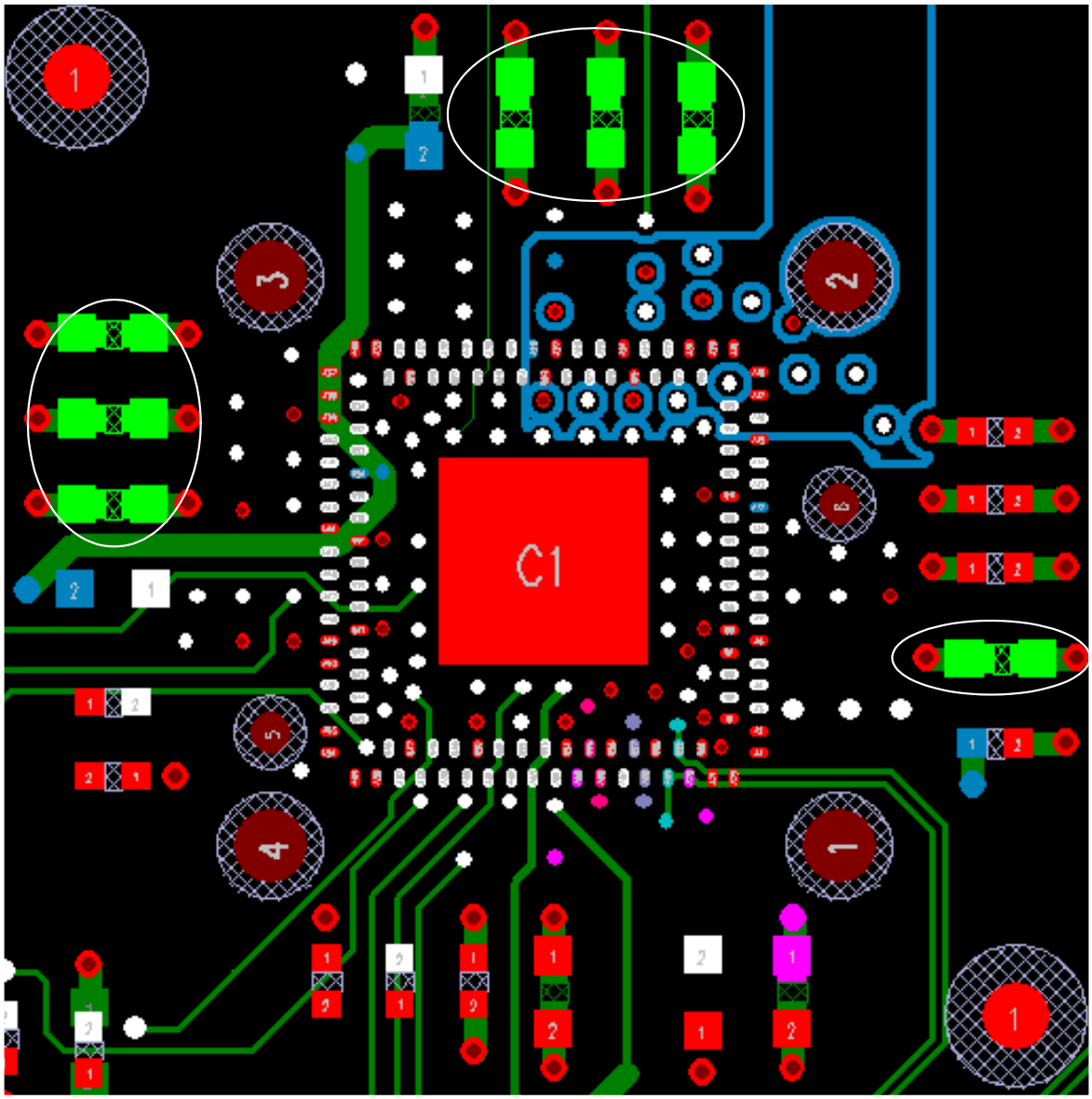
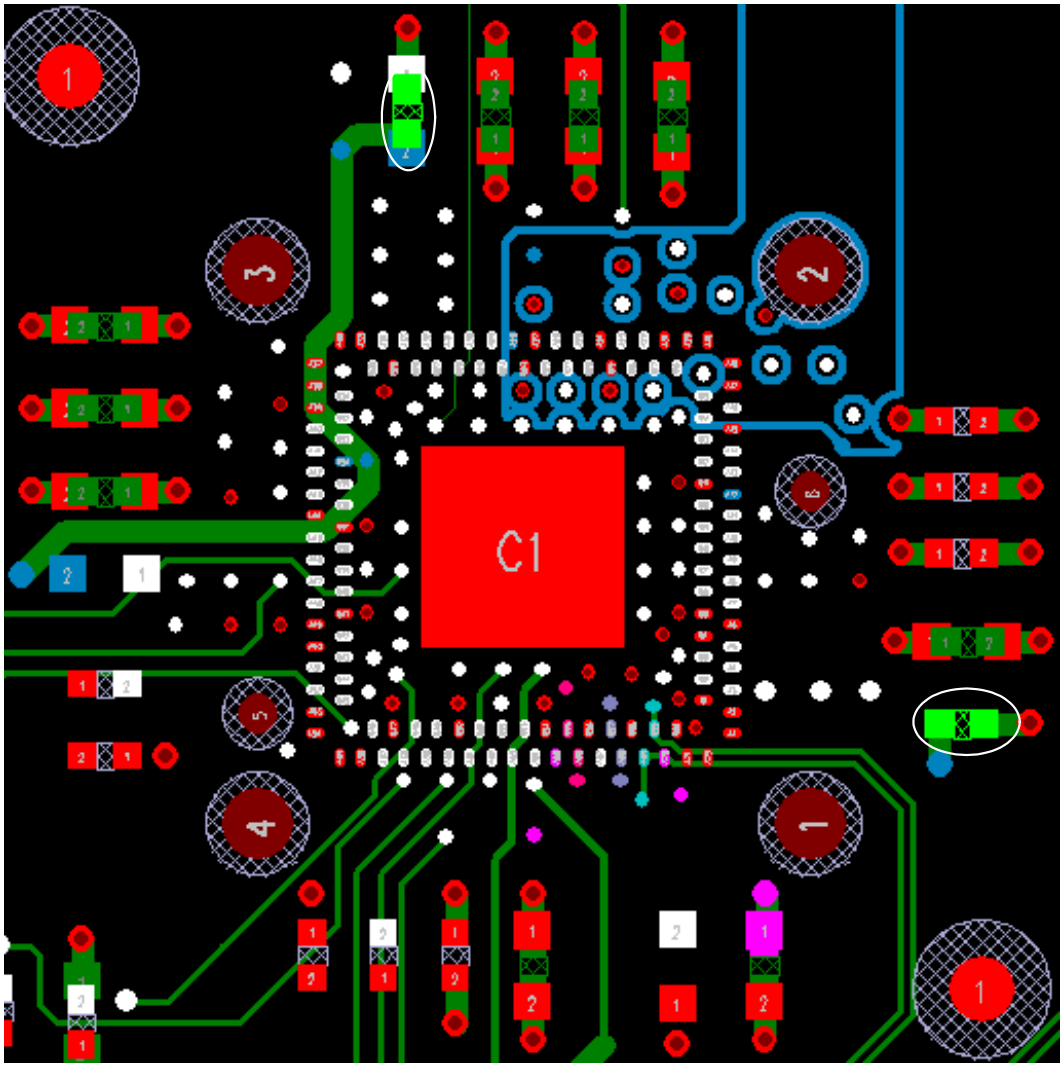


Figure 14: Top View of Bottom Layer, Decoupling Capacitors for VDD_PCI



GREEN : VDD_PCI Decoupling Capacitors (some are located at the bottom layer)

Figure 15: Top View of Bottom Layer, Decoupling Capacitors VIO_PCI



GREEN : VIO_PCI Decoupling Capacitors (some are located at the bottom layer)

3. PCI Bus Design Notes

Topics discussed include the following:

- "PCI Clocking Modes"
- "Bus Routing Rules"

3.1 PCI Clocking Modes

The PEB383 supports two clocking modes: Master and Slave. These clocking modes are discussed in the following sections.

3.1.1 PCI Slave Mode Clocking

Slave mode clocking requires an external PCI clock source (see Figure 16). The clock source must connect to the PEB383 PCI_CLK, as well as to all other PCI devices on the same bus. Clock signal trace lengths should all be matched.

Figure 16: Slave Mode Clocking

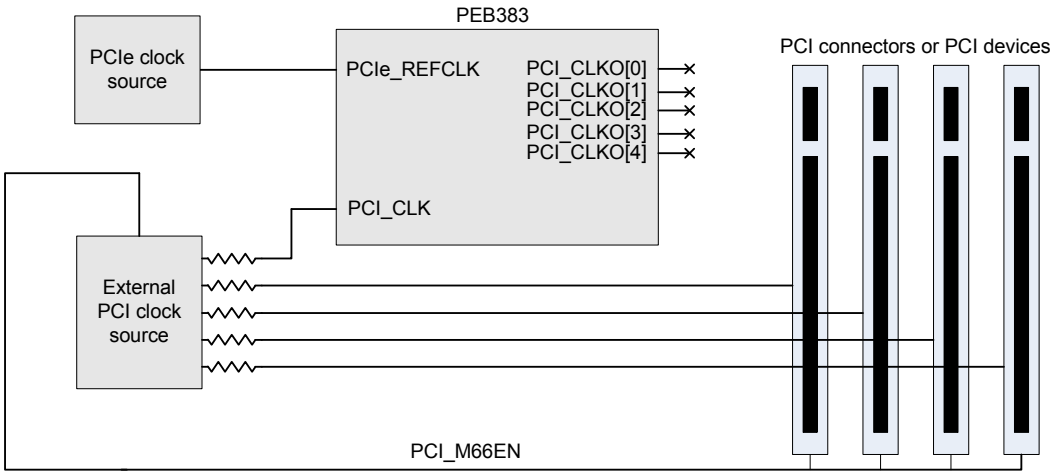


Table 6: Slave Mode Setup

Signal	Setting
PWRUP_PLL_BYPASS	Don't care
PCI_M66EN	Don't care

3.1.2 PCI Master Mode Clocking

Master mode clocking uses the PCIe input clock to generate the PCI clock outputs (see Figure 17). PCI_CLKO[4] should be connected to PCI_CLK for PCB trace and internal delay compensation. In master mode, it is important to set PCI_M66EN at the appropriate level because this signal is used to set the output clock frequency.

Figure 17: Master Mode Clocking – PCI Clock for All Frequencies

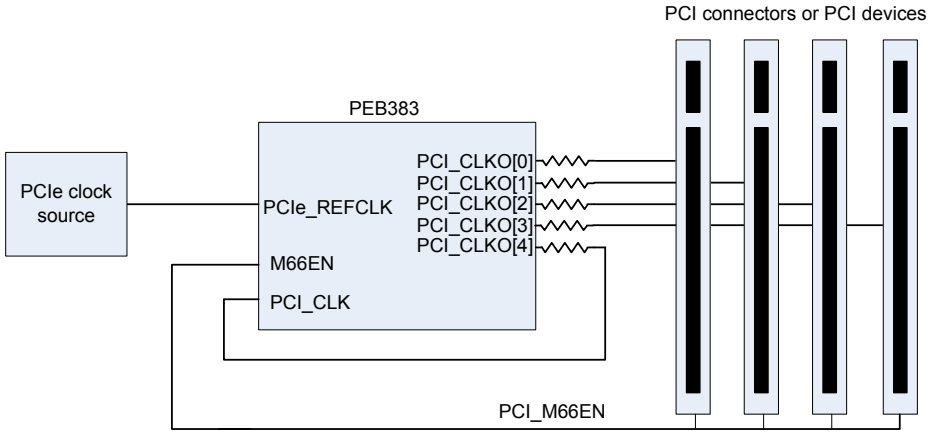


Table 7: Master Mode Setup

Signal	Setting
PWRUP_PLL_BYPASS	0

For unused PCI_CLKOs, they can be left unconnected. To save power, unused PCI_CLKOs should be disabled in the “Clock Out Enable Function and Debug Register” register.

3.2 Bus Routing Rules

The PCB trace parameters outlined in Tables 8 and 9 are derived from the *PCI Specification's* System Timing Budget and the PEB383's setup and hold timing parameters.

Table 8: PCI Clock Trace Routing Parameters

Parameter	Implementation Guideline
Clock length matching	Clock traces from the clock source to each PCI device should be length matched, including the trace to PEB383's PCI_CLK. When routing the clock signal to a PCI connector, the path through the connector and through the plug-in card finger-connector to the PCI device should be taken into account when calculating the PEB383's PCI_CLK trace length. The connector + plug-in card clock path length is 2.5 inches + connector delay. [a]
Trace impedance	60 Ohms +/- 15%
Minimum spacing	Three times the trace width from any other traces.
Resistor	Place 33-Ohm resistors close to PEB383's clock outputs.

a. Delay through the connector varies with the connector type. Consider adding 0.3" to 0.7" depending on the connector.

Table 9: PCI Bus Routing Parameters

Parameter	Implementation Guideline
Maximum bus length	For 66-MHz operation: 27 inches from the PEB383 to the last load on the bus, including connectors and plug-in card trace lengths.
Skew with clock	The clock traces should be matched in length. When all PCI devices see the clock rising edges at the same time, PCI bus timing budget specifies the propagation delay for the PCI bus signals between all the devices to be: 6ns for 66 MHz and 12ns for 33 MHz. However, the propagation delay must also include delays due to slow edge rates and other waveform distortion such as overshoots and undershoots. This propagation delay varies significantly depending on the bus topology and signaling level. As a general guideline the PCI bus skew with clock should be kept within: • 15" for 66-MHz operation • 30" for 33-MHz operation
Trace impedance	60 Ohms +/- 15%

PCI Pull Ups

As per the PCI specification, pull-up resistors are required on the signals listed in Table 10. PCI bus signals should be pulled up to the VIO rail.

Table 10: PCI Signal Requiring Pull-up Resistor

Signal Name	Resistor value
PCI_FRAMEn	8.2K Ohm
PCI_TRDYn	8.2K Ohm
PCI_IRDYn	8.2K Ohm
PCI_DEVSELn	8.2K Ohm
PCI_STOPn	8.2K Ohm
PCI_SERRn	8.2K Ohm
PCI_PERRn	8.2K Ohm
PCI_LOCKn	8.2K Ohm
PCI_INTAn	8.2K Ohm
PCI_INTBn	8.2K Ohm
PCI_INTCn	8.2K Ohm
PCI_INTDn	8.2K Ohm
PCI_REQn[3:0]	8.2K Ohm
PCI_GNTn[0]	8.2K Ohm only when an external arbiter is used
M66EN (when PEB383 is used on a system board)	10K Ohm