User's Manual

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R0K572390

SH7239 CPU Board User's Manual

Renesas MCU
SuperH™ RISC engine Family / SH7239 Series

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About This Manual

1. Purpose and Target Readers

This manual is designed to provide the user with an understanding of the functions and operating specifications of this CPU board. It is intended for users of this CPU board. A basic knowledge of electrical circuits, logical circuits, and microcomputers (MCUs) is necessary in order to use this manual.

This manual comprises an overview of the CPU board; its function, and operating specifications.

Carefully read all notes in the manual. These notes occur within the body of the text.

The Revision History summarizes primary modifications and additions to the previous versions. Refer to the text of the manual for details.

The following documents apply to the SH7239 CPU board R0K572390.

Document Type	Description	Document Title	Document No.
User's Manual	Describes functions (devices, memory maps, electrical characteristics), and operating specifications (connectors, and switches)	SH7239 CPU Board R0K572390 User's Manual	This publication
Installation Manual	Describes how to set up hardware and software	SH7239 CPU Board R0K572390 Installation Manual	R20UT0298EJ

The following documents apply to the SH7239 Group. Make sure to refer to the latest versions of these documents. The newest versions of the documents listed may be obtained from the Renesas Electronics website.

Document Type	Description	Document Title	Document No.
User's manual: Hardware	Hardware specifications (pin assignments, memory maps, peripheral function specifications, electrical characteristics, timing charts) and operation description Note: Refer to application notes for details on using peripheral functions	SH7239 Group, SH7237 Group User's manual: Hardware	R01UH0086EJ
Software manual	Description of CPU instruction set	SH-2A, SH2A-FPU Software manual	REJ09B0051
Application note	Applications, sample programs	Available from the Renesas Electronics website.	
Renesas technical update	Product specifications, updates on documents, etc.		

2. Frequently Used Abbreviations and Acronyms

ACIA	Asynchronous Communication Interface Adapter
bps	bits per second
CRC	Cyclic Redundancy Check
DMA	Direct Memory Access
DMAC	Direct Memory Access Controller
GSM	Global System for Mobile Communications
Hi-Z	High Impedance
IEBus	Inter Equipment bus
I/O	Input/Output
IrDA	Infrared Data Association
LSB	Least Significant Bit
MSB	Most Significant Bit
NC	Non-Connection
PLL	Phase Locked Loop
PWM	Pulse Width Modulation
SFR	Special Function Registers
SIM	Subscriber Identity Module
UART	Universal Asynchronous Receiver/Transmitter
VCO	Voltage Controlled Oscillator

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1. Overview

1.1 Introduction

The R0K572390 is a CPU board designed for evaluating the features and performance of the SH7239 Group of Renesas Electronics single-chip RISC microcomputers (MCUs). It is also used for developing and evaluating application software for these MCUs. The R0K572390 CPU board lineup consists of following two models:

- R0K572390C000BR, which includes SH7239A MCU (3.3 V, working at 160 MHz)
- R0K572390C020BR, which includes SH7239B MCU (5.0 V, working at 100 MHz)

The SH7239 MCU's internal peripheral pins are connected to common ring connectors and application headers on the R0K572390 to allow for timing evaluation with peripherals using measurements instruments, and the development of the expansion board according to its application. The Renesas Electronics E10A-USB on-chip emulator can be connected to the R0K572390.

1.2 Configuration

Figure 1.1 shows an example of a system configuration using the R0K572390.

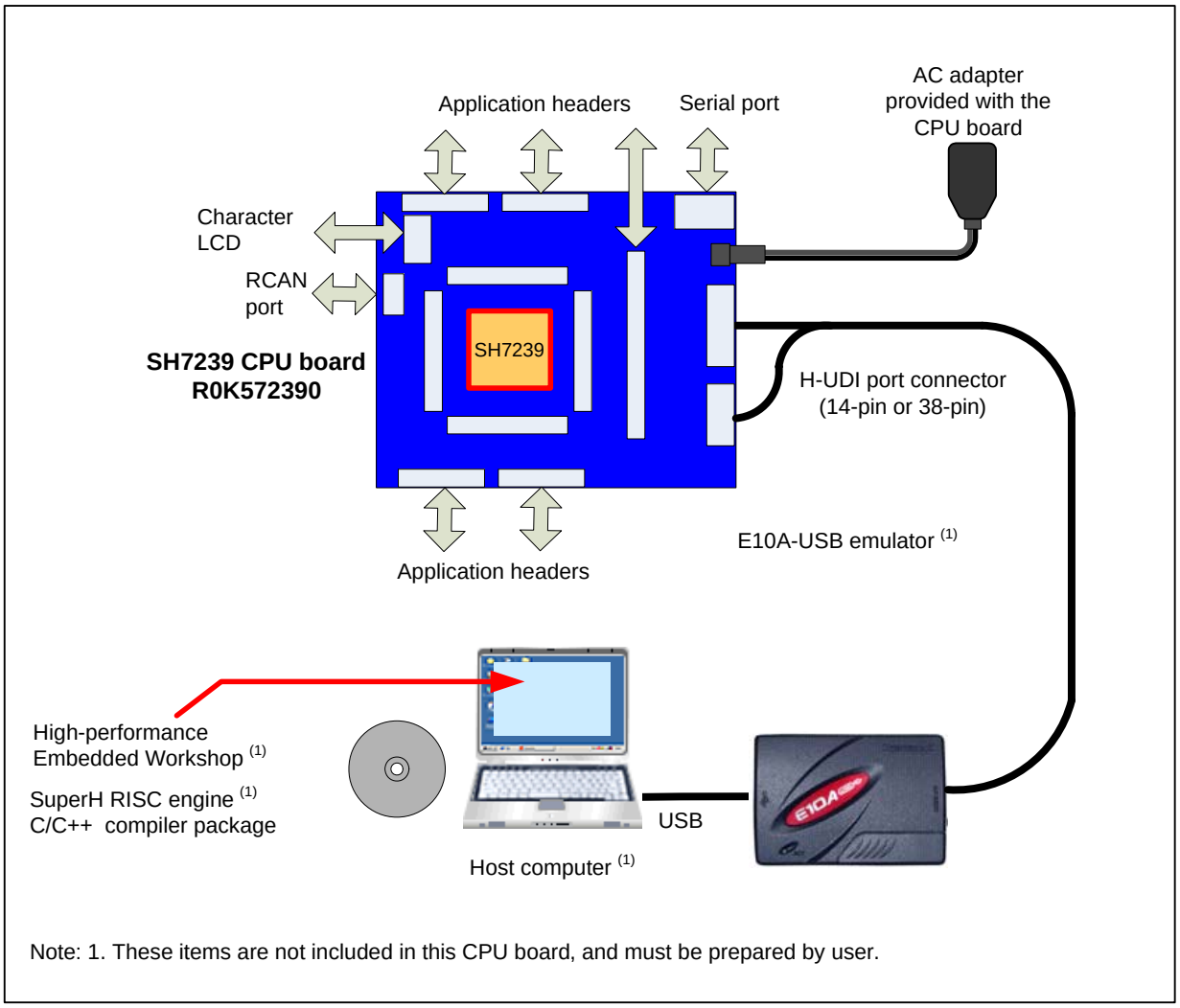


Figure 1.1 Configuration Using the R0K572390

1.3 Board Specifications

Table 1.1 lists the specifications of the R0K572390.

Table 1.1 R0K572390 Board Specifications

Item	Description
CPU	SH7239A (1) or SH7239B (2) • Input (XIN) clock: 10 MHz (1) or 12.5 MHz (2) • CPU clock: Up to 160 MHz (1) or 100 MHz (2) • Peripheral clock: Up to 40 MHz (1) or 50 Hz (2) • Internal memory Flash memory: 512 KB RAM: 64 KB FLD (flash memory to store data): 32 KB
Memory	• EEPROM: 64 KB (SPI interface) • SRAM: 64 KB (8-bit bus × 2, optional) (3)
Connectors	• Common ring connectors (All CPU signals, optional) • Application headers (Bus, I/O, VCC, GND, optional) • Serial port connector (D-sub, 9-pin) • RCAN port connector (3-pin, pin header) • 14-pin LCD interface connector • 14-pin H-UDI port connector • 38-pin H-UDI port connector
LEDs, potentiometer	• Power LED: 1 • Boot mode LED: 1 • User LEDs: 4 • 10-kΩ potentiometer: 1
Switches, jumpers	• Reset switch: 1 • User switches: 3 (NMI, IRQ3 or $\overline{\text{ADTRG}}$, IRQ4) • Mode setting DIP switches: 1 (2/package) • Power select jumper: 1 (Not populated) (4) • RCAN signal connection jumper: 1 (Not populated) • $\overline{\text{ADTRG}}$ signal connection jumper: 1 (Not populated)
Board specifications	• Dimensions: 100 mm × 120 mm • Mounting form: 4-layer, double-sided • Number of boards: 1

Notes 1. These parameters apply to the R0K572390C000BR.
2. These parameters apply to the R0K572390C020BR.
3. User is allowed to install SRAM on the R0K572390C000BR.
4. Power supply voltage is fixed to 3.3 V on the R0K572390C000BR, 5 V on the R0K572390C020BR.

1.4 Exterior

Figure 1.2 shows the exterior of the R0K572390.

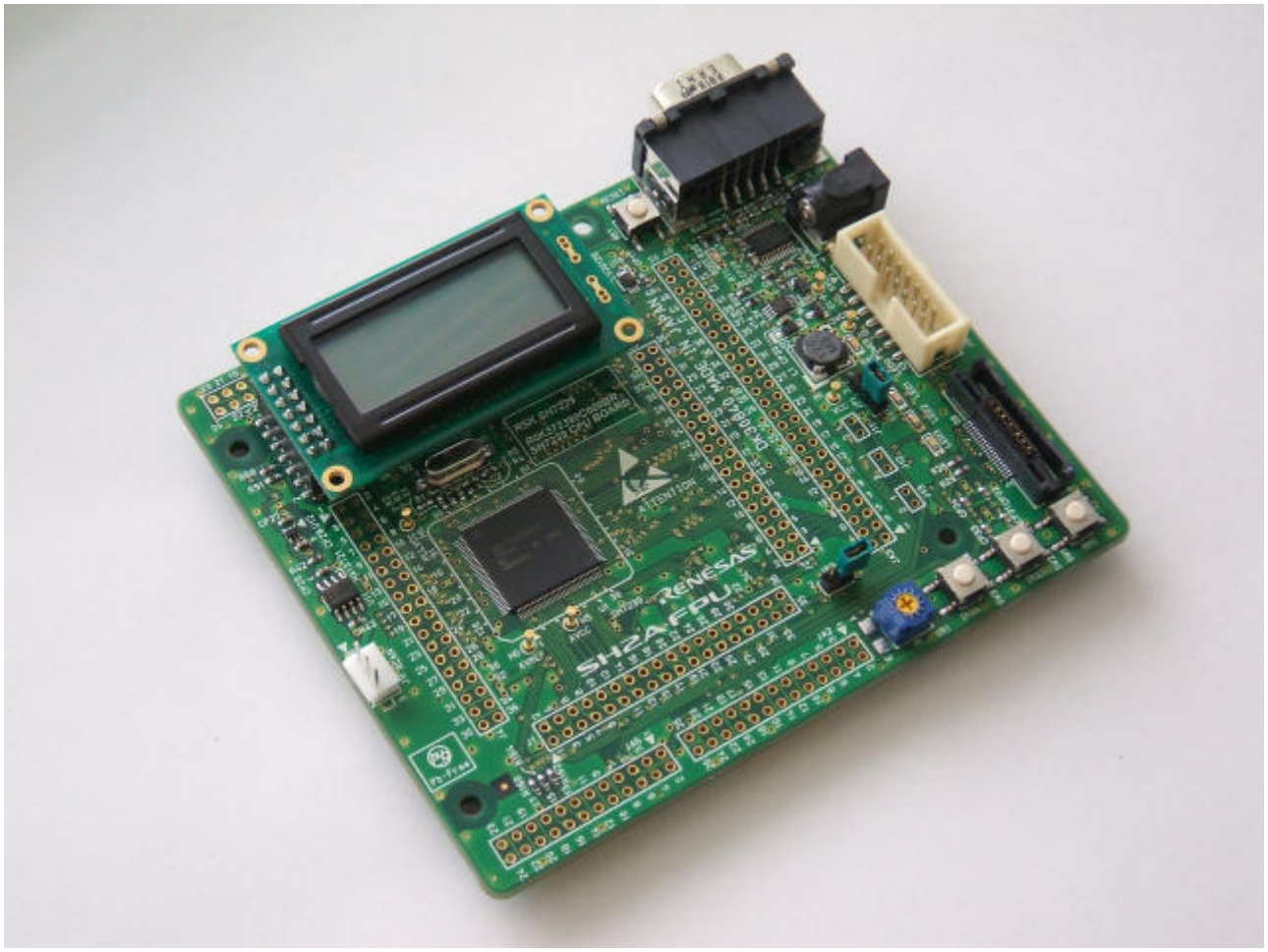


Figure 1.2 R0K572390 Exterior

1.5 Block Diagram

Figure 1.3 shows the block diagram of the R0K572390.

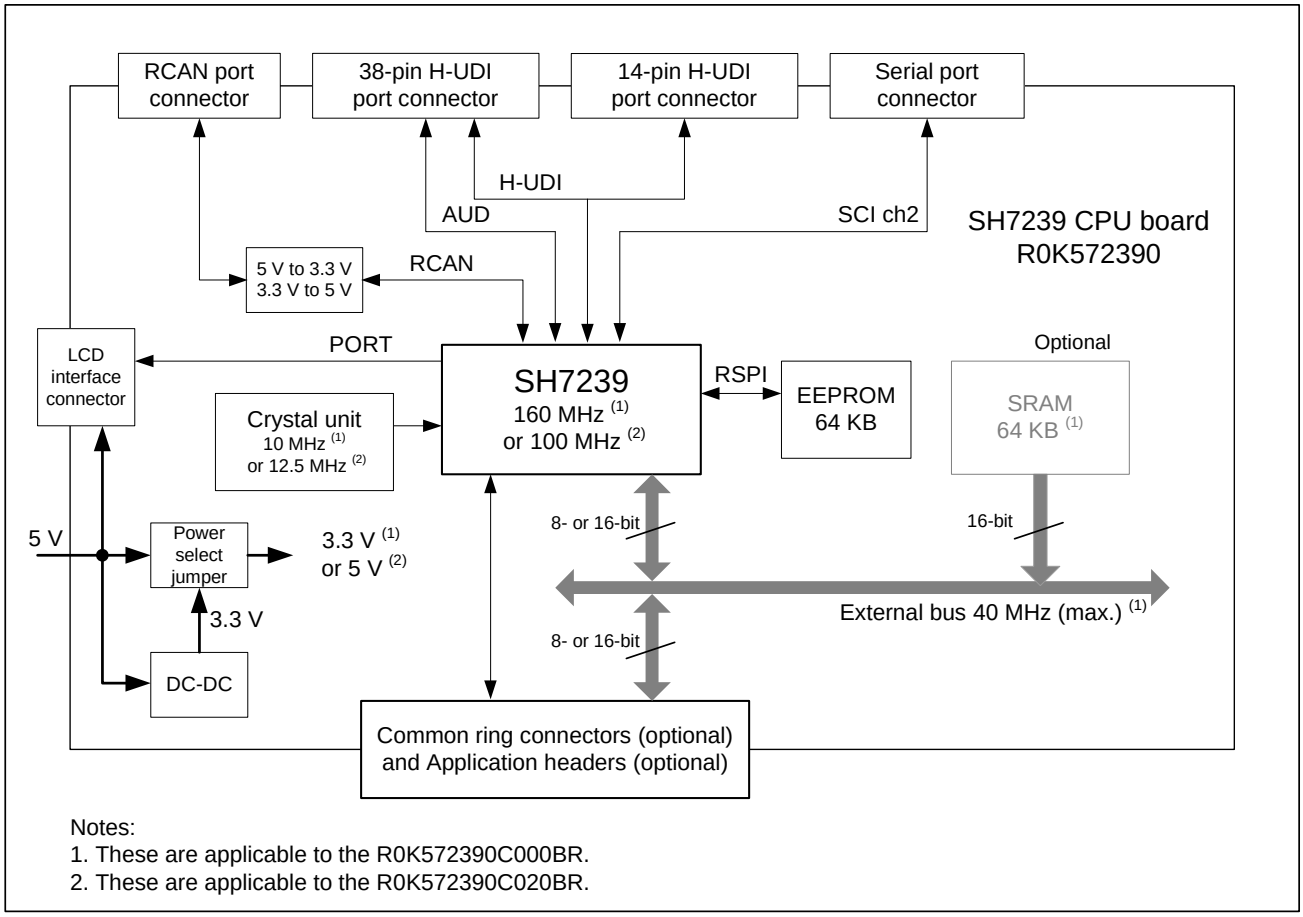


Figure 1.3 R0K572390 Block Diagram

1.6 Component Layout

Figure 1.4 shows the layout of the major components on the R0K572390.

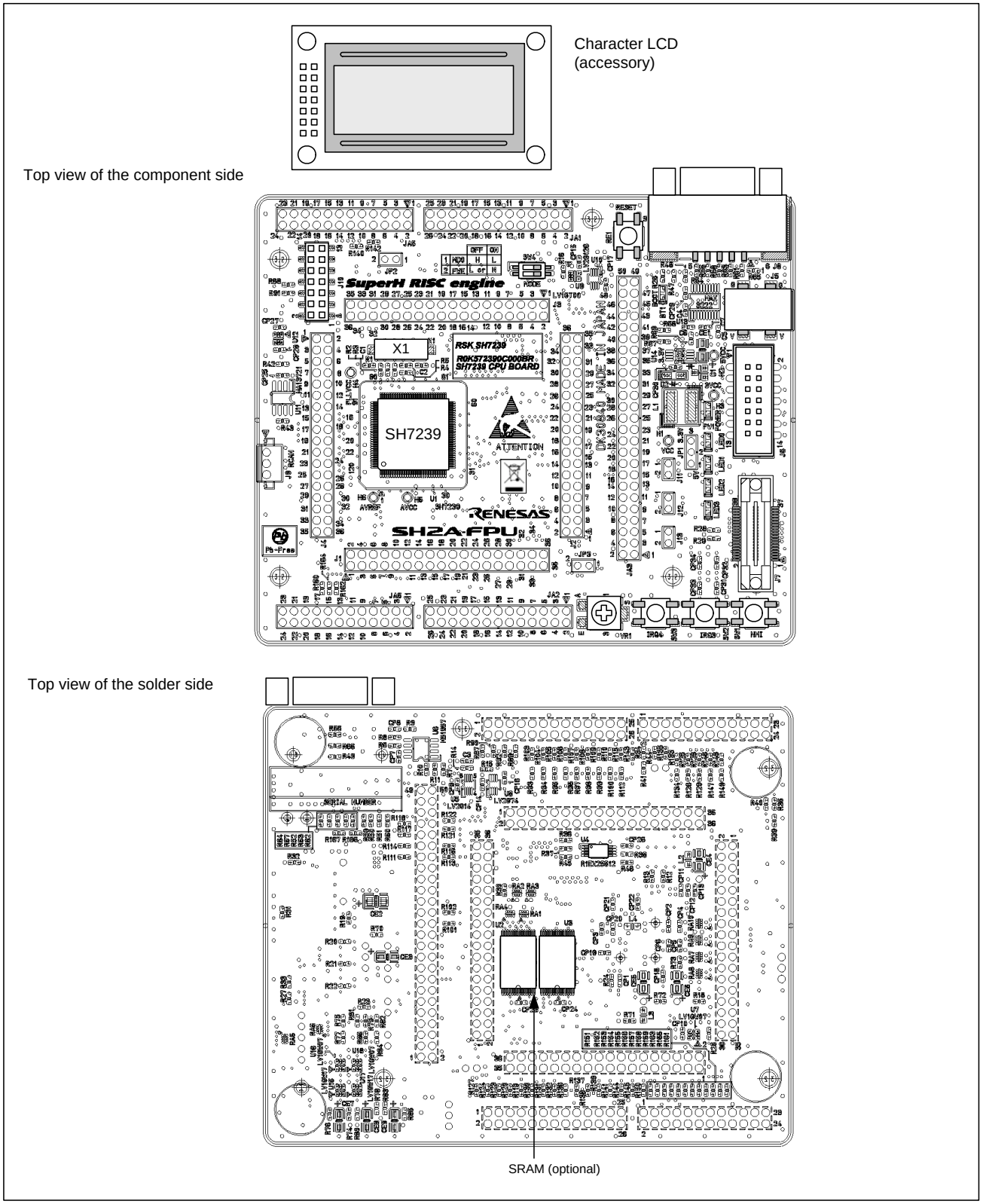


Figure 1.4 R0K572390 Component Layout

Table 1.2 lists the major components on the R0K572390.

Table 1.2 Major Components on the R0K572390

Symbol	Name	Remarks	Recommended Optional Components (Manufacturer Name and Part Number)
U1	CPU	SH7239A (1) (Renesas) SH7239B (2) (Renesas)	
U2, U3	SRAM	Optional (3)	M5M5256DVP-70G (Renesas)
U4	EEPROM	R1EX25512ATA00A (Renesas)	
U13	RS-232C transceiver	MAX3222CPWR (TI)	
U11	RCAN transceiver	HA13721RPJE (Renesas)	
U14	3.3 V regulator	LM2738-YMY 550kHz (NS)	
U6	Reset IC	M51957BFP (Renesas)	
X1	Crystal unit	CXZ49GFB10000H0PESZZ (1) CXZ49GFB12500H0PESZZ (2) (Kyocera Kinseki)	
J1 to J4	Common ring connectors	Optional	18-pin double row pin header
JA1, JA2	Application headers	Optional	13-pin double row pin header
JA3	Application header	Optional	25-pin double row pin header
JA5, JA6	Application headers	Optional	12-pin double row pin header
J5	DC power jack	KLDX-SMT2-0202-A (Kycon)	
J6	14-pin H-UDI port connector	HTST-107-01-T-DV (Samtec)	
J7	38-pin H-UDI port connector	2-5767004-2 (Tyco electronics)	
J8	Serial port connector	154188 (ERNI)	
J9	RCAN port connector	B3P-SHF-1AA(LF)(SN) (J.S.T.)	
J10	LCD interface connector	SSM-107-LM-DV-P-TR (Samtec)	
J11	External power supply connector	Optional	A2-2PA-2.54DSA (Hirose)
J12	External power supply connector	Optional	A2-2PA-2.54DSA (Hirose)
J13	External power supply connector	Optional	A2-2PA-2.54DSA (Hirose)
POWER	Power LED	Green	
BOOT	Boot mode LED	Orange	
LED0 to LED3	User LEDs	Green, orange, red, red	
VR1	Potentiometer	CT-6ETV10KΩ (NIDEC Copal)	
RESET	Reset switch	B3S-1000 (OMRON)	
SW1	NMI switch	B3S-1000 (OMRON)	
SW2, SW3	IRQ3, IRQ4 switches	B3S-1000 (OMRON)	
SW4	Mode setting DIP switches (2/package)	A6HF-2102 (OMRON)	
JP1	Power select jumper	Optional	2.54 mm pitch 3-way pin header
JP2	RCAN signal connection jumper	Optional	2.54 mm pitch 2-way pin header
JP3	$\overline{\text{ADTRG}}$ signal connection jumper	Optional	2.54 mm pitch 2-way pin header

Notes: 1. These parameters apply to the R0K572390C000BR.
2. These parameters apply to the R0K572390C020BR.
3. User is allowed to install SRAM on the R0K572390C000BR only.
4. Power supply voltage is fixed to 3.3 V on the R0K572390C000BR, 5 V on the R0K572390C020BR.

1.7 Memory Maps

Figure 1.5 and Figure 1.6 show memory map examples of the SH7239 and R0K572390.

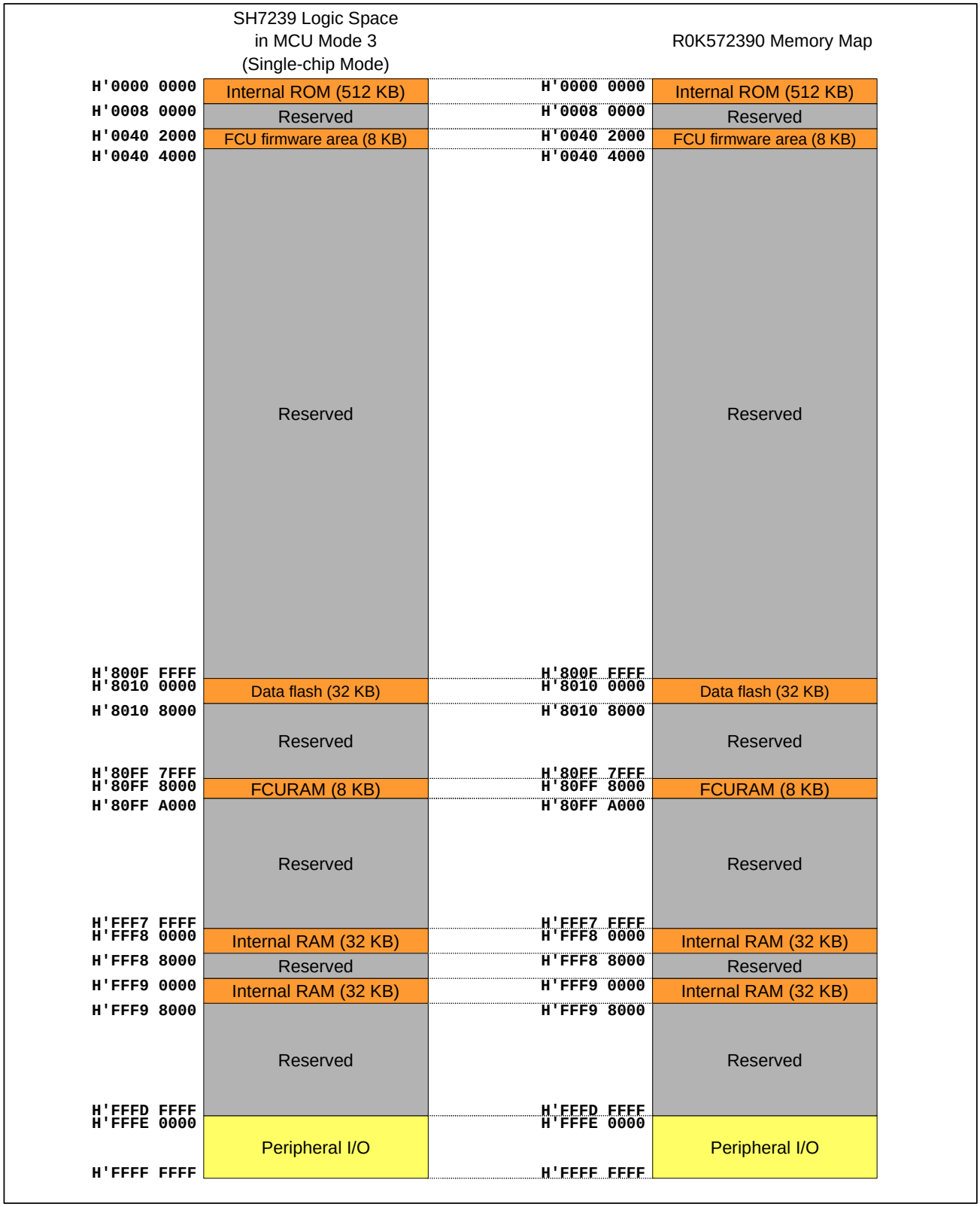


Figure 1.5 SH7239 Memory Map Example (MCU Mode 3)

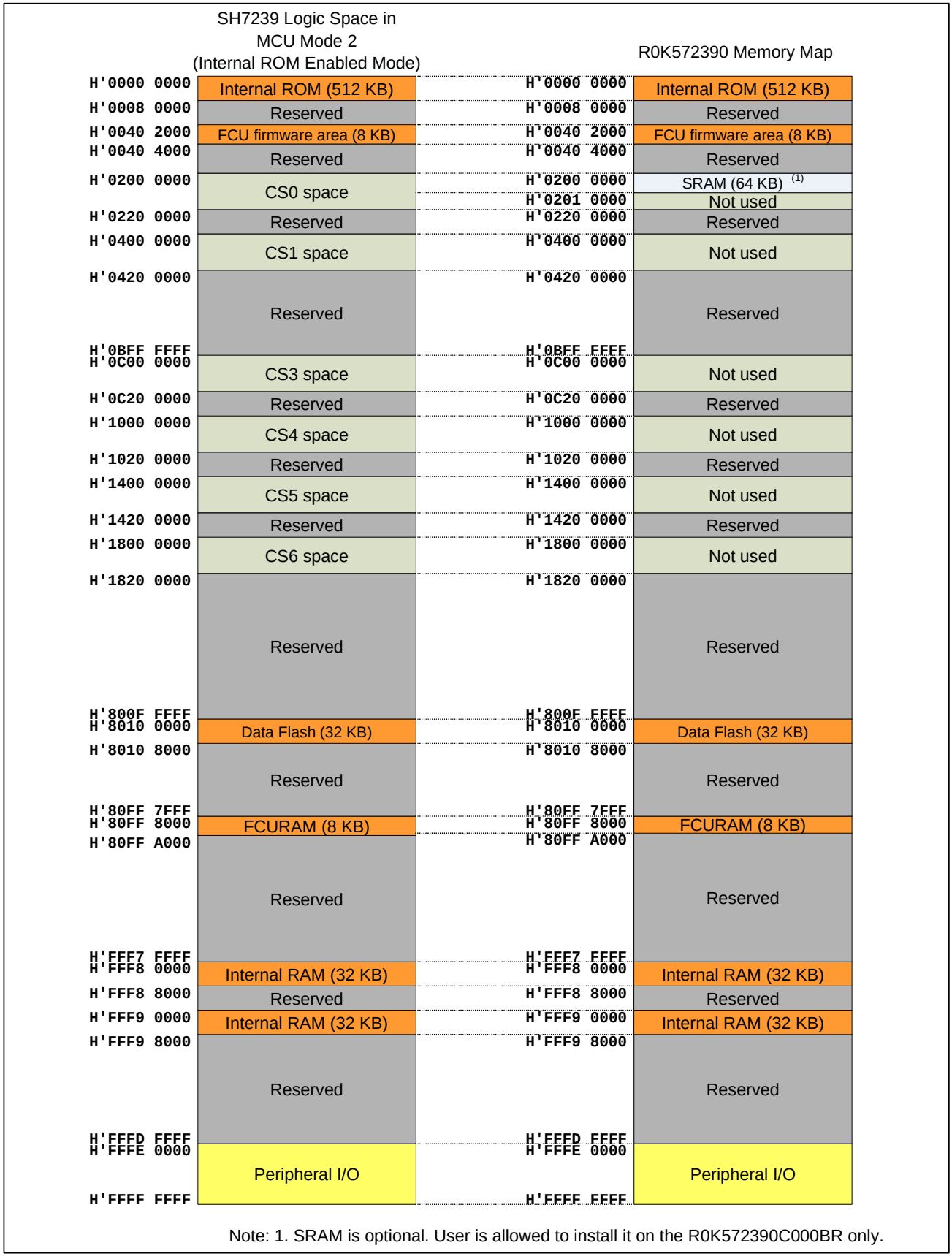


Figure 1.6 SH7239 Memory Map (MCU Mode 2, for R0K572390C000BR only)

1.8 Absolute Maximum Ratings

Table 1.3 lists the absolute maximum ratings of the R0K572390.

Table 1.3 R0K572390 Absolute Maximum Ratings

Symbol	Item	Value	Remarks
5VCC	5 V system power supply voltage	−0.3 to 6.0 V	Reference voltage: VSS
3VCC (1)	3.3 V system power supply voltage	−0.3 V to 4.0 V	Reference voltage: VSS
AVCC	5 V system analog power supply voltage	−0.3 V to 6.0 V	Reference voltage: AVSS
T_{opr}	Operating ambient temperature (2)	0°C to 50°C	Do not expose to condensation or corrosive gas
T_{stg}	Storage ambient temperature (2)	−10°C to 60°C	Do not expose to condensation or corrosive gas

Notes: 1. 3VCC is used to supply the 3.3 V system power supply voltage directly from the external power supply connector.
2. Ambient temperature refers to the air temperature in the vicinity of the board.

1.9 Operating Conditions

Table 1.4 lists the operating conditions for the R0K572390.

Table 1.4 R0K572390 Operating Conditions

Symbol	Item	Value	Remarks
5VCC	5 V system power supply voltage	4.75 V to 5.25 V	Reference voltage: VSS
3VCC (1)	3.3 V system power supply voltage	3.15 V to 3.45 V	Reference voltage: VSS
AVCC	5 V system analog power supply voltage	4.75 V to 5.25 V	Reference voltage: AVSS
T_{opr}	Maximum current consumption	1 A max.	Both 5 V system power supply (including analog), and 3.3 V system power supply
T_{stg}	Operating ambient temperature (2)	0°C to 50°C	Do not expose to condensation or corrosive gas

Notes: 1. 3VCC is used to supply the 3.3 V system power supply voltage directly from the external power supply connector.
2. Ambient temperature refers to the air temperature in the vicinity of the board.

2. Functions

2.1 Overview of Functions

The R0K572390 includes the function modules listed in the following table.

Table 2.1 R0K572390 Function Modules

Section	Function	Description
2.2	CPU	SH7239A (1) or SH7239B (2) • Input (XIN) clock: 10 MHz (1) or 12.5 MHz (2) • CPU clock: Up to 160 MHz (1) or 100 MHz (2) • Peripheral clock: Up to 40 MHz (1) or 50 Hz (2) • Internal memory Flash memory: 512 KB RAM: 64 KB FLD (flash memory to store data): 32 KB
2.3	External Memory	• EEPROM: 64 KB (SPI interface) • SRAM: 64 KB (8-bit bus × 2, optional) (3)
2.4	Serial Port Interface	Connects the SH7239 SCI channel 2 to the serial port connector
2.5	I/O Ports	Connects all the SH7239 signals to common ring connectors Connects the SH7239 bus and I/O ports to application headers
2.6	RCAN Interface	Connects the SH7239 RCAN pins to the RCAN port connector via the RCAN transceiver
2.7	LCD Interface	Character LCD interface
2.8	H-UDI Interface	Connects the SH7239 H-UDI/AUD pins to the H-UDI port connectors (14-pin, 38-pin) to enable debugging the R0K572390 using the E10A-USB emulator (4)
2.9	Switches and Jumpers	• Reset switch • User switches: 3 (Connects NMI, IRQ3 or $\overline{\text{ADTRG}}$, and IRQ4 pins) • Mode setting DIP switches: 1 (2/package) • Power select jumper: 1 (Not populated) • RCAN signal connection jumper: 1 (Not populated) • $\overline{\text{ADTRG}}$ signal connection jumper: 1 (Not populated)
2.10	LEDs and Potentiometer	• Power LED: 1 • Boot mode LED: 1 • User LEDs: 4 • 10-kΩ potentiometer: 1
2.11	Power Module	Controls the R0K572390 system power supply
2.12	Clock Module	Clock source: 10 MHz (1) or 12.5 MHz (2) crystal unit
2.13	Reset Module	Resets the devices installed on the R0K572390
–	Operating Specifications	Refer to chapter 3 for details on connectors, switches, LEDs, and the potentiometer

Notes 1. These parameters apply to the R0K572390C000BR.
2. These parameters apply to the R0K572390C020BR.
3. User is allowed to install SRAM on the R0K572390C000BR.
4. H-UDI port connector cannot be used when using addresses A16 to A20, and $\overline{\text{AH}}$ by the application headers.

2.2 CPU

The R0K572390 includes following two models according to the MCU product lineup.

- R0K572390C000BR: SH7239A MCU (3.3 V, CPU clock = 160 MHz max, peripheral clock = 40 MHz max)
- R0K572390C020BR: SH7239B MCU (5.0 V, CPU clock = 100 MHz max, peripheral clock = 50 MHz max)

The SH7239A and SH7239B MCUs have 512 KB of flash memory, 32 KB of FLD, and 64 KB of RAM to support various applications such as data processing and equipment control.

Figure 2.1 shows the SH7239 block diagram on the R0K572390.

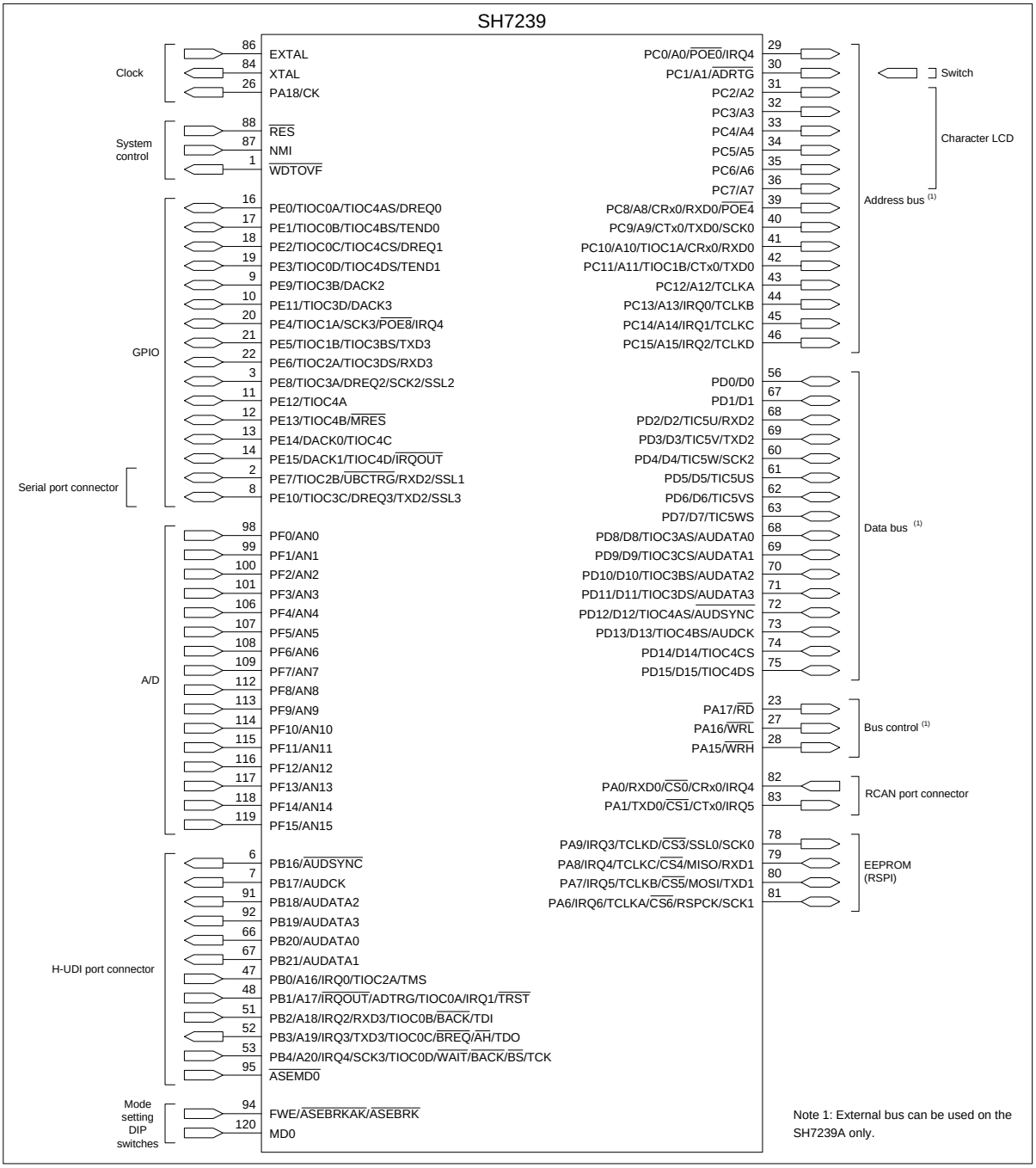


Figure 2.1 SH7239 Block Diagram

2.3 External Memory

2.3.1 SRAM

64-KB SRAM (32-Kword × 8-bit × 2) can be installed on the R0K572390 (SRAM is optional, and not installed by default). The SH7239 Bus State Controller $\overline{CS0}$ controls the SRAMs. The SRAM can be used only when setting the SH7239A in MCU mode 2. As $\overline{CS0}$ signal to control SRAM is also used as the RCAN CRx0, RCAN and SRAM cannot be used at the same time. When using SRAM, remove the resistor R41 and install the resistor R30 (not installed by default), and connect the signal to SRAM.

Figure 2.2 shows the SH7239 and SRAM configuration.

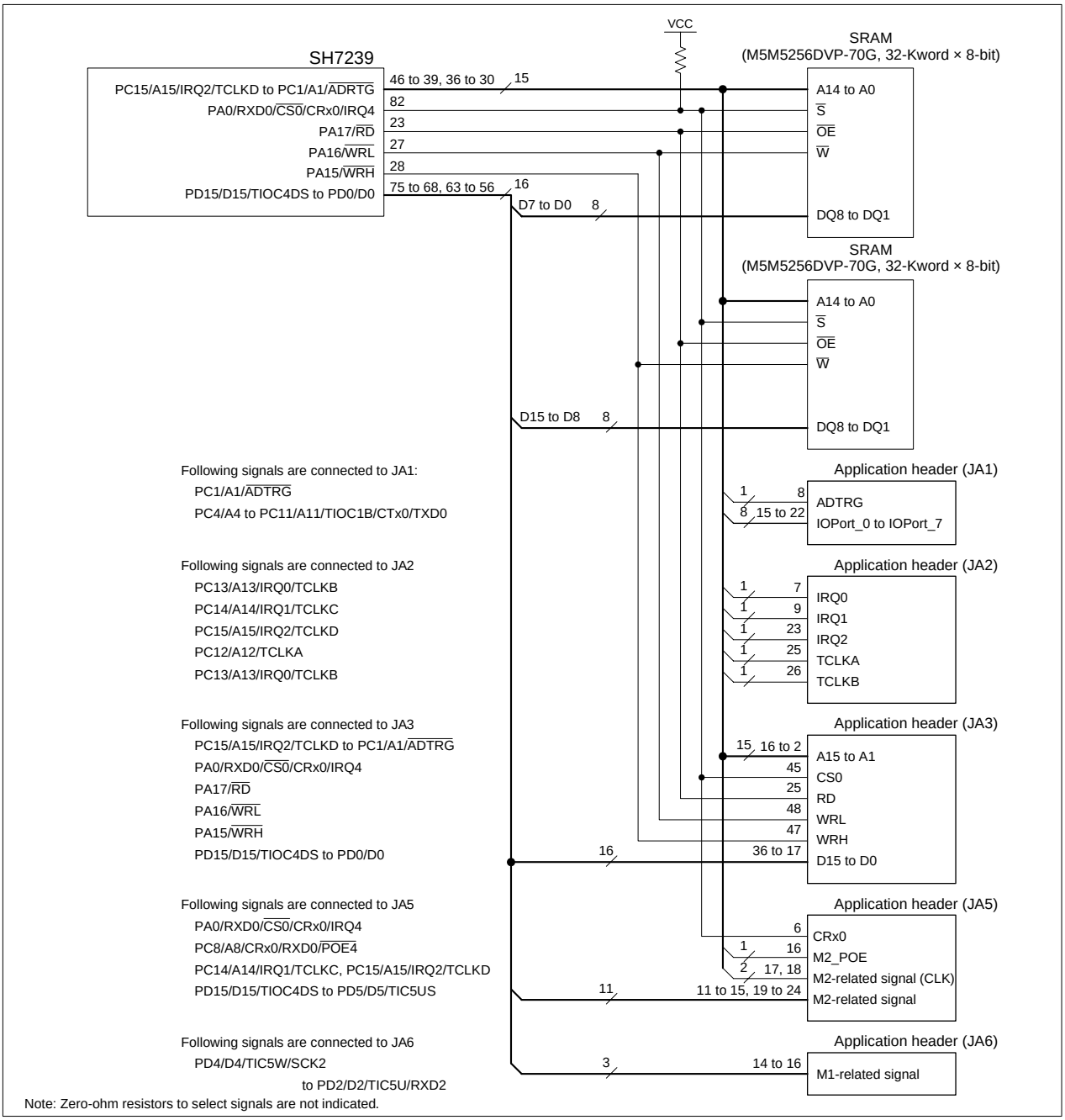


Figure 2.2 SRAM Configuration

Figure 2.3 shows SRAM read/write timing chart. Table 2.2 lists the Bus State Controller settings.

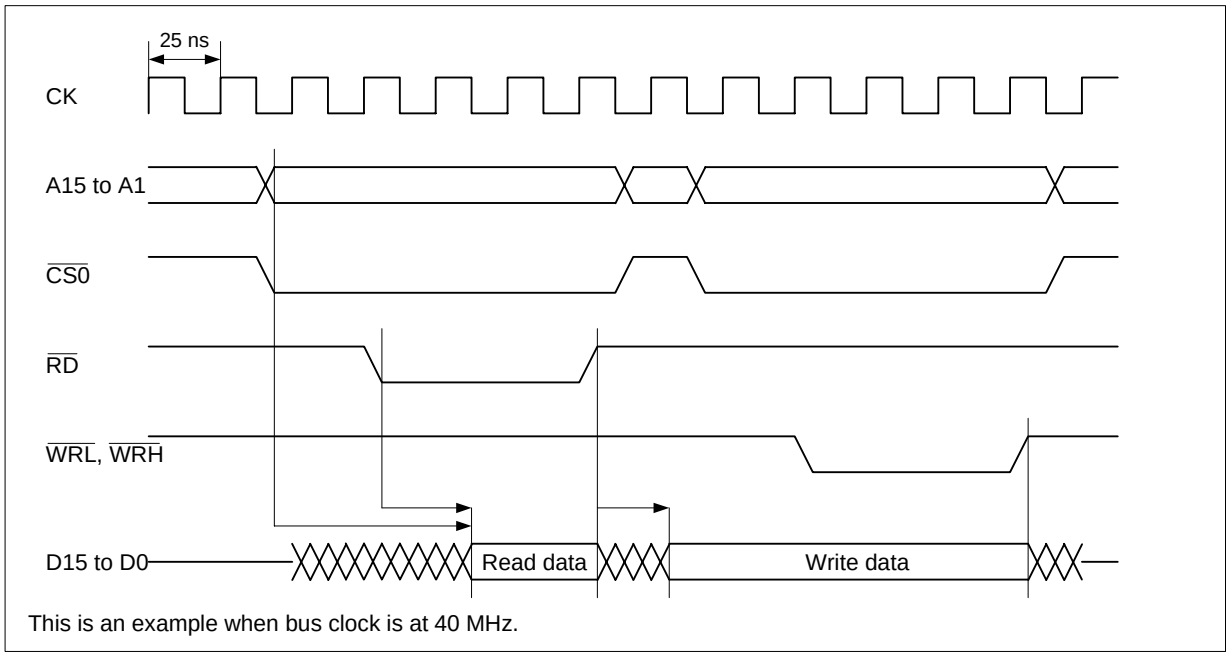


Figure 2.3 SRAM Read/Write Timing Chart

Table 2.2 Bus State Controller Settings

User Area	Target Device	Setting
CS0	M5M5256DVP-70G	CS0 space bus control register (CS0BCR): Recommended value: H'0240 0400 — Number of idles between Read-Write cycles: IWRWD [2:0] = IWRWS [2:0] = B'001; 1 idle cycle inserted — Memory: TYPE [2:0] = B'000; normal space — Data bus width: BSZ [1:0] = B'10; 16-bit bus CS0 space wait control register (CS0WCR): Recommended value: H'0000 0940 — Number of delay cycles from address, CS0 assertion to RD, WRxx assertion: SW [1:0] = B'01; 1.5 cycles — Number of access wait cycles: WR [3:0] = B'0010; 2 cycles — External wait mask specification: WM = B'1; Ignore external wait input — Number of delay cycles from RD, WRxx, negation to address, CS0 negation: HW [1:0] = B'00; 0.5 cycles

2.3.2 EEPROM

The R0K572390 includes a 64-KB EEPROM (64-Kword × 8-bit). The SH7239 Renesas Serial Peripheral Interface controls the EEPROM. Pins to control EEPROM are also connected to the user switch SW2, and application headers (JA1, JA2, and JA3) to be multiplexed with SCI channel 1 pin, MTU2 pins, IRQ3, $\overline{CS3}$, and $\overline{CS6}$ signals. Note that these signals cannot be used at the same time. Figure 2.4 shows the SH7239 and EEPROM configuration.

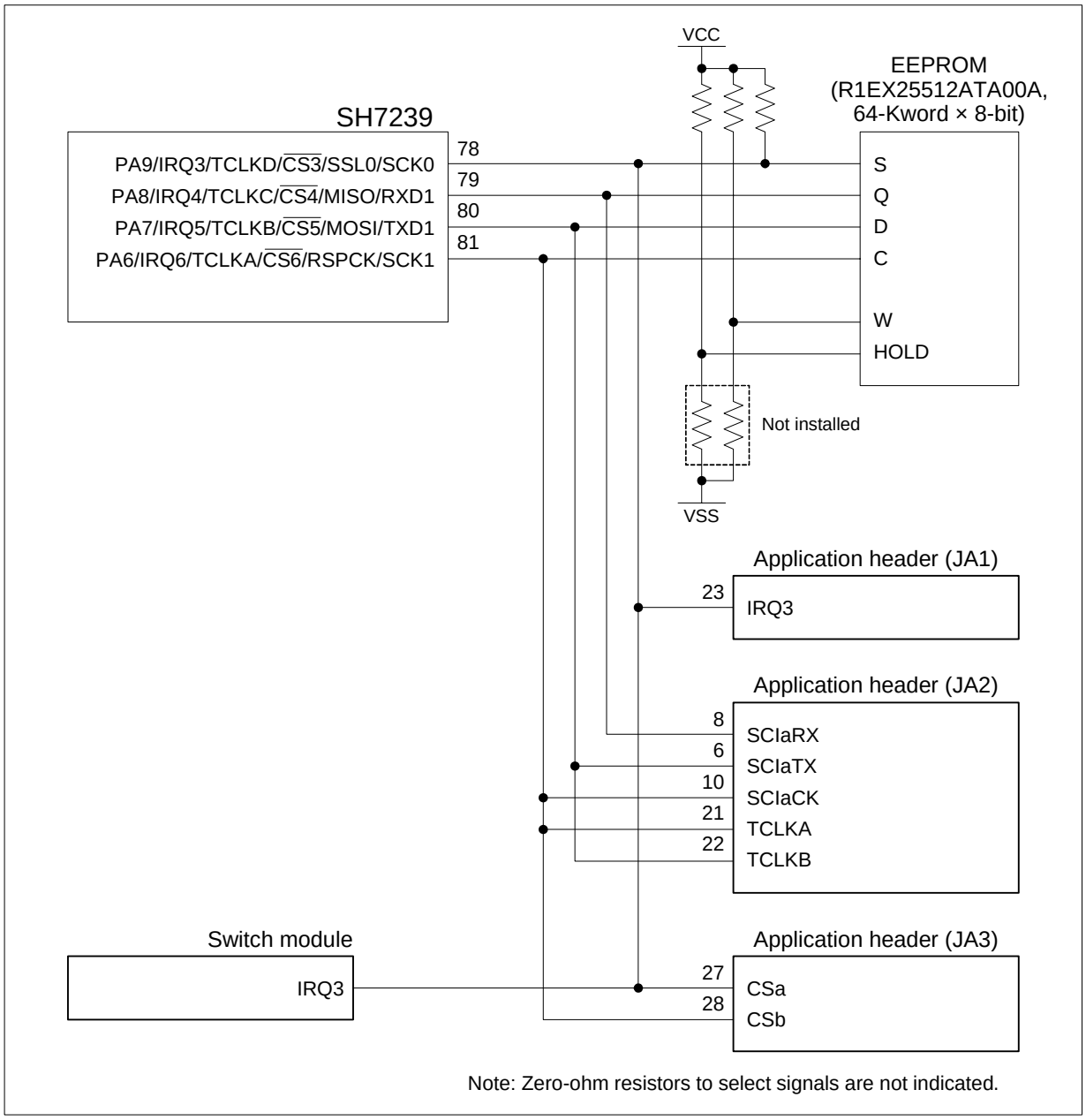


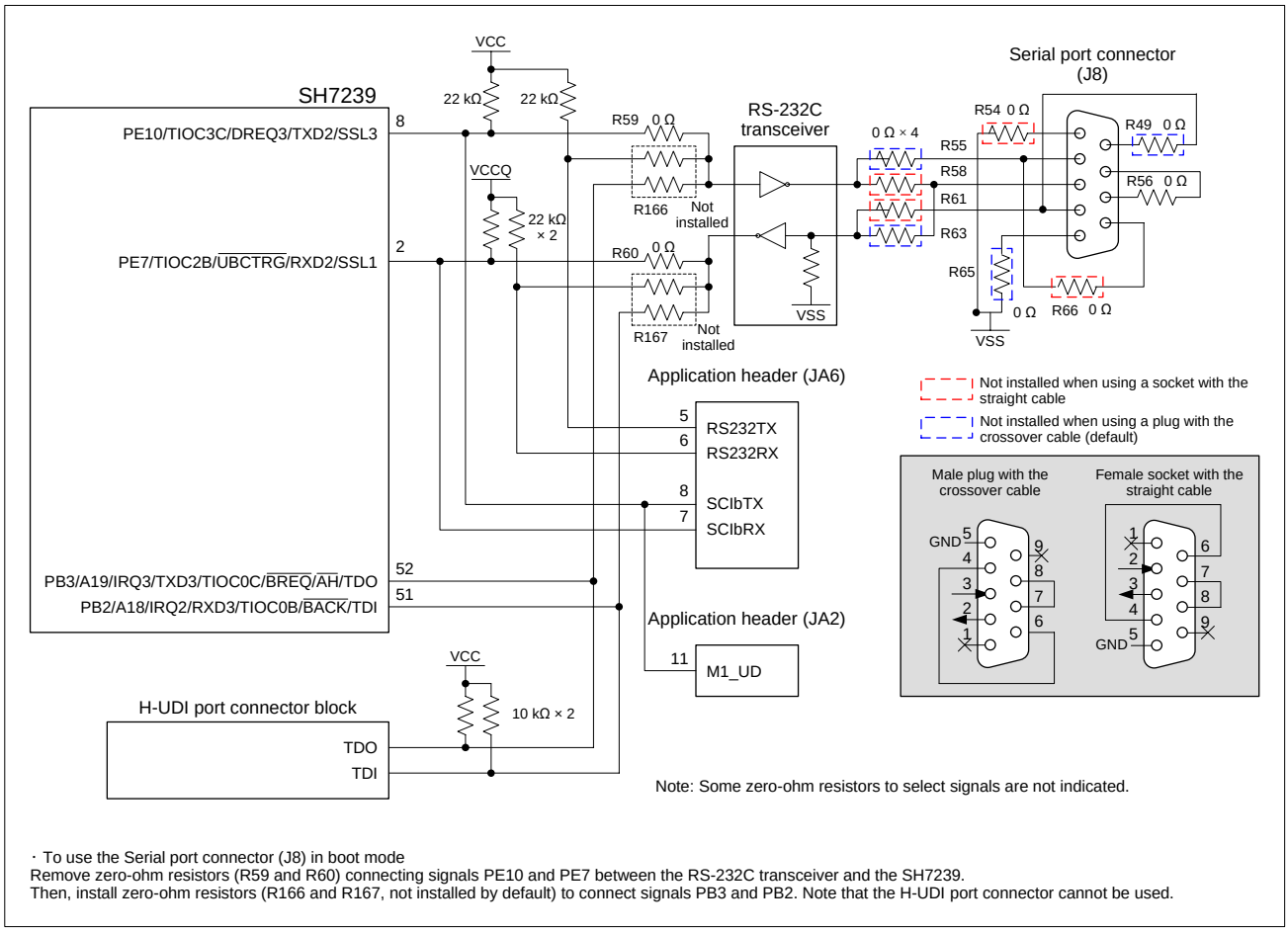
Figure 2.4 EEPROM Configuration

2.4 Serial Port Interface

On the R0K572390, SH7239 SCI channel 2 is connected to the serial port connector (J8) via the RS-232C transceiver. Also, the SH7239 SCI channel 2 is connected to pins 7 and 8 of the application header (JA6), pin 11 (used as the TIOC3C) of the application header (JA2). Install zero-ohm resistor in appropriate pin to connect pins 5 and 6 of the application header (JA6) to the serial port connector (J8) via the RS-232C transceiver. When using the SH7239 SCI channel 2 as the serial port, it cannot be used as the application header.

To use the serial port connector (J8) in boot mode, remove zero-ohm resistors R59 and R60 to connect signals PE10 and PE7 between the RS-232C transceiver and the SH7239. Then, install zero-ohm resistors R166 and R167 (not installed by default) to connect signals PB3 and PB2 between the RS-232C transceiver and the SH7239. Note that the H-UDI port connector cannot be used.

Figure 2.5 shows the serial port block diagram.



· To use the Serial port connector (J8) in boot mode
Remove zero-ohm resistors (R59 and R60) connecting signals PE10 and PE7 between the RS-232C transceiver and the SH7239.
Then, install zero-ohm resistors (R166 and R167, not installed by default) to connect signals PB3 and PB2. Note that the H-UDI port connector cannot be used.

Figure 2.5 Serial Port Block Diagram

2.5 I/O Ports

All SH7239 signals are connected to common ring connectors on the R0K572390. Most of the I/O ports are connected to application headers. Table 2.3 to Table 2.6 list I/O port functions. Some I/O ports are also connected to devices, I/O connectors, switches and LEDs. For details, refer to chapter 3 Operating Specifications.

Table 2.3 I/O Port Functions (1/4)

SH7239		Common ring connector				Application header					
No.	Pin Name	J1	J2	J3	J4	JA1	JA2	JA3	JA5	JA6	Function
1	$\overline{\text{WDTOVF}}$	1					[5]				$\overline{\text{WDTOVF}}$
2	PE7/TIOC2B/$\overline{\text{UBCTRG}}$/RXD2/SSL1	2								(7)	RXD2
3	PE8/TIOC3A/SCK2/DREQ2/SSL2	3								(10), [13]	SCK2, TIOC3A
4	VCC	4									
5	VSS	5									
6	PB16/$\overline{\text{AUDSYNC}}$	6									
7	PB17/AUDCK	7									
8	PE10/TIOC3C/TXD2/DREQ3/SSL3	8					[11]			(8)	TIOC3C, TXD2
9	PE9/TIOC3B/DACK2	9					13				TIOC3B
10	PE11/TIOC3D/DACK3	10					14				TIOC3D
11	PE12/TIOC4A	11					15				TIOC4A
12	PE13/TIOC4B/$\overline{\text{MRES}}$	12					17				TIOC4B
13	PE14/DACK0/TIOC4C	13					[16]			(2)	TIOC4C, DACK0
14	PE15/DACK1/TIOC4D/$\overline{\text{IRQOUT}}$	14					18				TIOC4D
15	VSS	15									
16	PE0/TIOC0A/TIOC4AS/DREQ0	16				(23)	(7)			(1)	TIOC0A, DREQ0
17	PE1/TIOC0B/TIOC4BS/TEND0	17					(9)		(9)	(3)	TIOC0B, TEND0
18	PE2/TIOC0C/TIOC4CS/DREQ1	18					(23)		(10)		TIOC0C
19	PE3/TIOC0D/TIOC4DS/TEND1	19							(14)	[16]	TIOC0D
20	PE4/TIOC1A/SCK3/$\overline{\text{POE8}}$/IRQ4	20					(23)		[9], (12)	(11), (14)	TIOC1A, IRQ4, SCK3
21	PE5/TIOC1B/TIOC3BS/TXD3	21					[19]			(9)	TIOC1B, TXD3
22	PE6/TIOC2A/TIOC3DS/RXD3	22					[20]		(13)	(12) (15)	TIOC2A, RXD3
23	PA17/$\overline{\text{RD}}$	23						25			$\overline{\text{RD}}$
24	VCL										
25	VSS	25									
26	PA18/CK	26						[44]			CK
27	PA16/$\overline{\text{WRL}}$	27						48			$\overline{\text{WRL}}$
28	PA15/$\overline{\text{WRH}}$	28						47			$\overline{\text{WRH}}$

Notes: 1. Brackets [ ] indicate the signals connected to the CPU pin via a device, and zero-ohm resistor (installed).
2. Parentheses ( ) indicate the signals connected to the CPU pin via zero-ohm resistor (NOT installed). Remove or install zero-ohm resistors according to connectors and pins to use. No signal conflicts are allowed.

Table 2.4 I/O Port Functions (2/4)

SH7239		Common ring connector				Application header					
No.	Pin Name	J1	J2	J3	J4	JA1	JA2	JA3	JA5	JA6	Function
29	PC0/A0/$\overline{\text{POE0}}$/IRQ4	29					24	1			$\overline{\text{POE0}}$, A0
30	PC1/A1/$\overline{\text{ADTRG}}$	30				8		2			$\overline{\text{ADTRG}}$, A1
31	PC2/A2		1					3			A2
32	PC3/A3		2					4			A3
33	PC4/A4		3			(15)		5			PC4, A4
34	PC5/A5		4			(16)		6			PC5, A5
35	PC6/A6		5			(17)		7			PC6, A6
36	PC7/A7		6			(18)		8			PC7, A7
37	VSS		7								
38	VCC		8								
39	PC8/A8/CRx0/RXD0/$\overline{\text{POE4}}$		9			(19)		9	16		PC8, A8, $\overline{\text{POE4}}$
40	PC9/A9/CTx0/TXD0/SCK0		10			(20)		10			PC9, A9
41	PC10/A10/TIOC1A/CRx0/RXD0		11			(21)		11			PC10, A10
42	PC11/A11/TIOC1B/CTx0/TXD0		12			(22)		12			PC11, A11
43	PC12/A12/TCLKA		13				25	13			TCLKA, A12
44	PC13/A13/IRQ0/TCLKB		14				[7], 26	14			IRQ0, TCLKB, A13,
45	PC14/A14/IRQ1/TCLKC		15				[9]	15	(17)		IRQ1, A14, TCLKC
46	PC15/A15/IRQ2/TCLKD		16				[23]	16	(18)		IRQ2, A15, TCLKD
47	PB0/A16/IRQ0/TIOC2A/TMS		17					(37)			A16
48	PB1/A17/$\overline{\text{IRQOUT}}$/$\overline{\text{ADTRG}}$/TIOC0A/IRQ1/$\overline{\text{TRST}}$		18					(38)			A17
49	VCC		19								
50	VSS		20								
51	PB2/A18/IRQ2/RXD3/TIOC0B/$\overline{\text{BACK}}$/TDI		21					(39)			A18
52	PB3/A19/IRQ3/TXD3/TIOC0C/$\overline{\text{BREQ}}$/$\overline{\text{AH}}$/TDO		22					(40), (46)			A19, $\overline{\text{AH}}$
53	PB4/A20/IRQ4/SCK3/TIOC0D/$\overline{\text{WAIT}}$/$\overline{\text{BACK}}$/$\overline{\text{BS}}$/TCK		23					(45)			A20
54	VCL										

Notes: 1. Brackets [ ] indicate the signals connected to the CPU pin via a device, and zero-ohm resistor (installed).
2. Parentheses ( ) indicate the signals connected to the CPU pin via zero-ohm resistor (NOT installed). Remove or install zero-ohm resistors according to connectors and pins to use. No signal conflicts are allowed.

Table 2.5 I/O Port Functions (3/4)

SH7239		Common ring connector				Application header					
No.	Pin Name	J1	J2	J3	J4	JA1	JA2	JA3	JA5	JA6	Function
55	VSS		25								
56	PD0/D0		26					17			D0
57	PD1/D1		27					18			D1
58	PD2/D2/TIC5U/RXD2		28					19		[14]	D2, TIC5U
59	PD3/D3/TIC5V/TXD2		29					20		[15]	D3, TIC5V
60	PD4/D4/TIC5W/SCK2		30					21		[16]	D4, TIC5W
61	PD5/D5/TIC5US			1				22	[12]		D5, TIC5US
62	PD6/D6/TIC5VS			2				23	[13]		D6, TIC5VS
63	PD7/D7/TIC5WS			3				24	[14]		D7, TIC5WS
64	VCC			4							
65	VSS			5							
66	PB20/AUDATA0			6							
67	PB21/AUDATA1			7							
68	PD8/D8/TIOC3AS/ AUDATA0			8				29	[15]		D8, TIOC3AS
69	PD9/D9/TIOC3CS/ AUDATA1			9				30	(11)		D9, TIOC3CS
70	PD10/D10/TIOC3BS/ AUDATA2			10				31	19		D10, TIOC3BS
71	PD11/D11/TIOC3DS/ AUDATA3			11				32	20		D11, TIOC3DS
72	PD12/D12/TIOC4AS/ $\overline{\text{AUDSYNC}}$			12				33	21		D12, TIOC4AS
73	PD13/D13/TIOC4BS/ AUDCK			13				34	23		D13, TIOC4BS
74	PD14/D14/TIOC4CS			14				35	22		D14, TIOC4CS
75	PD15/D15/TIOC4DS			15				36	24		D15, TIOC4DS
76	VSS			16							
77	VCC			17							
78	PA9/IRQ3/TCLKD/$\overline{\text{CS3}}$ /SSL0/SCK0			18		[23]		(27)			IRQ3, $\overline{\text{CS3}}$
79	PA8/IRQ4/TCLKC/$\overline{\text{CS4}}$ /MISO/RXD1			19			8				RXD1
80	PA7/IRQ5/TCLKB/$\overline{\text{CS5}}$ /MOSI/TXD1			20			(6), [22]				TXD1, TCLKB
81	PA6/IRQ6/TCLKA/$\overline{\text{CS6}}$ /RSPCK/SCK1			21			(10), [21]	(28)			SCLK1,TCLKA, $\overline{\text{CS6}}$
82	PA0/RXD0/$\overline{\text{CS0}}$/CRx0/ IRQ4			22				(45)	(6)		$\overline{\text{CS0}}$, CRx0
83	PA1/TXD0/$\overline{\text{CS1}}$/CTx0/ IRQ5			23					(5), [10]		CTx0, IRQ5

Notes: 1. Brackets [ ] indicate the signals connected to the CPU pin via a device, and zero-ohm resistor (installed).
2. Parentheses ( ) indicate the signals connected to the CPU pin via zero-ohm resistor (NOT installed). Remove or install zero-ohm resistors according to connectors and pins to use. No signal conflicts are allowed.

Table 2.6 I/O Port Functions (4/4)

SH7239		Common ring connector				Application header					
No.	Pin Name	J1	J2	J3	J4	JA1	JA2	JA3	JA5	JA6	Function
84	XTAL			(24)							
85	VSS			25							
86	EXTAL			(26)			(2)				EXTAL
87	NMI			27			3				NMI
88	$\overline{\text{RES}}$			28			[1]				$\overline{\text{RES}}$
89	PLLVSS										
90	PLLVCC										
91	PB18/AUDATA2				1						
92	PB19/AUDATA3				2						
93	VSS				3						
94	FWE/$\overline{\text{ASEBRKAK}}$/$\overline{\text{ASEBRK}}$				4						
95	$\overline{\text{ASEMD0}}$				5						
96	AVREFVSS				6						
97	AVSS				7	6					AVSS
98	PF0/AN0				8	9					AN0
99	PF1/AN1				9	10					AN1
100	PF2/AN2				10	11					AN2
101	PF3/AN3				11	12					AN3
102	AVCC				12	5					AVCC
103	AVREF				13	7					AVREF
104	AVREF				14						
105	AVCC				15						
106	PF4/AN4				16				1		AN4
107	PF5/AN5				17				2		AN5
108	PF6/AN6				18				3		AN6
109	PF7/AN7				19				4		AN7
110	AVSS				20						
111	AVREFVSS				21						
112	PF8/AN8				22	[15]					PF8
113	PF9/AN9				23	[16]					PF9
114	PF10/AN10				24	[17]					PF10
115	PF11/AN11				25	[18]					PF11
116	PF12/AN12				26	[19]					PF12
117	PF13/AN13				27	[20]					PF13
118	PF14/AN14				28	[21]					PF14
119	PF15/AN15				29	[22]					PF15
120	MD0				30						

Notes: 1. Brackets [ ] indicate the signals connected to the CPU pin via a device, and zero-ohm resistor (installed).
2. Parentheses ( ) indicate the signals connected to the CPU pin via zero-ohm resistor (NOT installed). Remove or install zero-ohm resistors according to connectors and pins to use. No signal conflicts are allowed.

2.6 RCAN Interface

The R0K572390 includes a 3-pin RCAN port connector (J9). The SH7239 CTx0 signal (CAN signal) is connected to J9 connector via a zero-ohm resistor and the RCAN transceiver IC, and the CRx0 signal is connected to J9 connector via a zero-ohm resistor, the level shifter, and the RCAN transceiver IC. CTx0 and CRx0 signals are also connected to the application header (JA5), which can be specified instead of using RCAN. When using the application header (JA5), remove zero-ohm resistors between the SH7239 and the RCAN transceiver IC, and install zero-ohm resistors between the SH7239 and the application header (JA5). Do not use CAN signals both at the RCAN port connector and the application header.

SH7239 PA0/RXD0/$\overline{\text{CS0}}$/CRx0/IRQ4 pin is multiplexed with $\overline{\text{CS0}}$ pin. Remove or install zero-ohm resistors to specify the pin function. When specifying the CRx0 pin function to use the RCAN port connector, use the pin as default. To specify the $\overline{\text{CS0}}$ pin function, make sure to remove the zero-ohm resistor R41. RCAN port connector (J9) cannot be used with the $\overline{\text{CS0}}$ pin function. Make sure not to specify PA0/RXD0/$\overline{\text{CS0}}$/CRx0/IRQ4 pin as output when the zero-ohm resistor R41 is installed.

Figure 2.6 shows the RCAN interface block diagram.

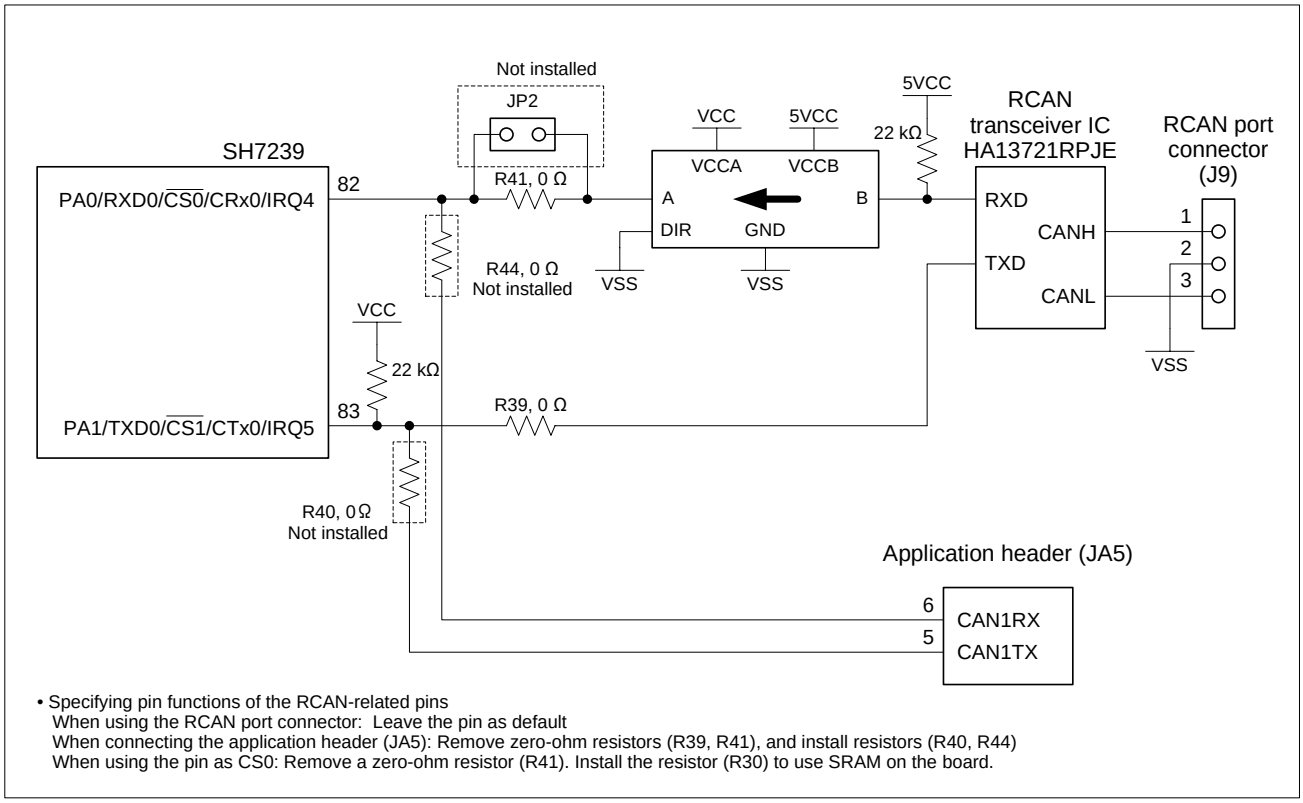


Figure 2.6 RCAN Interface Block Diagram

2.7 LCD Interface

The R0K572390 includes a 14-pin character LCD interface connector (J10). The SH7239 PC2 to PC7 pins control the character LCD module. These pins are also used as address to SRAM (optional) on the R0K572390. Pins PC2 to PC7 are also connected to application headers (JA1, JA3). No signal conflicts are allowed.

Figure 2.7 shows the character LCD interface block diagram.

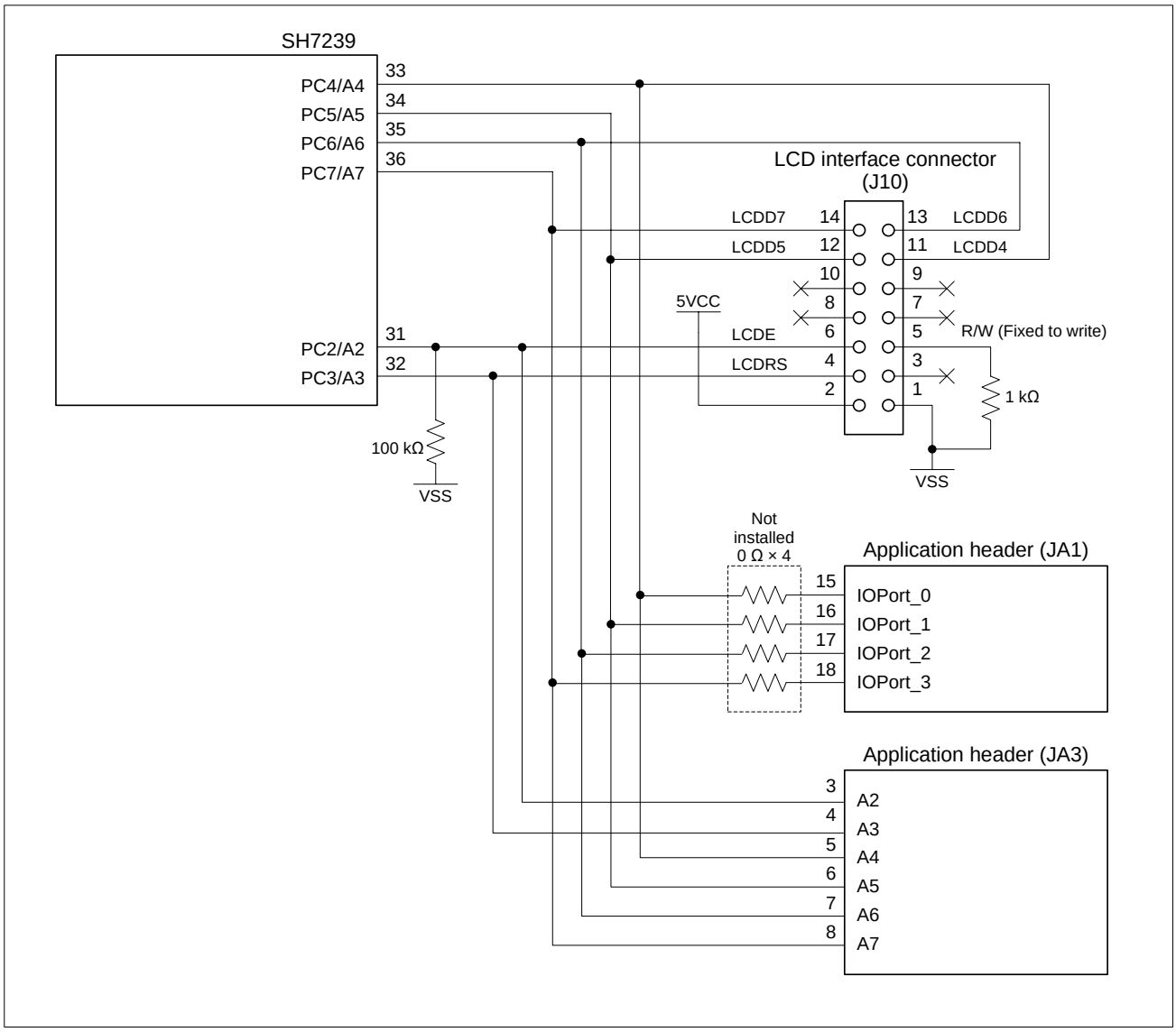


Figure 2.7 LCD Interface Block Diagram

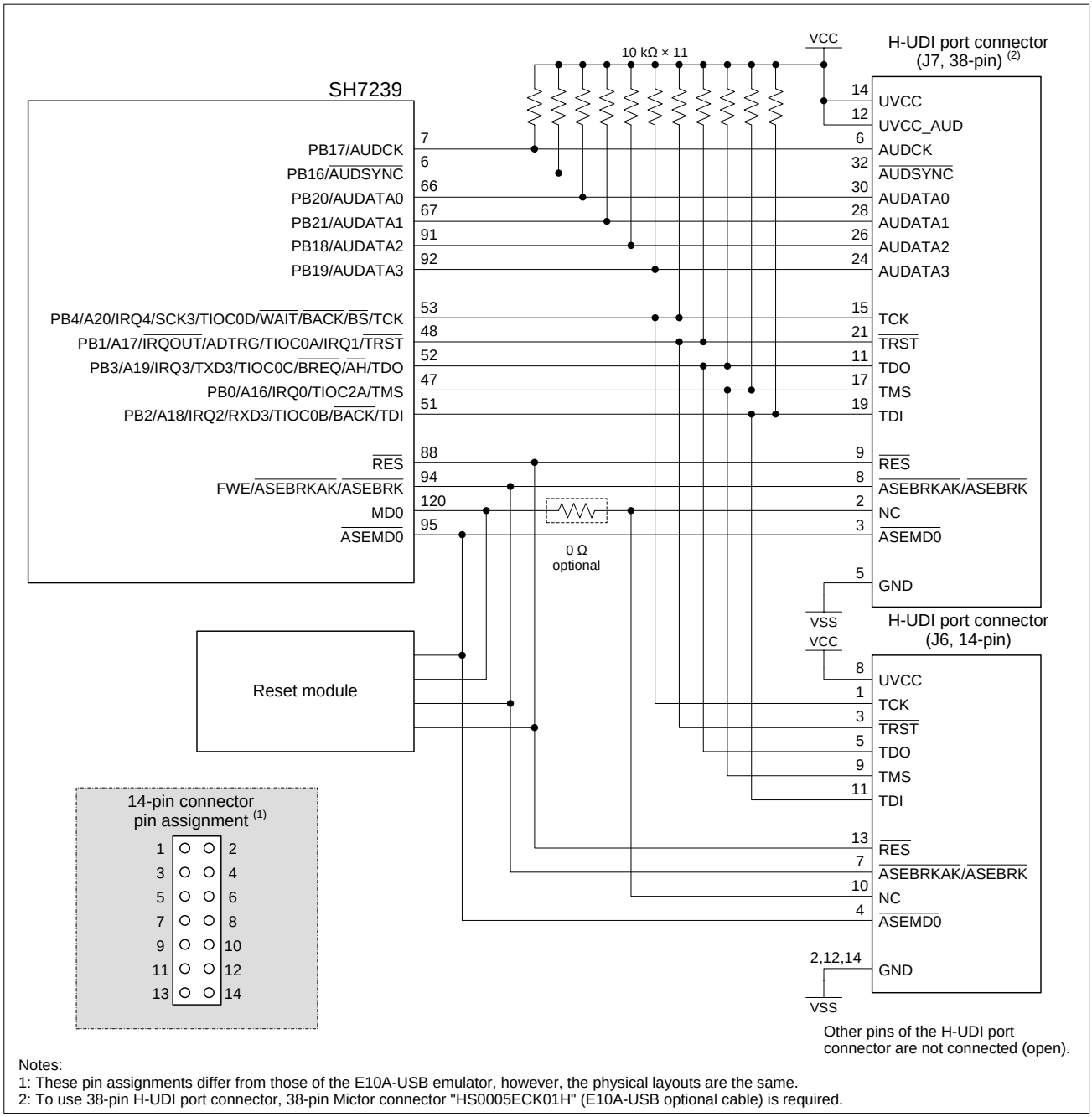
2.8 H-UDI Interface

The R0K572390 includes two H-UDI port connectors (J6, J7) to connect to the E10A-USB emulator.

The SH7239 FWE/$\overline{\text{ASEBRKAK}}$/$\overline{\text{ASEBRK}}$ pin is connected to the reset module. The reset module produces FWE signal logic using the reset switch and user switch SW1 (NMI), and switches signals between FWE and $\overline{\text{ASEBRKAK}}$/$\overline{\text{ASEBRK}}$ using the $\overline{\text{ASEMD0}}$ signal.

JTAG-related signals (TCK, $\overline{\text{TRST}}$, TMS, TDO, and TDI) of the H-UDI-related signals cannot be used as other functions. However, TXD3 and RXD3 signals can be used only in boot mode.

Figure 2.8 shows the H-UDI port connector block diagram.



Notes:
1: These pin assignments differ from those of the E10A-USB emulator, however, the physical layouts are the same.
2: To use 38-pin H-UDI port connector, 38-pin Mictor connector "HS0005ECK01H" (E10A-USB optional cable) is required.

Figure 2.8 H-UDI Port Connector Block Diagram

2.9 Switches and Jumpers

The R0K572390 includes push switches to reset, NMI and IRQ interrupt input, $\overline{\text{ADTRG}}$ input, and DIP switches to set the operating mode. Reset switch and user switch SW1 (NMI) sets the SH7239 programming mode. Refer to 2.13 Reset Module for details on the reset switch circuit and mode setting DIP switches.

User switch SW2 (IRQ3) is connected to PC1/A1/$\overline{\text{ADTRG}}$ pin via a zero-ohm resistor R82 (not installed) and a jumper JP3 (not populated) to multiplex the pin with $\overline{\text{ADTRG}}$ input. When specifying the $\overline{\text{ADTRG}}$ input, install the resistor R82. Make sure not to specify the PC1/A1/$\overline{\text{ADTRG}}$ as output when R82 is installed.

The R0K572390 provides jumpers to select the power supply source, and connects the RCAN signal. For details on jumpers, refer to Chapter 3 Operating Specifications.

Figure 2.9 shows the block diagram of interrupt switches.

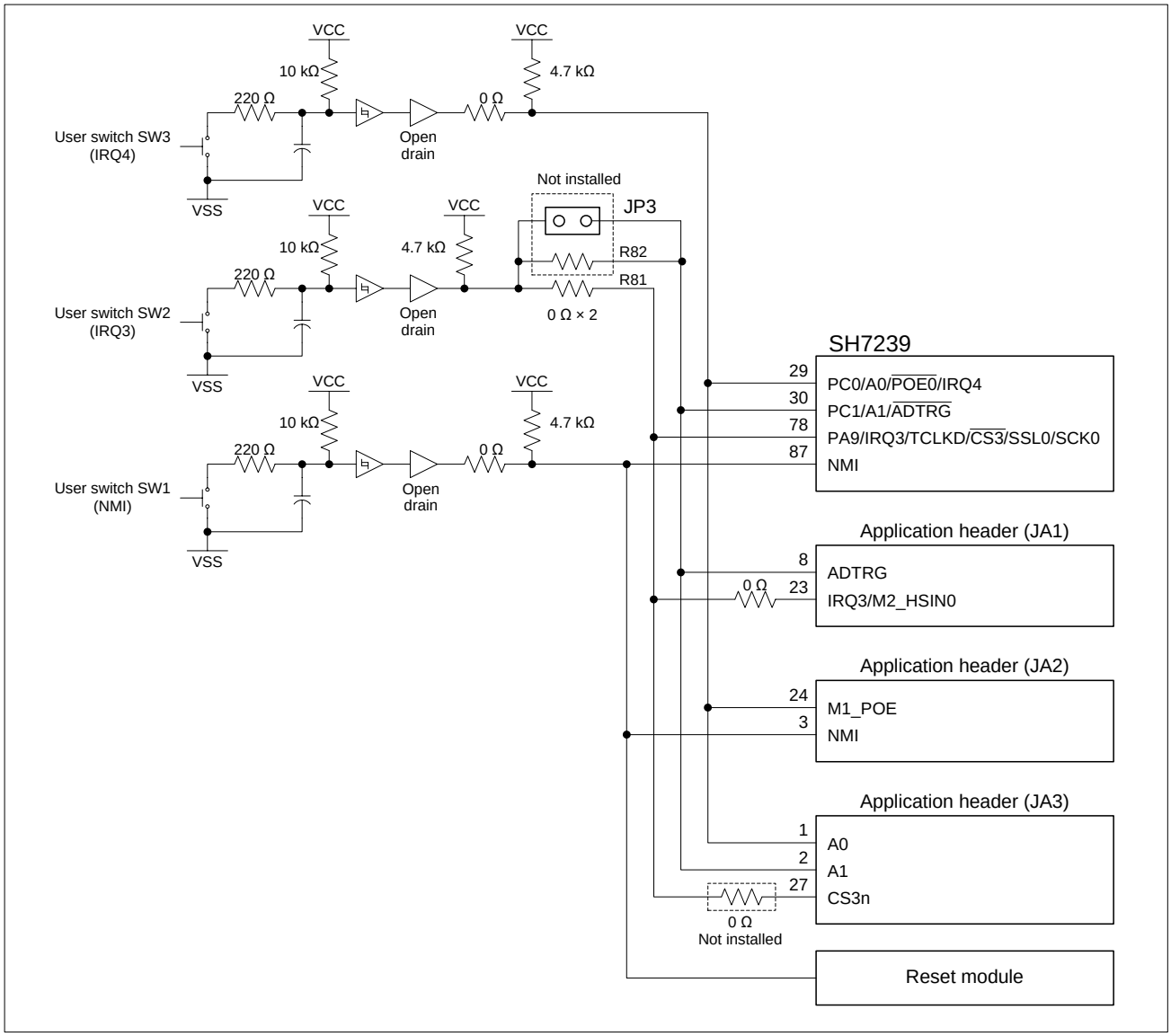


Figure 2.9 Switch Block Diagram

2.10 LEDs and Potentiometer

The R0K572390 includes a power LED (POWER), a boot mode LED (BOOT), and four user LEDs (LED0 to LED3). The POWER indicates the CPU board is ON. The BOOT indicates that the MCU is in boot mode (FWE = "H"). The SH7239 PE12 to PE15 pins control user LEDs. Also, the R0K572390 includes a potentiometer, which is connected to AN8 pin of the SH7239 A/D Converter.

Figure 2.10 shows LED and potentiometer block diagram.

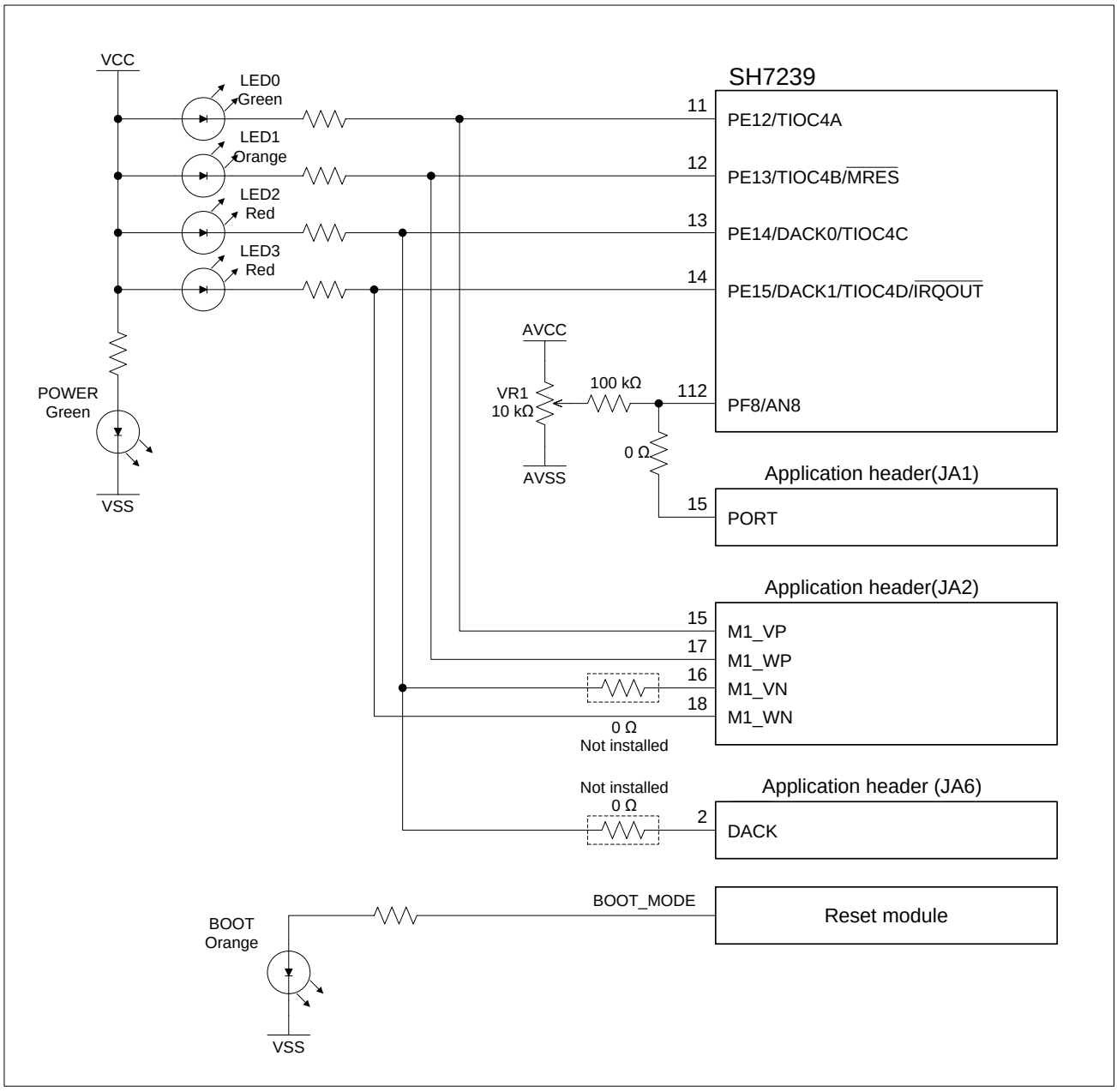


Figure 2.10 LED and Potentiometer Block Diagram

2.11 Power Module

A 5 V power supply is input to the R0K572390, and the regulator on the R0K572390 generates 3.3 V. As it is a step down DC-DC switching regulator, the desired voltage can be generated by changing the resistance value.

As the power select jumper JP1 is not populated by default, VCC is fixed to 3.3 V on the R0K572390C000BR with the SH7239A MCU. On the R0K572390C020BR with the SH7239B, VCC is fixed to 5 V.

The R0K572390 can use a 5 V DC output regulated power supply via the external power supply connector (J11). The SH7239 system power supply (VCC) and analog power supply (AVCC) can be supplied from external source. Apply the power to the system power supply via the external power supply connector (J13), and to the analog power supply via the external power supply (J12). To supply the power to the analog power supply individually, remove the zero-ohm resistor R71 which connects the 5 V power supply and analog power supply. External power supply connectors (J11 to J13) are not installed by default. Figure 2.11 shows the R0K572390 power supply circuit block diagram.

Note: When operating the R0K572390, make sure to apply power from the DC power jack (J5) or external power supply connectors (J11 to J13).

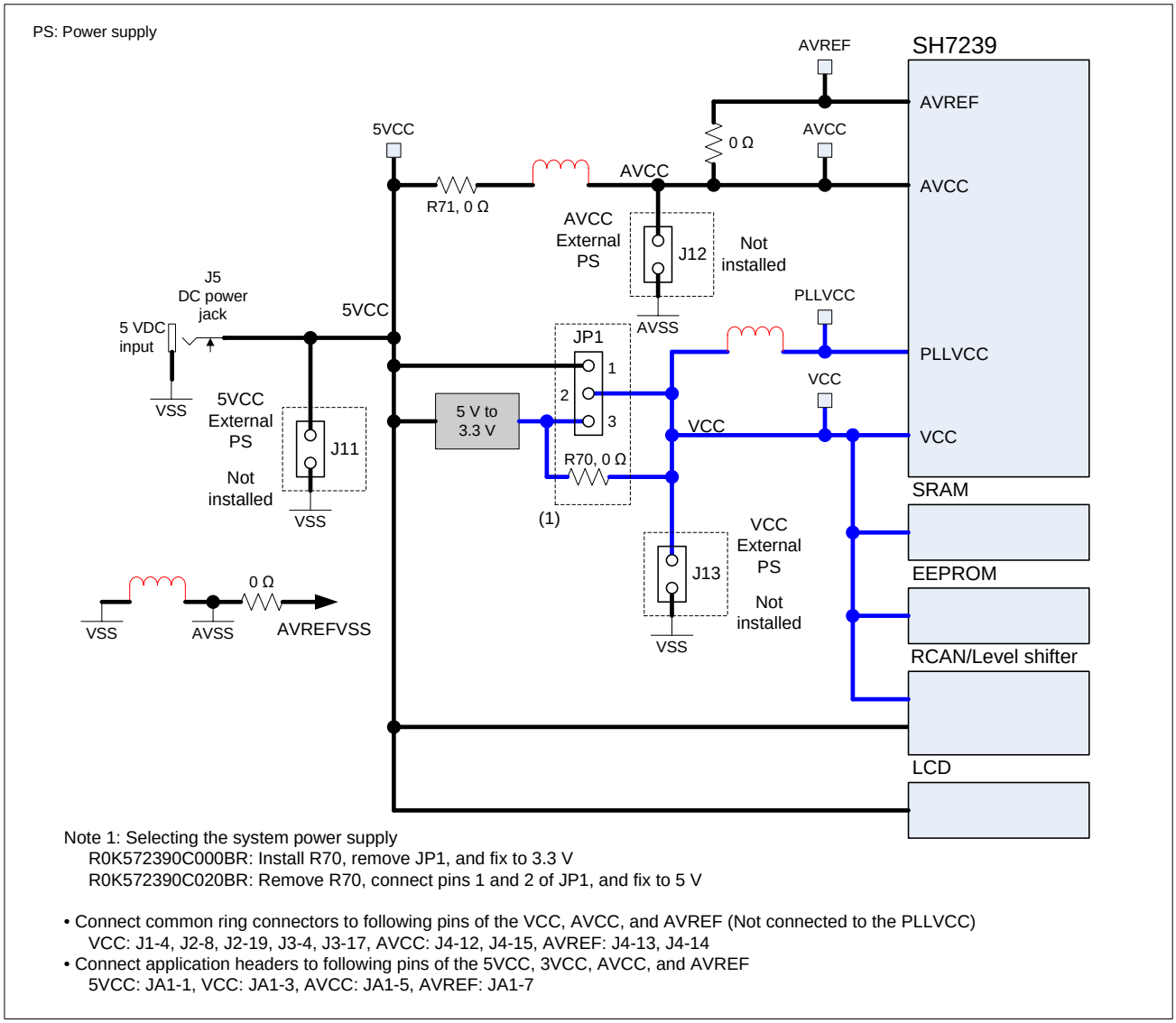


Figure 2.11 Power Supply Circuit Block Diagram

2.12 Clock Module

The R0K572390 connects a 10 MHz or 12.5 MHz crystal unit to SH7239 XTAL and EXTAL pins, according to the type of MCU.

- R0K572390C000BR connects 10 MHz crystal unit
- R0K572390C020BR connects 12.5 MHz crystal unit

Alternatively, an input clock signal can be provided to EXTAL pin via the Application header (JA2). Remove the crystal unit (X1) and install a zero-ohm resistor (R2, not installed by default) to input clock via JA2. Also, install a pull-up resistor (R1) if needed.

Figure 2.12 shows the R0K572390 clock module block diagram.

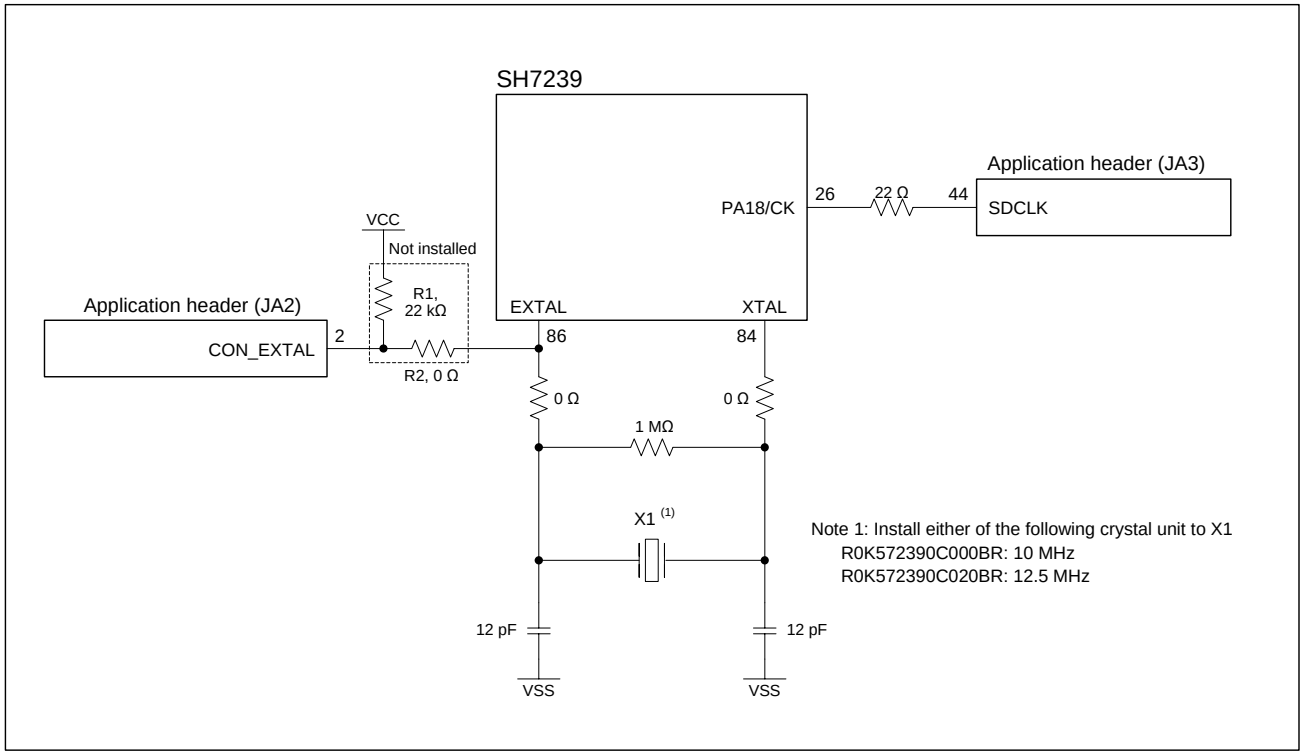


Figure 2.12 Clock Module Block Diagram

2.13 Reset Module

The R0K572390 reset module generates $\overline{\text{RES}}$ signal using the power-on reset, and reset switch. Also, the reset module controls the SH7239 boot mode (FWE signal) using the mode setting DIP switches (SW4), reset switch, user switch SW1 (NMI) and flip-flop, and controls FWE/$\overline{\text{ASEBRKAK}}$/$\overline{\text{ASEBRK}}$ signal using the $\overline{\text{ASEMD0}}$ signal.

For details on how to control SH7239 boot mode and FWE/$\overline{\text{ASEBRKAK}}$/$\overline{\text{ASEBRK}}$ signal, refer to 3.2.2 in Chapter 3 Operating Specifications. Figure 2.13 shows the R0K572390 reset module block diagram.

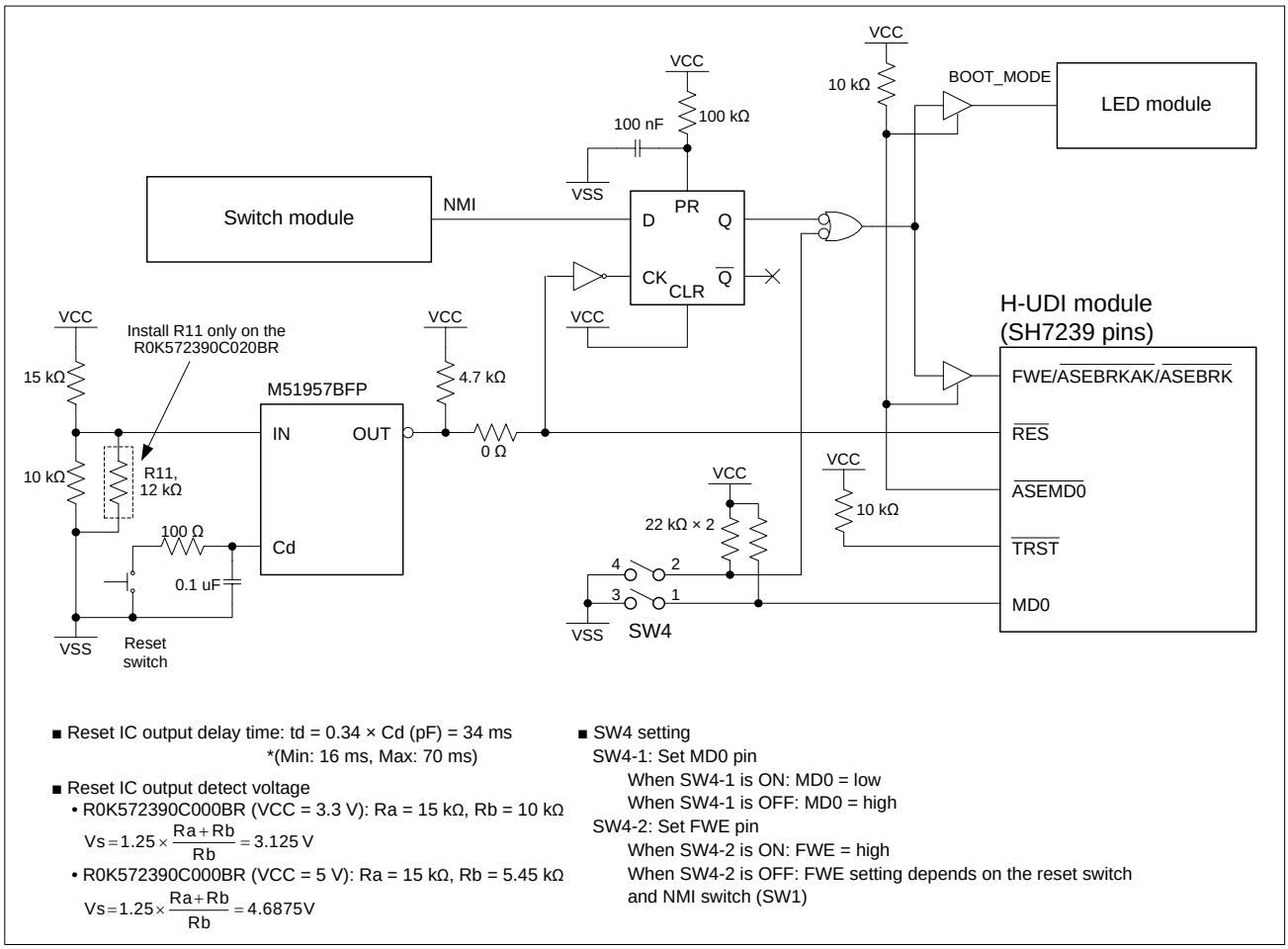
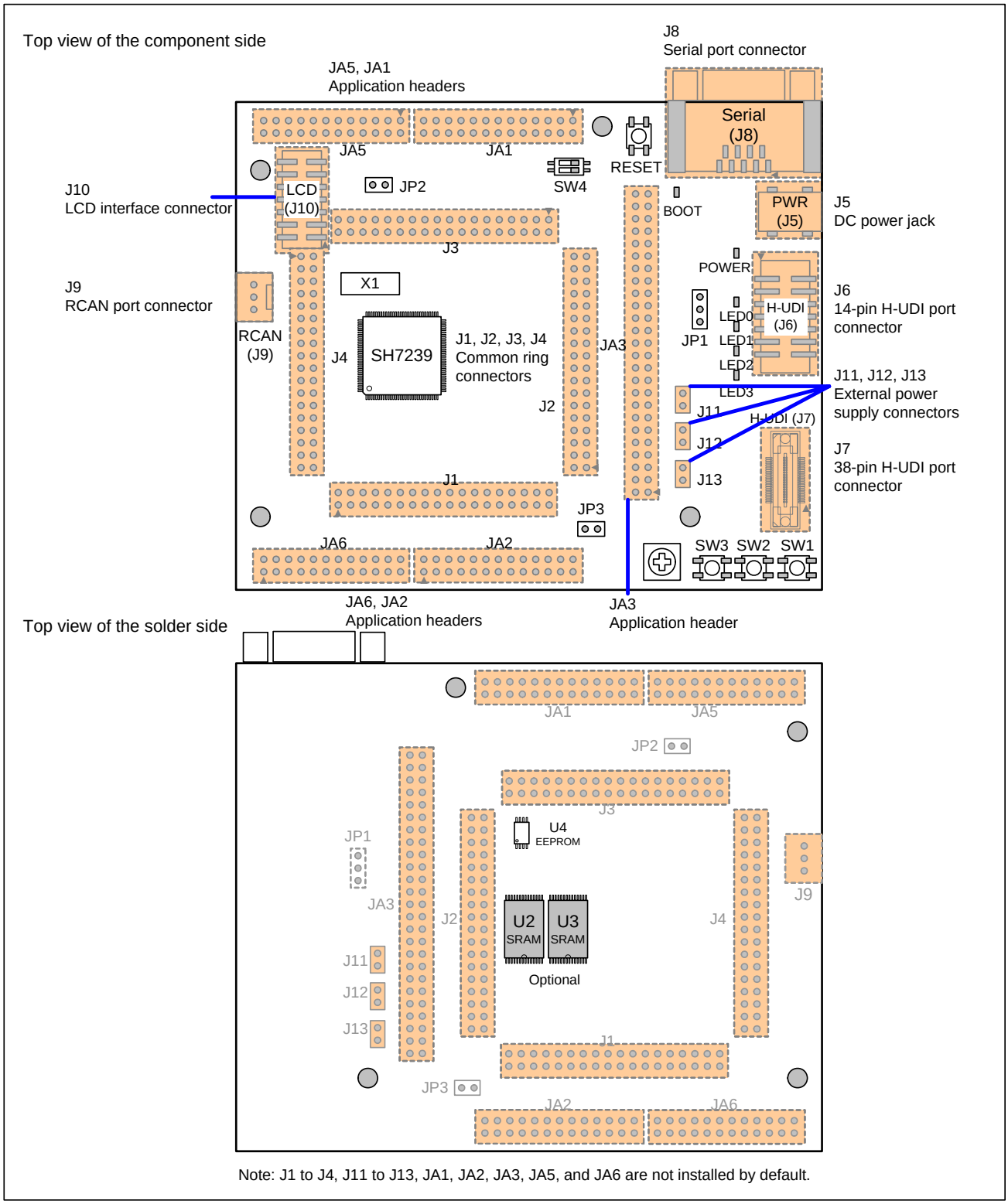


Figure 2.13 Reset Module Block Diagram

3. Operating Specifications

3.1 Connectors

Figure 3.1 shows the connector assignments for the R0K572390.



Note: J1 to J4, J11 to J13, JA1, JA2, JA3, JA5, and JA6 are not installed by default.

Figure 3.1 Connector Assignments

3.1.1 Application Headers (JA1, JA2, JA3, JA5, JA6)

The R0K572390 includes through-holes for mounting application headers (JA1, JA2, JA3, JA5, and JA6). MIL-STD connectors can be connected to through-holes to connect an expansion board.

Figure 3.2 shows the pin assignments for the application headers (top view of the component side).

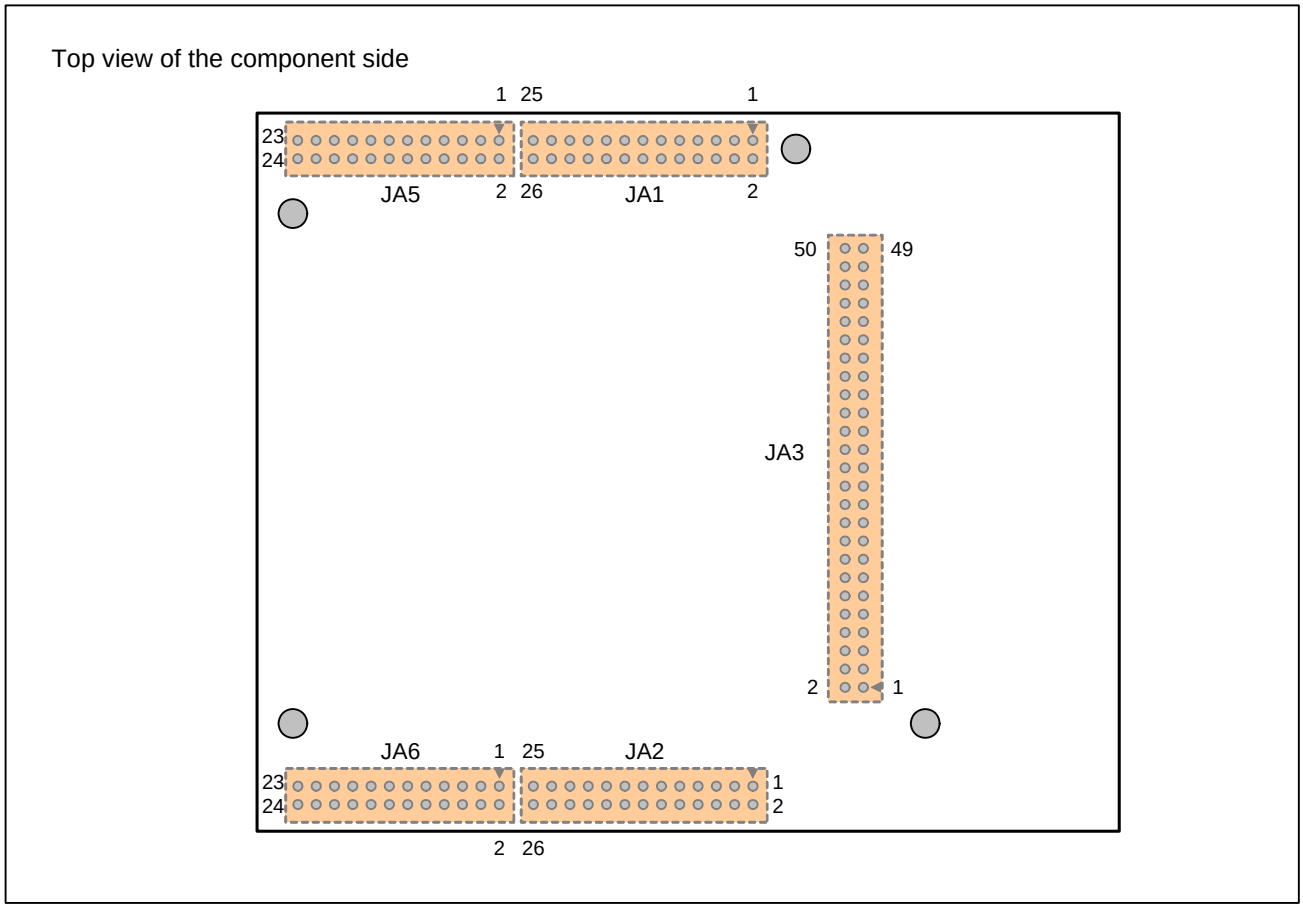


Figure 3.2 Application Header Pin Assignments (Top View of the Component Side)

Table 3.1 lists the pin descriptions for JA1.

Table 3.1 JA1 Pin Descriptions

Pin No.	Signal Name	Pin Function Used
1	5VCC (1)	5VCC
2	GND	GND
3	3VCC (1)	3VCC
4	GND	GND
5	AVCC (1)	AVCC
6	AGND	AGND
7	AVREF (1)	AVREF
8	PC1/A1/$\overline{\text{ADTRG}}$	$\overline{\text{ADTRG}}$
9	PF0/AN0	AN0
10	PF1/AN1	AN1
11	PF2/AN2	AN2
12	PF3/AN3	AN3
13	NC	–
14	NC	–
15	PF8/AN8, (1) PC4/A4 (2)	PF8, PC4
16	PF9/AN9, (1) PC5/A5 (2)	PF9, PC5
17	PF10/AN10, (1) PC6/A6 (2)	PF10, PC6
18	PF11/AN11, (1) PC7/A7 (2)	PF11, PC7
19	PF12/AN12, (1) PC8/A8/CRx0/RXD0/$\overline{\text{POE4}}$ (2)	PF12, PC8
20	PF13/AN13, (1) PC9/A9/CTx0/TXD0/SCK0 (2)	PF13, PC9
21	PF14/AN14, (1) PC10/A10/TIOC1A/CRx0/RXD0 (2)	PF14, PC10
22	PF15/AN15, (1) PC11/A11/TIOC1B/CTx0/TXD0 (2)	PF15, PC11
23	PA9/IRQ3/TCLKD/$\overline{\text{CS3}}$/SSL0/SCK0, (1) PE0/TIOC0A/TIOC4AS/DREQ0 (2)	IRQ3, TIOC0A
24	NC	–
25	NC	–
26	NC	–

Notes: 1. These pins are connected to through-holes via zero-ohm resistors (installed by default).
2. These pins are connected to through-holes via zero-ohm resistors (NOT installed by default).

Table 3.2 lists the pin descriptions for JA2.

Table 3.2 JA2 Pin Descriptions

Pin No.	Signal Name	Pin Function Used
1	RESET	
2	EXTAL (2)	EXTAL
3	NMI	NMI
4	GND	GND
5	$\overline{\text{WDTOVF}}$ (1)	$\overline{\text{WDTOVF}}$
6	PA7/IRQ5/TCLKB/$\overline{\text{CS5}}$/MOSI/TXD1 (2)	TXD1
7	PC13/A13/IRQ0/TCLKB, (1) PE0/TIOC0A/TIOC4AS/DREQ0 (2)	IRQ0, TIOC0A
8	PA8/IRQ4/TCLKC/$\overline{\text{CS4}}$/MISO/RXD1	RXD1
9	PC14/A14/IRQ1/TCLKC, (1) PE1/TIOC0B/TIOC4BS/TEND0 (2)	IRQ1, TIOC0B
10	PA6/IRQ6/TCLKA/$\overline{\text{CS6}}$/RSPCK/SCK1 (2)	SCK1
11	PE10/TIOC3C/TXD2/DREQ3/SSL3 (1)	TIOC3C
12	NC	–
13	PE9/TIOC3B/DACK2	TIOC3B
14	PE11/TIOC3D/DACK3	TIOC3D
15	PE12/TIOC4A	TIOC4A
16	PE14/DACK0/TIOC4C (1)	TIOC4C
17	PE13/TIOC4B/$\overline{\text{MRES}}$	TIOC4B
18	PE15/DACK1/TIOC4D/$\overline{\text{IRQOUT}}$	TIOC4D
19	PE5/TIOC1B/TIOC3BS/TXD3 (1)	TIOC1B
20	PE6/TIOC2A/TIOC3DS/RXD3 (1)	TIOC2A
21	PA6/IRQ6/TCLKA/$\overline{\text{CS6}}$/RSPCK/SCK1 (1)	TCLKA
22	PA7/IRQ5/TCLKB/$\overline{\text{CS5}}$/MOSI/TXD1 (1)	TCLKB
23	PC15/A15/IRQ2/TCLKD, (1) PE4/TIOC1A/SCK3/$\overline{\text{POE8}}$/IRQ4, (2) PE2/TIOC0C/TIOC4CS/DREQ1 (2)	IRQ2, TIOC1A, TIOC0C
24	PC0/A0/$\overline{\text{POE0}}$/IRQ4	$\overline{\text{POE0}}$
25	PC12/A12/TCLKA	TCLKA
26	PC13/A13/IRQ0/TCLKB	TCLKB

Notes: 1. These pins are connected to through-holes via zero-ohm resistors (installed by default).
2. These pins are connected to through-holes via zero-ohm resistors (NOT installed by default).

Table 3.3 and Table 3.4 list the pin descriptions for JA3.

Table 3.3 JA3 Pin Descriptions (1/2)

Pin No.	Signal Name	Pin Function Used
1	PC0/A0/$\overline{\text{POE0}}$/IRQ4	A0
2	PC1/A1/$\overline{\text{ADTRG}}$	A1
3	PC2/A2	A2
4	PC3/A3	A3
5	PC4/A4	A4
6	PC5/A5	A5
7	PC6/A6	A6
8	PC7/A7	A7
9	PC8/A8/CRx0/RXD0/$\overline{\text{POE4}}$	A8
10	PC9/A9/CTx0/TXD0/SCK0	A9
11	PC10/A10/TIOC1A/CRx0/RXD0	A10
12	PC11/A11/TIOC1B/CTx0/TXD0	A11
13	PC12/A12/TCLKA	A12
14	PC13/A13/IRQ0/TCLKB	A13
15	PC14/A14/IRQ1/TCLKC	A14
16	PC15/A15/IRQ2/TCLKD	A15
17	PD0/D0	D0
18	PD1/D1	D1
19	PD2/D2/TIC5U/RXD2	D2
20	PD3/D3/TIC5V/TXD2	D3
21	PD4/D4/TIC5W/SCK2	D4
22	PD5/D5/TIC5US	D5
23	PD6/D6/TIC5VS	D6
24	PD7/D7/TIC5WS	D7
25	PA17/$\overline{\text{RD}}$	$\overline{\text{RD}}$
26	NC	–
27	PA9/IRQ3/TCLKD/$\overline{\text{CS3}}$/SSL0/SCK0 (1)	$\overline{\text{CS3}}$
28	PA6/IRQ6/TCLKA/$\overline{\text{CS6}}$/RSPCK/SCK1 (1)	$\overline{\text{CS6}}$
29	PD8/D8/TIOC3AS/AUDATA0	D8
30	PD9/D9/TIOC3CS/AUDATA1	D9
31	PD10/D10/TIOC3BS/AUDATA2	D10
32	PD11/D11/TIOC3DS/AUDATA3	D11
33	PD12/D12/TIOC4AS/$\overline{\text{AUDSYNC}}$	D12
34	PD13/D13/TIOC4BS/AUDCK	D13
35	PD14/D14/TIOC4CS	D14
36	PD15/D15/TIOC4DS	D15

Note: 1. These pins are connected to through-holes via zero-ohm resistors (NOT installed by default).

Table 3.4 JA3 Pin Descriptions (2/2)

Pin No.	Signal Name	Pin Function Used
37	PB0/A16/IRQ0/TIOC2A/TMS (3)	A16
38	PB1/A17/IRQOUT/ADTRG/TIOC0A/IRQ1/TRST (3)	A17
39	PB2/A18/IRQ2/RXD3/TIOC0B/BACK/TDI (3)	A18
40	PB3/A19/IRQ3/TXD3/TIOC0C/BREQ/AH/TDO (3)	A19
41	PB4/A20/IRQ4/SCK3/TIOC0D/WAIT/BACK/BS/TCK (3)	A20
42	NC	–
43	NC	–
44	PA18/CK	CK
45	PA0/RXD0/CS0/CRx0/IRQ4, (2) PB4/A20/IRQ4/SCK3/TIOC0D/WAIT/BACK/BS/TCK (3)	CS0, WAIT
46	PB3/A19/IRQ3/TXD3/TIOC0C/BREQ/AH/TDO (3)	AH
47	PA15/WRH	WRH
48	PA16/WRL	WRL
49	NC	–
50	NC	–

Notes: 1. These pins are connected to through-holes via zero-ohm resistors (installed by default)
2. These pins are connected to through-holes via zero-ohm resistors (NOT installed by default).
3. These pins are connected to through-holes via zero-ohm resistors (NOT installed by default). As these pins are multiplexed with H-UDI JTAG signals, these pins cannot be used when using the emulator.

Table 3.5 lists the pin descriptions for JA5.

Table 3.5 JA5 Pin Descriptions

Pin No.	Signal Name	Pin Function Used
1	PF4/AN4	AN4
2	PF5/AN5	AN5
3	PF6/AN6	AN6
4	PF7/AN7	AN7
5	PA1/TXD0/$\overline{CS1}$/CTx0/IRQ5 (2)	CTx0
6	PA0/RXD0/$\overline{CS0}$/CRx0/IRQ4 (2)	CRx0
7	NC	–
8	NC	–
9	PE4/TIOC1A/SCK3/$\overline{POE8}$/IRQ4, (1) PE1/TIOC0B/TIOC4BS/TEND0 (2)	IRQ4, TIOC1A TIOC0B
10	PA1/TXD0/$\overline{CS1}$/CTx0/IRQ5, (1) PE2/TIOC0C/TIOC4CS/DREQ1 (2)	IRQ5, TIOC0O
11	PD9/D9/TIOC3CS/AUDATA1 (2)	TIOC3CS
12	PD5/D5/TIC5US, (1) PE4/TIOC1A/SCK3/$\overline{POE8}$/IRQ4, (2)	TIC5US, TIOC1A
13	PD6/D6/TIC5VS, (1) PE6/TIOC2A/TIOC3DS/RXD3 (2)	TIC5VS, TIOC2A
14	PD7/D7/TIC5WS, (1) PE3/TIOC0D/TIOC4DS/TEND1 (2)	TIC5WS, TIOC0D
15	PD8/D8/TIOC3AS/AUDATA0 (1)	TIOC3AS
16	PC8/A8/CRx0/RXD0/$\overline{POE4}$	$\overline{POE4}$
17	PC14/A14/IRQ1/TCLKC (2)	TCLKC
18	PC15/A15/IRQ2/TCLKD (2)	TCLKD
19	PD10/D10/TIOC3BS/AUDATA2	TIOC3BS
20	PD11/D11/TIOC3DS/AUDATA3	TIOC3DS
21	PD12/D12/TIOC4AS/$\overline{AUDSYNC}$	TIOC4AS
22	PD14/D14/TIOC4CS	TIOC4CS
23	PD13/D13/TIOC4BS/AUDCK	TIOC4BS
24	PD15/D15/TIOC4DS	TIOC4DS

Notes: 1. These pins are connected to through-holes via zero-ohm resistors (installed by default).
2. These pins are connected to through-holes via zero-ohm resistors (NOT installed by default).

Table 3.6 lists the pin descriptions for JA6.

Table 3.6 JA6 Pin Descriptions

Pin No.	Signal Name	Pin Function Used
1	PE0/TIOC0A/TIOC4AS/DREQ0 (2)	DREQ0
2	PE14/DACK0/TIOC4C (2)	DACK0
3	PE1/TIOC0B/TIOC4BS/TEND0 (2)	TEND0
4	NC	–
5	–	RS232TX
6	–	RS232RX
7	PE7/TIOC2B/$\overline{\text{UBCTRG}}$/RXD2/SSL1 (2)	RXD2
8	PE10/TIOC3C/TXD2/DREQ3/SSL3 (2)	TXD2
9	PE5/TIOC1B/TIOC3BS/TXD3 (2)	TXD3
10	PE8/TIOC3A/SCK2/DREQ2/SSL2 (2)	SCK2
11	PE4/TIOC1A/SCK3/$\overline{\text{POE8}}$/IRQ4 (2)	SCK3
12	PE6/TIOC2A/TIOC3DS/RXD3 (2)	RXD3
13	PE8/TIOC3A/SCK2/DREQ2/SSL2 (1)	TIOC3A
14	PD2/D2/TIC5U/RXD2, (1) PE4/TIOC1A/SCK3/$\overline{\text{POE8}}$/IRQ4 (2)	TIC5U, TIOC1A
15	PD3/D3/TIC5V/TXD2, (1) PE6/TIOC2A/TIOC3DS/RXD3 (2)	TIC5V, TIOC2A
16	PD4/D4/TIC5W/SCK2, (1) PE3/TIOC0D/TIOC4DS/TEND1 (2)	TIC5W, TIOC0D
17	NC	–
18	NC	–
19	NC	–
20	NC	–
21	NC	–
22	NC	–
23	NC	–
24	–	VSS

Notes: 1. These pins are connected to through-holes via zero-ohm resistors (installed by default).
2. These pins are connected to through-holes via zero-ohm resistors (NOT installed by default)

3.1.2 Common Ring Connectors (J1, J2, J3, J4)

The R0K572390 includes through-holes for installing common ring connectors (J1, J2, J3, and J4). These through-holes are connected to all the SH7239 signals, and MIL-STD connectors can be connected to through-holes to monitor SH7239 signals.

Figure 3.3 shows the pin assignment for the common ring connectors. Table 3.7 to Table 3.10 lists pin descriptions for common ring connectors.

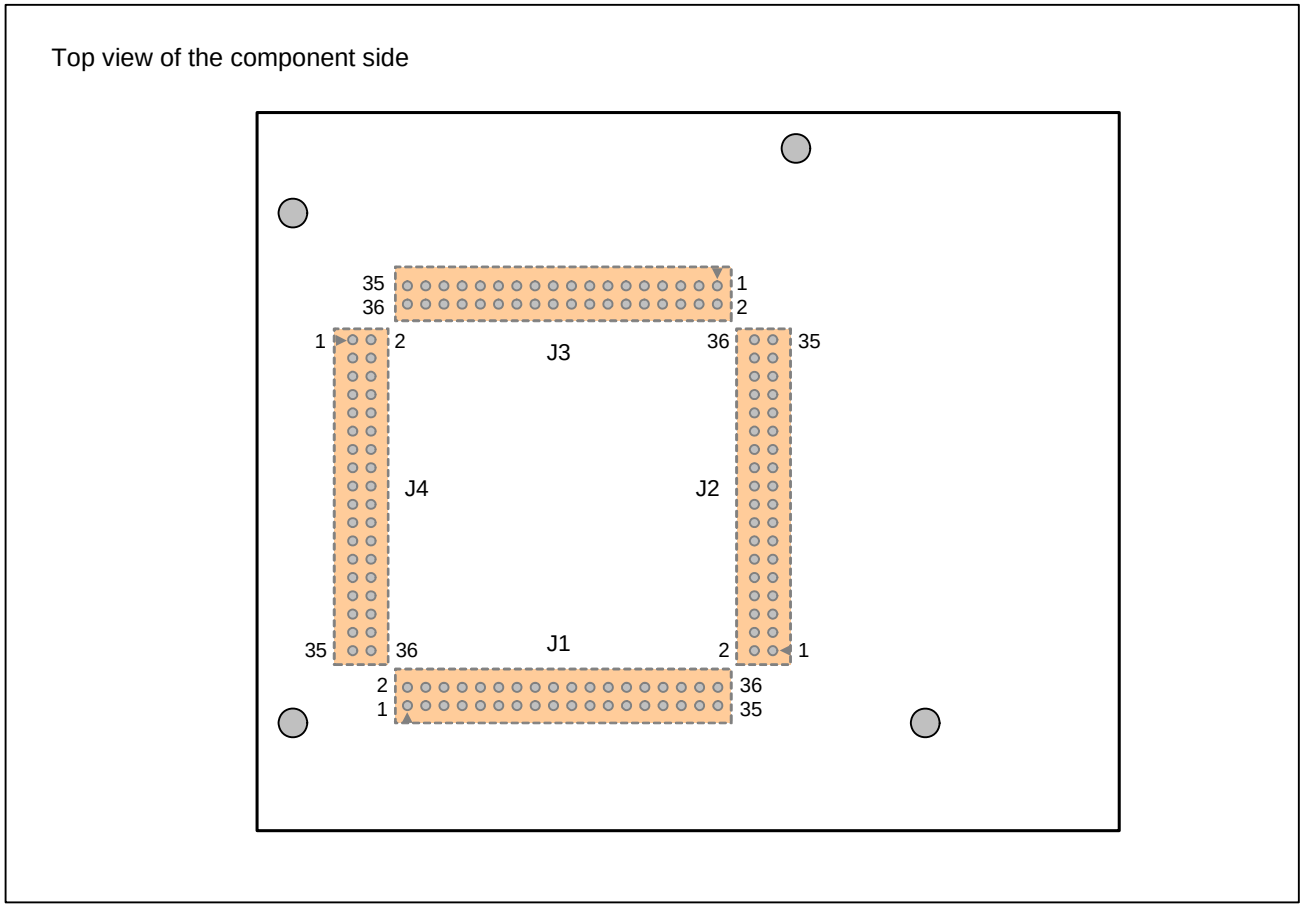


Figure 3.3 Common Ring Connector Pin Assignments (Top View of the Component Side)

Table 3.7 J1 Pin Descriptions

Pin No.	Signal Name	Pin No.	Signal Name
1	WDTOVF	2	PE7/TIOC2B/UBCTRG/RXD2/SSL1
3	PE8/TIOC3A/SCK2/DREQ2/SSL2	4	VCC
5	VSS	6	PB16/AUDSYNC
7	PB17/AUDCK	8	PE10/TIOC3C/TXD2/DREQ3/SSL3
9	PE9/TIOC3B/DACK2	10	PE11/TIOC3D/DACK3
11	PE12/TIOC4A	12	PE13/TIOC4B/MRES
13	PE14/DACK0/TIOC4C	14	PE15/DACK1/TIOC4D/IRQOUT
15	VSS	16	PE0/TIOC0A/TIOC4AS/DREQ0
17	PE1/TIOC0B/TIOC4BS/TEND0	18	PE2/TIOC0C/TIOC4CS/DREQ1
19	PE3/TIOC0D/TIOC4DS/TEND1	20	PE4/TIOC1A/SCK3/POE8/IRQ4
21	PE5/TIOC1B/TIOC3BS/TXD3	22	PE6/TIOC2A/TIOC3DS/RXD3
23	PA17/RD	24	NC
25	VSS	26	PA18/CK
27	PA16/WRL	28	PA15/WRH
29	PC0/A0/POE0/IRQ4	30	PC1/A1/ADTRG
31	NC	32	NC
33	NC	34	NC
35	NC	36	NC

Table 3.8 J2 Pin Descriptions

Pin No.	Signal Name	Pin No.	Signal Name
1	PC2/A2	2	PC3/A3
3	PC4/A4	4	PC5/A5
5	PC6/A6	6	PC7/A7
7	VSS	8	VCC
9	PC8/A8/CRx0/RXD0/POE4	10	PC9/A9/CTx0/TXD0/SCK0
11	PC10/A10/TIOC1A/CRx0/RXD0	12	PC11/A11/TIOC1B/CTx0/TXD0
13	PC12/A12/TCLKA	14	PC13/A13/IRQ0/TCLKB
15	PC14/A14/IRQ1/TCLKC	16	PC15/A15/IRQ2/TCLKD
17	PB0/A16/IRQ0/TIOC2A/TMS	18	PB1/A17/IRQOUT/ADTRG/TIOC0A/IRQ1/TRST
19	VCC	20	VSS
21	PB2/A18/IRQ2/RXD3/TIOC0B/BACK/TDI	22	PB3/A19/IRQ3/TXD3/TIOC0C/BREQ/AH/TDO
23	PB4/A20/IRQ4/SCK3/TIOC0D/WAIT/BACK/BS/TCK	24	NC
25	VSS	26	PD0/D0
27	PD1/D1	28	PD2/D2/TIC5U/RXD2
29	PD3/D3/TIC5V/TXD2	30	PD4/D4/TIC5W/SCK2
31	NC	32	NC
33	NC	34	NC
35	NC	36	NC

Table 3.9 J3 Pin Descriptions

Pin No.	Signal Name	Pin No.	Signal Name
1	PD5/D5/TIC5US	2	PD6/D6/TIC5VS
3	PD7/D7/TIC5WS	4	VCC
5	VSS	6	PB20/AUDATA0
7	PB21/AUDATA1	8	PD8/D8/TIOC3AS/AUDATA0
9	PD9/D9/TIOC3CS/AUDATA1	10	PD10/D10/TIOC3BS/AUDATA2
11	PD11/D11/TIOC3DS/AUDATA3	12	PD12/D12/TIOC4AS/$\overline{\text{AUDSYNC}}$
13	PD13/D13/TIOC4BS/AUDCK	14	PD14/D14/TIOC4CS
15	PD15/D15/TIOC4DS	16	VSS
17	VCC	18	PA9/IRQ3/TCLKD/$\overline{\text{CS3}}$/SSL0/SCK0
19	PA8/IRQ4/TCLKC/$\overline{\text{CS4}}$/MISO/RXD1	20	PA7/IRQ5/TCLKB/$\overline{\text{CS5}}$/MOSI/TXD1
21	PA6/IRQ6/TCLKA/$\overline{\text{CS6}}$/RSPCK/SCK1	22	PA0/RXD0/$\overline{\text{CS0}}$/CRx0/IRQ4
23	PA1/TXD0/$\overline{\text{CS1}}$/CTx0/IRQ5	24	XTAL (1)
25	VSS	26	EXTAL (1)
27	NMI	28	$\overline{\text{RES}}$
29	NC	30	NC
31	NC	32	NC
33	NC	34	NC
35	NC	36	NC

Note: 1. These pins are connected to through-holes via zero-ohm resistors (NOT installed by default).

Table 3.10 J4 Pin Descriptions

Pin No.	Signal Name	Pin No.	Signal Name
1	PB18/AUDATA2	2	PB19/AUDATA3
3	VSS	4	FWE/$\overline{\text{ASEBRKAK}}$/$\overline{\text{ASEBRK}}$
5	$\overline{\text{ASEMD0}}$	6	AVREFVSS
7	AVSS	8	PF0/AN0
9	PF1/AN1	10	PF2/AN2
11	PF3/AN3	12	AVCC
13	AVREF	14	AVREF
15	AVCC	16	PF4/AN4
17	PF5/AN5	18	PF6/AN6
19	PF7/AN7	20	AVSS
21	AVREFVSS	22	PF8/AN8
23	PF9/AN9	24	PF10/AN10
25	PF11/AN11	26	PF12/AN12
27	PF13/AN13	28	PF14/AN14
29	PF15/AN15	30	MD0
31	NC	32	NC
33	NC	34	NC
35	NC	36	NC

3.1.3 DC Power Jack (J5)

The R0K572390 includes a DC power jack (J5).

Figure 3.4 shows the pin assignments for J5. Table 3.11 lists pin descriptions for J5.

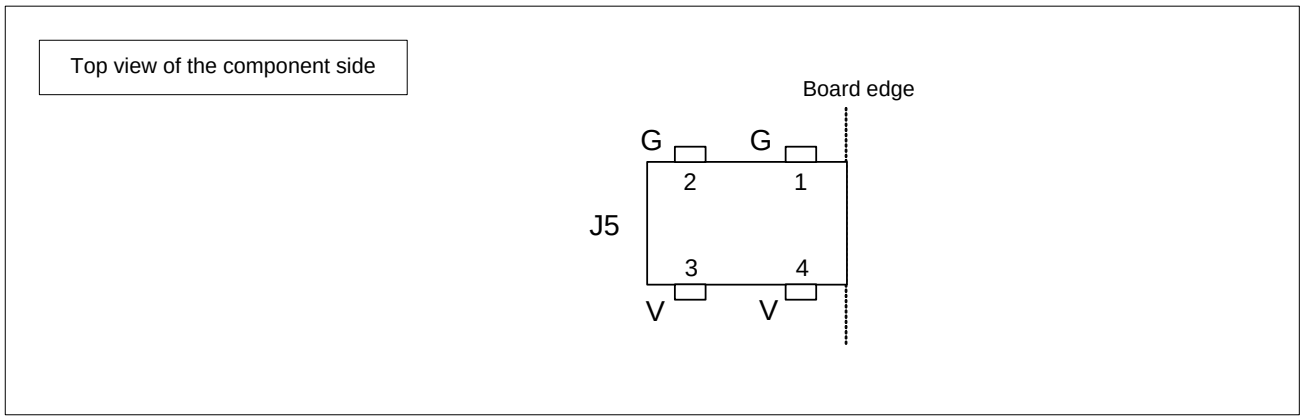


Figure 3.4 J5 Pin Assignments

Table 3.11 J5 Pin Descriptions

Pin No.	Signal Name
1	GND
2	GND
3	+5 V
4	+5 V

3.1.4 H-UDI Port Connectors (J6 and J7)

The R0K572390 includes 14-pin (J6) and 38-pin (J7) H-UDI port connectors to connect E10A-USB emulator.

Figure 3.5 shows the pin assignments for J6 and J7. Table 3.12 and Table 3.13 list the pin descriptions for J6 and J7.

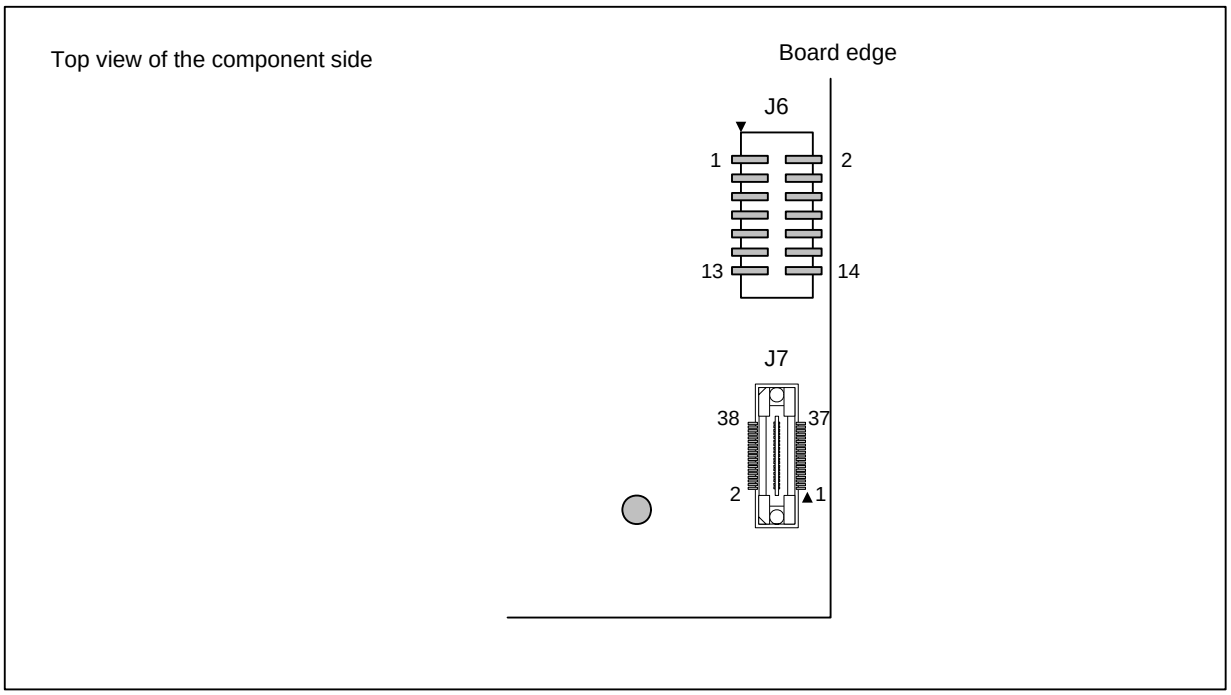


Figure 3.5 J6 and J7 Pin Assignments

Table 3.12 J6 Pin Descriptions

Pin No.	Signal Name	Pin No.	Signal Name
1	TCK	2	GND
3	$\overline{\text{TRST}}$	4	$\overline{\text{ASEMD0}}$
5	TDO	6	NC
7	$\overline{\text{ASEBRKAK}}$/$\overline{\text{ASEBRK}}$	8	UVCC
9	TMS	10	NC
11	TDI	12	GND
13	$\overline{\text{RES}}$	14	GND

Note: Pin assignments for 14-pin H-UDI port connector (J6) differ from those of the E10A-USB emulator, however, the physical layouts are the same.

Table 3.13 J7 Pin Descriptions

Pin No.	Signal Name	Pin No.	Signal Name
1	NC	2	NC
3	$\overline{\text{ASEMD0}}$	4	NC
5	GND	6	AUDCK
7	NC	8	$\overline{\text{ASEBRKAK}}$/$\overline{\text{ASEBRK}}$
9	$\overline{\text{RES}}$	10	NC
11	TDO	12	UVCC_AUD
13	NC	14	UVCC
15	TCK	16	NC
17	TMS	18	NC
19	TDI	20	NC
21	$\overline{\text{TRST}}$	22	NC
23	NC	24	AUDATA3
25	NC	26	AUDATA2
27	NC	28	AUDATA1
29	NC	30	AUDATA0
31	NC	32	$\overline{\text{AUDSYNC}}$
33	NC	34	NC
35	NC	36	NC
37	NC	38	NC

Note: To use 38-pin H-UDI port connector, a user interface cable for 38-pin Mictor connector "HS0005ECK01H" (E10A-USB optional cable) is required.

3.1.5 Serial Port Connector (J8)

The R0K572390 includes a serial port connector (J8). J8 connector has two options for wiring on the R0K572390, using a male jack with the crossover cable, or a female socket with the straight cable by removing and installing zero-ohm resistors R49, R54, R55, R56, R58, R61, R63, R65, and R66 as appropriate. The R0K572390 installs resistors R54, R56, R58, R61, and R66 to include a male jack with crossover cable by default.

Figure 3.6 shows the pin assignments for J8. Table 3.14 lists the pin descriptions for J8. These are pin assignments and descriptions for using a male jack with crossover cable by default.

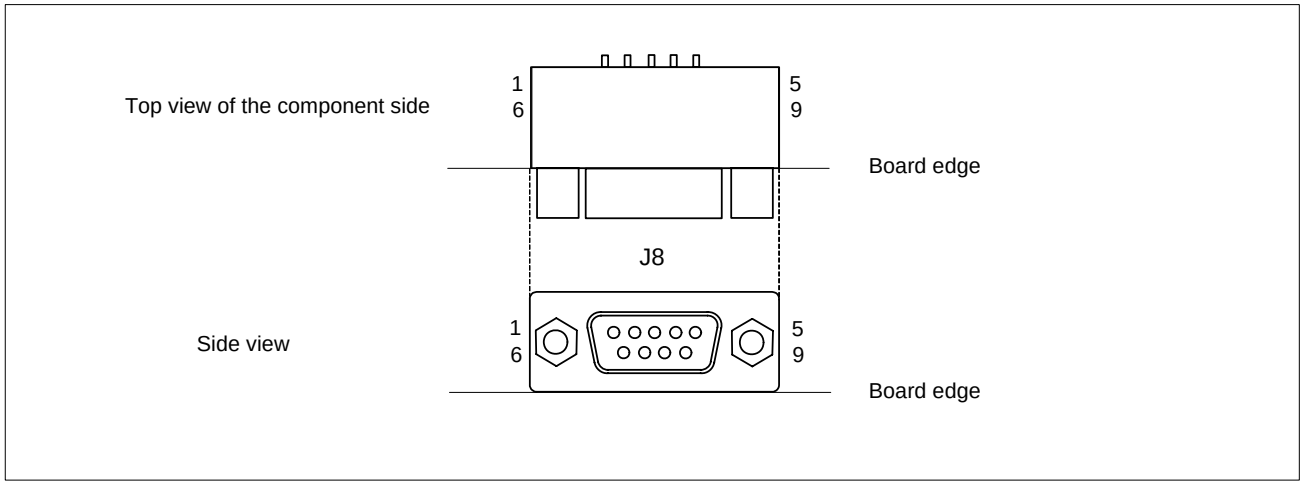


Figure 3.6 J8 Pin Assignments

Table 3.14 J8 Pin Descriptions

Pin No.	Signal Name	Pin No.	Signal Name
1	NC	6	DSR
2	RXD	7	RTS
3	TXD	8	CTS
4	DTR	9	NC
5	GND		

Note: Pins 4 to 6, and 7 to 8 are loopback-connected, respectively.

3.1.6 RCAN Port Connector (J9)

The R0K572390 includes an RCAN port connector (J9) to support RCAN transmission and reception.

Figure 3.7 shows the pin assignments for J9. Table 3.15 lists the pin descriptions for J8.

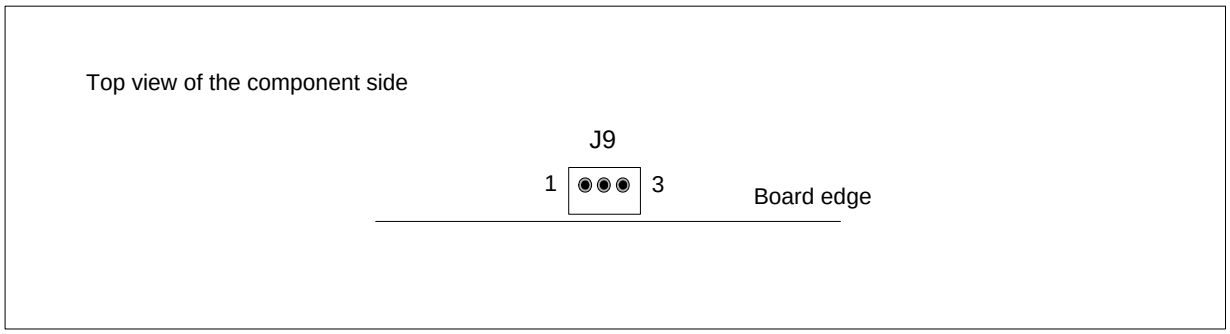


Figure 3.7 J9 Pin Assignments

Table 3.15 J9 Pin Descriptions

Pin No.	Signal Name
1	CANH (U11)
2	GND
3	CANL (U11)

Note: The SH7239 PA0/RXD0/$\overline{CS0}$/CRx0/IRQ4 pin is also used as $\overline{CS0}$ pin. Install the zero-ohm resistor R41 to switch the pin function. To use PA0 pin as CRx0 by the RCAN port connector (J9) to communicate, R41 should be installed. Remove R41 to use the pin as other functions such as $\overline{CS0}$, and RCAN port connector cannot be used.

3.1.7 LCD Interface Connector (J10)

The R0K572390 includes an LCD interface connector (J10).

Figure 3.8 shows the pin assignments for J10. Table 3.16 lists the pin descriptions for J10.

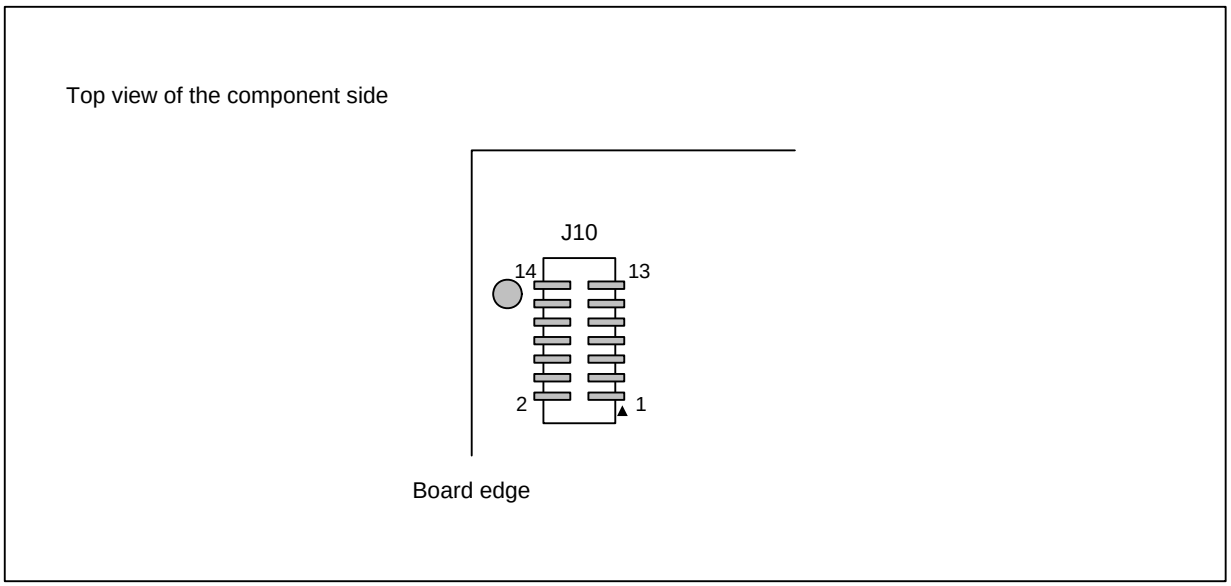


Figure 3.8 J10 Pin Assignments

Table 3.16 J10 Pin Descriptions

Pin No.	Signal Name	Pin No.	Signal Name
1	GND	2	5VCC
3	NC	4	PC3/A3
5	R/W (Pulled down by a 1 kΩ resistor)	6	PC2/A2
7	NC	8	NC
9	NC	10	NC
11	PC4/A4	12	PC5/A5
13	PC6/A6	14	PC7/A7

3.1.8 External Power Supply Connectors (J11, J12, J13)

The R0K572390 includes three external power supply connectors to apply 5 V digital, 3.3 V digital and 5 V analog power from external source, not via the DC power jack (J5). J11 to J13 connectors are not installed by default. The R0K572390 is applied 5 V power from J11 connector, instead of DC power jack by default. Alternatively, remove a zero-ohm resistor R71 to supply 5 V analog power from J11 connector to the board, or remove a zero-ohm resistor R70 to supply 3.3 V digital from J13 connector to the board.

Figure 3.9 shows the pin assignments for external power supply connectors. Table 3.17 to Table 3.19 list the pin descriptions for external power supply connectors.

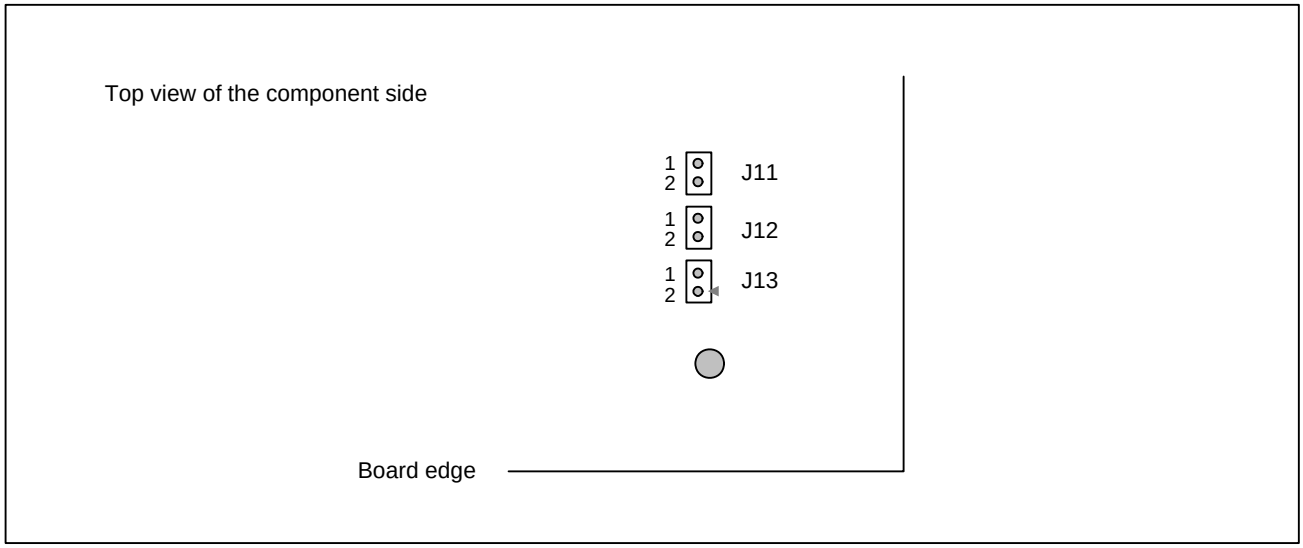


Figure 3.9 External Power Supply Connectors Pin Assignments

Table 3.17 J11 Pin Descriptions

Pin No.	Signal Name	Pin No.	Signal Name
1	5VCC	2	GND

Note: When supplying 5VCC from J11, do not use DC power jack (J5) to supply the power to the board. The R0K572390 may be destroyed when the power is supplied both from J5 and J11.

Table 3.18 J12 Pin Descriptions

Pin No.	Signal Name	Pin No.	Signal Name
1	AVCC	2	AVSS

Note: When supplying AVCC from J12, make sure to remove the zero-ohm resistor R71. The R0K572390 may be destroyed when AVCC is supplied from J12 with R71 installed.

Table 3.19 J13 Pin Descriptions

Pin No.	Signal Name	Pin No.	Signal Name
1	VCC	2	GND

Note: When supplying VCC from J13 on the R0K572390C000BR, make sure to remove the zero-ohm resistor R70. The R0K572390 may be destroyed when VCC is supplied from J13 with R70 installed.

3.2 Operating Components

The R0K572390 includes switches, jumpers, LEDs, and a potentiometer as operating components.

Figure 3.10 shows the assignments of the R0K572390 operating components.

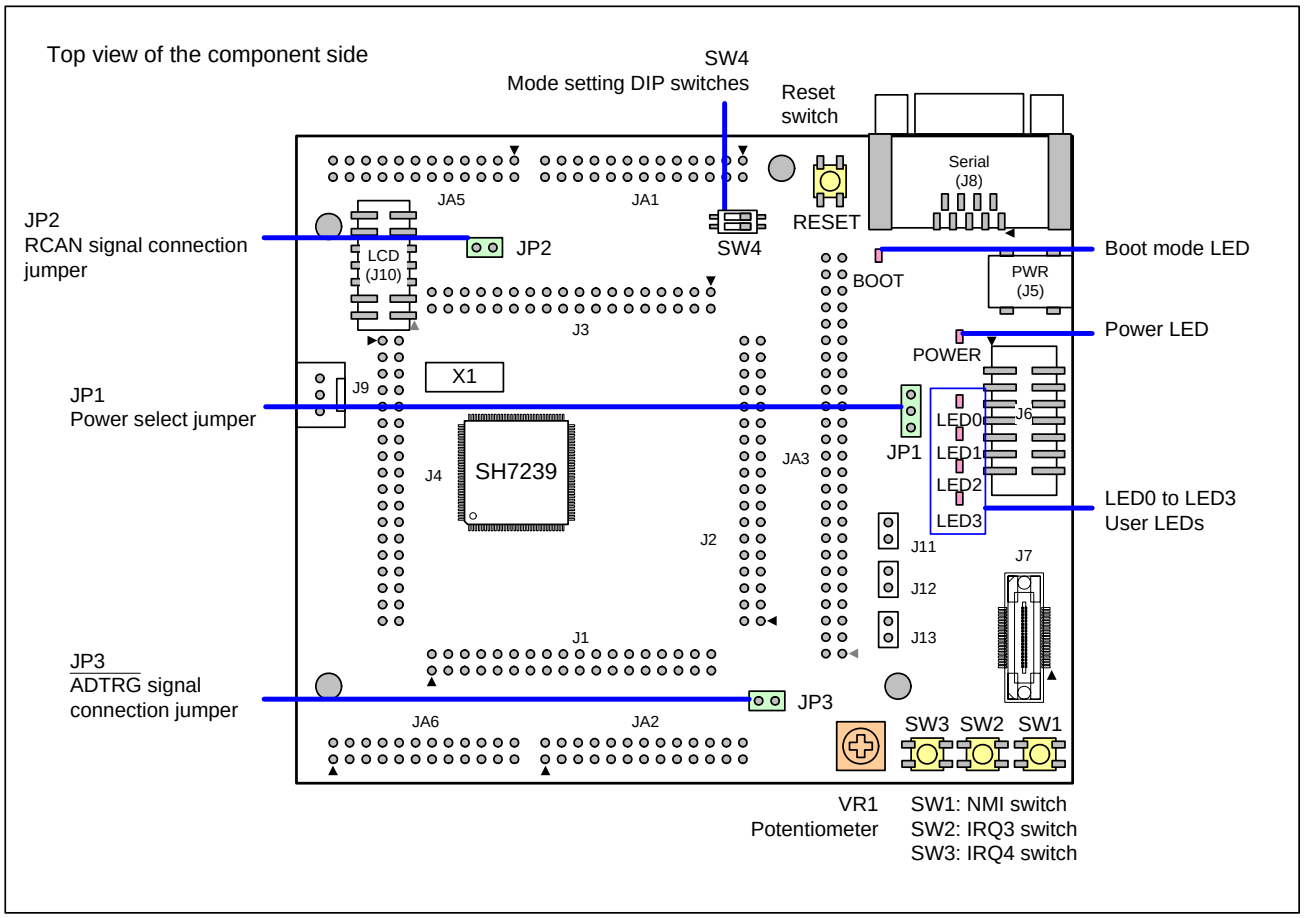


Figure 3.10 R0K572390 Operating Component Assignments

3.2.1 Jumpers (JP1, JP2, JP3)

The R0K572390 provides three jumpers (JP1, JP2, and JP3). These jumpers are not populated by default.

- JP1: Power select jumper
  JP1 is a jumper to specify whether to supply 5VCC or 3.3VCC power to the SH7239 and other devices on the board. Short-circuit pins 1 and 2 of JP1 to supply 5VCC, and short-circuit pins 2 and 3 of JP1 to supply 3.3VCC.
  JP1 is not populated by default. VCC power supply voltage is fixed to 3.3 V by the zero-ohm resistor R70 on the R0K572390C000BR. On the R0K572390C020BR, short-circuit pins 1 and 2 of JP1 to fix the VCC to 5 V.
- JP2: RCAN signal connection jumper
  JP2 is a jumper to specify whether to connect the SH7239 RCAN-related signal PA0/RXD0/$\overline{\text{CS0}}$/CRx0/IRQ4 to the RCAN port connector (J9). Short-circuit JP2 to connect to J9 connector.
  SH7239 PA0/RXD0/$\overline{\text{CS0}}$/CRx0/IRQ4 pin is also used as $\overline{\text{CS0}}$ to control SRAM. To use the pin as $\overline{\text{CS0}}$ signal, leave JP2 as opened. Note that the RCAN port connector (J9) cannot be used.
  JP2 is not populated by default, and PA0/RXD0/$\overline{\text{CS0}}$/CRx0/IRQ4 signal is connected to the RCAN port connector (J9) by the zero-ohm resistor R41.
- JP3: $\overline{\text{ADTRG}}$ signal connection jumper
  JP3 is a jumper to specify whether to connect user switch SW2 (IRQ3) output to PC1/A1/$\overline{\text{ADTRG}}$ pin. To use the pin as the $\overline{\text{ADTRG}}$ input, short-circuit JP3. Leave JP3 as opened to use PC1/A1/$\overline{\text{ADTRG}}$ pin as output pin (i.e. A1).
  JP3 is not populated by default. Install a zero-ohm resistor R82 (not installed by default) to connect user switch SW2 (IRQ3) output to PC1/A1/$\overline{\text{ADTRG}}$ pin.

Table 3.20 lists the power select jumper (JP1) settings. Table 3.21 lists the RCAN signal connection jumper (JP2) settings. Table 3.22 lists the $\overline{\text{ADTRG}}$ signal connection jumper (JP3).

Table 3.20 Power Select Jumper (JP1) Settings

Number	Setting	Description
JP1	1–2	Supplies 5 V power to the VCCQ
	2–3	Supplies 3.3 V power to the VCCQ

Table 3.21 RCAN Signal Connection Jumper (JP2) Settings

Number	Setting	Description
JP2	Short-circuit	Connects PA0/RXD0/$\overline{\text{CS0}}$/CRx0/IRQ4 signal to the RCAN port connector (J9)
	Open	Leaves PA0/RXD0/$\overline{\text{CS0}}$/CRx0/IRQ4 signal disconnected from the RCAN port connector (J9)

Table 3.22 $\overline{\text{ADTRG}}$ Signal Connection Jumper (JP3) Settings

Number	Setting	Description
JP3	Short-circuit	Connects user switch SW2 (IRQ3) output to PC1/A1/$\overline{\text{ADTRG}}$ pin
	Open	Leaves user switch SW2 (IRQ3) output disconnected from PC1/A1/$\overline{\text{ADTRG}}$ pin

Note: Do not change the jumper settings while the board is ON. Make sure to turn the power OFF before changing the settings.

3.2.2 Switches

The R0K572390 includes four push switches and mode setting DIP switches.

Table 3.23 lists switches, and Table 3.24 lists the mode setting DIP switches settings.

Table 3.23 R0K572390 Switches

Number	Description	Remarks
RESET	Reset switch	Refer to 2.13 for details on connecting signals
SW1	User switch (NMI input)	Refer to 2.9 for details on connecting signals
SW2	User switch (IRQ3 input and $\overline{\text{ADTRG}}$ input)	
SW3	User switch (IRQ4 input)	
SW4	Mode setting DIP switches (2/package)	

Table 3.24 Mode Setting DIP Switches (SW4) Settings

Number	Setting	Description
SW4-1	ON	Sets the SH7239 MD0 pin to low (MCU extension mode)
	OFF	Sets the SH7239 MD0 pin to high (Single-chip mode, default setting)
SW4-2	ON	Sets the SH7239 FWE signal to high (On-board programming mode)
	OFF	SH7239 FWE signal depends on the reset switch and user switch SW1 (NMI), (default setting)

Note: As the FWE signal is multiplexed with the $\overline{\text{ASEBRKAK}}$/$\overline{\text{ASEBRK}}$ signal, the above SW4-2 setting is enabled only when $\overline{\text{ASEMD0}}$ is high.

- Setting the FWE signal state by the push switch

  Combination of the reset switch (RESET) and user switch SW1 (NMI) enables setting the boot mode (FWE signal state). The R0K572390 enters user mode (FWE is high) when turning ON the power or press the reset switch (RESET). To enter boot mode, press and hold down the user switch SW1 (NMI) while pressing the reset switch (RESET). As the FWE signal is multiplexed with the $\overline{\text{ASEBRKAK}}$/$\overline{\text{ASEBRK}}$ signal, the $\overline{\text{ASEBRKAK}}$/$\overline{\text{ASEBRK}}$ signal is enabled when an emulator is connected to the R0K572390 and $\overline{\text{ASEMD0}}$ signal is low.
- To use the $\overline{\text{ADTRG}}$ input

  User switch SW2 (IRQ3) can also be used as the $\overline{\text{ADTRG}}$ input. Install a zero-ohm resistor R82 (not installed by default) to use SW2 as the $\overline{\text{ADTRG}}$ input.

3.2.3 Potentiometer

The R0K572390 includes a potentiometer to evaluate AN8 input.

Table 3.25 lists the information of the potentiometer installed on the R0K572390. For its accuracy, refer to the datasheet provided by the manufacturer.

Table 3.25 Potentiometer

Symbol	Part Number	Manufacturer Name
VR1	CT-6ETV10KΩ	NIDEC Copal Electronics Corporation

3.2.4 LEDs

The R0K572390 includes six LEDs. Table 3.26 lists LEDs on the R0K572390.

Table 3.26 LEDs

Number	Color	Description/Remarks
POWER	Green	Power LED (POWER is illuminated when the power supply voltage is supplied)
BOOT	Orange	Boot mode LED (BOOT is illuminated when FWE is high in on-board programming mode)
LED0	Green	User LED0 (LED0 is illuminated when PE12 outputs low level signal)
LED1	Orange	User LED1 (LED1 is illuminated when PE13 outputs low level signal)
LED2	Red	User LED2 (LED2 is illuminated when PE14 outputs low level signal)
LED3	Red	User LED3 (LED3 is illuminated when PE15 outputs low level signal)

3.3 Dimensions

Figure 3.11 shows the R0K572390 dimensions.

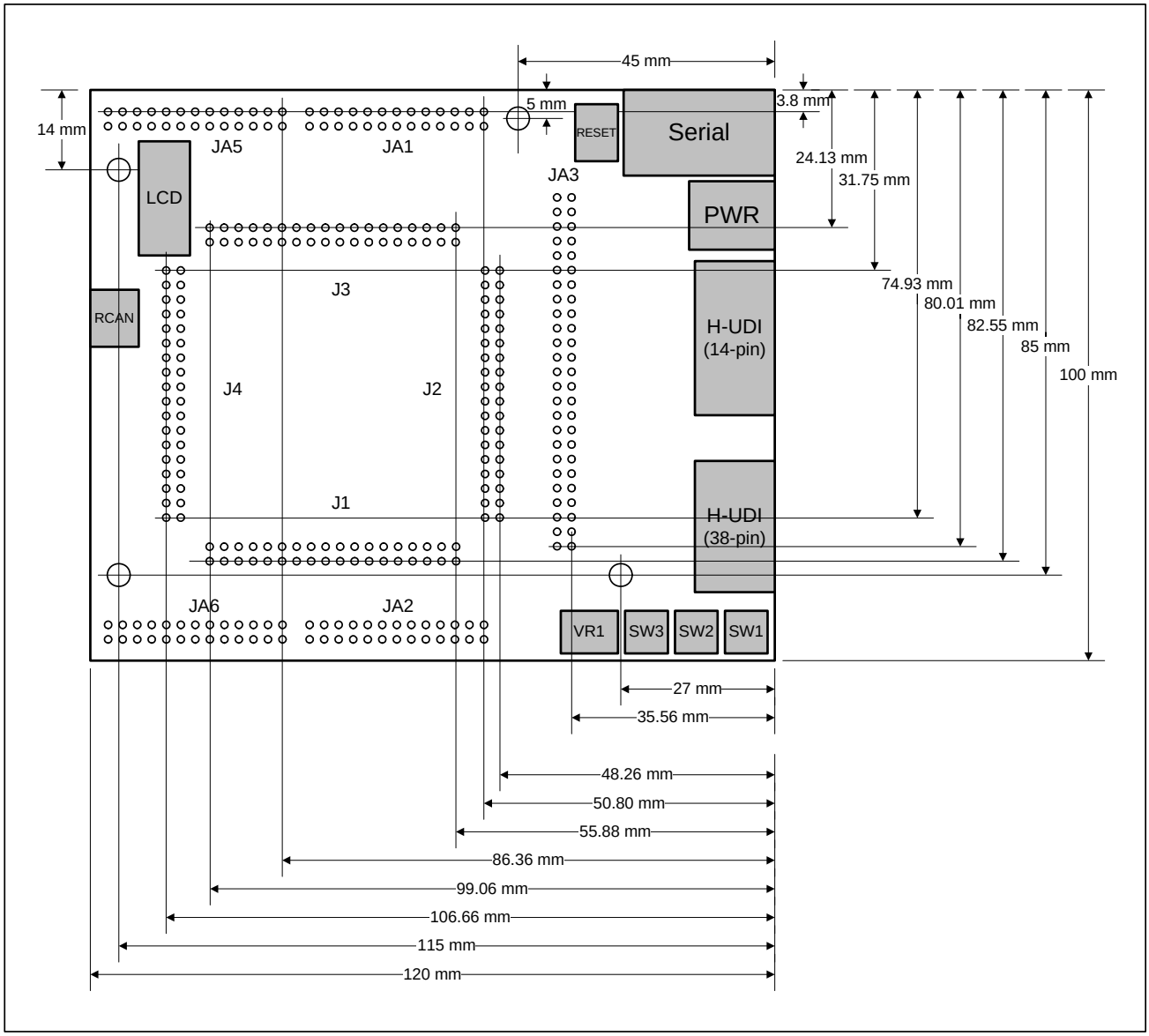


Figure 3.11 R0K572390 Dimensions

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Appendix R0K572390 Schematics

SH7239 CPU Board R0K572390 SCHEMATICS

TITLE	PAGE
INDEX	1
CPU SH7239,Reset,Boot,LED	2
SRAM,RCAN,SERIAL,AUD,H-UDI,EEPROM,A/D	3
Power,Push SW,Ring connectors	4
Application headers,LCD Connector	5

Note:

5VCC	= Digital 5V	R	= Fixed Resistors
3VCC	= 3.3V	RA	= Resister Array
AVCC	= CPU Analog 5V	VR	= Potentiometers
AVREF	= CPU Analog 5V Reference	C	= Ceramic Caps
VCC	= CPU/etc. 3.3V/5V	CE	= Electrolytic Caps
PLLVCC	= CPU PLL 3.3V/5V	CP	= Decoupling Caps (Put one cap per each source pin)
		L	= Inductors
		D	= Diodes
		H	= Test terminals

R(_) :not mounted

R(*) :for R0K572390C000BR(3.3V model) only

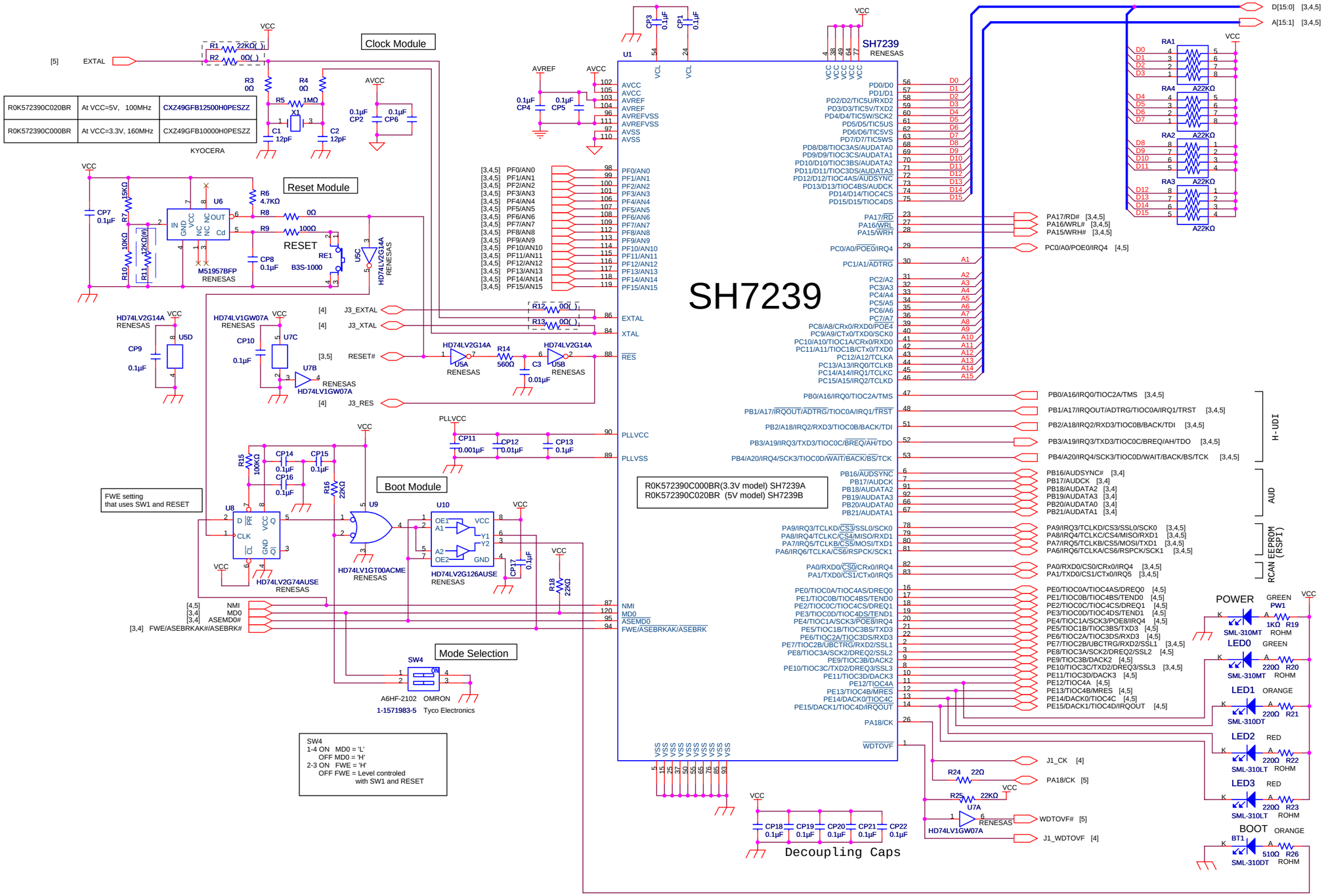
R(#) :for R0K572390C020BR(5V model) only

Serial port D-Sub 9-pin

R(M) :for Male connector only

R(F) :for Female connector only

CHANGE					
Ver. 1.00 It corresponds for R0K572390C000BR(3.3V model) and R0K572390C020BR(5V model)	SCALE		RENESAS SOLUTIONS CORPORATION		R0K572390 INDEX (1 / 5)
	DATE	10-10-27	DRAWN / CHECKED / DESIGNED / APPROVED		DK30840-B



R0K572390C020BR	At VCC=5V, 100MHz	CXZ49GFB12500H0PESZZ
R0K572390C000BR	At VCC=3.3V, 160MHz	CXZ49GFB10000H0PESZZ

KYOCERA

:not mounted :for R0K572390C020BR(5V model) only

CHANGE

Ver. 1.00

It corresponds
for R0K572390C000BR(3.3V model)
and R0K572390C020BR(5V model)

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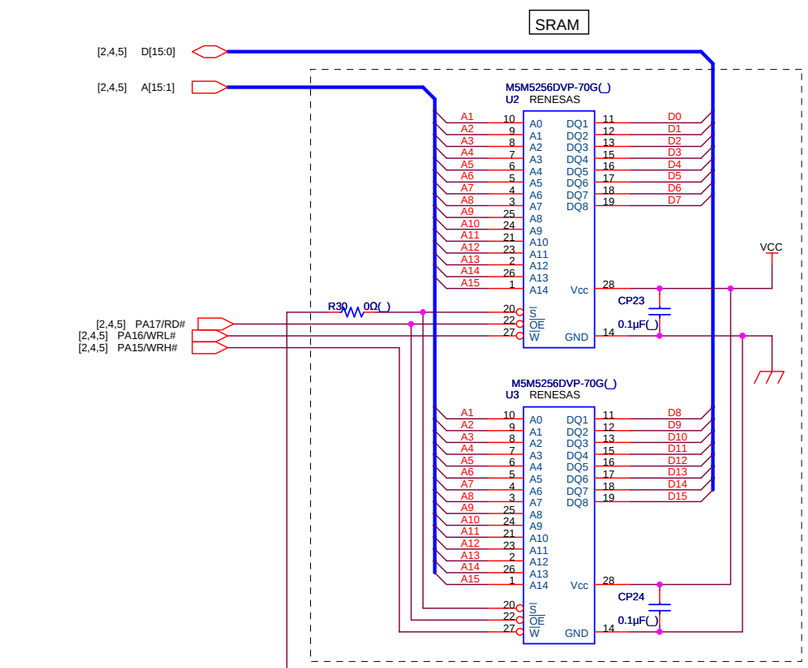
DATE 10-10-27

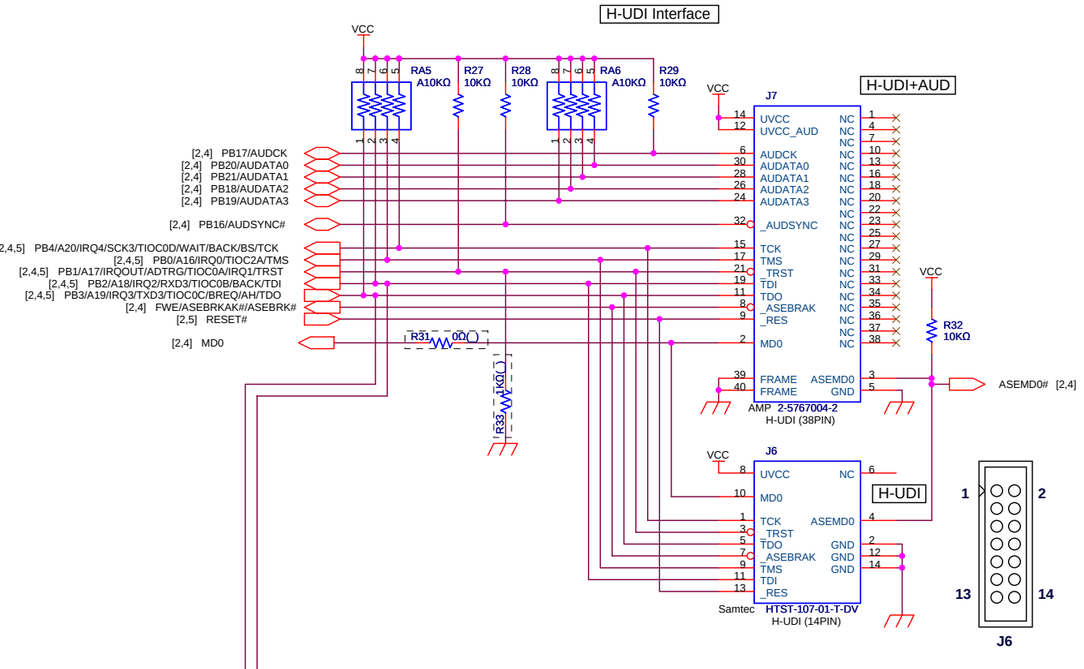
DRAWN	CHECKED	DESIGNED	APPROVED

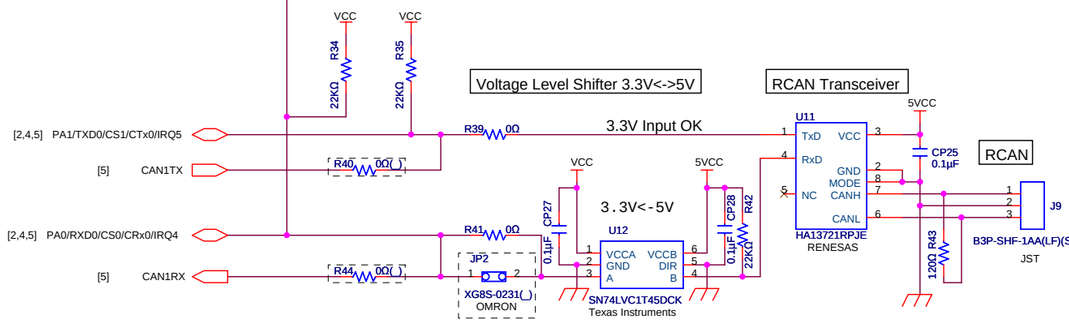
RENESAS SOLUTIONS CORPORATION

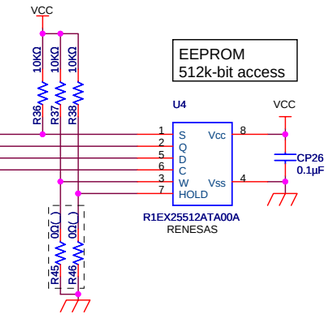
R0K572390
CPU SH7239,Reset,Boot,LED
(2 / 5)

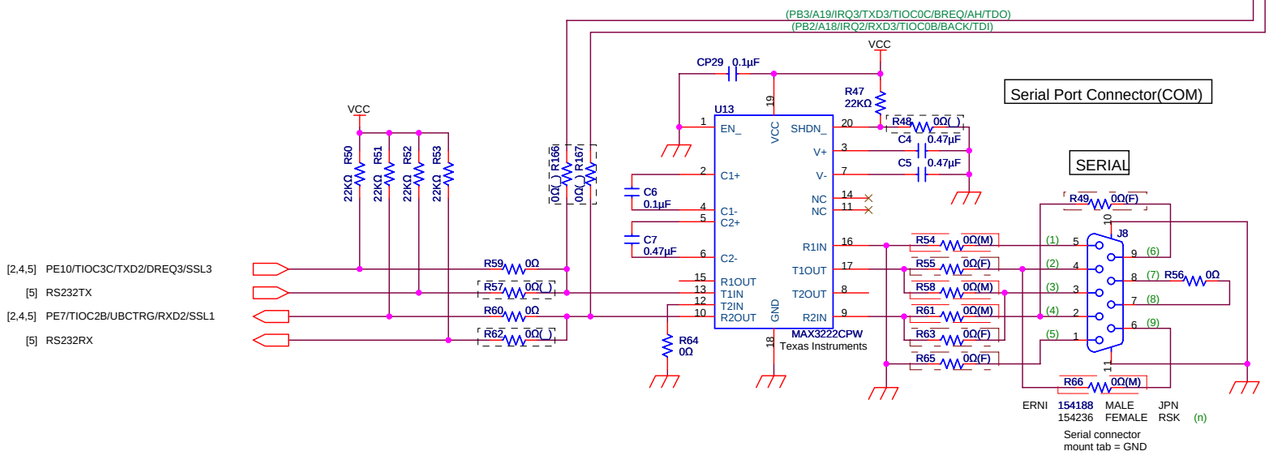
DK30840-B





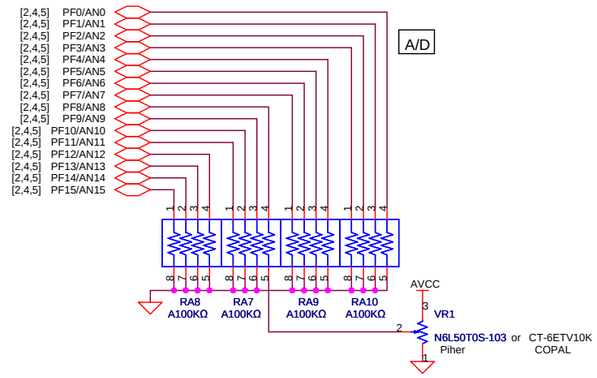






Mounted resistors	
MALE	FEMALE
R54,	R65,
R56,	R63,
R58,	R56,
R61,	R55,
R66	R49

Removed resistors	
MALE	FEMALE
R49,	R66,
R55,	R61,
R63,	R58,
R65	R54



:not mounted

:for Male connector only

:for Female connector only

CHANGE					
Ver. 1.00 It corresponds for R0K572390C000BR(3.3V model) and R0K572390C020BR(5V model)		RENESAS SOLUTIONS CORPORATION			R0K572390 SRAM,RCAN,SERIAL,AUD,H-UDI, EEPROM,A/D (3 / 5)
	SCALE	DRAWN	CHECKED	DESIGNED	APPROVED
	DATE 10-10-27				DK30840-B

5V To 3.3V Switching Regulator

Power Connector

PWR

J5 — KLDX-SMT2-0202-A (Kycon)

D1 BAT54-7-F DIODES

U14 LM2738-YMY NATIONAL SEMICONDUCTORS (VIN C, BOOST, VIN D, SW, EN, GND, GND, FB)

CP30 0.01µF

L1 CDRH6D28NP-120NC SUMIDA

D2 CRS08 TOSHIBA

R69 100KΩ

R67 31.6KΩ

R68 10KΩ

CE1 10µF

CE2 47µF

5VCC 3VCC

POWER TEST PIN

H2 _5V

H3 _3V

JP1 XG8S-0331(_) OMRON

R70 0Ω(*)

If R0K572390C020BR(5V model), Connect hole pin1 and 2 of JP1 with wire.

5VCC EXTERNAL

J11 HIROSE A2-2PA-2.54DSA(_)

AVCC EXTERNAL

J12 HIROSE A2-2PA-2.54DSA(_)

VCC EXTERNAL

J13 HIROSE A2-2PA-2.54DSA(_)

H1 _VCC — CE3 10µF

H4 _PLLVCC — L2 BLM21PG300SN1 MURATA — CE4 10µF

H5 _AVCC — R71 0Ω — L3 BLM21PG300SN1 MURATA — CE5 10µF

H6 _AVREF — R72 0Ω — CE6 10µF

GND - AGND - AVREFVSS

L4 BLM21PG300SN1 MURATA — R73 0Ω

NMI SWITCH CIRCUIT

NMI — SW1 B3S-1000 OMRON

R74 10KΩ — R76 220Ω — U15A — U16A — R77 0Ω — (NMI)

R75 4.7KΩ

HD74LV1GW17A — CE7 2.2µF — HD74LV1GW07A

CP31 0.1µF — U15C — CP32 0.1µF — U16C — RENESAS HD74LV1GW17A / HD74LV1GW07A

IRQ3 SWITCH CIRCUIT

IRQ3 — SW2 B3S-1000 OMRON

R78 10KΩ — R80 220Ω — U15B — U16B — R79 10KΩ — R81 0Ω — (PA9/IRQ3/TCLKD/CS3/SSL0/SCK0)

R82 0Ω( ) — (ADTRG)

JP3 XG8S-0231(_) OMRON

SW2 usage for ADTRG

HD74LV1GW17A — CE8 2.2µF — HD74LV1GW07A

IRQ4 SWITCH CIRCUIT

IRQ4 — SW3 B3S-1000 OMRON

R83 10KΩ — R85 220Ω — U17A — U18A — R86 0Ω — PC0/A0/POE0/IRQ4 [2,5]

R84 4.7KΩ

HD74LV1GW17A — CE9 2.2µF — HD74LV1GW07A

CP33 0.1µF — U17C — CP34 0.1µF — U18C — RENESAS HD74LV1GW17A / HD74LV1GW07A

U17B — HD74LV1GW17A RENESAS

U18B — HD74LV1GW07A RENESAS

SH7239 Ring Connector

[2,3,5] A[15:1]

[2,3,5] D[15:0]

J1 — FFC-36BMEP1B(_) Honda

[2] J1_WDTOVF

[2,3,5] PE7/TIOC2B/UBCTRG/RXD2/SSL1

[2,5] PE8/TIOC3A/SCK2/DREQ2/SSL2

[2,3] PB16/AUDSYNC#

[2,3] PB17/AUDCK

[2,3,5] PE10/TIOC3C/TXD2/DREQ3/SSL3

[2,5] PE9/TIOC3B/DACK2

[2,5] PE11/TIOC3D/DACK3

[2,5] PE12/TIOC4A

[2,5] PE13/TIOC4B/MRES

[2,5] PE14/DACK0/TIOC4C

[2,5] PE15/DACK1/TIOC4D/IRQOUT

[2,5] PE0/TIOC0A/TIOC4AS/DREQ0

[2,5] PE1/TIOC0B/TIOC4BS/TEND0

[2,5] PE2/TIOC0C/TIOC4CS/DREQ1

[2,5] PE3/TIOC0D/TIOC4DS/TEND1

[2,5] PE4/TIOC1A/SCK3/POE8/IRQ4

[2,5] PE5/TIOC1B/TIOC3BS/TXD3

[2,5] PE6/TIOC2A/TIOC3DS/RXD3

[2,3,5] PA17/RD#

[2] J1_CK

[2,3,5] PA16/WRL#

[2,3,5] PA15/WRH#

[2,5] PC0/A0/POE0/IRQ4

A1

J2 — FFC-36BMEP1B(_) Honda

A2 A3 A4 A5 A6 A7 A8 A9 A10 A11 A12 A13 A14 A15

[2,3,5] PB0/A16/IRQ0/TIOC2A/TMS

[2,3,5] PB1/A17/IRQOUT/ADTRG/TIOC0A/IRQ1/TRST

[2,3,5] PB2/A18/IRQ2/RXD3/TIOC0B/BACK/TDI

[2,3,5] PB3/A19/IRQ3/TXD3/TIOC0C/BREQ/AH/TDO

[2,3,5] PB4/A20/IRQ4/SCK3/TIOC0D/WAIT/BACK/BS/TCK

D0 D1 D2 D3 D4

J3 — FFC-36BMEP1B(_) Honda

D5 D6 D7 D8 D9 D10 D11 D12 D13 D14 D15

[2,3] PB20/AUDATA0

[2,3] PB21/AUDATA1

[2,3,5] PA9/IRQ3/TCLKD/CS3/SSL0/SCK0

[2,3,5] PA8/IRQ4/TCLKC/CS4/MISO/RXD1

[2,3,5] PA7/IRQ5/TCLKB/CS5/MOSI/TXD1

[2,3,5] PA6/IRQ6/TCLKA/CS6/RSPCK/SCK1

[2,3,5] PA0/RXD0/CS0/CRx0/IRQ4

[2,3,5] PA1/TXD0/CS1/CTx0/IRQ5

[2] J3_XTAL

[2] J3_EXTAL

[2,5] NMI

[2] J3_RES

J4 — FFC-36BMEP1B(_) Honda

AVCC AVREF

[2,3] PB18/AUDATA2

[2,3] PB19/AUDATA3

[2,3] FWE/ASEBRKAK#/ASEBRK#

[2,3] ASEMD0#

[2,3,5] PF0/AN0

[2,3,5] PF1/AN1

[2,3,5] PF2/AN2

[2,3,5] PF3/AN3

[2,3,5] PF4/AN4

[2,3,5] PF5/AN5

[2,3,5] PF6/AN6

[2,3,5] PF7/AN7

[2,3,5] PF8/AN8

[2,3,5] PF9/AN9

[2,3,5] PF10/AN10

[2,3,5] PF11/AN11

[2,3,5] PF12/AN12

[2,3,5] PF13/AN13

[2,3,5] PF14/AN14

[2,3,5] PF15/AN15

[2,3] MD0

:not mounted — :for R0K572390C000BR(3.3V model) only — :for R0K572390C020BR(5V model) only

CHANGE

Ver. 1.00

It corresponds
for R0K572390C000BR(3.3V model)
and R0K572390C020BR(5V model)

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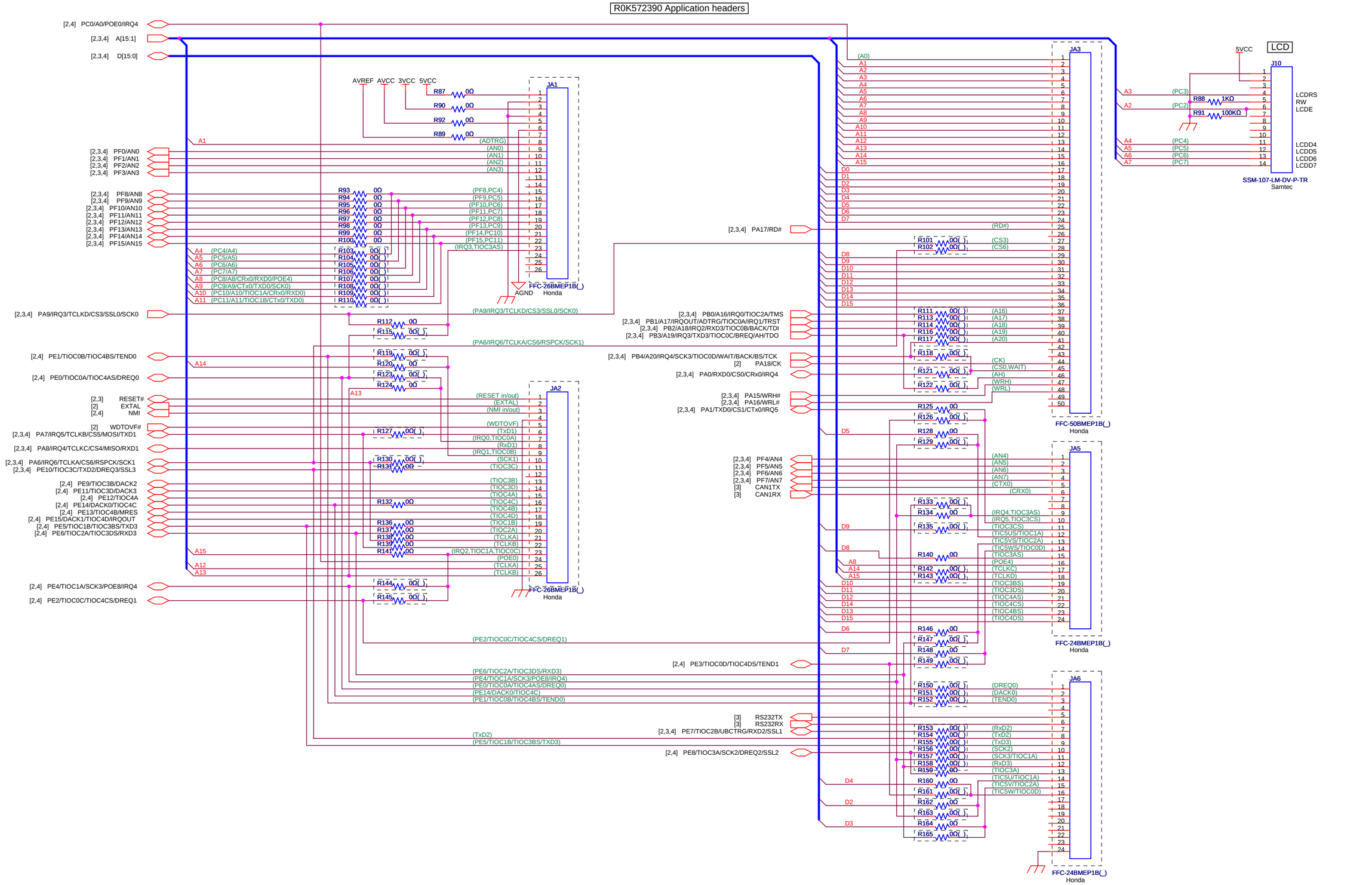
DRAWN	CHECKED	DESIGNED	APPROVED

R0K572390
Power,Push SW,Ring connectors
(4 / 5)

DK30840-B

R0K572390 Application headers



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		SCALE	DRAWN	CHECKED / DESIGNED / APPROVED	DK30840-B
		DATE 10-10-27			

REVISION HISTORY	SH7239 CPU Board R0K572390 User's Manual

Rev.	Date	Description	
		Page	Summary
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SH7239 CPU Board R0K572390 User's Manual

Publication Date: Rev. 1.00 Nov. 08, 2010
Published by: Renesas Electronics Corporation

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Colophon 1.0

SH7239 CPU Board
R0K572390

Renesas Electronics Corporation

R20UT0297EJ0100