User´s Manual

32

RH850 Evaluation Platform

RH850/F1x-176pin PiggyBack board V3

Y-RH850-F1X-176PIN-PB-T1-V3

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1. Handling of Unused Pins

   Handle unused pins in accordance with the directions given under Handling of Unused Pins in the manual.

   — The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.

2. Processing at Power-on

   The state of the product is undefined at the moment when power is supplied.

   — The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.
   In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed.
   In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.

3. Prohibition of Access to Reserved Addresses

   Access to reserved addresses is prohibited.

   — The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.

4. Clock Signals

   After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.

   — When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.

5. Differences between Products

   Before changing from one product to another, i.e. to a product with a different part number, confirm that the change will not lead to problems.

   — The characteristics of Microprocessing unit or Microcontroller unit products in the same group but having a different part number may differ in terms of the internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

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Chapter 1 Introduction

The RH850/F1x Application Board is part of the RH850 Evaluation Platform and serves as a simple and easy to use platform for evaluating the features and performance of Renesas Electronics 32-bit RH850/F1x microcontrollers. The piggyback board (Y-RH850-F1X-176PIN-PB-T1-V3) can be used as a standalone board, or can be mated with a mainboard (e.g. Y-RH850-X1X-MB-Tx-Vx) for extended functionality.

Main features:

- Socket for mounting of device
- Standalone operation of the board
- Direct supply of device voltage (typ. 3.3V-5.0V)
- Device programming capability
- Device debugging capability
- Pin headers for direct access to each device pin
- Reset switch
- MainOSC and SubOSC circuitry
- Signal LEDs
- Jumpers for device mode selection
- Connectors to MainBoard

This document describes the functionality provided by the piggyback board and guides the user through its operation.

For details regarding the operation of the microcontroller, refer to the related User's Manual and Datasheet

This manual describes the following board revisions:

- Y-RH850-F1X-176PIN-PB-T1-V3 (EESS-0400-135-01)
- Y-RH850-F1X-176PIN-PB-T1-V3 (EESS-0400-135-02)

The main difference to the previous board revision (Y-RH850-F1X-176PIN-PB-T1-V2) are:

- Added support for the RH850/F1KM-S4 device
- Added jumpers for mode selection
- Added signal LEDs
- Added EVTO signal for the debug interface

Chapter 2 Overview

2.1 Overview

Figures 1 and 2 provide the views of the Piggyback Board (EESS-0400-135-02).

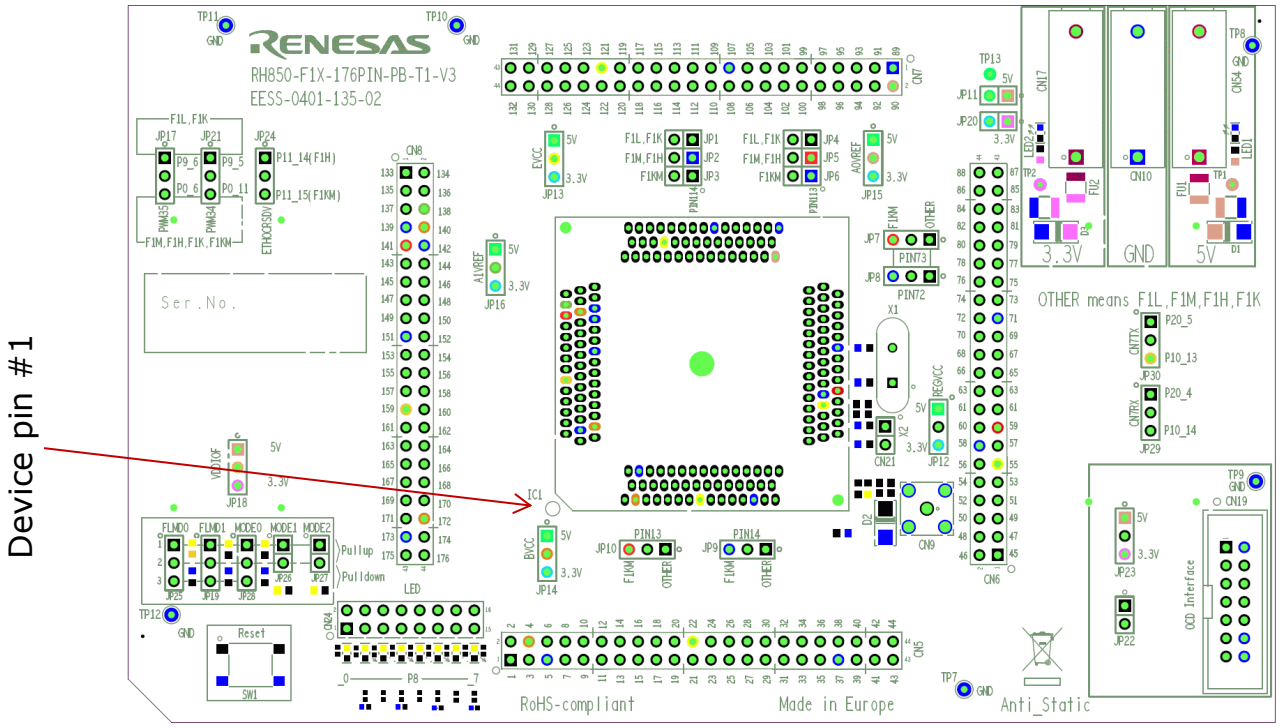


Figure 1 – PiggyBoard top view

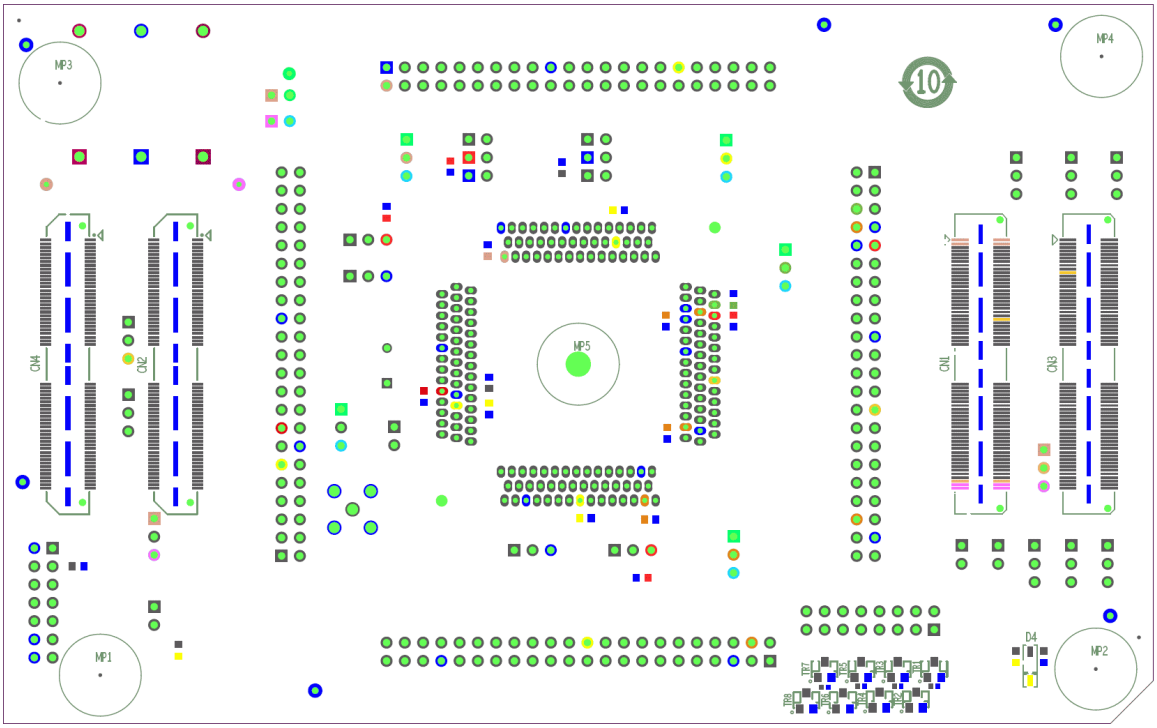


Figure 2 – PiggyBoard bottom view

2.2 Mounting of the device

The board is designed for use with the following devices (each in the 176pin package version):

- RH850/F1L
- RH850/F1M
- RH850/F1H
- RH850/F1K
- RH850/F1KM-S4

The device must be placed inside the socket IC1. To insert the device, press down the lid, align the #1 pin of the device to the #1pin of the socket, insert the device inside the socket and release the lid.

Chapter 3 Jumper Configuration

The function of the board can be configured via jumpers. This chapter describes the standard configuration, i.e. jumper setting for the intended devices. For the supported function of the used device, please refer to the corresponding HW user's manual.

The table has the following meaning:

- x-y: Connect the pins x and y; valid for 3-pin jumpers (e.g. JP24)

The pin #1 can be identified by a small circle in the vicinity of the jumper

Depending on the used device a configuration of several jumpers is required. The detailed configuration is shown below:

	F1L	F1M	F1H	F1K	F1KM-S4	Function
JP1	closed	open	open	closed	open	Selection of Pin 114: P9_6, VSS or REGVCC
JP2	open	closed	closed	open	open	
JP3	open	open	open	open	closed	
JP4	closed	open	open	closed	open	Selection of Pin 113: P9_5, REGVCC or VSS
JP5	open	closed	closed	open	open	
JP6	open	open	open	open	closed	
JP7 1-2	closed	closed	closed	closed	open	Selection of Pin 73: P1_6 or ISOVCL
JP7 2-3	open	open	open	open	closed	
JP8 1-2	closed	closed	closed	closed	open	Selection of Pin 72: P1_7 or VSS
JP8 2-3	open	open	open	open	closed	
JP9 1-2	closed	closed	closed	closed	open	Selection of Pin 14: P11_14 or VSS
JP9 2-3	open	open	open	open	closed	
JP10 1-2	closed	closed	closed	closed	open	Selection of Pin 73: P11_13 or ISOVCL
JP10 2-3	open	open	open	open	closed	
JP21 1-2	closed	open	open	Either	open	Selection of PWGA34: Either from P9_5 or P0_11
JP21 2-3	open	closed	closed	Or	closed	
JP17 1-2	closed	open	open	Either	open	Selection of PWGA35: Either P9_6 or P0_6
JP17 2-3	open	closed	closed	Or	closed	
JP24 1-2	open	open	Either	open	open	Selection of ETH0RXERR: Either P11_14 or P11_15
JP24 2-3	open	open	Or	open	open	
JP29[1] 1-2	open	open	open	open	Either	Selection of CAN7RX: Either P20_4 or P10_14
JP29[1] 2-3	open	open	open	open	Or	
JP30[1] 1-2	open	open	open	open	Either	Selection of CAN7TX: Either P20_5 or P10_13
JP30[1] 2-3	open	open	open	open	Or	

[1] Note available on the EESS-0400-135-01 board version.

The jumper setting also are shown in this picture:

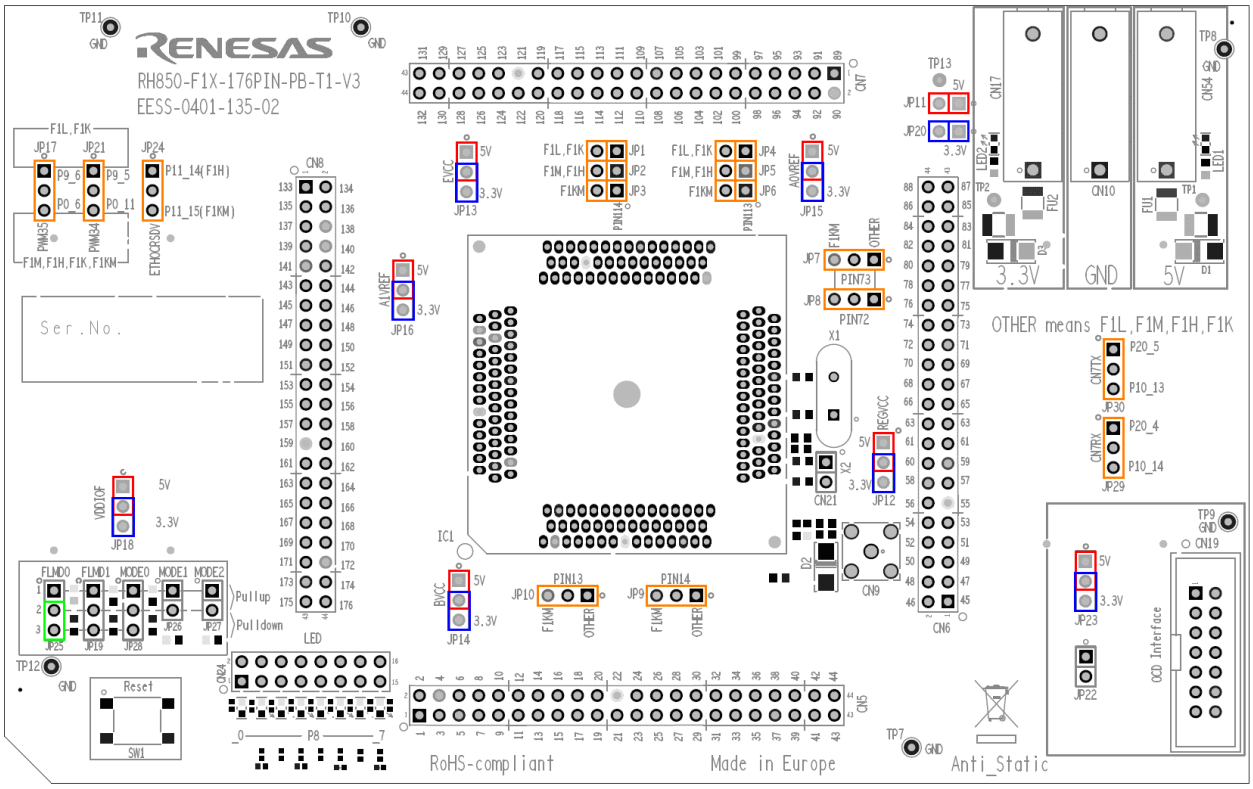


Figure 3 – Jumper setting overview

- The green jumper JP25 for FLMDO0 always must be closed for a ‘normal’ (user mode and debug) operation of the device.
- The red jumpers must be set for a single “Voltage 1” (typ +5.0V) operation of the device.
- The blue jumper must be set for a single “Voltage 2” (typ +3.3V) operation of the device.
- The orange jumpers must be selected depending on the used device. See the printing on the board for the applicable setting.

For jumper settings related to the device operation mode, refer to the chapter 8.2.

Chapter 4 Power supply

4.1 Board power connection

For operation of the device, a supply voltage must be connected to the board. Though a single supply voltage is sufficient for the operation of the device, two (different) voltages can be supplied to the board.

Within this document the following voltages are considered as ‘typical’ connections:

Voltage1 = 5.0V

Voltage2 = 3.3V

The following connectors are available to supply those voltages:

- Three 4mm ‘banana-type’ connectors:
  - Two red connectors for voltages *Voltage1* (CN54) and *Voltage2* (CN17).
  - A black connector for VSS connection (CN10).

  Note: The three connectors are supplied with the board but not assembled.
- The E1 emulator that is used for debug purposes and flash programming can also supply a single operating voltage (‘Dbg_Voltage’).
  The voltage is programmable via the E1 GUI as 3.3 or 5.0V (typ).
  See the documentation of the E1 and chapter 5 ‘Debug and Programming interface’ for details.
  Note: The E1 voltage is connected to *Voltage1*, what is *typically* 5V. Still, 3.3V can be provided by the E1.
- In case the PiggyBoard is mounted on a MainBoard, the voltages *Voltage1* and *Voltage2* are supplied by the on-board regulators of the MainBoard.

NOTE: *Do not supply any voltage directly to the PiggyBoard in case it is mounted on the MainBoard.*

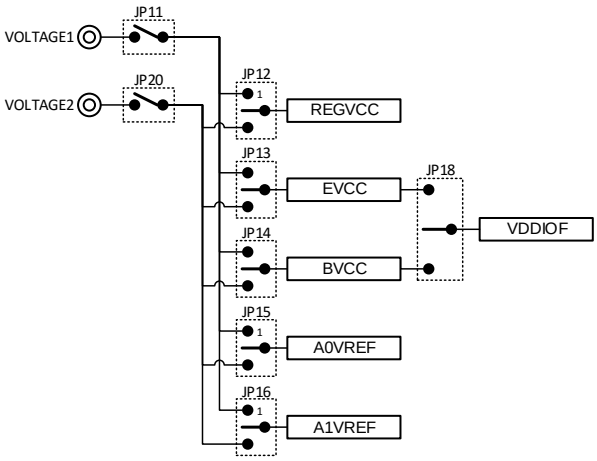
For each of the two voltages, ‘Voltage 1 ‘ and ‘Voltage 2’, a green LED (LED1 and LED2) is available to signal that the related voltage is available on the PiggyBoard.

4.2 Voltage distribution

The table shows the required device power supply pins and their function:

Device supply pin	Name on PiggyBoard	Function
REGVCC	REGVDD	Supply for the device internal regulators for the digital logic.
EVCC	EVDD	Supply for ports.
BVCC	BVDD	Supply for ports.
A0VREF		Supply for ports and analog functions of ADC0.
A1VREF		Supply for ports and analog functions of ADC1.
VDDIOF		IO supply voltage for components located on a connected mainboard.

- For each of the above voltages, the voltage source can be selected from *Voltage1* (typ. 5.0V) or *Voltage2* (typ. 3.3V) by the jumpers JP12-JP16, JP18, respectively the jumpers JP11 and JP20.



Chapter 5 Clock sources

Three external crystal oscillators for the device clock supply are provided with the board.

5.1 MainOsc

A crystal or ceramic resonator can be mounted on socket X1.
The applicable frequency range can be found is the devices electrical specification.

A 8MHz and a 16MHz oscillator is supplied with the board.

5.2 SubOSC

An oscillator with a frequency of 32.768kHz is supplied with the board and can be soldered into the connector X2.

Chapter 6 Debug and Programming interface

For connection of the microcontroller debug and flash programming tools, the connector CN19 is provided.

The signal connection of the connector CN19 is shown in the picture below:

CN19 pin	Device Port	Device signal
1	JP0_2	DCUTCK / LPDCLK
2	GND	GND
3	JP0_4	DCUTRST
4	FLMD0	FLMD0
5	JP0_1	DCUTDO / LPDO
6	P10_8*	FLMD1
7	JP0_0	DCUTDI / LPDI
8	‘Dbg_Voltage’	-
9	JP0_3	DCUTMS
10	JP0_6	EVTO*
11	JP0_5	DCURDY / LPDCLKOUT
12	GND	-
13	RESET	-
14	GND	-

*See chapter 9.5 for further details on the connection of this device port.

The ‘Dbg_Voltage’ (on CN19 pin 8) is monitored or supplied by the debug and flash programming tools. Therefore, it is necessary to select either Voltage1 (5V) or the Voltage2 (3.3V) by pin header JP23:

JP23 pin	Selection for Dbg_Voltage
1-2	5V is selected
2-3	3.3V is selected

Chapter 7 Connectors for ports of device

Connection to each pin of the device is possible via the connectors CN5 to CN8.

Note: The pin headers are directly connected to the pins of the device, therefore special care must be taken to avoid any electrostatic or other damage to the device.

7.1 Connectors to MainBoard

Three connectors (CN1 to CN3) are available to connect the PiggyBoard to a MainBoard.

The signal connection of each connector is described in the following tables:

7.1.1 Connector CN1

Pin	Function	Device Port		Pin	Function	Device Port
1	VOLTAGE1	-		2	VOLTAGE1	-
3	VOLTAGE1	-		4	VOLTAGE1	-
5	RESET	_RESET		6	NMI	P9_0
7	WAKE	-		8	-	-
9	INT0	P9_1		10	INT1	P0_6
11	INT2	P9_2		12	INT3	P9_3
13	-	-		14	-	-
15	UART0TX	P10_10		16	UART1TX	P0_5
17	UART0RX	P10_9		18	UART1RX	P0_4
19	LIN0TX	P10_10		20	LIN1TX	P0_8
21	LIN0RX	P10_9		22	LIN1RX	P0_7
23	IIC0SDL	P10_3		24	IIC1SDL	P9_1
25	IIC0SDA	P10_2		26	IIC1SDA	P9_0
27	CAN0TX	P10_1		28	CAN1TX	P0_3
29	CAN0RX	P10_0		30	CAN1RX	P0_2
31	SENTIN0	P8_0		32	SENTIN1	P9_0
33	SENTOUT0	P8_1		34	SENTOUT1	P9_1
35	PSI50Rx	-		36	PSI51Rx	-
37	PSI50Tx	-		38	PSI51Tx	-
39	PSI50Snyc	-		40	PSI51Sync	-
41	FLX0TX	P11_1		42	FLX0EN	P10_11
43	FLX0RX	P10_14		44	FLXSTPWT	P10_12
45	FLX1TX	P10_8		46	FX1EN	P10_13
47	FLX1RX	P10_9		48	FX1CLK	P10_10
49	-	-		50	-	-
51	ETH0MDIO	P12_4		52	ETH0MDC	P12_5
53	ETH0RXD0	P10_1		54	EH0TXD0	P18_1
55	ETH0RXD1	P10_2		56	EH0TXD1	P18_2
57	ETH0RXD2	P10_4		58	EH0TXD2	P18_3

Pin	Function	Device Port		Pin	Function	Device Port
59	ETH0RXD3	P10_5		60	EH0TXD3	P18_4
61	ETH0RXDCLK	P10_0		62	ETH0TXCLK	P18_7
63	ETH0RXER	P11_14 or P11_15		64	ETH0TXER	P18_6
65	ETH0CRSDV	P11_13		66	ETH0TXEN	P18_5
67	ETH0RXDV	P11_11		68	ETH0COL	P11_10
69	ETH0RESET	P2_6		70	ETH0LINK	P18_0
71	-	-		72	-	-
73	USB0UDMF	-		74	USB0UDMH	-
75	USB0UDPF	-		76	USB0UDPH	-
77	-	-		78	-	-
79	-	-		80	-	-
81	-	-		82	-	-
83	-	-		84	-	-
85	DIGIO_0	P8_0		86	DIGIO_1	P8_1
87	DIGIO_2	P8_2		88	DIGIO_3	P8_3
89	DIGIO_4	P8_4		90	DIGIO_5	P8_5
91	DIGIO_6	P8_6		92	DIGIO_7	P11_0
93	DIGIO_8	P10_0		94	DIGIO_9	P10_7
95	DIGIO_10	P10_8		96	DIGIO_11	P10_15
97	DIGIO_12	P0_9		98	DIGIO_13	P0_10
99	DIGIO_14	P0_11		100	DIGIO_15	P0_12
101	-	-		102	-	-
103	MUX0	P10_4		104	MUX1	P10_5
105	MUX2	P10_6		106	-	-
107	ADC0	AP0_0		108	ADC1	AP0_1
109	ADC2	AP0_2		110	ADC3	AP0_3
111	ADC4	AP0_4		112	ADC5	AP0_5
113	ADC6	AP0_6		114	ADC7	AP0_7
115	VDDIOF	-		116	VDDIOF	-
117	VOLTAGE2	-		118	VOLTAGE2	-
119	VOLTAGE2	-		120	VOLTAGE2	-

7.1.2 Connector CN2

Pin	Function	Device Port	Pin	Function	Device Port
1	CAN2Tx	P12_0	2	CAN3Tx	P1_3
3	CAN2Rx	P11_15	4	CAN3Rx	P1_2
5	CAN4Tx	P1_13	6	CAN5Tx	P11_6
7	CAN4Rx	P1_12	8	CAN5Rx	P11_5
9	LIN2Tx	P0_10	10	LIN3Tx	P1_15
11	LIN2Rx	P0_9	12	LIN3Rx	P1_14
13	LIN4Tx	P1_11	14	LIN5Tx	P8_12
15	LIN4Rx	P1_10	16	LIN5Rx	P8_11
17	LIN6Tx	P0_12	18	LIN7Tx	P12_4
19	LIN6Rx	P0_11	20	LIN7Rx	P12_3
21	LIN8Tx	P2_3	22	LIN9Tx	P2_5
23	LIN8Rx	P2_2	24	LIN9Rx	P2_4
25	LIN10Tx	P8_2	26	LIN11Tx	P0_5
27	LIN10Rx	P8_10	28	LIN11Rx	P0_4
29	LIN12Tx	P0_14	30	LIN13Tx	P1_1
31	LIN12Rx	P0_13	32	LIN13Rx	P1_0
33	LIN14Tx	P8_9	34	LIN15Tx	P1_5
35	LIN14Rx	P8_8	36	LIN15Rx	P1_4
37	-	-	38	-	-
39	-	-	40	-	-
41	-	-	42	-	-
43	-	-	44	-	-
45	-	-	46	-	-
47	CAN6Tx	P2_1	48	CAN7Tx	P20_5[1)] or P10_13
49	CAN6Rx	P2_0	50	CAN7Rx	P20_4[1)] or P10_14
51	-	-	52	-	-
53	-	-	54	-	-
55	-	-	56	-	-
57	-	-	58	-	-
59	-	-	60	-	-
61	-	-	62	-	-
63	-	-	64	-	-
65	-	-	66	-	-
67	-	-	68	-	-
69	-	-	70	-	-
71	-	-	72	-	-
73	-	-	74	-	-
75	-	-	76	-	-
77	-	-	78	-	-
79	-	-	80	-	-
81	-	-	82	-	-

Pin	Function	Device Port	Pin	Function	Device Port
83	-	-	84	-	-
85	-	-	86	-	-
87	-	-	88	-	-
89	-	-	90	-	-
91	-	-	92	-	-
93	-	-	94	-	-
95	-	-	96	-	-
97	-	-	98	-	-
99	-	-	100	-	-
101	-	-	102	-	-
103	-	-	104	-	-
105	-	-	106	-	-
107	-	-	108	-	-
109	-	-	110	-	-
111	-	-	112	-	-
113	-	-	114	-	-
115	-	-	116	-	-
117	-	-	118	-	-
119	-	-	120	-	-

[1)] Not available on the EESS-0400-135-01 board version.

7.1.3 Connector CN3

Pin	Function	Device Port	Pin	Function	Device Port
1	PWM00	P10_0	2	PWM01	P10_1
3	PWM02	P10_2	4	PWM03	P10_3
5	PWM04	P10_7	6	PWM05	P10_8
7	PWM06	P10_9	8	PWM07	P10_10
9	PWM08	P9_0	10	PWM09	P9_1
11	PWM10	P0_4	12	PWM11	P0_1
13	PWM12	P0_2	14	PWM13	P0_3
15	PWM14	P8_0	16	PWM15	P8_1
17	PWM16	P10_11	18	PWM17	P10_12
19	PWM18	P10_13	20	PWM19	P10_14
21	PWM20	P9_2	22	PWM21	P9_3
23	PWM22	P8_2	24	PWM23	P8_3
25	PWM24	P10_15	26	PWM25	P11_0
27	PWM26	P11_1	28	PWM27	P11_2
29	PWM28	P11_3	30	PWM29	P11_4
31	PWM30	P11_5	32	PWM31	P11_6
33	PWM32	P11_7	34	PWM33	P9_4
35	PWM34	P9_5 or P0_11	36	PWM35	P9_6 or P0_6
37	PWM36	P8_4	38	PWM37	P8_5
39	PWM38	P8_6	40	PWM39	P8_7
41	PWM40	P8_8	42	PWM41	P8_9
43	PWM42	P8_10	44	PWM43	P8_11
45	PWM44	P8_12	46	PWM45	P0_12
47	PWM46	P0_13	48	PWM47	P0_14
49	PWM48	P11_8	50	PWM49	P11_9
51	PWM50	P11_10	52	PWM51	P11_11
53	PWM52	P11_12	54	PWM53	P11_13
55	PWM54	P11_14	56	PWM55	P11_15
57	PWM56	P12_0	58	PWM57	P12_1
59	PWM58	P12_2	60	PWM59	P20_4
61	PWM60	P20_5	62	PWM61	P18_0
63	PWM62	P18_1	64	PWM63	P18_2
65	PWM64	P20_0	66	PWM65	P20_1
67	PWM66	P20_2	68	PWM67	P20_3
69	PWM68	P12_3	70	PWM69	P12_4
71	PWM70	P12_5	72	PWM71	P18_3
73	PWM72	-	74	PWM73	-
75	PWM74	-	76	PWM75	-
77	PWM76	-	78	PWM77	-
79	PWM78	-	80	PWM79	-
81	PWMADC00	AP0_8	82	PWMADC01	AP0_9

Pin	Function	Device Port	Pin	Function	Device Port
83	PWMADC02	AP0_10	84	PWMADC03	AP0_11
85	PWMADC04	AP0_12	86	PWMADC05	AP0_13
87	PWMADC06	AP0_14	88	PWMADC07	AP0_15
89	PWMADC08	AP1_0	90	PWMADC09	AP1_1
91	PWMADC10	AP1_2	92	PWMADC11	AP1_3
93	PWMADC12	AP1_4	94	PWMADC13	AP1_5
95	PWMADC14	AP1_6	96	PWMADC15	AP1_7
97	-	-	98	-	-
99	-	-	100	-	-
101	-	-	102	-	-
103	-	-	104	-	-
105	-	-	106	-	-
107	-	-	108	-	-
109	-	-	110	-	-
111	-	-	112	-	-
113	-	-	114	-	-
115	-	-	116	-	-
117	-	-	118	-	-
119	-	-	120	-	-

Chapter 8 Other circuitry

8.1 Push button for RESET

In order to issue a RESET to the device, the push-button SW1 is available.

8.2 Mode Selection

The PiggyBack Board gives the possibility to configure the following mode pins

- FLMD0 via jumper JP25
- FLMD1 via jumper JP19
- MODE0 via jumper JP28
- MODE1 via jumper JP26
- MODE2 via jumper JP27

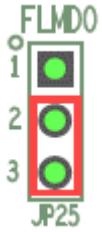
To apply “High” or “Low” to the mode pins, the pins 1 and 2, or the pins 2 and 3 (if available) of the corresponding jumper must be closed, respectively.

Note: Pin 1 of all jumpers is marked by a small circle.

CAUTION*: Be careful in configuration of mode related pins. Wrong configuration and operation of the device outside of its specification can cause irregular behaviour of the device and long term damage cannot be excluded. Be sure to check the corresponding User’s Manual for details, which modes are specified for the used device*

Note:
In the very most cases the ‘Normal operating mode’ of the device will be used. This mode is for execution of the user program. The on-chip debug functions also use this mode.

To select the ‘Normal operating mode’ of the device, the FLMD0 pin must be pulled low. To do so, close the pins 2-3 on the jumper JP25:



All other jumper related to the mode selection can be left open.

8.3 Signalling LEDs

Eight LEDs are provided to allow visual observation of the output state of device port pins. Device pins P8_0 to P8_7 are connected to the even pins 2 to 16 of the pin header CN24, while the LEDs 1 to 8 are connected to the odd pins 1 to 15, respectively.

Thus the LEDs can be either connected to

- the device port pins P8_0 to P8_7 by closing the connection on CN24 using a jumper, or
- any device port pin by using the provided wire connections.

Chapter 9 Precautions

9.1 JP24 signal naming

The signal name printed on the PCB top side below JP24 *ETH0CRSDV* is not correct.

The correct signal name as used in the schematic is *ETH0RXER* (or ETNB0RXERR as it is used in the User's Manual).

9.2 Ethernet CRS signal

The Ethernet ETH0CRS signal is not available at the MainBoard connector CN1 in case an F1KM device is used.

On the PiggyBoard the device pin 13, port P11_13, is routed to the connector CN1, pin 65.

On F1H the port P11_13 holds the Ethernet ETH0CRS signal.

In the F1KM the Ethernet ETH0CRS signal is located on P11_12 (pin 12). Therefore that signal/function is not routed directly to the MainBoard.

- Note that in the typical Ethernet use case of a 100Mbit connection the ETH0CRS signal is not required for the communication to the Ethernet PHY.

9.3 EVTO signal

The board with the production number 'EESS-0401-135-01' does not have the EVTO signal connection to the debug connector CN19.pin10.

9.4 JP29 and JP30 for CAN7

The board with the production number 'EESS-0401-135-01' does not have the Jumpers J29 and J30 for the selection of the CAN7 signal device ports.

For those ports the port P10_13 is used for the signal CAN7TX and the port P10_14 is used for the signal CAN7RX.

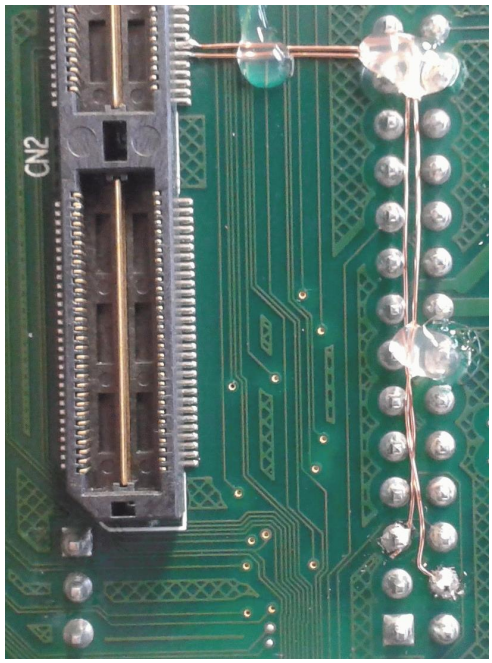
9.5 JP22

On the board with the production number 'EESS-0401-135-01' the jumper JP22 is used to connect *P10_15 / signal FLMD1* of the device to the connector CN19.6. This jumper is not available on the board with the other production numbers.
In case the FLMD1 signal must be controlled by the debug/programming tool, the jumper JP22 must be closed.

On the board with a production number 'EESS-0401-135-02' the jumper JP22 is used to connect a pull-up resistor to the EVTO signal on CN19.10.

9.6 CAN6 signals on CN2

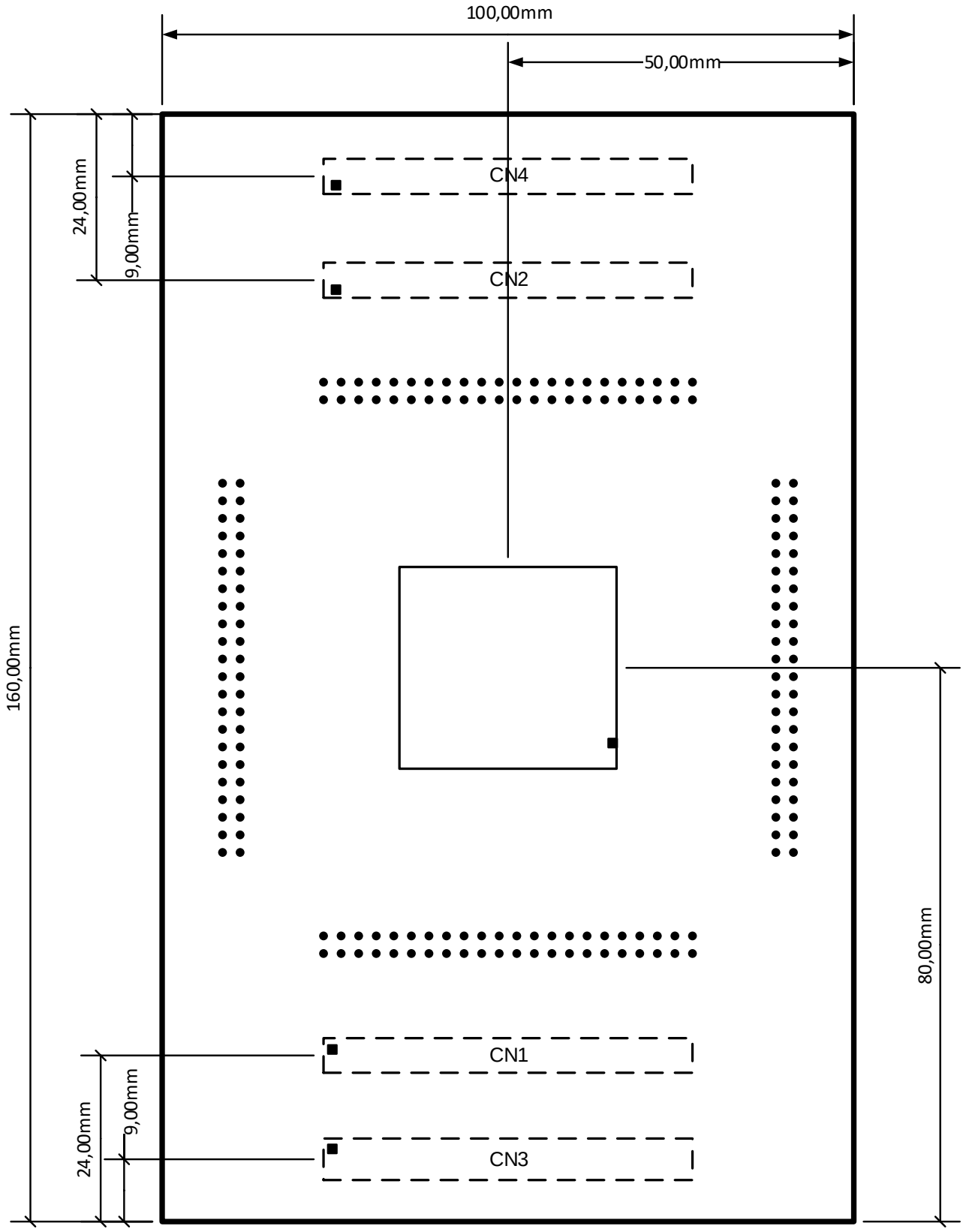
On some boards of the version ‘EESS-0400-135-01’ the following rework is not applied:



In case your board is affected and you want to make use of the CAN6 functionality via CN2, either of the two solutions can be applied:

- Make a manual connection of the signals using the supplied cables.
  - The CAN6RX signal is available on the PiggyBoard pin-header <CN6 pin 5> (device port P2_0).
    On the Network MainBoard RH850-X1X-MB-T2-V1 the related signal is located on the pin-header JP70, pin 1.
  - The CAN6TX signal is available on the PiggyBoard pin-header <CN6 pin 4> (device port P2_1).
    On the Network MainBoard RH850-X1X-MB-T2-V1 the related signal is located on the pin-header JP70, pin 2.
- Please contact your board supplier for a repair.
  European customers can use the following link:
  https://www.renesas.com/en-eu/products/software-tools/tools-product-support/tool-repair.html

Chapter 10 Mechanical dimensions

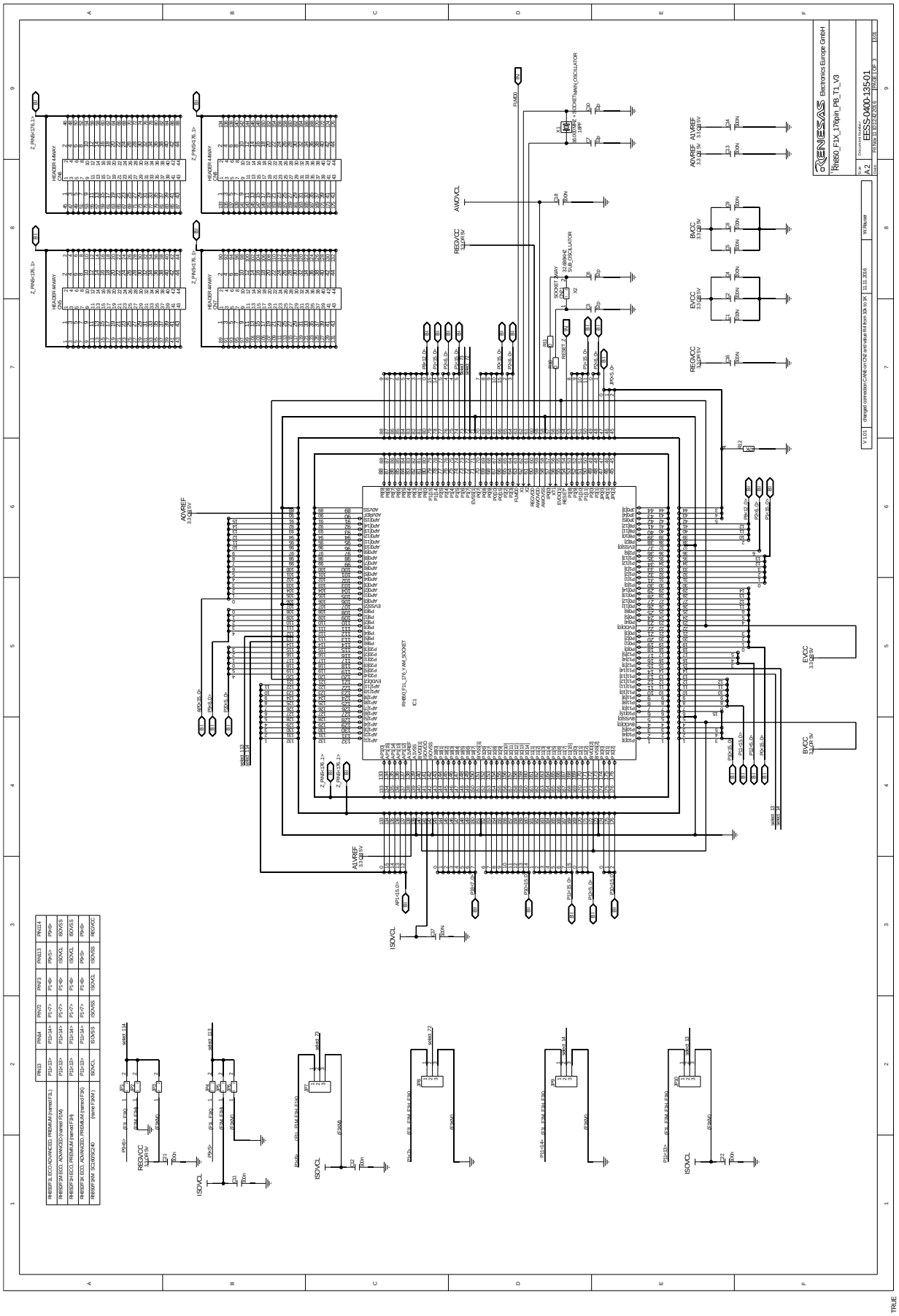


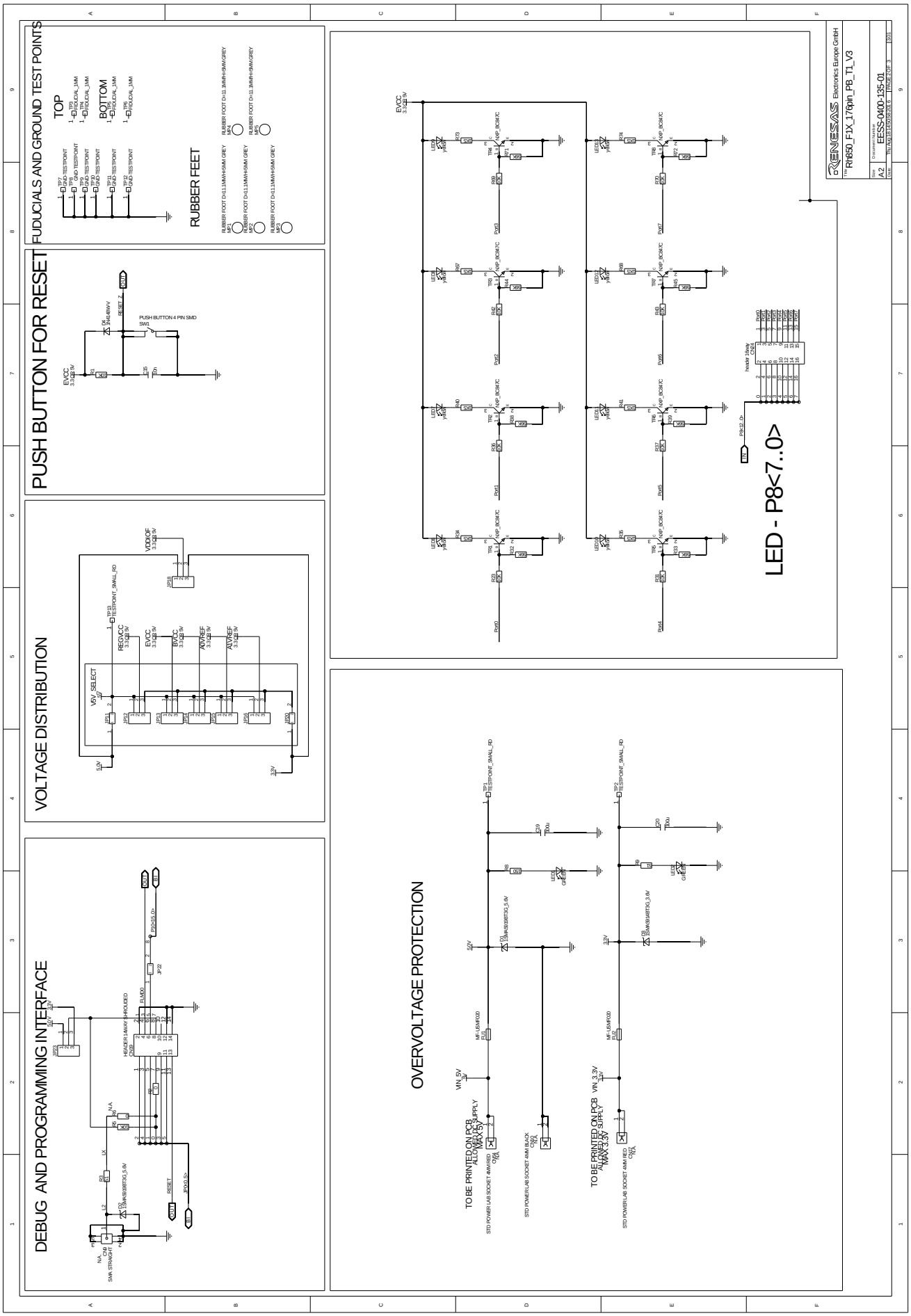
Chapter 11 Schematic

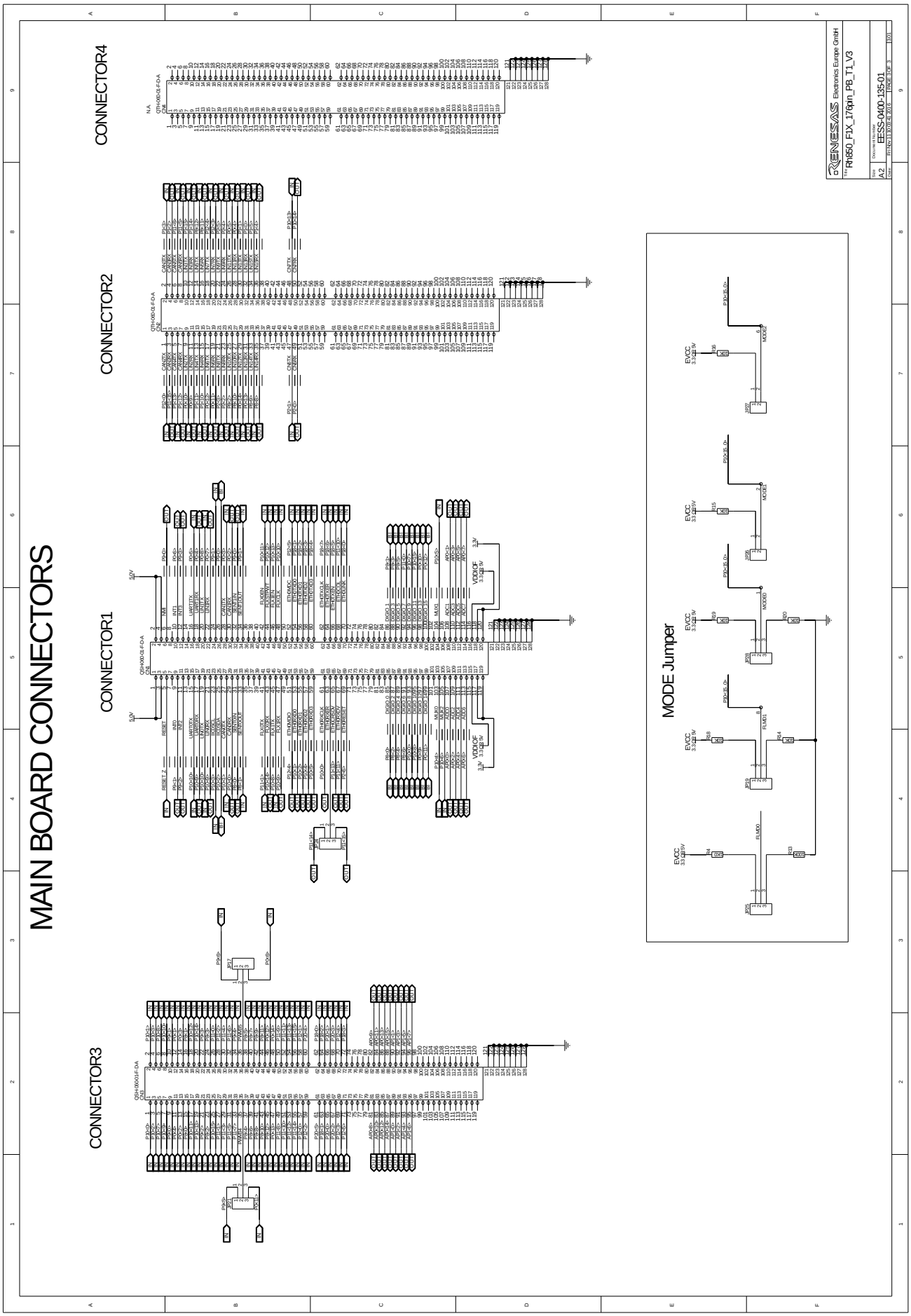
This chapter shows the schematics of the two available board versions:

- EESS-0400-135-01
- EESS-0400-135-02

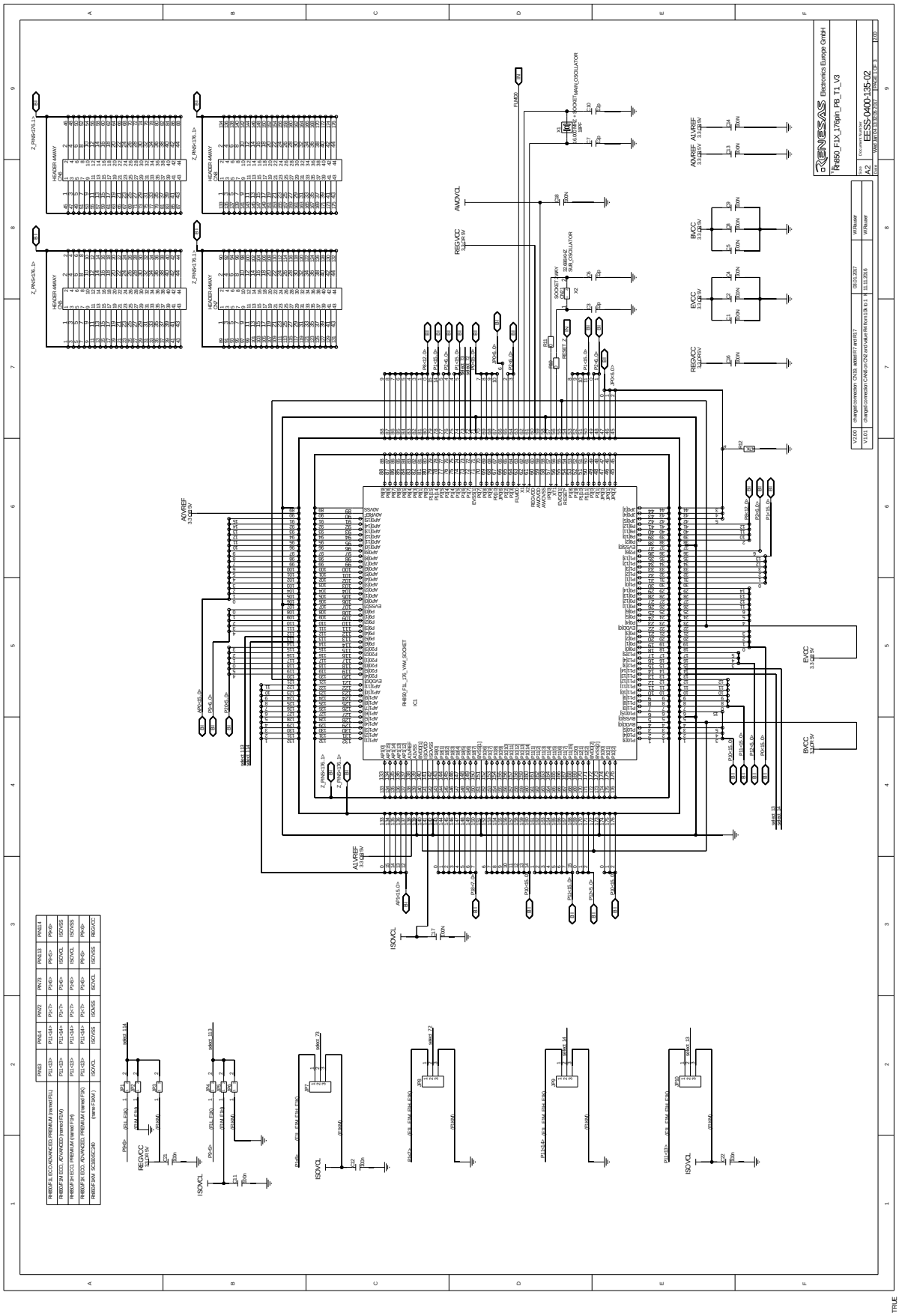
11.1 Schematic for EESS-0400-135-01

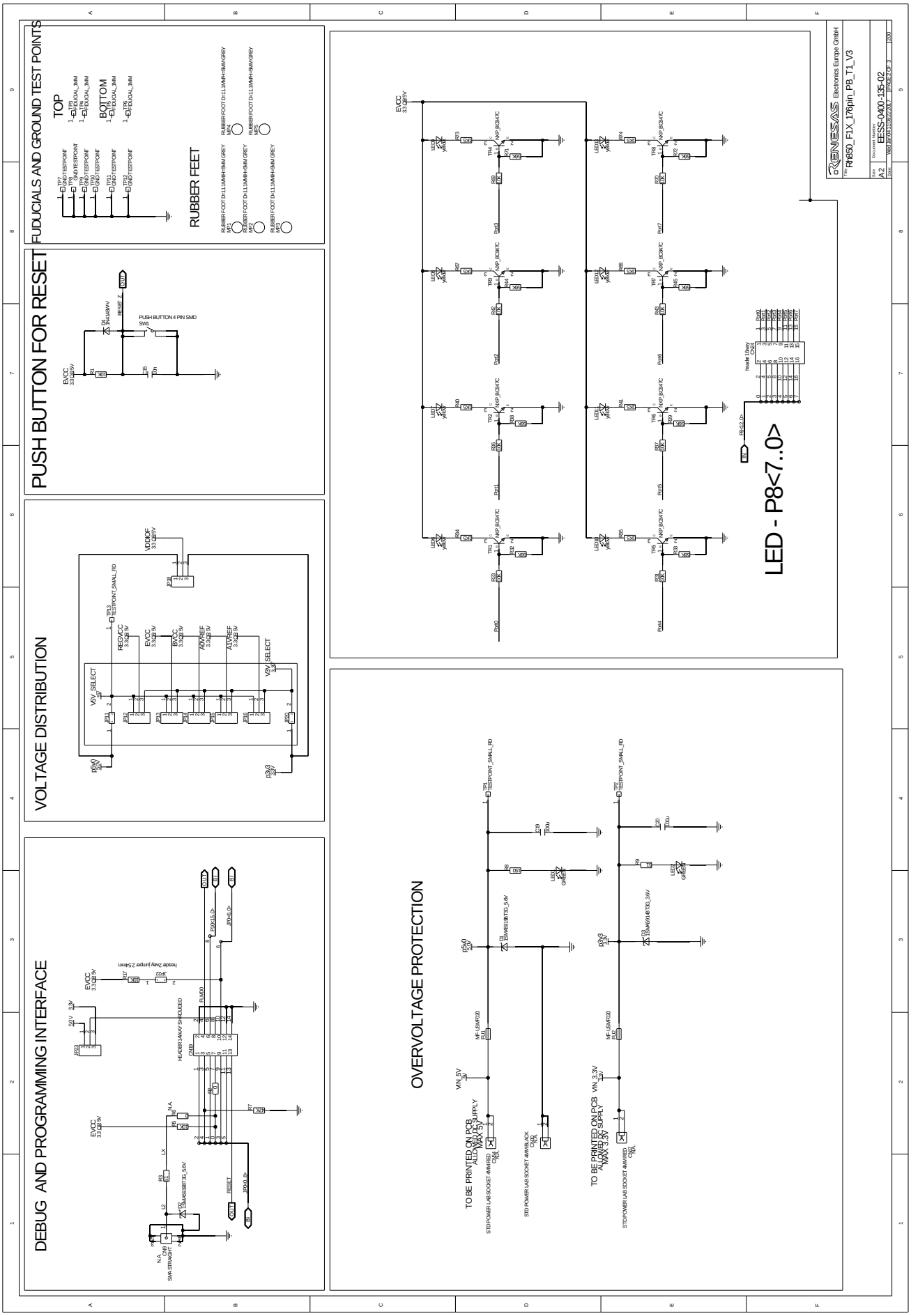


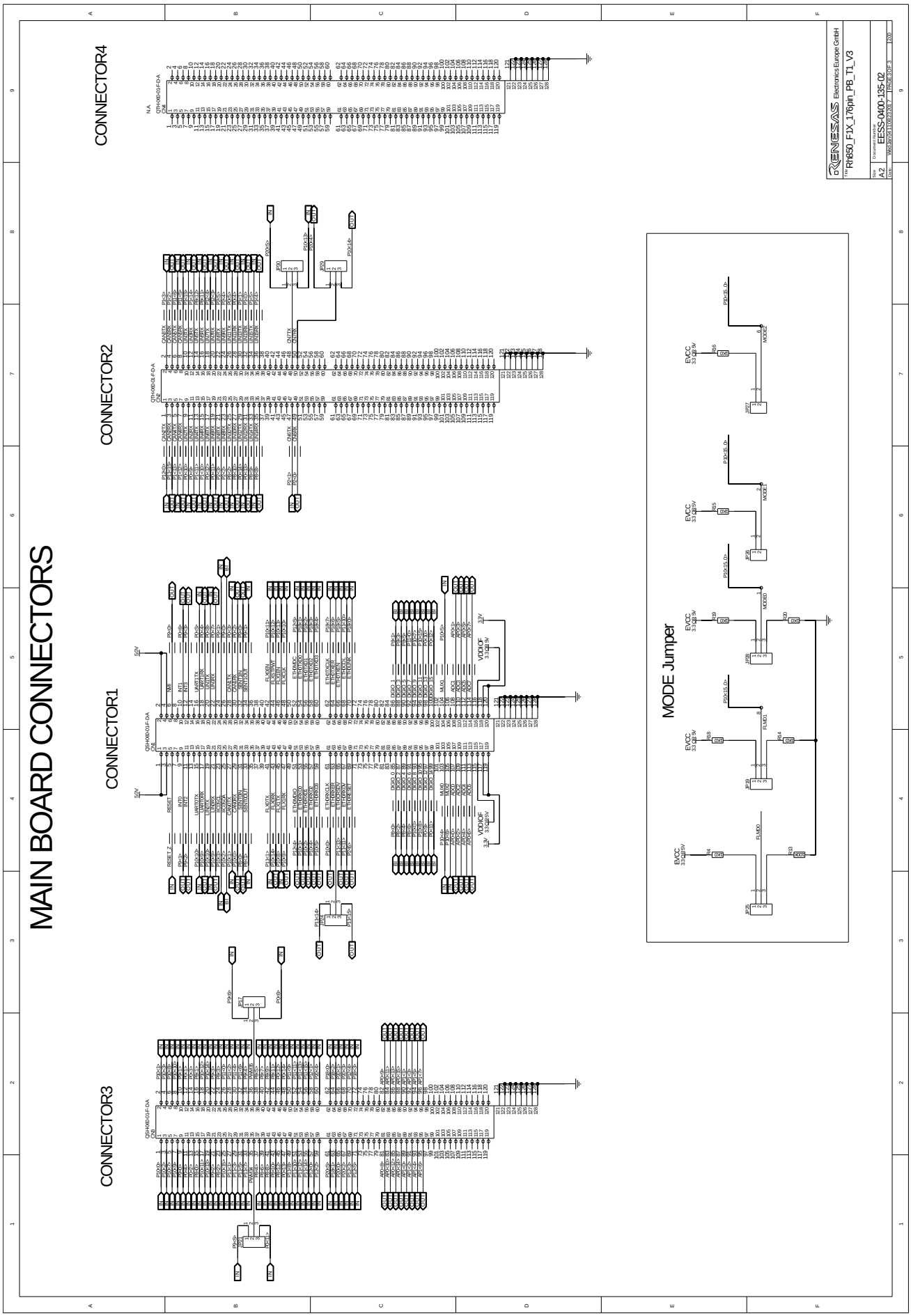

FUDUCIALS AND GROUND TEST POINTS
TOP
BOTTOM
RUBBER FEET
PUSH BUTTON FOR RESET
VOLTAGE DISTRIBUTION
DEBUG AND PROGRAMMING INTERFACE
OVERVOLTAGE PROTECTION
LED - P8<7..0>
RENESAS Electronics Europe GmbH
RH850_F1X_176pin_PB_T1_V3
R7F7016903AFGK
HSBS-0400-135-01
A2


MAIN BOARD CONNECTORS
CONNECTOR1
CONNECTOR2
CONNECTOR3
CONNECTOR4
MODE Jumper
RENESAS Electronics Europe GmbH
Rh850_F1X_176pin_PB_T1_V3
EESS-0400-135-01

11.2 Schematic for EESS-0400-135-02




FUDUCIALS AND GROUND TEST POINTS
TOP
BOTTOM
RUBBER FEET
PUSH BUTTON FOR RESET
VOLTAGE DISTRIBUTION
DEBUG AND PROGRAMMING INTERFACE
OVERVOLTAGE PROTECTION
LED - P8<7..0>
RENESAS Electronics Europe GmbH
RH850_F1X_176pin_PB_T1_V3
FES-0400-135-02


MAIN BOARD CONNECTORS
CONNECTOR4
CONNECTOR2
CONNECTOR1
CONNECTOR3
MODE Jumper
RENESAS Electronics Europe GmbH
RH850_F1X_176pin_PB_T1_V3
RTE-5400-135-02

Chapter 12 Revision History

The table provides information about the major changes of the document versions.

Date	Version	Description
2016-11-14	1.00	Initial release
2017-06-06	1.10	• Corrected jumper setting of JP25 (FLMD0) in figure 3 (chapter 3). • Added chapter 9 ‘Precautions’. • Added schematic for EESS-0400-135-01 in chapter 11
2017-10-20	1.20	• Added chapter 9.6 • Corrected signal assignment of connector CN1 in chapter 7.1.1 • Added comments for specific implementations of the EESS-0400-135-01 board version

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