User Manual

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RH850 Evaluation Platform

RH850/E2x-373BGA PiggyBack Board T2

Y-RH850-E2X-373PIN-PB-T2-V3

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Chapter 1 Introduction

The RH850/E2x Application Board is part of the RH850 Evaluation Platform and serves as a simple and easy to use platform for evaluating the features and performance of Renesas Electronics 32-bit RH850/E2x microcontrollers. RH850/E2x microcontrollers in a BGA-373 package can be used together with this board by utilizing the separately available mount adapter (Y-LSPACK373A2521RE01). Main purpose of this board is to mount the separately available emulation adapter boards (Y-RH850-E2X-40NM-EMU-ADAPTER or RTE7702012EAB00000J) via the exchange adapter boards (Y-RH850-E2X-EA-373PIN or RTE7702011CBG373T000J).

The PiggyBack board (Y-RH850-E2X-373PIN-PB-T2-V3) can be used as standalone board or can be mated with any mainboard (Y-RH850-X1X-MB-Tx-Vx or Y-RH850-X2X-MB-Tx-Vx) of the RH850 Evaluation Platform for extended functionality.

Main features:

- Target connector socket
- Standalone operation of the board
- Direct supply of device voltage (typ. 5V, 3.3V and 1.28V/1.12V[*1]) as well as generation of the core voltage (typ. 1.28V/1.12V[*1]) from an on-board voltage regulator
- Device programming capability
- Device debugging capability
- Pin headers for direct access to the functional device pins
- Reset switch
- MainOSC circuitry
- Connectors to Mainboard
- Operating temperature from 0°C to +40°C

This document describes the functionality provided by the PiggyBack board and guides the user through its operation.

For details regarding the operation of the microcontroller, refer to the corresponding User's Manual.

Note 1: Please refer to **Chapter 3 'Power supply'** for more details.

Chapter 2 Overview

2.1 Overview of Y-RH850-E2X-373PIN-PB-T2-V3

Figures 1 and 2 provide a schematic view of the Y-RH850-E2X-373PIN-PB-T2-V3 PiggyBack board.

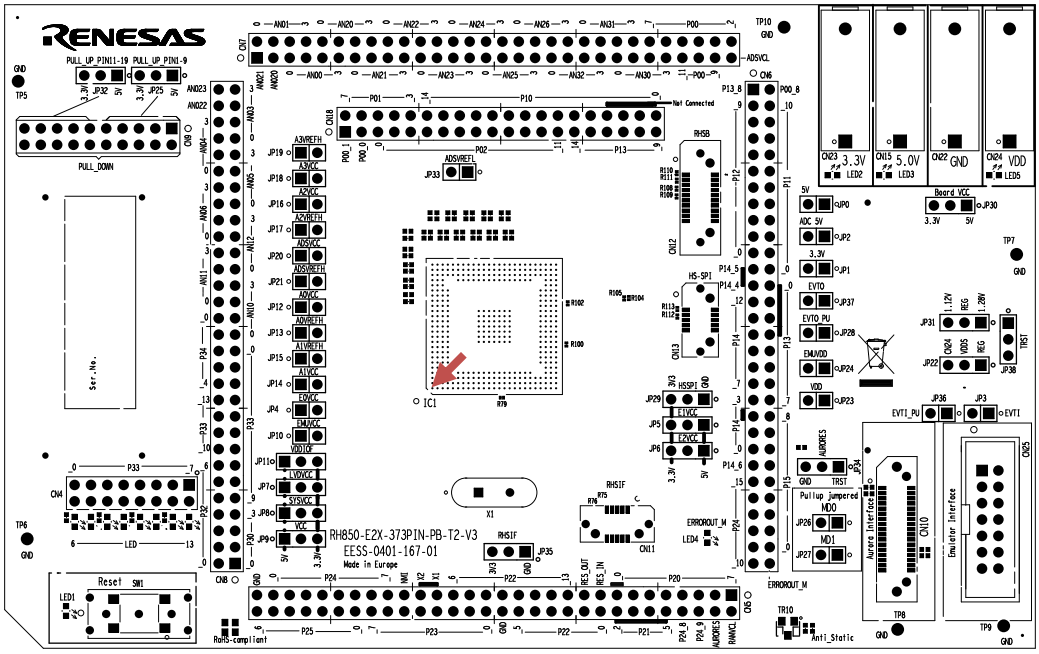


Figure 1 PiggyBack Board Top View

The red arrow denotes the position of socket pin #1.

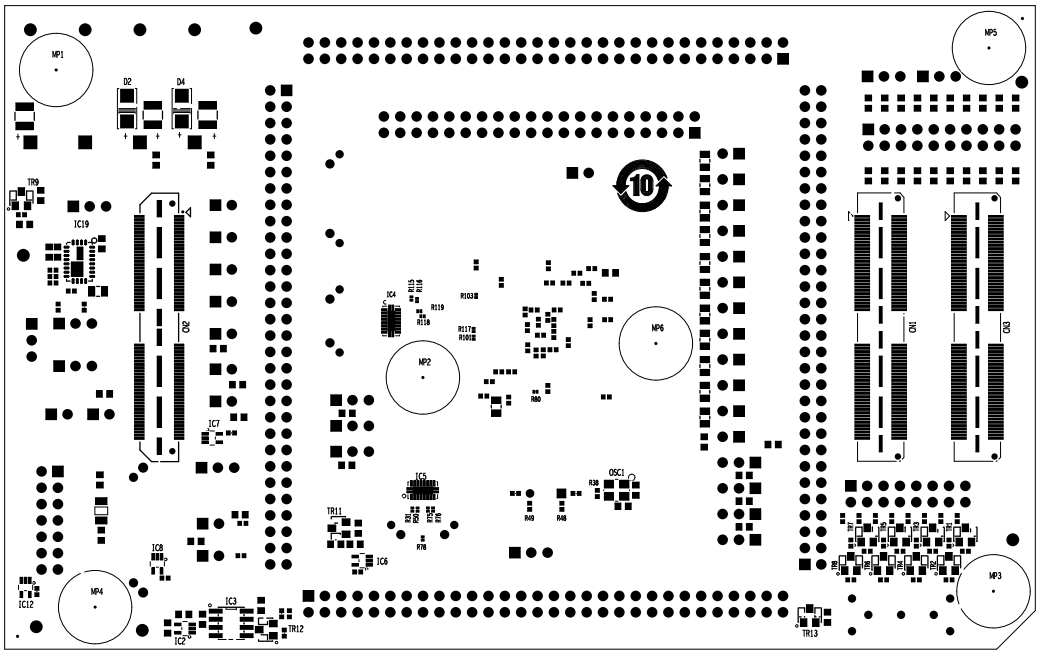


Figure 2 PiggyBack Board Bottom View

2.2 Mounting of the Emulation Adapter Board

The Y-RH850-E2X-373PIN-PB-T2-V3 PiggyBack board can be mated together with a RH850/E2x Emulation Adapter board. For this purpose, Exchange Adapter boards are available.

CAUTION: *Due to the symmetrical nature of a BGA package, there is no protection against erroneous polarity. Therefore, the following instruction must be followed carefully to not damage the boards and devices.*

The #1 pin of the PiggyBack board (see red arrow in **Figure 1**) must be aligned with the #1 pin of the Emulation Adapter and the Exchange Adapter board (see red arrow in **Figure 3** and **Figure 4**).

Thus, compared to the PiggyBack board, the Emulation Adapter board must be mounted with a clock-wise rotation of 90° as depicted in **Figure 3** and **Figure 4**.

Note: The emulation adapter board 'Y-RH850-E2X-40NM-EMU-ADAPTER' is equipped with the RH850/E2x-FCC1 device in BGA600 package. Please note that the corresponding Exchange Adapter board 'Y-RH850-E2X-EA-373PIN' is not shown in **Figure 3**.

The emulation adapter board 'RTE7702012EAB00000J' is equipped with the RH850/E2x-FCC2 device in BGA600 package. Please note that the corresponding Exchange Adapter board 'RTE7702011CBG373T000J' is not shown in **Figure 4**.

Please refer to the dedicated users' manuals of the products for more details.

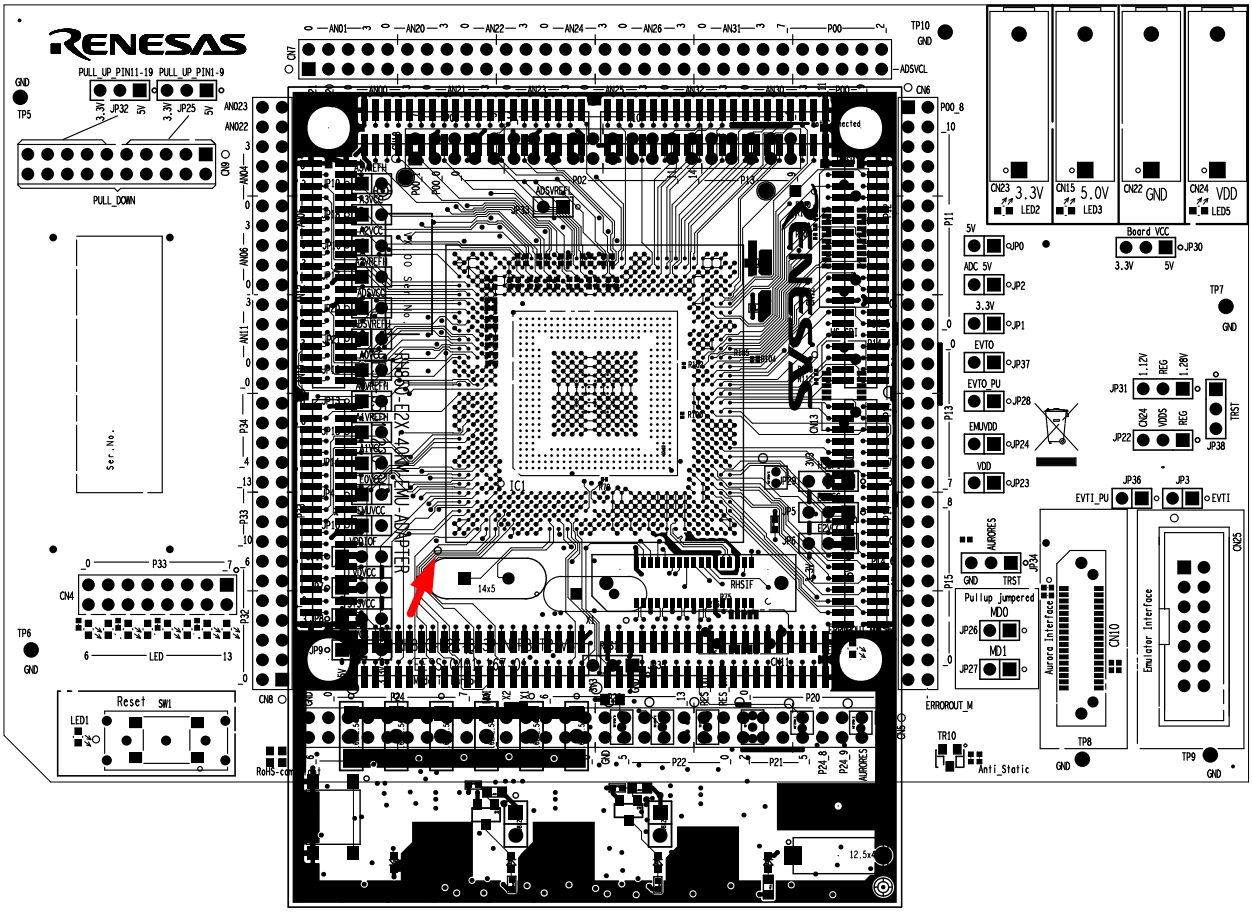


Figure 3 Alignment of PiggyBack and Emulation Adapter Board (Y-RH850-E2X-40NM-EMU-ADAPTER)

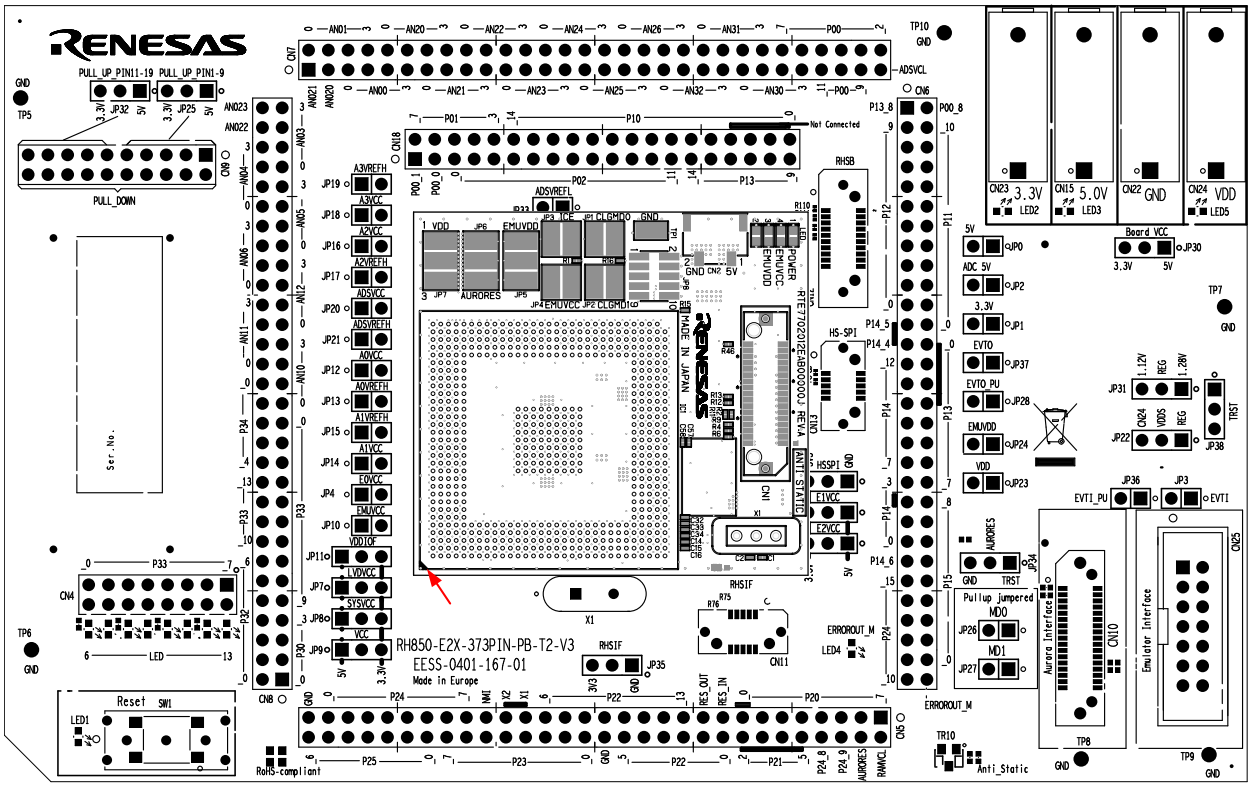


Figure 4 Alignment of PiggyBack and Emulation Adapter Board (RTE7702012EAB00000J)

Chapter 3 Power supply

3.1 Board power connection

For operation of the device, a supply voltage must be connected to the board. There are several possibilities to power the device.

Within this document the following voltages are considered as ‘typical’ values:

Voltage1 = 5V

Voltage2 = 3.3V

Voltage3 = 1.28V or 1.12V

Direct voltage supply

Three different voltages can be supplied to the board.

The following connectors are available to supply those voltages directly:

- Four 4mm ‘banana-type’ connectors:
  - Three red connectors for voltages 5V (CN15), 3.3V (CN23) and 1.28V/1.12V (CN24).
  - A black connector for ground (GND) connection (CN22).
  Note: The four connectors are supplied with the board but not assembled.

For details about voltage distribution, refer to **Chapter 3.2 ‘Voltage distribution’**.

Supply by Mainboard

In case the PiggyBack board is mounted on a Mainboard, the 5V and 3.3V is supplied by the on-board regulator of the Mainboard.

CAUTION: *Do not supply 5V or 3.3V directly to the PiggyBack board in case it is mounted on the Mainboard.*

For each of the voltages, 5V, 3.3V and 1.28V/1.12V a green LED (LED3, LED2 and LED5, respectively) is available to signal that the related voltage is available on the PiggyBack board. The corresponding LEDs are placed directly beneath the connectors of the related voltage.

3.2 Voltage distribution

The table shows the required device power supply pins. For detailed explanation of their function and specification, please refer to the user documentation of the corresponding device:

Table 1 Available Power Domains for MCU

Device Supply Pin
SYSVCC
VCC
EnVCC (n = 0-2)
LVDVCC
EMUVCC
AnVCC (n = 0-3)
AnVREFH (n = 0-3)
ADSVCC
ADSVREFH
EMUVDD
VDD

Additional power supply for the Mainboard and the operation of the PiggyBack board can be selected:

Table 2 Available Power Domains for Board Operation

Supply voltage	Function
VDDIOF	IO supply voltage for components located on a connected mainboard.
BOARD_VCC	Source for all devices (e.g. voltage regulator) on the PiggyBack board

The following figure shows the configurable voltage distribution on the PiggyBack board.

- Jumpers can interrupt all power supply lines. This provides the possibility to measure the current consumption of each individual power domain of the device (JP4 – 10, JP12 – 21 and JP23 – 24).
- The IO supply voltage for the Mainboard (VDDIOF) can be connected via jumper JP11 to 5V or 3.3V if the PiggyBack board is mounted on a Mainboard.
- VDD and EMUVDD can be powered either directly from the ‘banana-type’ connector (CN24) or by an on-board voltage regulator.
- The source for the on-board voltage regulator, as well as the source for all on-board devices (BOARD_VCC) needs to be configured via jumper JP30 to either 5V or 3.3V.
- The source for VDD is selectable by the jumper JP22. The jumper JP23 and JP24 connect the voltage, configured by JP22 with the VDD and EMUVDD pins, respectively.

- With jumper JP31 the output voltage of the on-board voltage regulator can be configured to either 1.28V or 1.12V depending on the requirement of the used device. Please refer to the HW user's manual for the detailed specification.

  Note: Although typically 1.25V or 1.09V is specified as the input voltage to VDD and EMUVDD the output of the voltage regulator IC19 is slightly increased to 1.28V or 1.12V, respectively (see **Chapter 11 'Schematic'**). With this sufficient high voltage is applied to the device pins, even in case of any possible voltage drops.

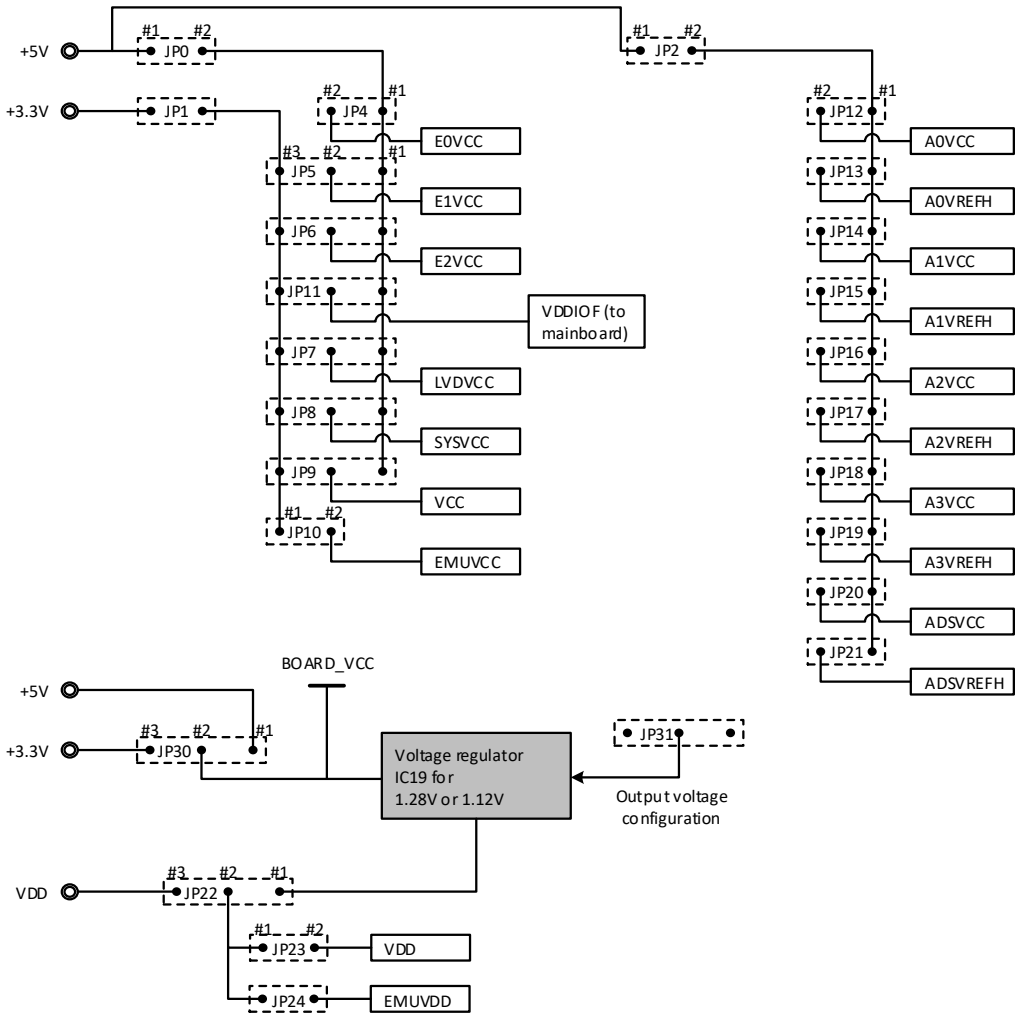


Figure 5 Voltage Distribution on the PiggyBack Board

For more details, please refer to **Chapter 11 'Schematic'**. For typical configuration of the jumpers, please refer to **Chapter 8 'Jumper Configuration'**.

Chapter 4 Clock sources

External crystal oscillators for the device clock supply are provided with the board.

4.1 MainOsc

A crystal or ceramic resonator can be mounted on socket X1.

A 20 MHz and 40MHz oscillator are supplied with the board.

The signals X1 (EXTAL) and X2 (XTAL) are by default not connected to a pin header to minimize disturbance on the resonator signal. If needed the signals can be connected to CN5 (pins #37 and 39) via connecting with 0Ohm resistances R48 and R49. For details, please refer to **Chapter 11 'Schematic'**.

4.2 Programmable Oscillator

It is possible to mount a programmable crystal oscillator on the PiggyBack board at OSC1. The available footprint and circuitry is designed for a SG-8002CE programmable crystal oscillator from Epson Toyocom. The output from this oscillator can be connected to port EXTAL via resistor R38. The SG-8002CE is neither mounted nor provided with the board. For details about the available circuitry, refer to **Chapter 11 'Schematic'**. A resonator mounted on socket X1 must not be used in parallel to another clock source.

Chapter 5 Debug and Programming interface

The signal ‘EVTO’ can be pulled up to ‘E0VCC’ via JP28. Please refer to the documentation of the used tool, whether this is needed.

The signal ‘EVTI’ can be pulled up to ‘E0VCC’ via JP36. Please refer to the documentation of the used tool, whether this is needed.

The signal ‘TRST’ can be pulled up to ‘SYSVCC’ or connected to the ‘TRST’ line of the used tool via jumper JP38.

For typical configuration of the jumpers, please refer to **Chapter 8 ‘Jumper Configuration’**.

5.1 14 Pin Debug Connector

For connection of the microcontroller to debug and flash programming tools, the connector CN25 with 14 pins is available.

The signal connection of the connector CN25 is shown in the table below:

Table 3 Pin Assignment of CN25

CN25 Pin	Function
1	TCK
2	GND
3	JP38 #3 (TRST) *1
4	MD0
5	TDO
6	-
7	TDI
8	VCC
9	TMS
10	EVTO (P33_9) *2
11	DRDY
12	GND
13	RES_IN
14	GND

Note 1: For connecting CN25 pin #3 with the TRST pin of the MCU, JP38 pins #2 and #3 needs to be closed.

Note 2: For connecting CN25 pin #10 with the pin P33_9 of the MCU, JP37 needs to be closed. Please note that additionally P33_9 port function needs to be assigned to EVTO.

For more details, please refer to **Chapter 11 ‘Schematic’**. For typical configuration of the jumpers, please refer to **Chapter 8 ‘Jumper Configuration’**.

5.2 34 Pin Aurora Connector

For connection of the microcontroller to a trace tool CN10 is available.

The signal connection of the connector CN10 is shown in the table below:

Table 4 Pin Assignment of CN10

CN10 Pin	Function		CN10 Pin	Function
1	TODP0		2	VCC
3	TODN0		4	TCK
5	GND		6	TMS
7	Reserved (NC)		8	TDI
9	Reserved (NC)		10	TDO
11	GND		12	TRST
13	Reserved (NC)		14	MD0
15	Reserved (NC)		16	EVTI (P33_8) *1
17	GND		18	EVTO (P33_9) *2
19	Reserved (NC)		20	MD1
21	Reserved (NC)		22	RES_IN
23	GND		24	GND
25	Reserved (NC)		26	CICREFP
27	WDTDIS (NC)		28	CICREFN
29	GND		30	GND
31	ETK-BREQ (NC)		32	DRDY
33	ETK-BGNT (NC)		34	RES_OUT

Access to the signal AURORES is possible via JP34. With this jumper AURORES can also be connected to TRST or pulled-down to GND

Note 1: For connecting CN10 pin #16 with the pin P33_8 of the MCU JP3 needs to be closed. Please note that additionally P33_8 port function needs to be assigned to ‘EVTI’.
Additionally, if ‘EVTI’ function is not used the connected port pin P33_8 could be used as GPIO instead. Then the signal must be disconnected via JP3.

Note 2: For connecting CN10 pin #18 with the pin P33_9 of the MCU JP37 needs to be closed. Please note that additionally P33_9 port function needs to be assigned to ‘EVTO’.
Additionally, if ‘EVTO’ function is not used the connected port pin P33_9 could be used as GPIO instead. Then the signal must be disconnected via JP37.

For more details, please refer to **Chapter 11 ‘Schematic’**. For typical configuration of the jumpers, please refer to **Chapter 8 ‘Jumper Configuration’**.

Chapter 6 Connectors for ports of device

Connection to most functional pins of the devices is possible via the connectors CN5 to CN8 and CN18.
Some functions might not be available on the pin headers, e.g. high frequency signals, as this would disturb the integrity of such signals. The actual voltage levels of the various voltage domains can be measured at the individual jumpers. For more details, please refer to **sec. 3.2 'Voltage distribution'** and **Chapter 11 'Schematic'.**

CAUTION: *The pin headers are directly connected to the pins of the device. Therefore, special care must be taken to avoid any electrostatic or other damage to the device.*

6.1 Toggle Switch for RESET

To issue a RESET to the device, the toggle switch SW1 is available.

The switch is a Nidec Copal Electronics Miniature Toggle Switch 'BT1H-2M4-Z' with two positions to issue a RESET.

The switching function is depicted in **Figure 6**. To issue a RESET to the device the switch needs to be toggled either to the left or to the right side. To the right side – 'ON' – a static RESET can be applied, while on the left side – '(ON)' – a momentary RESET is applied, and the switch will return into the 'OFF' position again. Please note that the position of the switch is defined from the side of the part number marking, which is highlighted with a red arrow.

Switching function / Part No.	Viewed from part No. marking side		
			
★BT1H-2M4-Z	(ON)	OFF	ON
Connecting terminals	2—1	—	2—3

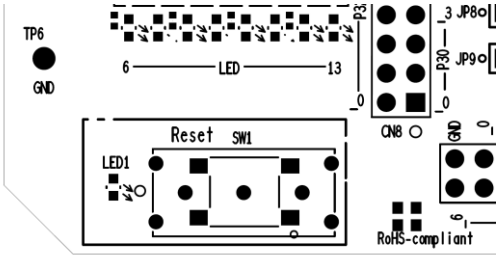


Figure 6 RESET Switching Function

LED1 is indicating the function of the switch, i.e. LED1 illuminates when the RESET is asserted by the switch. Please note that LED1 cannot indicate a RESET by another source e.g. a connected tool.

6.2 Mode Selection

The PiggyBack Board gives the possibility to configure the following mode pins

- MD0 via jumper JP26
- MD1 via jumper JP27

To apply "High" to the mode pins, the corresponding jumpers can be set.

CAUTION: *Be careful in configuration of mode related pins, as wrong configuration can cause irregular behavior of the devices. Be sure to check the corresponding User's Manual for details, which modes can be selected for the used device.*

6.3 Connectors to Mainboard

Three connectors (CN1, CN2 and CN3) are available to connect the PiggyBack board to a Mainboard. Regarding the function on the Mainboard, please refer to the UM of any supported Mainboard (Y-RH850-X1X-MB-Tx-Vx or Y-RH850-X2x-MB-Tx-Vx) of the RH850 Evaluation Platform.

For details about the signal assignment to the connectors, please refer to **Chapter 11 'Schematic'**.

6.3.1 Assignment of CAN Pins

The available Mainboards (Y-RH850-X1X-MB-Tx-Vx or Y-RH850-X2x-MB-Tx-Vx) of the RH850 Evaluation Platform provide connectors for CAN communication. The channel number of the Mainboards does not necessarily match the channel number of RH850/E2x devices.

The following table shows the assignment.

Table 5 CAN Function Assignment

Mainboard	PiggyBack Board (MCU)	
	Port Pin	CAN Alternative Function
CAN0TX	P32_1	CTX2
CAN0RX	P32_0	CRX2
CAN1TX	P15_2	CTX1
CAN1RX	P15_1	CRX1
CAN2TX	P02_0	CTX0
CAN2RX	P02_2	CRX0
CAN3TX	P32_6	CTX3
CAN3RX	P32_4	CRX3
CAN4TX	P15_7	CTX4
CAN4RX	P15_8	CRX4
CAN5TX	P15_5	CTX5
CAN5RX	P15_3	CRX5

6.4 RHSIF I/F

CN11 is available to connect to the RHSIF I/F signals of the device. The connector is a Samtec 'ERF8-005-05.0-L-DV-L-TR' type connector and the following table shows the signal assignment.

Table 6 RHSIF I/F Pin Assignment

CN11 Pin	Function*1	Device Pin*1	Function*2	Device Pin*2		CN11 Pin	Function	Device Pin
1	HSIF0_TXDP	P21_5	HSIF0_RXDP	P21_3		2	GND	-
3	HSIF0_TXDN	P21_4	HSIF0_RXDN	P21_2		4	GND	-
5	GND	-	GND	-		6	HSIF0_REFCLK	P20_0
7	HSIF0_RXDP	P21_3	HSIF0_TXDP	P21_5		8	GND	-
9	HSIF0_RXDN	P21_2	HSIF0_TXDN	P21_4		10	GND	-
11	Common shield GND					12	Common shield GND	

Note 1 & 2: The function of CN11 pins 1, 3, 7 and 9 depend on the configuration of JP35

- JP35 pins 1 and 2 connected: Function *1 is effective
- JP35 pins 2 and 3 connected: Function *2 is effective

All signals are by default not connected to a pin header to minimize disturbance on the signal. If needed the signals can be connected to CN5 (pins #10, 12 and 14 – 16) via connecting with 0Ohm resistances R31, R50, R75, R76 and R78. For details, please refer to **Chapter 11 'Schematic'**.

6.5 HS-SPI I/F

CN13 is available to connect to the HS-SPI I/F signals of the device. The connector is a Samtec 'ERF8-005-05.0-L-DV-L-TR' type connector and the following table shows the signal assignment.

Table 7 HS-SPI I/F Pin Assignment

CN13 Pin	Function	Device Pin		CN13 Pin	Function*1	Device Pin*1	Function*2	Device Pin*2
1	CLKP	P13_1		2	TXDP	P13_3	RXDP	P14_4
3	CLKN	P13_0		4	TXDN	P13_2	RXDN	P14_5
5	GND	-		6	GND	-	GND	-
7	GND	-		8	RXDP	P14_4	TXDP	P13_3
9	SSL/SSLI*3	P14_2		10	RXDN	P14_5	TXDN	P13_2
11	Common shield GND			12	Common shield GND			

Note 1 & 2: The function of CN13 pins 2, 4, 8 and 10 depend on the configuration of JP29

- JP29 pins 1 and 2 connected: Function *1 is effective
- JP29 pins 2 and 3 connected: Function *2 is effective

Note 3: The function of the pin P14_2 can be configured in the used MCU device. For details, please refer to the HW user's manual of the used device.

All signals (except SSL/SSLI on CN6 #41) are by default not connected to a pin header to minimize disturbance on the signal. If needed the signals can be connected to CN6 (pins #23, 25, 26, 28, 30, and 32) via connecting with 0Ohm resistances R112, R113, R115, R116, R118 and R119. For details, please refer to **Chapter 11 'Schematic'**.

6.6 RHSB I/F

CN12 is available to connect to the RHSB I/F signals of the device. The connector is a Samtec 'ERF8-010-05.0-L-DV-L-TR' type connector and the following table shows the signal assignment

Table 8 RHSB I/F Pin Assignment

CN12 Pin	Function	Device Pin	CN12 Pin	Function	Device Pin
1	RHSB1FCLN	P10_1	2	RHSB1CSD0	P10_7
3	RHSB1FCLP	P10_0	4	RHSB1EMRG	P12_0
5	GND	-	6	RHSB1SI0	P12_2
7	RHSB1SON	P10_3	8	RHSB1SI1	P12_4
9	RHSB1SOP	P10_2	10	RHSB1CSD1	P10_6
11	RHSB0FCLN	P13_0	12	RHSB0CSD0	P14_7
13	RHSB0FCLP	P13_1	14	RHSB0EMRG	P12_7
15	GND	-	16	RHSB0SI0	P12_3
17	RHSB0SON	P13_2[*1]	18	RHSB0SI1	P12_1
19	RHSB0SOP	P13_3[*1]	20	RHSB0CSD1	P12_5
21	Common shield GND		22	Common shield GND	

Note 1: By default, these signals are not directly connected to the corresponding device pins. To use these signals for the RHSB I/F CN12 pins #17 and #19 must be connected to the device via 0Ohm resistances R104 and R105. In case of using the HS-SPI I/F (refer to section **6.5**), it is recommended to not apply the latter resistances. This it to minimize signal disturbance. For details, please refer to **Chapter 11 'Schematic'**.

The signals assigned to CN12 pins #1, 3, 7, 9, 17 and 19 are by default not connected to a pin header to minimize disturbance on the signal. If needed the signals can be connected to CN6 (pins #30 and 32) and CN18 (pins #34, 36, 38 and 40) via connecting with 0Ohm resistances R108 – R111 and R115 and R116. Please also consider above note 1. For details, please refer to **Chapter 11 'Schematic'**.

Chapter 7 Other circuitry

7.1 Signaling for ERROROUT_M

A red LED (LED4) is available two indicate a “low” output signal from ERROROUT_M.

7.2 Pin Headers for Pull-Down and Pull-Up

A connector CN9 is available to enable easy connection to 3.3V / 5V or GND via pull-up or pull-down resistances, respectively.

Hereby uneven pins from 1 to 19 (in total ten) are configured as pull-up pin headers, while the even numbers from 2 to 20 (in total ten) can be used for pull-down. JP25 and JP32 configure the voltage connected to the uneven pins to 3.3V or 5V. JP25 configures uneven pins 1 – 9 and JP32 configures uneven pins 11 – 19.

By connecting device port pins from CN5 – 8 and CN18 to CN9 it is therefore possible to pull a desired port pin to “Low” or “High”.

7.3 Signaling LEDs

Eight LEDs are provided to allow visual observation of the output state of device pins. Device pins P33_0 to P33_7 are connected to the uneven pins 15 to 1 of the pin header CN4, while the LEDs 6 to 13 are connected to the even pins 16 to 2, respectively. Thus, the LEDs can be connected to the device port pins P33_0 to P33_7 via jumper or to any device port pin by connecting directly to the even pin headers of CN4.

Chapter 8 Jumper Configuration

Jumper are available to configure the function of the board. This chapter describes the standard configuration, i.e. jumper setting for the intended devices, to enable basic operation. For a detailed explanation of the supported function of the used device, please refer to the corresponding HW user's manual.

Note: In particular, the section "11.3 Example of Power Supply Connection" of the corresponding RH850/E2x HW user's manual should be followed to check valid combination of voltages.

8.1 Jumper Configuration without Emulation Adapter Board 'Y-RH850-E2X-40NM-EMU-ADAPTER'

If the board is used as standalone, with a mainboard or together with the emulation adapter board 'RTE7702012EAB00000J', the following **Table 9** must be followed.

Table 9 Recommended Jumper Settings

Purpose	Jumper #	Device			
		RH850/E2M in BGA373		RH850/E2H in BGA373	
		FCC1 for E2M	E2M	FCC2 for E2H	E2H
5.0V Main	0	o	o	o	o
3.3V Main*1	1	o (opt)	- (opt)	o (opt)	- (opt)
5.0V Analog Main	2	o	o	o	o
EVTI Connect*4	3	- (opt)	- (opt)	- (opt)	- (opt)
E0VCC	4	o	o	o	o
E1VCC Config	5	#1-#2	#1-#2	#1-#2	#1-#2
E2VCC Config	6	#1-#2	#1-#2	#1-#2	#1-#2
LVDVCC Config	7	#1-#2	#1-#2	#1-#2	#1-#2
SYSVCC Config	8	#1-#2	#1-#2	#1-#2	#1-#2
VCC Config	9	#1-#2	#1-#2	#1-#2	#1-#2
EMUVCC*1	10	o (opt)	-	o (opt)	-
VDDIOF Config	11	#1-#2	#1-#2	#1-#2	#1-#2
A0VCC	12	o	o	o	o
A0VREFH	13	o	o	o	o
A1VCC	14	o	o	o	o
A1VREFH	15	o	o	o	o
A2VCC	16	o	o	o	o
A2VREFH	17	o	o	o	o
A3VCC	18	o	o	o	o
A3VREFH	19	o	o	o	o
ADSVCC	20	o	o	o	o
ADSVREFH	21	o	o	o	o
1.28V / 1.12V Source	22	#1-#2	#1-#2	#1-#2	#1-#2
VDD	23	o	o	o	o
EMUVDD*1	24	o (opt)	-	o (opt)	-
CN9 Pull-Up 1-9	25	- (opt)	- (opt)	- (opt)	- (opt)
MD0 Pull-Up	26	- (opt)	- (opt)	- (opt)	- (opt)
MD1 Pull-Up	27	- (opt)	- (opt)	- (opt)	- (opt)
EVTO Pull-Up*4	28	- (opt)	- (opt)	- (opt)	- (opt)
HS-SPI IC4 Config	29	- (opt)	- (opt)	- (opt)	- (opt)
BOARD_VCC Config*2	30	#1-#2	#1-#2	#1-#2	#1-#2
1.28V / 1.12V Config	31	#1-#2	#1-#2	#2-#3	#2-#3
CN9 Pull-Up 11-19	32	- (opt)	- (opt)	- (opt)	- (opt)

Purpose	Jumper #	Device			
		RH850/E2M in BGA373		RH850/E2H in BGA373	
		FCC1 for E2M	E2M	FCC2 for E2H	E2H
ADSVREFL Pull-Down	33	o	o	o	o
AURORES Config*3	34	#1-#2 (opt)	#2-#3 only	#1-#2 (opt)	#2-#3 only
RHSIF IC5 Config	35	- (opt)	- (opt)	- (opt)	- (opt)
EVTI Pull-Up*4	36	- (opt)	- (opt)	- (opt)	- (opt)
EVTO Connect*4	37	- (opt)	- (opt)	- (opt)	- (opt)
TRST Config	38	#2-#3	#2-#3	#2-#3	#2-#3

Note 1: Optionally for the FCC (emulation) devices only. If any of the FCC specific features are used (e.g. ERAM, Aurora Trace …) these jumpers need to be set.

Note 2: Set JP30 to same voltage as JP8 (SYSVCC Config).

Note 3: Optionally for the FCC (emulation) device only if Aurora Trace is used. Please refer to the user's documentation of the used tool for dedicated requirement.

Note 4: Whether EVTO and/or EVTI signals are supported and need to be pulled up depends on the used tool. Please clarify with your tool vendor about the specification.

The table has the following meaning:

- o: Jumper must be connected.
- o (opt): Recommended to be connected. Can be left open if not necessary for use case
- -: Jumper must be left open
- - (opt): Not mandatory to connect. Can be connected, if necessary for use case
- #x-#y: Connect the pins #x and #y for the standard configuration. Possible to configure depending on the use case and on the allowed specification of the used device.

A small circle near the jumper on the board and a rectangular representation of the pin in the overview picture in sec. **2.1** identifies the #1 pin of the jumper.

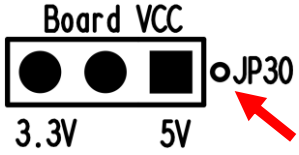


Figure 7 Identifying the Pin #1 at a Jumper

In this example (JP30), the pin #1 is on the right side. The red arrow highlights the marking circle.

8.2 Jumper Configuration with Emulation Adapter Board 'Y-RH850-E2X-40NM-EMU-ADAPTER'

If the board is combined with the emulation adapter board 'Y-RH850-E2X-40NM-EMU-ADAPTER', the restrictions shown in **Table 10** must be followed additionally.

Table 10 Recommended Jumper Settings for Combined Usage

Purpose	Emulation Adapter Board		Piggyback Board	
	Jumper #	Setting	Jumper #	Setting
E0VCC	4	-	4	o
E1VCC Config			5	#1-#2 only
E2VCC Config			6	#1-#2 only
LVDVCC Config	7	-	7	#1-#2
SYSVCC Config*1	8	-	8	#1-#2
VCC Config*1	9	-	9	#1-#2
A0VCC	12	-	12	o
A0VREFH			13	o
A1VCC			14	o
A1VREFH			15	o
A2VCC			16	o
A2VREFH			17	o
A3VCC			18	o
A3VREFH			19	o
ADSVCC	20	-	20	o
ADSVREFH			21	o
EMUVCC	n.a.	n.a.	10	-
EMUVDD	n.a.	n.a.	24	-

Note 1: Select the same voltage for SYSVCC and VCC (JP8 and JP9).

The table has the following meaning:

- o: Jumper must be connected.
- -: Jumper must be left open
- #x-#y: Connect the pins #x and #y for the standard configuration. Possible to configure depending on the use case and on the allowed specification of the used device.
- N.a.: Not applicable. Jumper is not available on the board. Hence, no setting is possible.

Chapter 9 Precautions

9.1 Power-Off Sequence

A dedicated sequence needs to be applied, when the power supplied to the board is turned off.

Please follow below sequence:

1. At first assert a RESET via SW1 and keep the Reset asserted.
2. Turn off the board power supply.
3. After power supply is shut down, put the SW1 to ‘OFF’ position.

For details how to apply a RESET, please refer to ‘**6.1 Toggle Switch for RESET’**.

9.2 Pin Function Assignment of HS-SPI Pins

To enable HS-SPI communication between two PiggyBack boards some of the signals need to be switched. Thus, the device pins P13_2, P13_3, P14_4 and P14_5 are connected to a differential multiplexer IC (IC4). The inputs of this device are only 3.3V tolerant.

It is therefore not allowed to configure above mentioned pins to GPIO or any alternative functions other than the LVDS functions used on this board. For details, please refer to section **6.5** and **Chapter 11 ‘Schematic’**, as well as the corresponding User’s Manual of the used device.

Chapter 10 Mechanical dimensions

All dimensions given in mm.

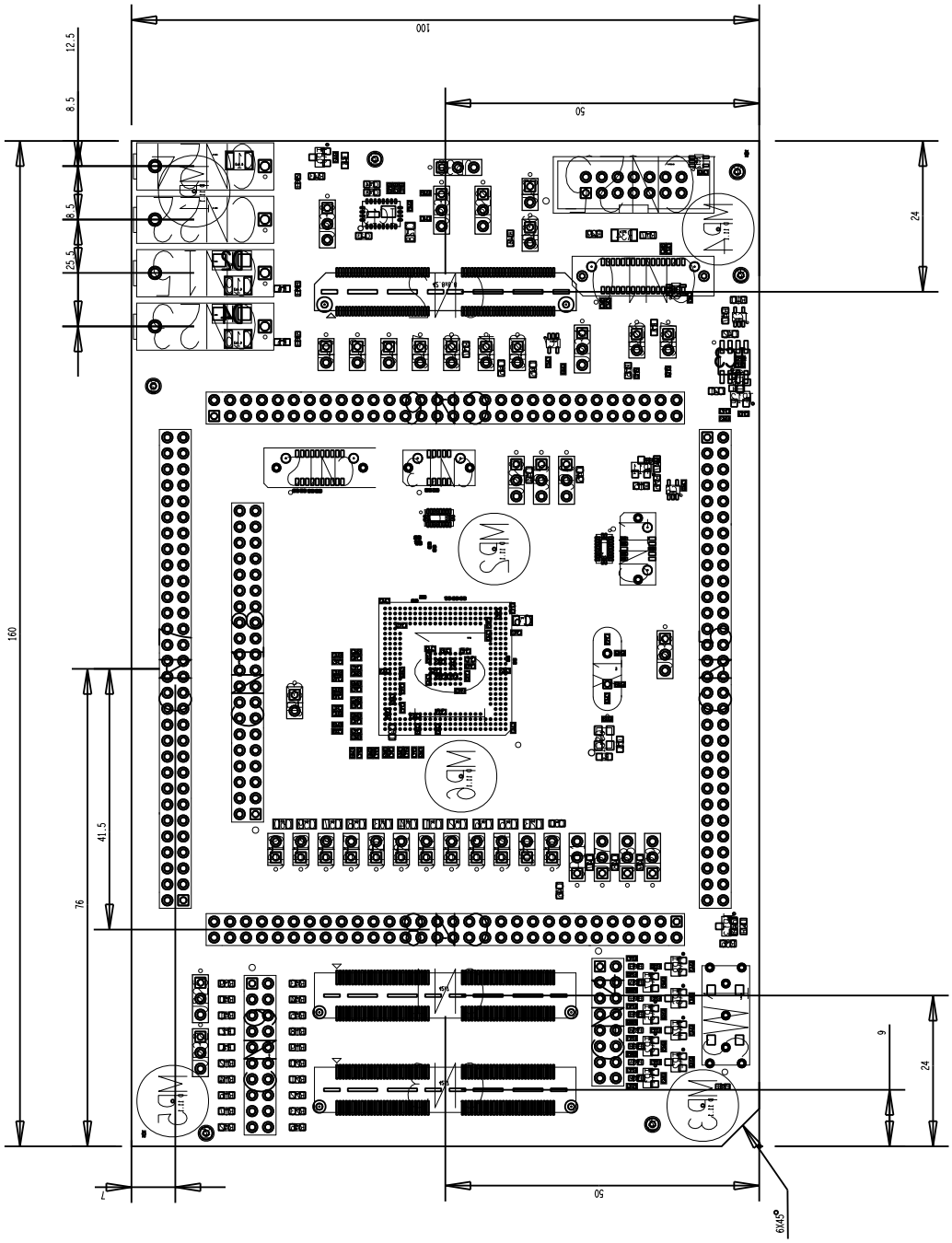


Figure 8 Dimensions of the PiggyBack Board

Chapter 11 Schematic

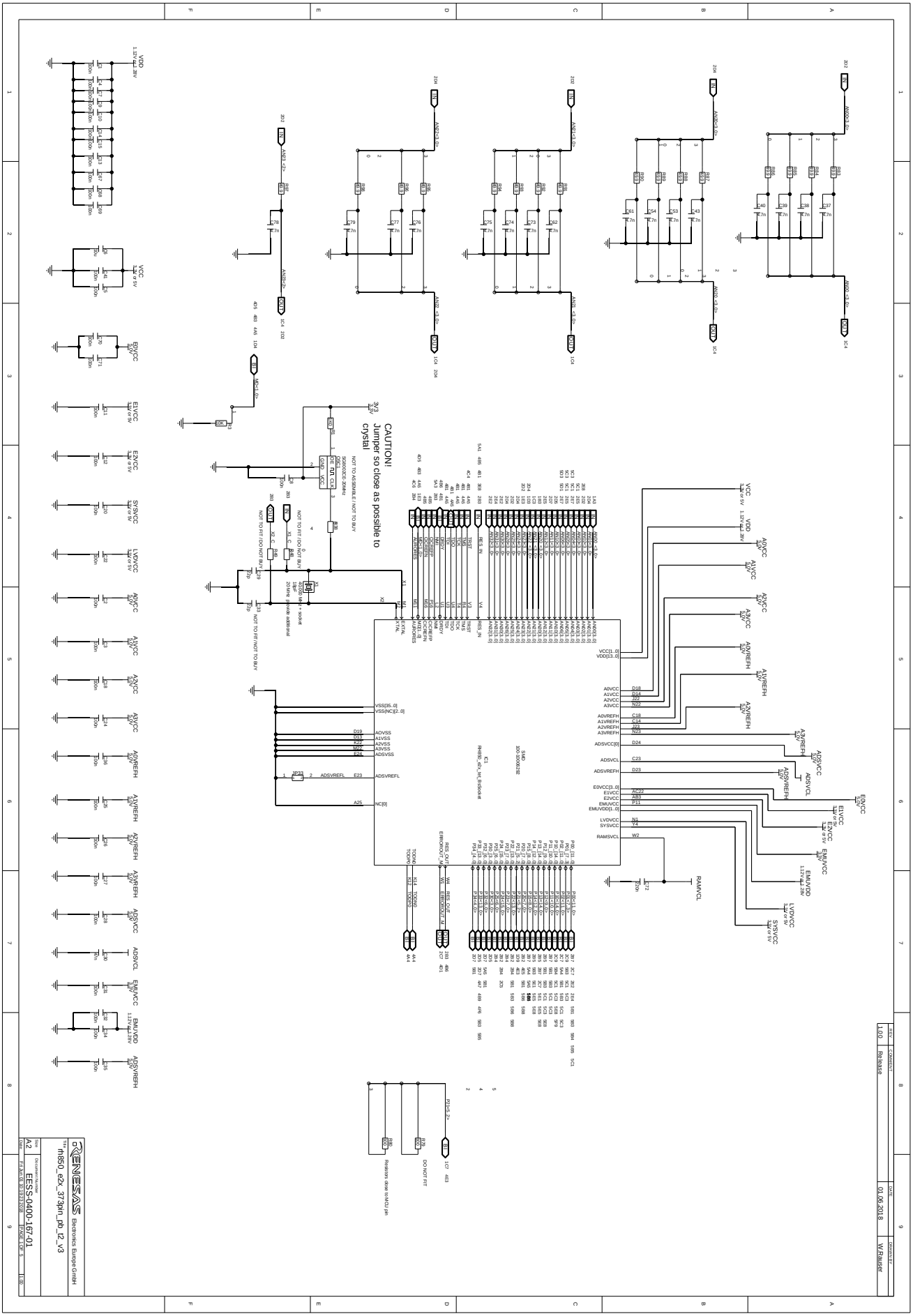
CAUTION: *The schematics shown in this document are not intended to be used as a reference for mass production. Any usage in an application design is in sole responsibility of the customer.*

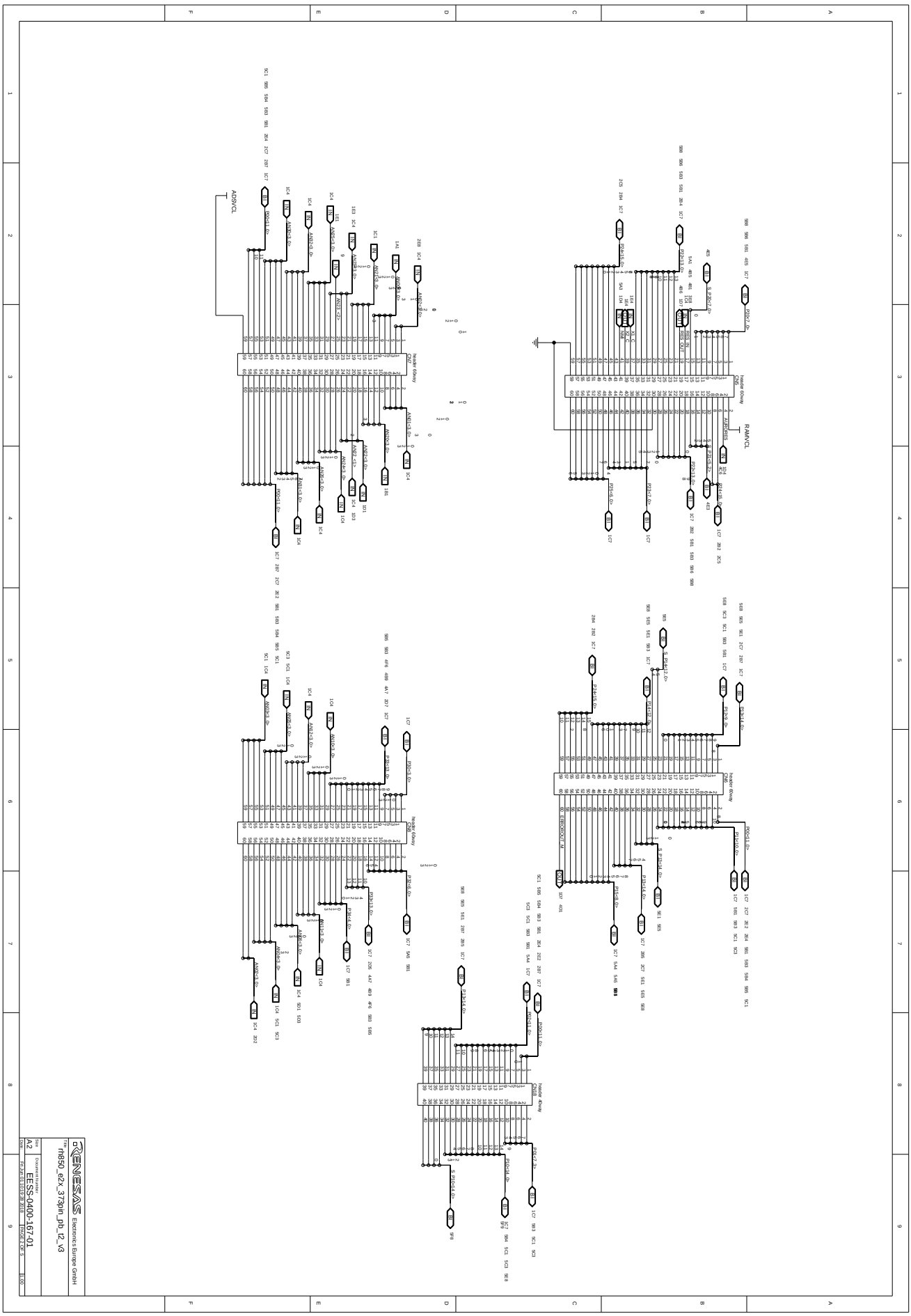
The following components described in the schematic are not provided with the board:

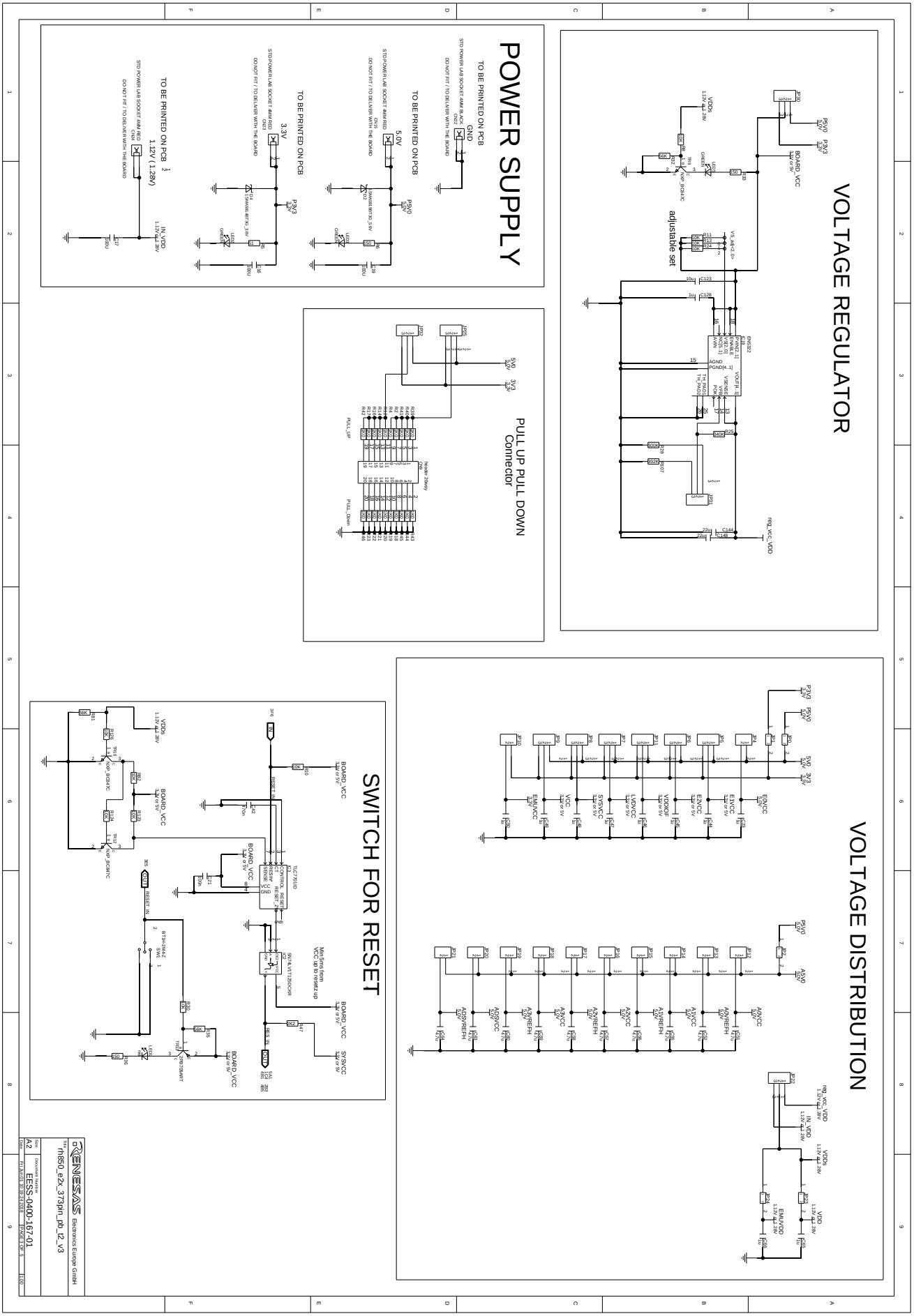
- Oscillator OSC1
- Capacitors C29 and C33
- Resistances
    - R48 and R49
    - R31, R50, R75, R76, R78, R79, R101, R108 – R113, R115, R116, R118 and R119

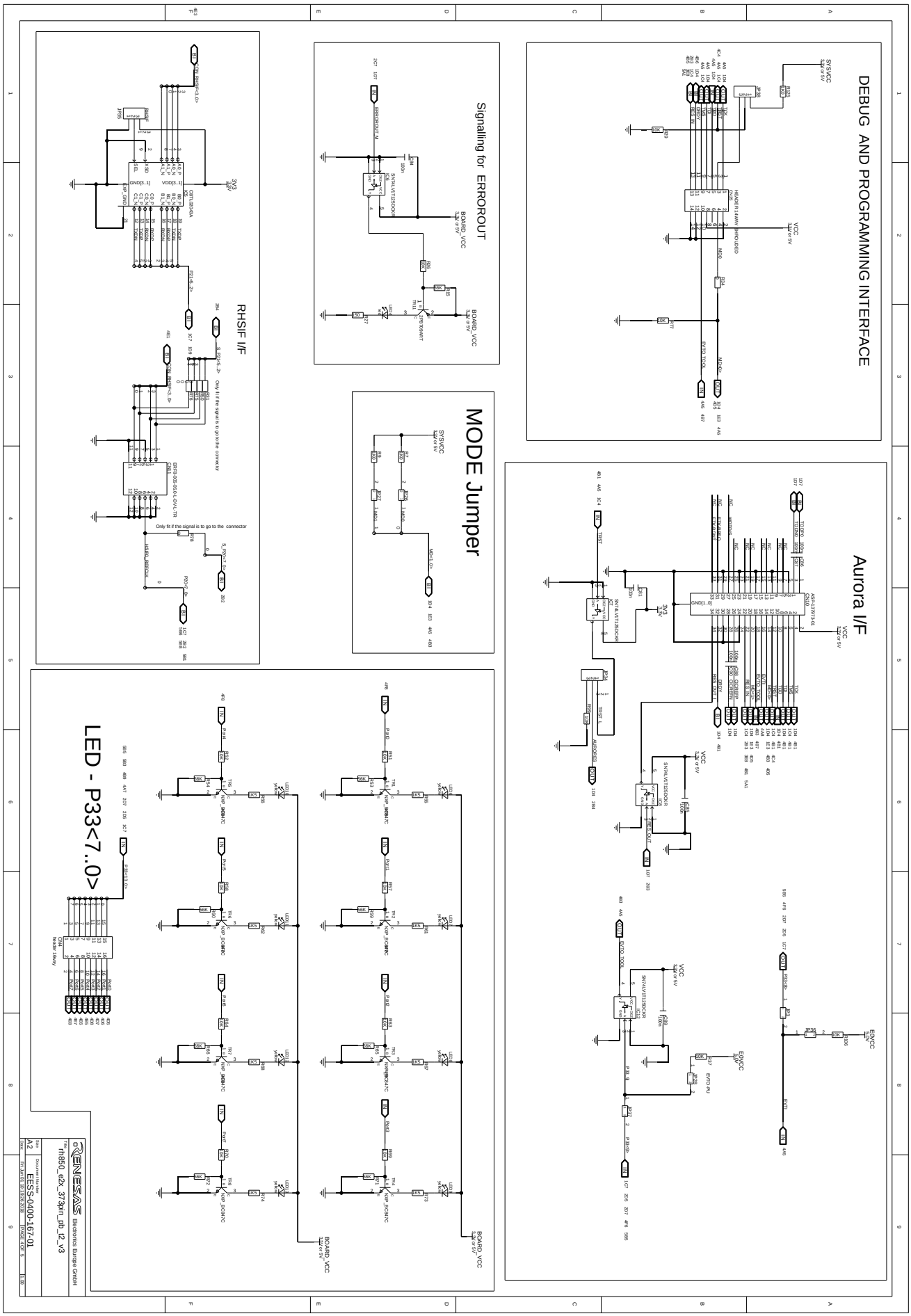
The following components described in the schematic are provided with but not mounted on the board:

- Standard 4mm power lab sockets
    - CN22
    - CN15, CN23 and CN24









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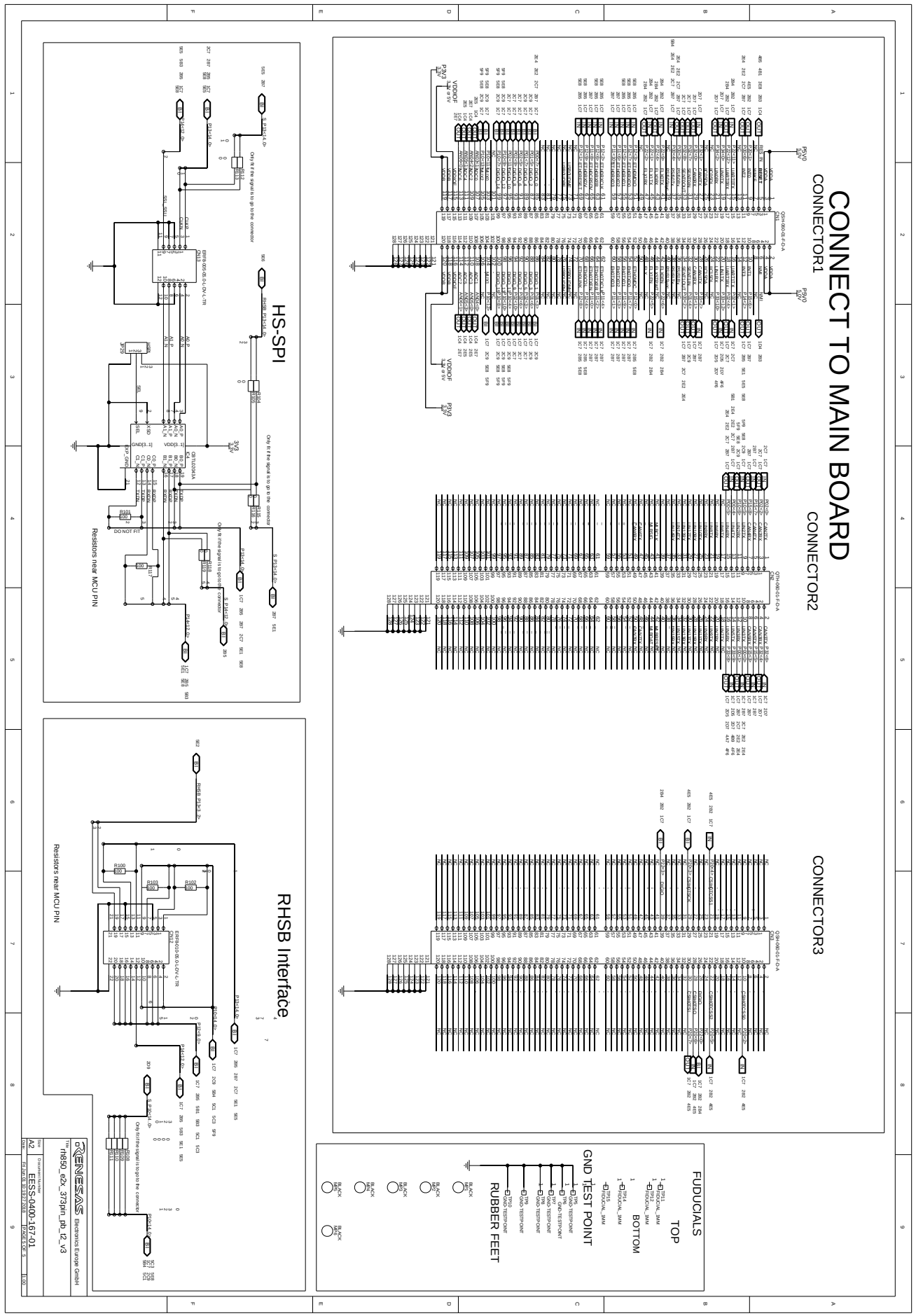

These intangible goods are not subject to Annex I of common Dual-Use list (428/2009) in its current version.

Chapter 12 Revision History

The table provides information about the major changes of the document versions.

Date	Version	Description
2019-04-30	1.0	Initial release

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