
User Guide

GreenPAK 32 PINs Adapter Board

Abstract

This user guide provides basic guidelines for the developers to get familiar with the GreenPAK 32 PINs Adapter Board. It gives an overview of the hardware, as well as the functional description of this board.

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1 Terms and Definitions

GND	Ground
GP	General Purpose
IC	Integrated Circuit
IDE	Integrated Development Environment
PC	Pin Connector
TP	Test Point
V _{DD}	Power Supply

2 Introduction

Thank you for choosing Renesas Electronics Corporation's products. You can design your own projects starting from a blank project or by altering the sample projects provided at <https://www.renesas.com>.

2.1 GreenPAK Designer

GreenPAK Designer is an easy-to-use full-featured integrated development environment (IDE) that allows you to specify exactly how you want the device to be configured. This provides you direct access to all GreenPAK device features and complete control over the routing and configuration of a PAK project with just one tool.

With GreenPAK Designer, you can:

- Design the configuration which corresponds to your project needs;
- Verify the project using software interface to GreenPAK Advanced Development Platform hardware;
- With simple-to-use and intuitive software and hardware tools you can reduce your project development time and get to market faster.

To start working with GreenPAK Designer please take the following steps:

- Download and install GreenPAK Designer software;
- Configure modules that you will need for your project;
- Interconnect and configure modules;
- Specify the pin out;
- Test your design with the GreenPAK Advanced Development Platform.

2.2 Support

Free support for GreenPAK Advanced Development Platform is available online at <https://www.renesas.com>.

GreenPAK Designer will automatically notify you when a new version of software is available. For manual updates please go to <https://www.renesas.com/software-tool/go-configure-software-hub>.

These resources are also available under the **Help** menu of GreenPAK Designer.

3 Getting Started

3.1 Install Software

GreenPAK Designer software is available free of charge from the Renesas website at <https://www.renesas.com/software-tool/go-configure-software-hub> page.

3.2 Uninstall Software

The software can be uninstalled in the way typical for your operating system. Please refer to your operating system support documentation if you need the specific instructions or visit Section 2.2 of this document for additional support from Renesas.

4 Hardware

4.1 Overview

GreenPAK 32 PINs Adapter Board is used only with GreenPAK Advanced Development Platform as TPs expander.

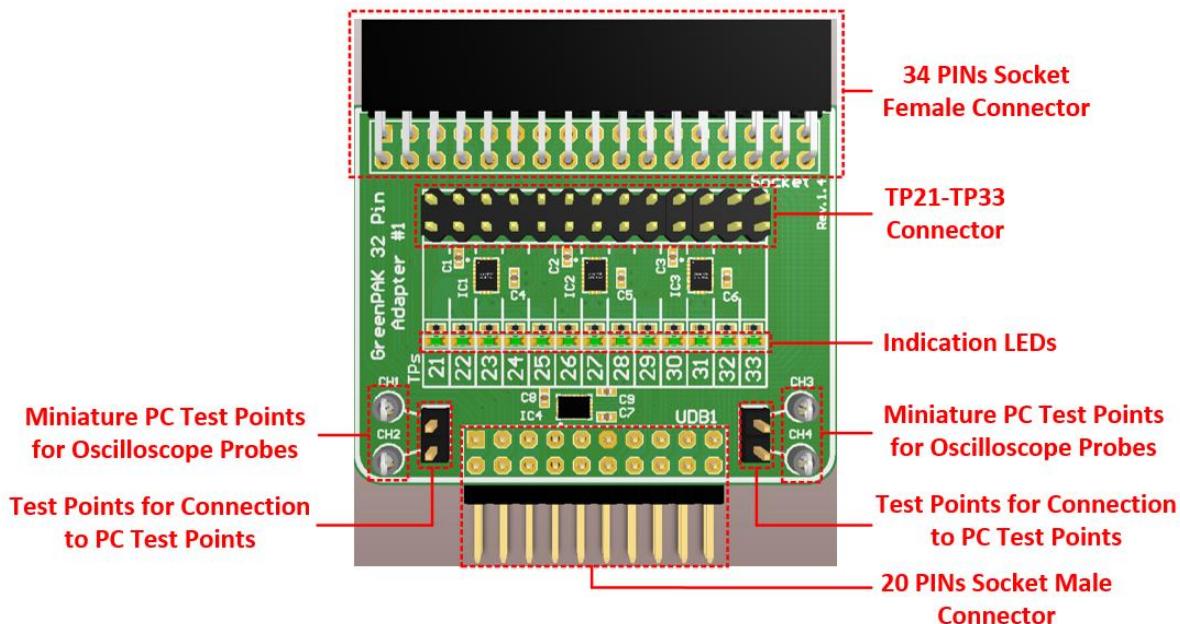


Figure 1: GreenPAK 32 PINs Adapter Board, Top View

Figure 2 shows connection of 34 PINs socket to Advanced Development Platform via 32 PINs Adapter Board.

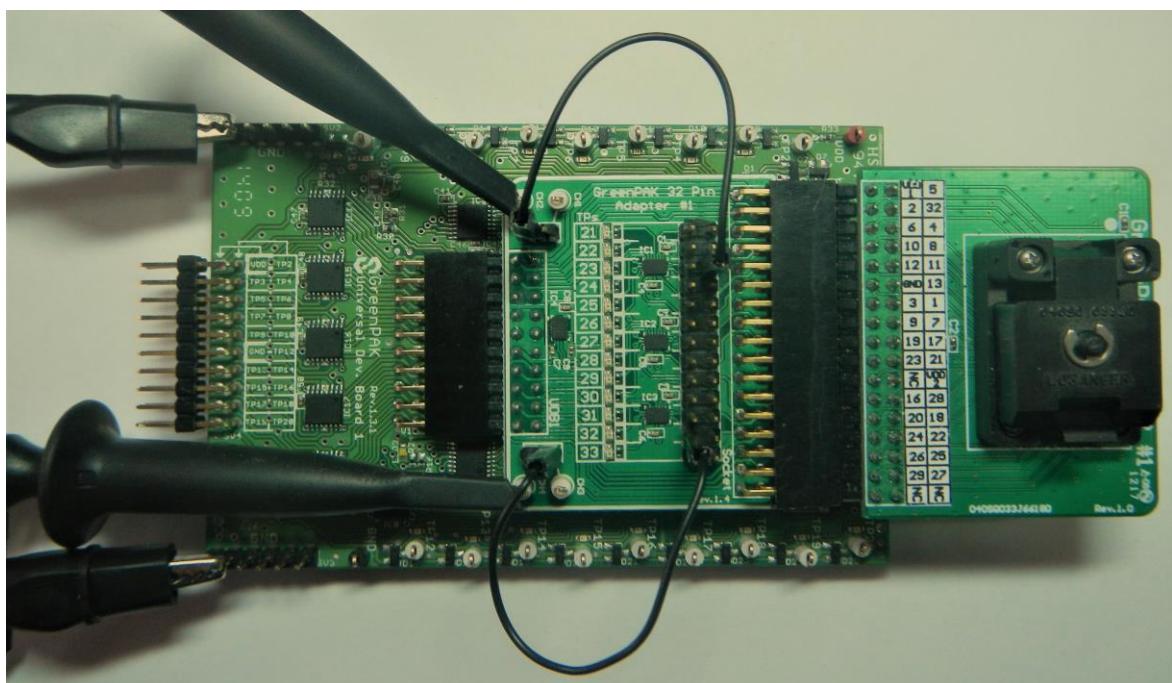


Figure 2: 34 PINs Socket Connection to Advanced Dev. Platform via 32 PINs Adapter Board

As can be seen, the miniature PCs are used to hook up oscilloscope probes. And TPs for connection to PCs can be used to connect PCs to TP21-TP33 using wire jumpers.

4.2 Functional Description

4.2.1 Power Supply

Power sources for GreenPAK 32 Pin Adapters Board are TP1 (V_{DD1}) and TP12 (V_{DD2}) of GreenPAK Advanced Development Platform. So, it is powered from the same source as the chip connected into it.

4.2.2 34 PINs Socket Female Connector

This connector is used to connect GreenPAK 32 Pin Adapter Board to 34 Pin Socket Board. [Figure 3](#) shows the connector pinout.

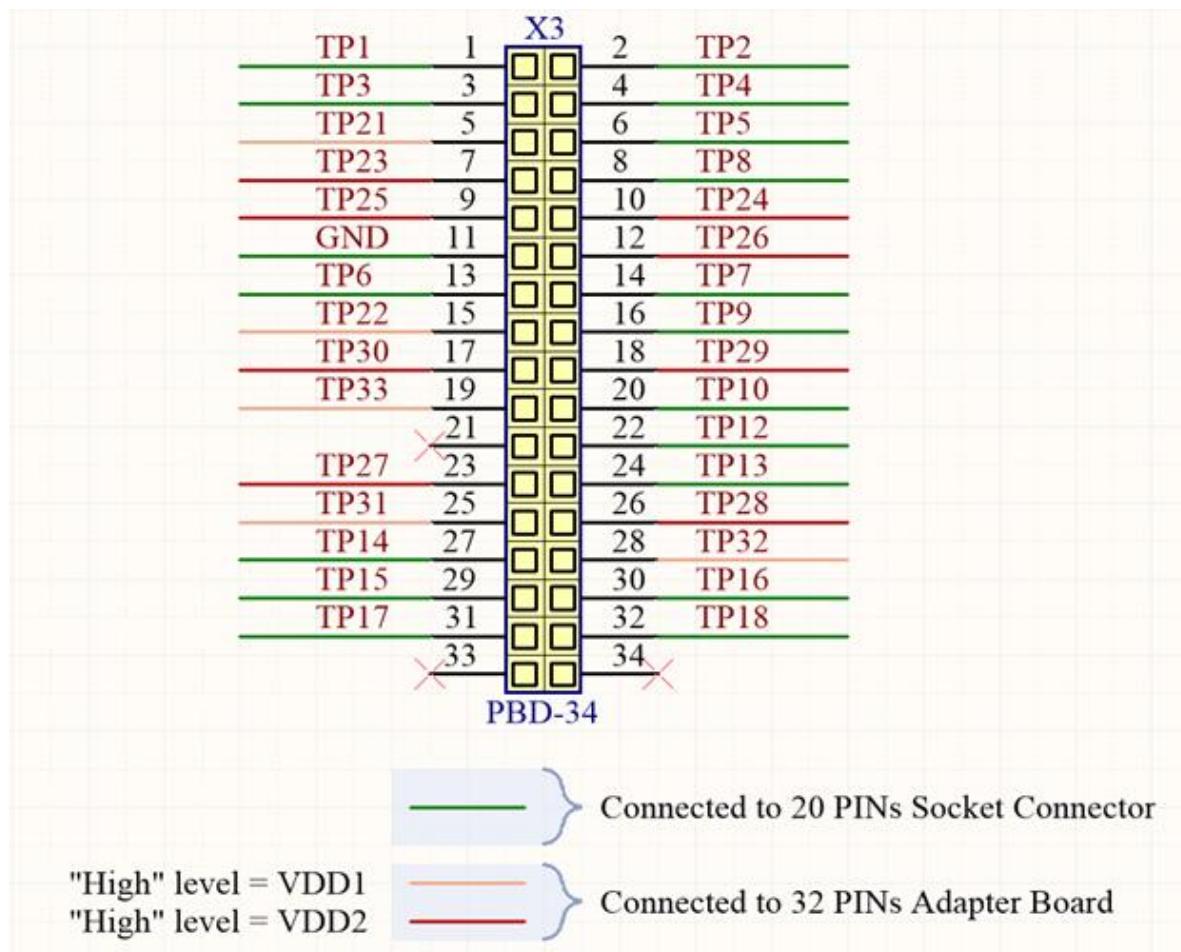


Figure 3: PINs Socket Female Connector Pinout

4.2.3 20 PINs Socket Male Connector

This 20-pins connector is used to connect 32 PIN Adapter to GreenPAK Advanced Development Platform. [Figure 4](#) shows the connector pinout.

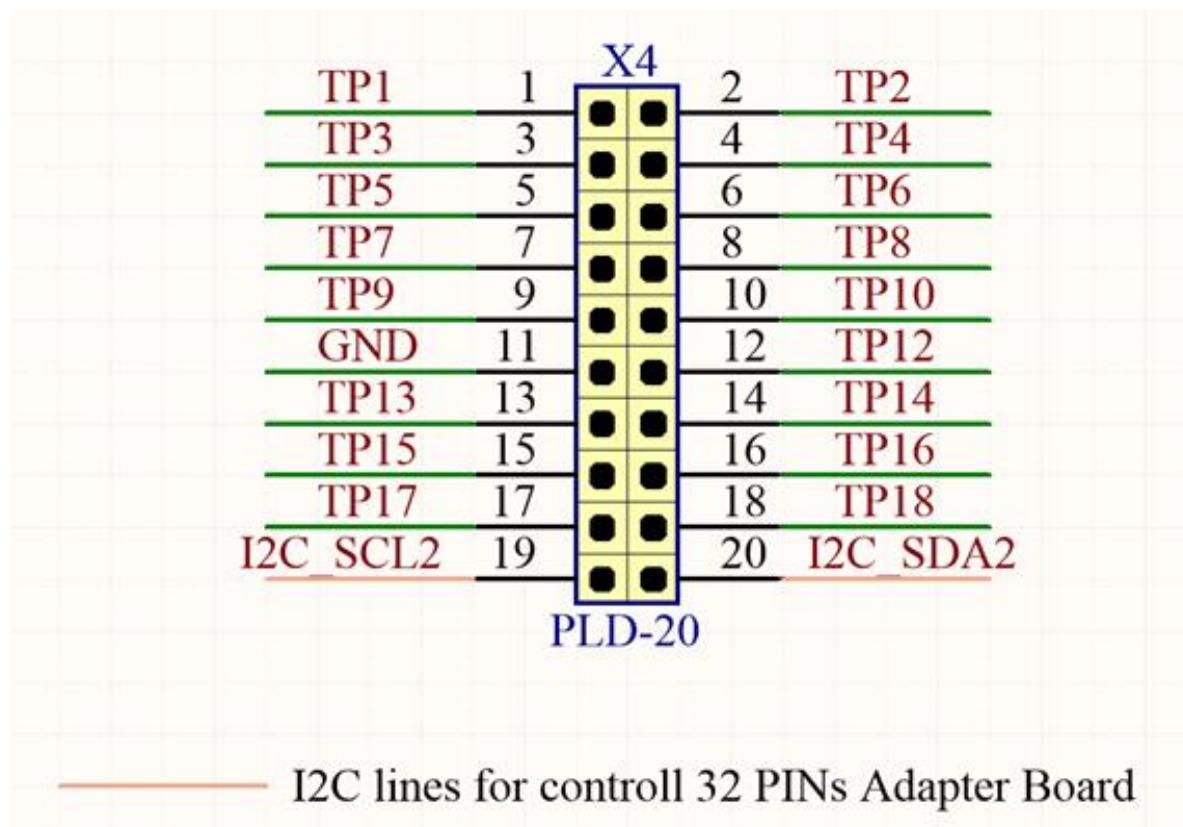


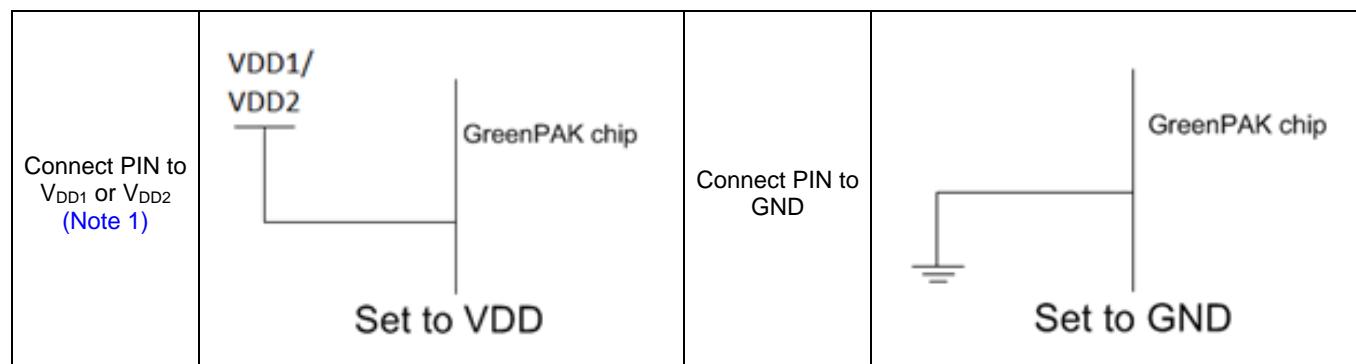
Figure 4: PINs Socket Male Connector Pinout

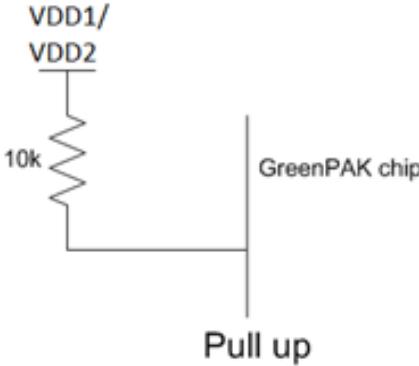
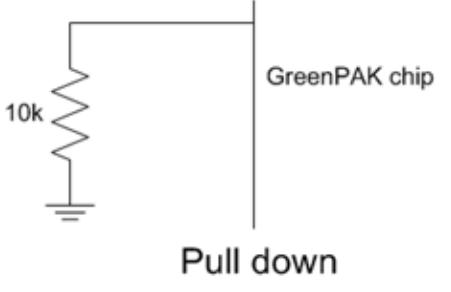
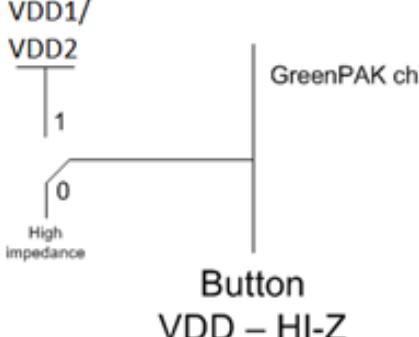
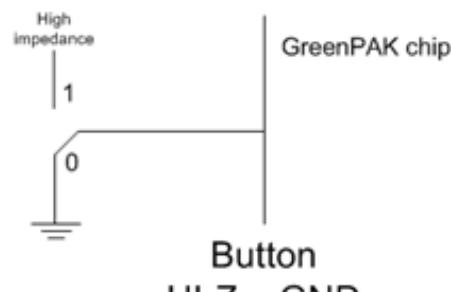
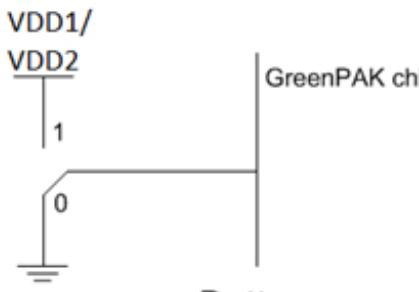
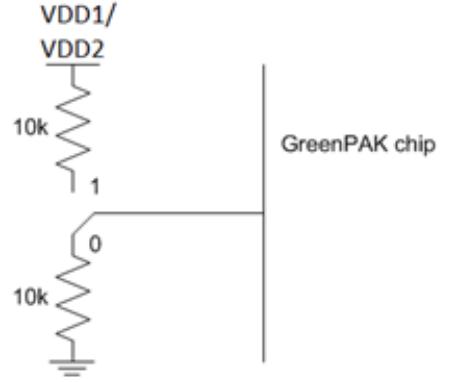
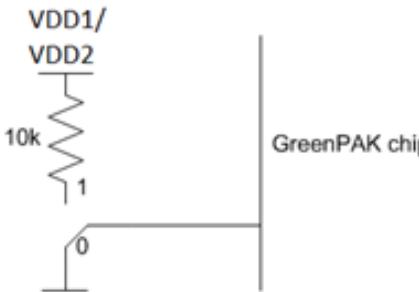
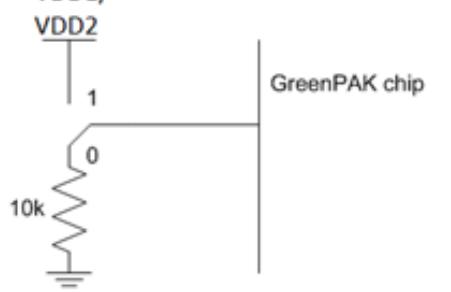
4.2.4 Pins Connectivity

32 PINs Adapter Board makes available such connections: V_{DD}, GND, Pull-up, Pull-down, Configurable Button.

The list of available connections for each test point is presented in [Table 1](#).

Table 1: Data Pins Connections Schematics



Connect PIN to V _{DD1} or V _{DD2} (Note 1) through IC 10 k Ω Pull-up resistor		Connect PIN to GND through IC 10 k Ω Pull-down resistor	
Upper connection to V _{DD1} or V _{DD2} (Note 1); bottom connection to high impedance IC input		Upper connection to high impedance IC input; bottom connection to GND	
Upper connection to V _{DD1} or V _{DD2} (Note 1); bottom connection to GND		Upper connection to V _{DD1} or V _{DD2} (Note 1) through IC 10 k Ω Pull-up resistor; bottom connection to GND through IC 10 k Ω Pull-down resistor	
Upper connection to V _{DD1} or V _{DD2} (Note 1) through IC 10 k Ω Pull-up resistor; bottom connection to GND		Upper connection to V _{DD1} or V _{DD2} (Note 1); bottom connection to GND through IC 10 k Ω Pull-down resistor	

Note 1 Connection to V_{DD1} or V_{DD2} depends on which logical voltage level pin belongs to. For this information see chip [datasheet](#).

Figure 5 shows the schematic connection of the GP data pins.

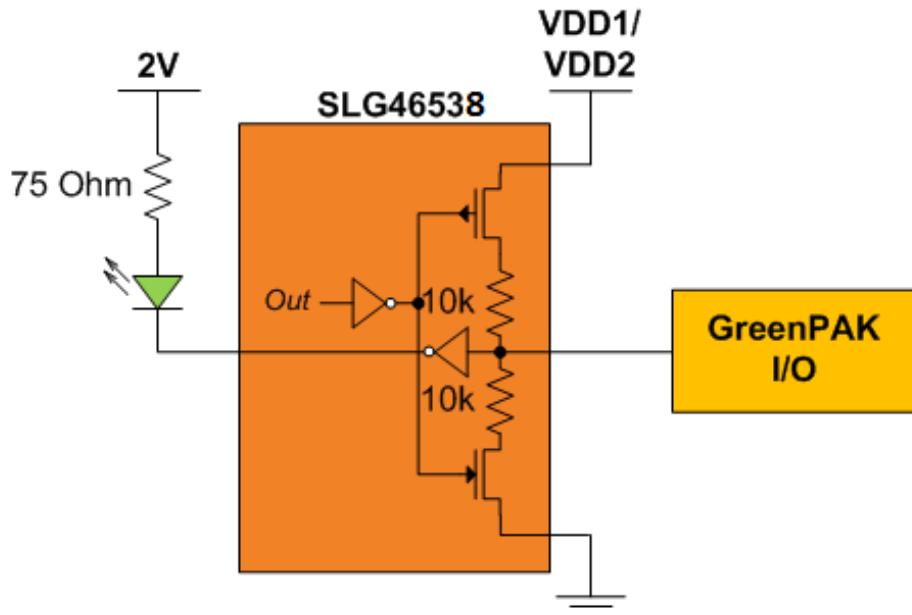


Figure 5: Schematic Connection of the Data Pin

4.2.5 Chip PIN versus Board Test Point

Before you start working with a chip you need to understand the difference between such concepts as PIN (chip pin) and TP (board test point). Figure 6 shows where PINs and TPs are situated.

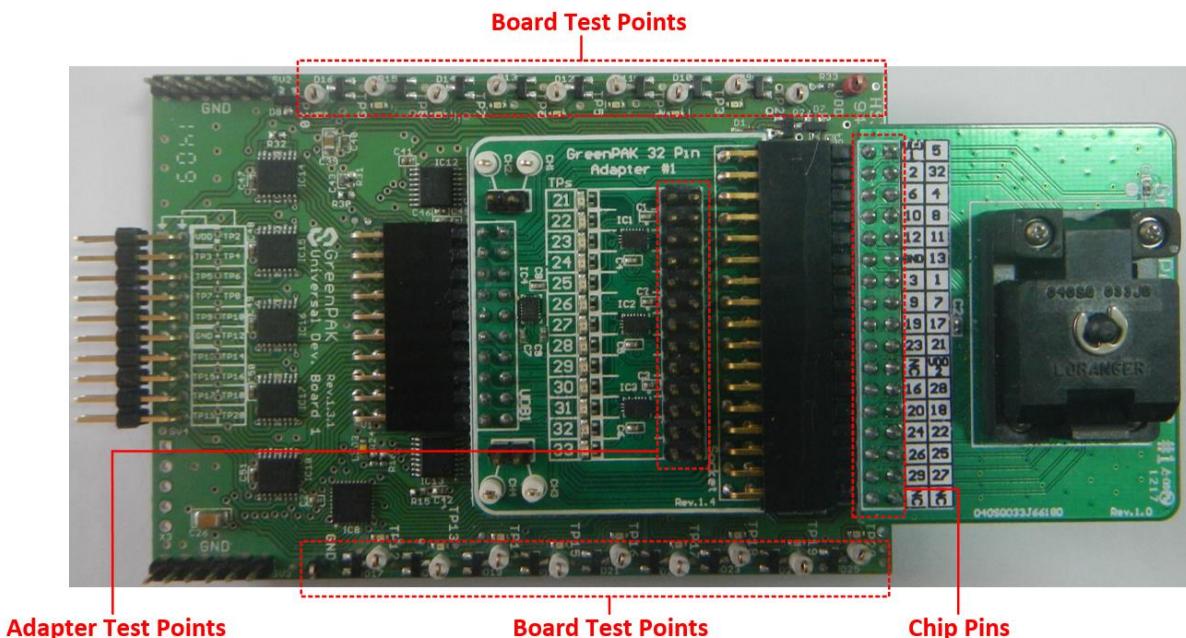


Figure 6: Pins and TPs Location

PINs refer to the physical pins that are on the chip package (their marking can be found in the datasheet). TPs refer to the Socket Board connector pins. TP and PIN numbers may not match since different PINs on the chip have different functions, see [Figure 7](#).

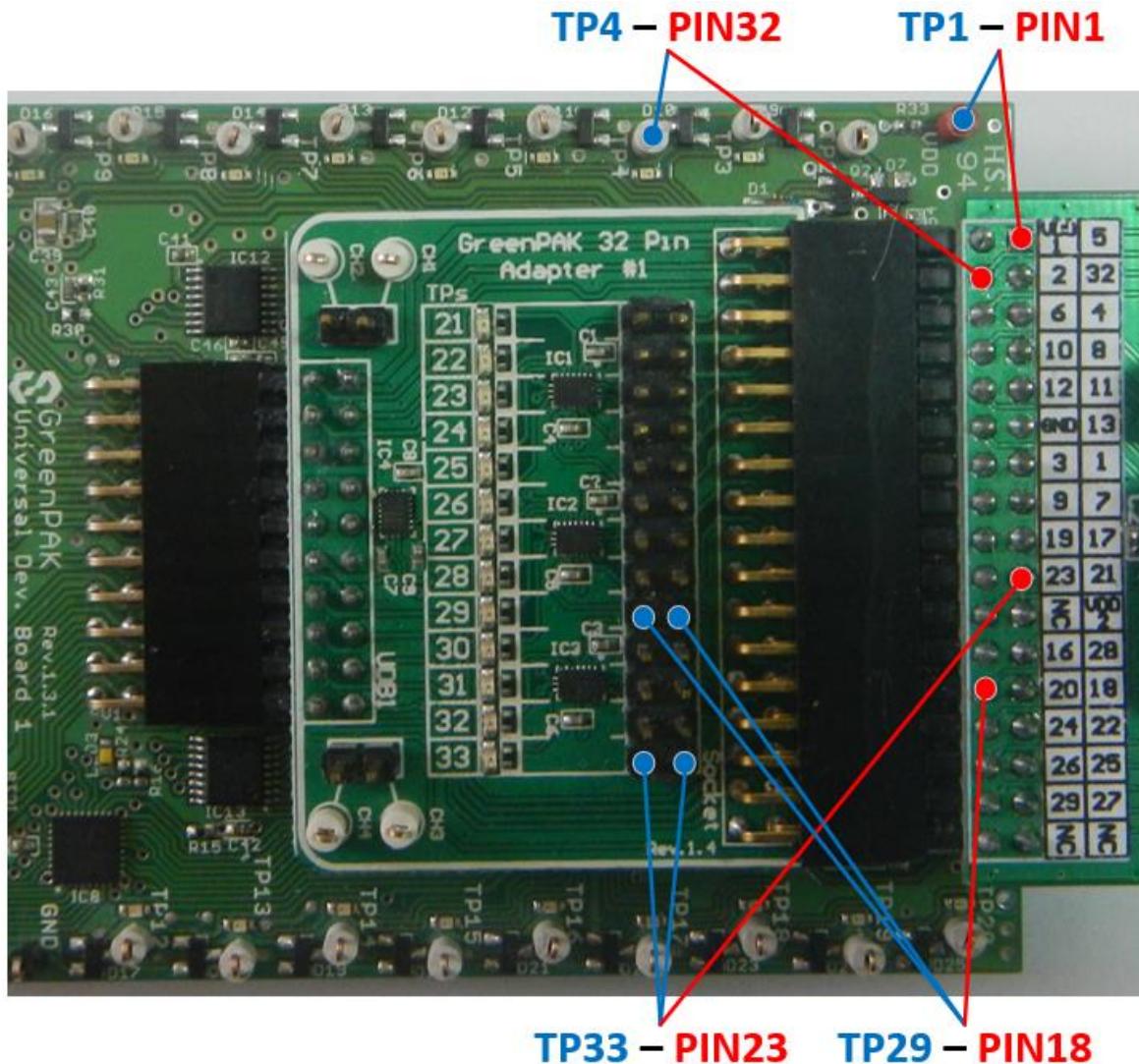


Figure 7: Pins and TPs Accordance (for SLG46534)

Appendix A Electrical Specification

Mode	Parameter	Min	Typ	Max	Units
General	Test Point Capacitance	1	--	--	pF
	Input Leakage Current	--	--	1	uA
Virtual Button, V _{DD} /GND, Pull-Up/Down Driver	Output Level High	--	V _{DD1} / V _{DD2}	--	--
	Output Level Low	--	GND	--	--
	Pull-Up/Down Resistance	8.66	11.9	15.05	kΩ

Revision History

Revision	Date	Description
1.1	18-Mar-2022	Renesas rebranding
1.0	14-Sep-2020	Updated according to Dialog's Writing Guideline

Status Definitions

Status	Definition
DRAFT	The content of this document is under review and subject to formal approval, which may result in modifications or additions.
APPROVED or unmarked	The content of this document has been approved for publication.

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