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1. Control Logic

1.1 General Description

The control logic of the ZSSC3154 consists of the calibration microcontroller (CMC), the module control logic of the analog-to-digital converter (ADC) and the serial digital interface. The configuration of the various modes of the device is done by programming settings in EEPROM.

The CMC controls the measurement cycle and performs the calculations for sensor signal conditioning. This eliminates the gain deviation, the offset, the temperature deviation, and the non-linearity of the pre-amplified and A/D converted sensor signal. The A/D conversion is executed as a continuous measurement cycle. The conditioning calculation by the CMC is performed in parallel with the A/D conversion.

The ZSSC3154 communicates with an external microcontroller, especially for calibration purposes, via a serial digital interface. A communication protocol according to the I2C standard is supported. Additionally Renesas's ZACwire™ interface is implemented for one-wire communication (OWI). These serial interfaces are used for the calibration of the sensor system consisting of a transducer and the ZSSC3154. The serial interface provides the read out of the results of sensor signal conditioning as digital values during the calibration. The internal processing of received interface commands is done by the CMC. As a consequence, the measurement cycle is interrupted if a command is received. Only the read out of data is controlled by the serial interface itself, and this does not interrupt the CMC.

1.2 CMC Description

The calibration microcontroller (CMC) is especially adapted to the tasks connected with the signal conditioning.

These are the main features:

- The microcontroller uses 16-bit processing width and is programmed via ROM.
- A watchdog timer controls the proper operation of the microcontroller.
- Constants/coefficients for the conditioning calculation are stored in the EEPROM. The EEPROM is mirrored to the RAM after power-on or after re-initialization from EEPROM by sending a specific command to the serial interface.
- Parity is checked continuously during every read from RAM. If incorrect data is detected, the Diagnostic Mode is activated (an error code is written to the serial digital output, and the analog output is set to the diagnostic level).

1.3 General Working Modes

ZSSC3154 supports three different working modes:

- Normal Operation Mode (NOM)
- Command Mode (CM)
- Diagnostic Mode (DM)

1.3.1 Normal Operation Mode (NOM)

The Normal Operation Mode (NOM) is the recommended working mode for applications. After power-on, the ZSSC3154 completes an initialization routine during which the EEPROM is mirrored to RAM and the contents are checked against a stored signature. If enabled, a ROM signature check is processed (see Table 19). If any error is detected, the Diagnostic Mode is activated. Otherwise the configuration of the ZSSC3154 is set, the serial digital interfaces are enabled, and NOM is started.

In NOM, the continuous measurement cycle and conditioning calculations are processed. The signal conditioning results generate the analog output at pins AOUT1 and AOUT2. The measurement cycle covers one or two main signals. The differential bridge sensor signal is always available. In addition, a temperature sensor

signal or the half-bridge signal can be measured. Various analog output modes are available (refer to section 3.1).

Provided that the EEPROM is programmed correctly, NOM runs without sending any command to the digital serial interface. Readout of the conditioning results via the digital serial interface (I2C) is possible. This does not interrupt the continuous processing of the signal conditioning routine.

After power-on, a startup window is opened for one-wire communication (OWI) via the AOUT1 pin. During the startup window, the output levels at the AOUT1 pin depend on the selected OWI mode and the configured analog output mode (see section 4.4). To activate the Command Mode (CM) for end-of-line configuration and calibration, send the START_CM command via OWI communication during the startup window (refer to the data sheet for timing specifications for the startup window). In CM, NOM is stopped and the ZSSC3154 waits for further commands.

The ZSSC3154 provides two analog voltage outputs at the AOUT1 and AOUT2 pins. The full bridge sensor signal is always output at the AOUT1 pin. For the compensation of temperature dependent deviations via conditioning calculations, a calibration temperature is measured.

At the AOUT2 pin, there are several EEPROM configurable options for the output mode (see section 3):

- full bridge sensor signal (2x FB Mode),
- half bridge sensor signal (FB/HB Mode) and
- temperature measurement result.

The output full bridge signal at AOUT2 is updated alternating with AOUT1, half bridge signal and temperature is updated as shown in the measurement cycle. A separate temperature measurement is available for the output of a conditioned temperature signal. A half-bridge measurement is available for validating the main bridge sensor signal.

The measurement cycle is adapted to the selected measurement and safety tasks configured in EEPROM CFGAPP2: AOT2MDand CFGSF, respectively. The measurement cycle is reduced to the minimum necessary measurement phases (see Figure 1). All measured signals are auto-zero compensated to eliminate offsets resulting from the selected measurement channel.

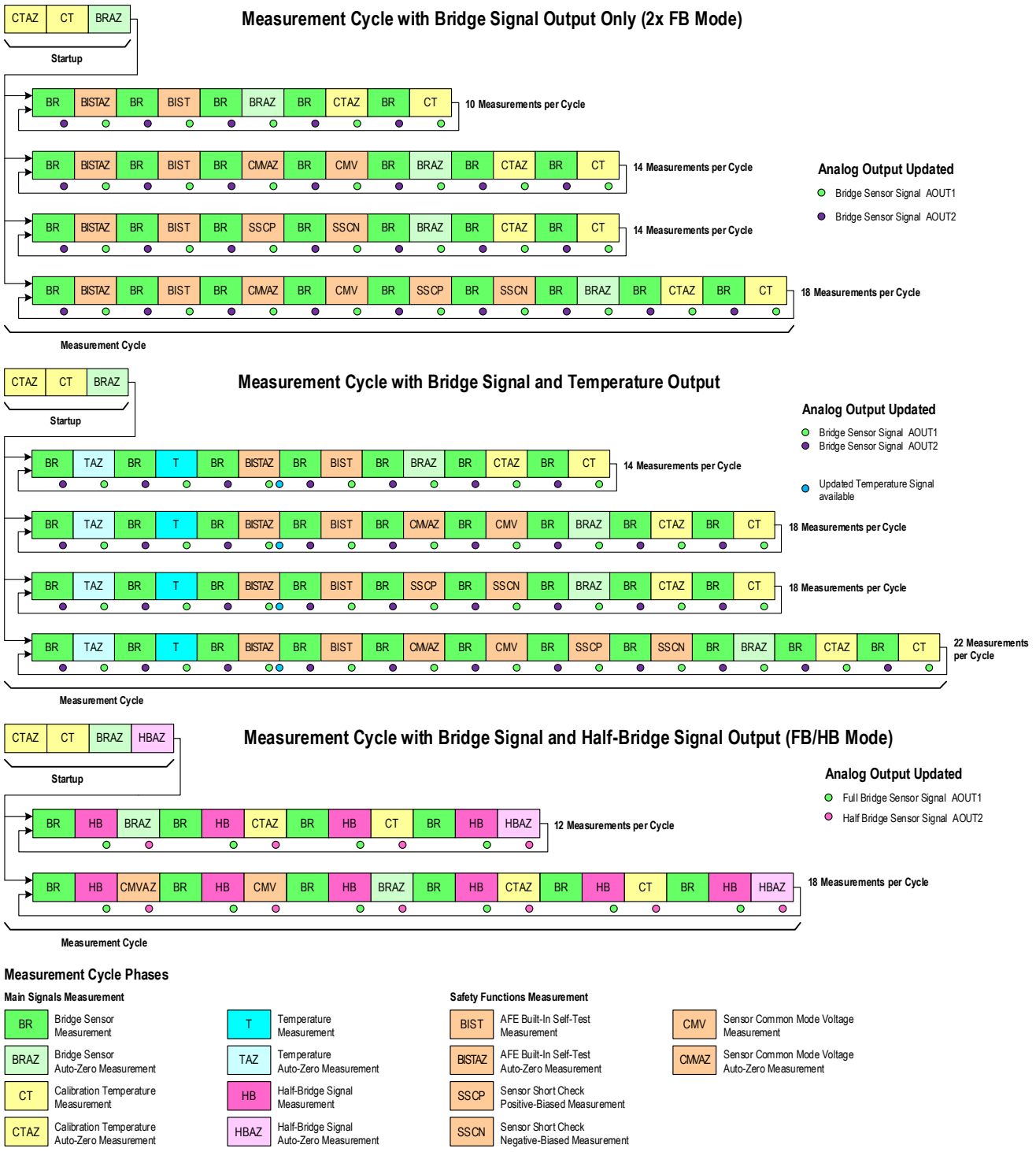


Figure 1. Measurement Cycle

1.3.2 Command Mode (CM)

The Command Mode (CM) is the working mode that is used for calibration data acquisition and access to the internal RAM and EEPROM of the ZSSC3154. The CM start command START_CM aborts the running NOM, so the measurement cycle stops. The ZSSC3154 changes to CM only after receiving the START_CM command by digital serial communication (I2C or OWI). This protects the ZSSC3154 against interruption of processing the NOM (continuous signal conditioning mode) and/or unintentional changes of configuration. In CM, the full set of commands is supported (see section 5.1).

Starting CM via I2C communication (SCL and SDA pins) is possible at any time. If starting CM via one-wire communication (AOUT1 pin), the START_CM command must be transmitted during the startup window.

If the ZSSC3154 receives a command other than START_CM in NOM, it is not valid. It is ignored, and no interrupt to the continuous measurement cycle is generated.

In CM, the full command set is enabled for processing. During processing of a received command, the digital serial interfaces are disabled; no further commands are recognized. After finishing the processing, the CMC waits for further commands or processes requested measurement loops continuously. EEPROM programming is only enabled after receiving the EEP_WRITE_EN command.

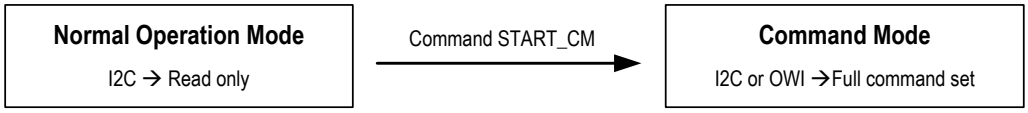


Figure 2. Modes of Digital Serial Communication

1.3.3 Diagnostic Mode (DM)

“Safe State” of the ZSSC3154 is the Diagnostic Mode (DM) if ZSSC3154 is used in safety relevant applications.

The ZSSC3154 detects various failures. When a failure is detected, Diagnostic Mode (DM) is activated. DM is indicated by setting both output pins AOUT1 and AOUT2 to the diagnostic fault band. The level of diagnostic output is configured by the DFBH pin. If the DFBH pin is open, the output is set to Diagnostic Fault Band Low (DFBL). If pin DFBH is connected to VSSA, output is set to Diagnostic Fault Band High (DFBH).

When using digital serial communication protocols (I2C or OWI) to read out conditioning results data, the error status is indicated by two bits in every data word.

DM generates a significant error code that can be read using the command GET_ERR_STATUS.

OWI communication is enabled during DM. Because the analog output pin AOUT1 is driven to the diagnostic range, the AOUT1 pin must be overwritten when starting OWI communication. The communication master must provide driving capability (AOUT1 current limitation: < 20mA).

Note that many of the error detection features can be enabled/disabled by configuration word CFGSF (refer to section 6.4).

There are three options for Diagnostic Mode:

- Static Diagnostic Mode (StaticDM). In StaticDM, the measurement cycle is stopped and failure notification is activated.
  If enabled by the configuration bit CFGSF:DMRES, a reset after the timeout of a watchdog is executed.
- Temporary Diagnostic Mode. There is a failure counting sequence that can result in a temporary DM. DM is activated after two consecutively detected failure events and is deactivated after a failure counter counts down if the failure condition is no longer detected. The measurement cycle is continuously processed during temporary DM.
- Power and Ground Loss. Power and ground loss cases are signaled by setting the analog output pins to high-impedance states. The output levels are determined by the external loads.

1.3.4 Failure Detection Mechanisms and Error Codes

Table 1. Failure Detection Functionality and Error Codes

Failure Detection Mechanism	Description	Error Code	Failure Detection Requested	Activation	Messaging Time	Action
Oscillator Fail Detection	Oscillator is observed generating clock pulses by an asynchronous timing logic.	-		Always on	< 200µs	Temporary DM
EEPROM Signature	Checks signature of RAM mirror against signature stored in EEPROM.	6600_{HEX}		Always on	Startup	Static DM
ROM Signature	Checks CMC ROM signature. Note that this check potentially increases startup time by 10ms.	6500_{HEX}	Yes	CFGSF: CHKROM	Startup	
EEPROM Multiple-Bit Error	Detection of non-correctable multiple-bit error per 16-bit word.	6440_{HEX}		Always on	Startup	
Arithmetic Check	Functional check of arithmetic unit.	6480_{HEX}		Always on	One measurement cycle	Static DMor@ CFGSF: DMRES=1 Static DM & Reset after Watchdog Timeout (enabled by)
Register Parity	Permanent parity check of configuration registers.	6410_{HEX}		Always on	Immediate	
RAM Parity	Parity check at every RAM access.	6404_{HEX}		Always on	Immediate	
Watchdog	Watchdog timeout during start routine (65536 clocks if CFGAFE:ADCSLOW=0; 131072 clocks if ADCSLOW=1; refer to Table 15) or measurement cycle (2 × conversion cycle time).	6402_{HEX}		Always on	Startup, 2 or 3 measurement times	
BCC	Broken chip check.	$AA00_{HEX}$	Yes	CFGSF: CHKBCC	Two measurement cycles	Temporary DM
TSC	Temperature sensor check: Detection of overdriving the analog front-end during temperature measurement.	$C900_{HEX}$	Yes	CFGSF: CHKTSC		
SAC	Sensor aging check.	$A880_{HEX}$	Application [1]	CFGSF: CHKSAC		
SCC	Sensor connection check.	$A840_{HEX}$	Application [1]	CFGSF: CHKSCC		
SSC	Sensor short check.	$A820_{HEX}$	Application [1]	CFGSF: CHKSSC		
AFEBIST	Analog front-end (AFE) built-in self-test; not executed if half-bridge signal measurement is configured.	$A810_{HEX}$	Yes	AFEBIST MIN / MAX		
MCCH	Main channel check – high: Detection of positive overdriving of the analog front-end during bridge measurement.	$A808_{HEX}$	Application [1]	CFGSF: CHKMCCH		
MCCL	Main channel check – low: Detection of negative overdriving of the analog front-end during bridge measurement.	$A804_{HEX}$	Application [1]	CFGSF: CHKMCCL		
Power or Ground Loss	Power or ground loss detection.	–		Always on	< 5ms	Reset

1. Related to sensor supervision – activation depends on application requirements and sensor properties.
2. Note: Error codes can be bit-wise masked. Bit [15] (MSB) is even parity. Bits [14:13] are error status flags. Error status is 1 (Temporary DM), 2 (Temporary DM, Temperature Fail), or 3 (Static DM).
3. If the error status is 0 but the error code at bits [12:0] is set, this means that the indicated error was temporarily detected during normal operation but is currently not active anymore.
4. Note that the reset after the watchdog timeout clears any error codes that were previously generated.

1.3.4.1 Broken Chip Check (BCC)

The BCC detects damage and fractions of the silicon chip and its passivation caused by the production and assembly process. The check can be applied by the GET_BCC_STATUS command during the calibration process or cyclically in the measurement cycle during NOM.

1.3.4.2 Temperature Sensor Check (TSC)

The temperature sensor check detects whether the ADC dynamic range has been exceeded during the temperature measurement. The temperature signal raw value is checked to determine if it is less than 128 or greater than (2^{14} – 128).

This can result from various causes: the external temperature sensor is disconnected; the analog temperature input channel is not sufficiently calibrated or defective; or the temperature signal is out of targeted range.

1.3.4.3 Bridge Sensor Aging Check (SAC)

The sensor aging check detects long-term altering of the bridge sensor resistors that would result in a shift of the calibrated output characteristics. The SAC evaluates the common mode voltage of the sensor bridge once per measurement cycle if enabled. The measurement result is checked for compliance with programmed limits (CMVMIN / CMVMAX).

SAC data acquisition is determined by **Equation 1**.

SAC conversion result CMVAZC

$$Z_{CMVAZC} = 2^{14} \times \left(\left(\frac{VBP + VBN}{2 \times (VBR\_T - VBR\_B)} - \frac{1}{2} \right) \times 2.666 + 1/2 \right) \quad \textbf{Equation 1}$$

Where

VBP, VBN, VBR_T, VBR_B: Voltage at the related pins

The limits for failure detection depend on sensor properties and must be determined by the user.

1.3.4.4 Analog Front-End Built-In Self-Test (AFEBIST)

The analog front-end (AFE) built-in self-test detects whether the AFE (the programmable amplifier and the A/D converter) is functioning correctly. Adjusted to the configured analog gain, an internally generated analog input signal is measured via the main channel. The measurement result is checked against programmed limits (AFEBISTMIN / AFEBISTMAX; see Table 14).

AFEBIST adds two further measurement phases to the measurement cycle and validates the measurement channel similarly to the FB/HB comparison when the half-bridge measurement is activated. So, AFEBIST is only measured if the half-bridge measurement is not activated.

Hence AFEBIST validation can be disabled by setting the limits AFEBISTMIN / AFEBISTMAX to 0_{HEX} and $3FFF_{HEX}$, respectively.

Note: AFEBIST limits must be calibrated because the results depend on properties of the device:

1. Adjust ADC configuration (resolution, timing) and PGA gain as used for the sensor to be calibrated
2. Process the “START_AD_ BIST_AZC” command (0x52) and read out the conversion result (maybe do an average of e.g. 10 read out conversation results) -> ***AFEBIST_RSLT***
3. Calculate AFEBIST limits based on the acquired AFEBIST conversion result:

- AFEBISTMIN = (1 - DELTA_BIST_LIMIT) * ***AFEBIST_RSLT***
- AFEBISTMAX = (1 + DELTA_BIST_LIMIT) * ***AFEBIST_RSLT***

4. Write calculated AFEBIST limits to the NVM, store all acquired and calculated data in calibration database

Table 2. AFEBIST LIMIT

Parameter	Symbol	Conditions	Min	Nominal	Max	Unit
DELTA_BIST_LIMIT	dBISTLIM		5			%

1. See section 1.3.4.4 for details.

1.3.4.5 Bridge Sensor Connection Check (SCC)

The sensor connection check monitors the connection of the bridge sensor at the VBP and VBN pins. An internally determined current is applied to the sensor, and the resulting differential input signal is evaluated once per measurement cycle if enabled.

The following failures are detected by SCC:

- High-resistive sensor bridge elements (e.g., a diaphragm rapture)
- Connection loss at the pins VBP, VBN, VBR_T or VBR_B
- Short between pins VBP or VBN and pins VBR_T or VBR_B
- Enabling the SCC High Capacitor Mode (CFGSF:CHKSCCHIC; see Table 19) is recommended in applications with a high capacitive load greater than 1nF up to 10nF at the input pins VBP and VBN.

1.3.4.6 Bridge Sensor Short Check (SSC)

The sensor short check detects a short between the bridge sensor input pins VBP and VBN (connections less than 50Ω nominal). An internally determined current is applied to the sensor in both directions, resulting in differential input signals, which are evaluated once per measurement cycle if enabled. If a short occurs, the input signal difference of both is less than an internally determined limit. SSC is not applicable if HB mode is used.

1.3.4.7 Main Channel Check (MCCH/MCCL)

The main channel check detects whether the ADC dynamic range has been exceeded during the bridge measurement. The bridge signal raw value is checked to determine if the value is less than 128 or greater than (2^{14} – 128). This can result from various causes: the bridge sensor is disconnected; the main input channel is defective or not sufficiently calibrated; or the bridge signal is out of targeted range.

The main channel check distinguishes between positive (MCCH) and negative (MCCL) overdrive to allow tailored overdrive handling at the bridge channel.

1.3.4.8 Power and Ground Loss

The detection of a power or ground loss is indicated by pulling the analog outputs AOUT1 and AOUT2 to the Diagnostic Fault Band. The level of the diagnostic output depends on the lost node and load connection to ground or supply. In such cases, the ZSSC3154 is inactive and the specified leakage current in combination with the load resistor guarantees reaching DFBH or DFBL.

2. Signal Conditioning

2.1 A/D Conversion

During NOM, the analog preconditioned sensor signal is continuously converted from analog to digital. The A/D conversion is performed with a 14-bit resolution r_{ADC} for all measurements in the measurement cycle (e.g., bridge sensor signal, temperature, half-bridge, auto-zero, etc.). The A/D conversion is configurable regarding the inherent range shift rs_{ADC} for the bridge sensor signal and half-bridge signal measurement. All resulting digital raw values are determined by the following equations:

Analog differential input voltage to A/D conversion (V_{ADC_DIFF})

$$V_{ADC\_DIFF} = a_{IN} \times V_{IN\_DIFF} + a_{XZC} \times V_{XZC} \qquad \textbf{Equation 2}$$

Where

V_{IN_DIFF}	Differential input voltage to analog front-end
V_{XZC}	Extended zero compensation voltage (programmable via CFGAFE:BRXZC and CFGAFE2:HBXZC; see section 6.4)
a_{IN}	Gain of analog front-end
a_{XZC}	Gain for extended zero compensation voltage
V_{ADC_DIFF}	Differential input voltage to ADC

Digital raw A/D conversion result (Z_{ADC})

$$Z_{ADC} = 2^{r_{ADC}} \times \left(\frac{V_{ADC\_DIFF} + V_{OFF}}{V_{ADC\_REF}} + rs_{ADC} \right)$$ **Equation 3**

Where

V_{OFF}	Residual offset voltage of analog front-end (which is eliminated by auto-zero compensation)
V_{ADC_REF}	ADC reference voltage (ratiometric reference for measurement)
r_{ADC}	Resolution of A/D conversion (14-bit)
rs_{ADC}	Range shift of A/D conversion (bridge or half-bridge: ½, ¼, 1/8, 1/16; temperature: ½)

Auto-zero value (Z_{AZ})

$$Z_{AZ} = 2^{r_{ADC}} \times \left(\frac{V_{OFF}}{V_{ADC\_REF}} + rs_{ADC} \right)$$ **Equation 4**

Auto-zero corrected raw A/D conversion result (Z_{CORR})

$$Z_{CORR} = Z_{ADC} - Z_{AZ} = 2^{r_{ADC}} \times \frac{V_{ADC\_DIFF}}{V_{ADC\_REF}}$$ **Equation 5**

2.2 Bridge Sensor Signal Conditioning Formula

The digital raw value $Z_{BR,CORR}$ for the measured bridge sensor signal is processed with a conditioning formula to remove offset and temperature dependency and to compensate nonlinearity up to 3rd order. The signal conditioning equation is processed by the CMC and is defined as follows:

Range definition of inputs ($Z_{BR,CORR}$ and $Z_{CT,CORR}$)

$$Z_{BR,CORR} \in [\ -2^{r_{ADC}};\ 2^{r_{ADC}})$$ **Equation 6**

$$Z_{CT,CORR} \in [\ -2^{r_{ADC}-1};\ 2^{r_{ADC}-1})$$ **Equation 7**

Where

r_{ADC}	Resolution of A/D conversion(14-bit)
$Z_{BR,CORR}$	Raw A/D conversion result for bridge sensor signal (auto-zero compensated)
$Z_{CT,CORR}$	Raw A/D conversion result for calibration temperature (auto-zero compensated)

In the following conditioning formulas, equation **Equation 8** compensates the offset and fits the gain including its temperature dependence. The nonlinearity for the intermediate result Y is then corrected in equation **Equation 9** . The result of these equations is a non-negative value BR for measured bridge sensor signal in the range [0; 1).

Note that the conditioning coefficients ci are positive or negative values in two's complement.

Bridge signal conditioning equations

$$Y = \frac{Z_{BR,CORR} + c_0 + 2^{-(r_{ADC}-1)} \times c_4 \times Z_{CT,CORR} + 2^{-2(r_{ADC}-1)} \times c_5 \times Z_{CT,CORR}^2}{c_1 + 2^{-(r_{ADC}-1)} \times c_6 \times Z_{CT,CORR} + 2^{-2(r_{ADC}-1)} \times c_7 \times Z_{CT,CORR}^2} \qquad Y \in [0;1)$$ **Equation 8**

$$BR = Y \times (\ 1 - 2^{-15} \times c_2 - 2^{-15} \times c_3) + 2^{-15} \times c_2 \times Y^2 + 2^{-15} \times c_3 \times Y^3 \qquad BR \in [0;1)$$ **Equation 9**

Where

Conditioning coefficients stored in EEPROM registers 00_{HEX} to 07_{HEX}:

ci ∈ [-2^{15}; 2^{15}), two's complement.

c_0	Bridge offset
c_1	Bridge gain
c_2	Non-linearity correction 2nd order

c_3 Non-linearity correction 3rd order

c_4 Temperature coefficient bridge offset 1st order

c_5 Temperature coefficient bridge offset 2nd order

c_6 Temperature coefficient gain 1st order

c_7 Temperature coefficient gain 2nd order

2.3 Temperature Signal Conditioning Formula

The temperature measurement is enabled by selecting the appropriate analog output mode for the AOUT2 pin (CFGAPP2:AOUT2MD; see Table 18). The digital raw value $Z_{T,CORR}$ for the measured temperature is processed with a conditioning formula to remove offset and to compensate nonlinearity up to 2nd order. The signal conditioning equation is processed by the CMC and is defined as follows:

Range definition of input ($Z_{T,CORR}$):

$$Z_{T,CORR} \in [\ -2^{r_{ADC}-1};\ 2^{r_{ADC}-1}) \qquad \textbf{Equation 10}$$

Where

r_{ADC} Resolution of A/D conversion (14-bit)

$Z_{T,CORR}$ Raw A/D conversion result for temperature (auto-zero compensated)

In the following temperature conditioning formulas, equation **Equation 11** compensates the offset and fits the gain. The nonlinearity for the intermediate result Y_T is then corrected in equation **Equation 12** . The result of these equations is a non-negative value T for measured temperature in the range [0; 1).

Note that the conditioning coefficients ti are positive or negative values in two's complement format.

Temperature signal conditioning equations

$$Y_T = \frac{Z_{T,CORR}+t_0}{t_1} \quad Y_T \in [0;1) \qquad \textbf{Equation 11}$$

$$T = Y_T \times (1 - 2^{-15} \times t_2) + 2^{-15} \times t_2 \times Y_T^2 \qquad T \in [0;1) \qquad \textbf{Equation 12}$$

Where

Conditioning coefficients stored in EEPROM registers 08_{HEX} to $0A_{HEX}$ when temperature measurement is selected:

$t_i \in [-2^{15}; 2^{15})$, two's complement.

t_0 Temperature offset

t_1 Temperature gain

t_2 Temperature non-linearity correction 2nd order

2.4 Half-Bridge Signal Conditioning Formula

The half-bridge signal measurement is enabled by selecting the appropriate analog output mode for the AOUT2 pin (CFGAPP2:AOUT2MD; see Table 18). The digital raw value $Z_{HB,CORR}$ for the measured half-bridge signal is processed with a conditioning formula to remove offset and temperature dependency and to compensate nonlinearity up to 2nd order. The signal conditioning equation is processed by the CMC and is defined as follows:

Range definition of input ($Z_{HB,CORR}$ and $Z_{CT,CORR}$):

$$Z_{HB,CORR} \in [\ -2^{r_{ADC}};\ 2^{r_{ADC}})$$ **Equation 13**

$$Z_{CT,CORR} \in [\ -2^{r_{ADC}-1};\ 2^{r_{ADC}-1})$$ **Equation 14**

Where

r_{ADC} Resolution of A/D conversion (14-bit)

$Z_{HB,CORR}$ Raw A/D conversion result for half-bridge sensor signal (auto-zero compensated)

$Z_{CT,CORR}$ Raw A/D conversion result for calibration temperature (auto-zero compensated)

In the following conditioning formulas, equation **Equation 15** compensates the offset and fits the gain including its temperature dependence. The nonlinearity for the intermediate result Y_{HB} is then corrected in equation **Equation 16** . The result of these equations is a non-negative value HB for the measured half-bridge signal in the range [0; 1).

Note that the conditioning coefficients hi are positive or negative values in two's complement format.

Half-bridge signal conditioning equations:

$$Y_{HB} = \frac{Z_{HB,CORR}+h_0+2^{-(r_{ADC}-1)}\times h_4\times Z_{CT,CORR}+2^{-2(r_{ADC}-1)}\times h_5\times Z_{CT,CORR}^2}{h_1+2^{-(r_{ADC}-1)}\times h_6\times Z_{CT,CORR}+2^{-2(r_{ADC}-1)}\times h_7\times Z_{CT,CORR}^2} \qquad Y_{HB} \in [0;1)$$ **Equation 15**

$$HB = Y_{HB} \times (\ 1 - 2^{-15} \times\ h_2) + 2^{-15} \times\ h_2 \times\ Y_{HB}^2\ \ HB \in [0;1)$$ **Equation 16**

Where

Conditioning coefficients stored in EEPROM registers 08^{HEX} to $0E^{HEX}$ when half-bridge measurement is selected:

$h_i \in [-2^{15}; 2^{15})$, two's complement.

h_0 Half-bridge offset

h_1 Half-bridge gain

h_2 Half-bridge non-linearity correction 2nd order

h_4 Temperature coefficient half-bridge offset 1st order

h_5 Temperature coefficient half-bridge offset 2nd order

h_6 Temperature coefficient half-bridge gain 1st order

h_7 Temperature coefficient half-bridge gain 2nd order

2.5 Fitting Conditioning Result to Analog Output

The analog output is generated by a 5632-step D/A converter. This guarantees 12-bit analog output resolution for a typical output range of 10-to-90% VDDA or larger. For the calibration of the conditioning coefficients, the target output values must be fitted to that DAC resolution.

The fitting factor is $0.6875 = \frac{5632}{2^{13}}$ and is applied to the normalized target values BR, T, HB $\in$ [0; 1).

Note that this fitting is supported by the ZSSC3154 Evaluation Kit Software, which can be freely downloaded from Renesas's web site (ZSSC3154 - Automotive Sensor Signal Conditioner with Dual Analog Output | Renesas), but fitting is not part of the *RBIC1.DLL*, which is available on request for use with customer proprietary software.

2.6 Digital Filter Function for Analog Output

The ZSSC3154 offers digital (averaging) low-pass filters for the two analog output signals at pins AOUT1 and AOUT2. The output signal and mode at the AOUT2 pin are configured by EEPROM CFGAPP2:AOUT2MD (see section 6.4 and Table 18).

In NOM, the conditioned bridge sensor signal is always continually output at the AOUT1 pin. The AOUT1 output value is filtered with the integrating coefficient LPFAVRGBR and the differential coefficient LPFDIFFBR (see Table 14)

If the AOUT2 pin is configured to output a function of the bridge sensor signal, the AOUT2 output value is calculated with the conditioned and filtered bridge sensor value that is output at the AOUT1 pin.

If the AOUT2 pin is configured to output the temperature signal, the AOUT2 output value is filtered with the integrating coefficient LPFAVRGT and the differential coefficient LPFDIFFT.

If the AOUT2 pin is configured to output the half-bridge signal or a function of this signal, the AOUT2 output value is filtered with the integrating coefficient LPFAVRGHB and the differential coefficient LPFDIFFHB.

If the half-bridge sensor signal is output at the AOUT2 pin for validating the analog output of the bridge sensor signal at the AOUT1 pin, using equal filter coefficients is recommended.

The filter function is implemented as follows:

Digital Filter Function ($S_{OUT,0}$ and $S_{OUT,i}$)

$$S_{OUT,0} = S_0 \qquad \textbf{Equation 17}$$

$$S_{OUT,i} = S_{OUT,i-1} + \left(S_i - S_{OUT,i-1}\right) \times \frac{LPFDIFF+1}{2^{LPFAVRG}} \qquad i > 0 \qquad \textbf{Equation 18}$$

with $LPFAVRG,\ LPFDIFF \in [0; 7]$ and $S_{OUT,i} \in [0; 1)$

Where

S_i	Conditioned signal output result (refer to sections 2.2 through 2.4)
$S_{OUT,i}$	Filtered signal output result
LPFAVRG	Averaging filter coefficient
LPFDIFF	Differential filter coefficient

The result of the filter function is a non-negative value SOUT in the range [0; 1) which is used for continuously updating the analog output value during the measurement cycle.

Note that filtering is not applicable if CFGAPP:ADCMD is set to 11_{BIN} (7-bit) (see Table 15).

Note that setting the coefficients LPFAVRG and LPFDIFF to 0 disables the filter function.

Important: For proper function, ensure that the factor $\frac{\text{LPFDIFF}+1}{2^{\text{LPFAVRG}}}$ never becomes larger than 2!

Note that the readout of measurement values in NOM via I2C delivers conditioned but unfiltered result values S_i.

2.7 Analog Output Signal Range and Limitation

The filtered conditioning results S_{OUT} for the measured bridge signal, the temperature signal, or the half-bridge signal are output at the analog output pins AOUT1 and AOUT2 with a resolution greater than 12 bits. The analog output voltage is generated using a resistor-string DAC with 5632 steps, of which 5120 steps (256 to 5375) can be addressed. As a result, an adjustable range from 5% to 95% of the supply voltage is guaranteed, including all possible tolerances.

Setting the analog output outside the allowed range (for example via the SET_AOUTx command) will result in entering the diagnostic mode (DM) and setting the output to the DFB (Diagnostic Fault Band) level.

The ZSSC3154 offers an output limitation function for the analog output SOUT that clips the output signal with the configurable limits AOUTMINx and AOUTMAXx as illustrated in Figure 3. These output minimum and

maximum limits (13-bit accuracy) are defined in EEPROM with separate settings for the bridge, temperature, and half-bridge signal limits (see Table 14).

Note that these limit-setting registers ($0F_{HEX}$ through 12_{HEX}) are shared with the digital filter configuration (the 3 LSBs).

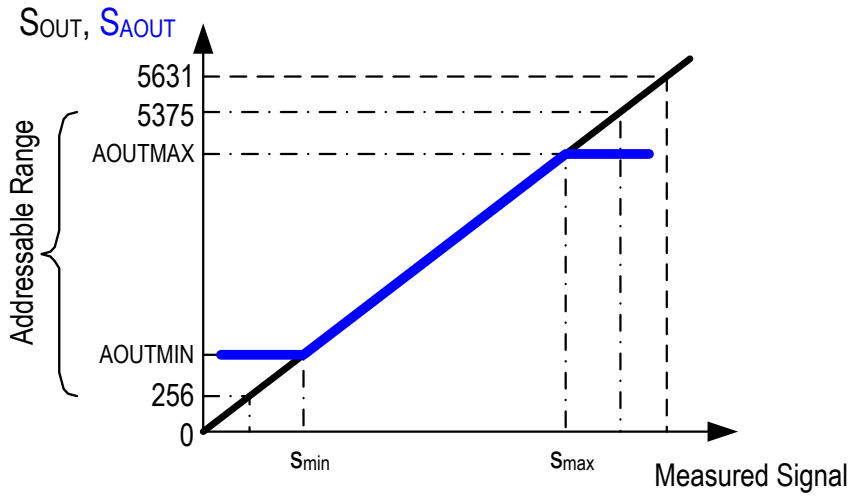


Figure 3. Accessible Output Signal Range and Limitation

Analog Output Limitation (S_{AOUT})

$$S_{AOUT}(S_{OUT} > AOUTMAX) = AOUTMAX \quad \textbf{Equation 19}$$

$$S_{AOUT}(S_{OUT} \in [AOUTMAX; AOUTMIN]) = S_{OUT} \quad \textbf{Equation 20}$$

$$S_{AOUT}(S_{OUT} < AOUTMIN) = AOUTMIN \quad \textbf{Equation 21}$$

$$\text{with AOUTMIN, AOUTMAX} \in [256; 5375] = [100_{HEX}; 14FF_{HEX}] \quad \textbf{Equation 22}$$

Where

- S_{OUT} Conditioned and filtered signal output result (refer to section 2.6)
- S_{AOUT} Clipped analog output result
- AOUTMIN Lower analog output limit
- AOUTMAX Upper analog output limit

The analog output voltage V_{AOUT} is ratiometric to the power supply (V_{VDDE} - V_{VSSE}) and can be calculated using the following formula.

Analog Output Voltage (V_{AOUT})

$$V_{AOUT} = (V_{VDDE} - V_{VSSE}) \times \frac{S_{AOUT}}{5632} \quad \textbf{Equation 23}$$

Where

- S_{AOUT} Conditioned, filtered and clipped signal output result
- V_{AOUT} Analog output voltage
- V_{VDDE}, V_{VSSE} Voltages at VDDE and VSSE pins

Note that the readout of measured values in NOM via I2C delivers conditioned but unfiltered and unclipped values for S.

Note that if the output is a function f of the bridge sensor signal via AOUT2 (1 – BR, ½ × BR, or ½ × (1 – BR)), which can be configured by CFGAPP2:AOUT2MD, the function is applied to the conditioned, filtered, and clipped bridge signal BR_{AOUT}. The resulting clipping limits for f(BR) at AOUT2 are consequently f(AOUTMINBR) and f(AOUTMAXBR).

3. Analog Output

3.1 Analog Output Modes

The ZSSC3154 provides two analog voltage outputs at the pins AOUT1 and AOUT2.

In NOM, the conditioned bridge sensor signal is continually output at the AOUT1 pin.

At the AOUT2 pin, several output modes are supported that are configured by EEPROM CFGAPP2:AOUT2MD:

- Continual output of the conditioned temperature signal
  The selected temperature sensor is configured with CFGAPP:TS. It is possible to select the same sensor as is used for calibration temperature or to select a different temperature sensor (see Table 17)
- Continual output of the conditioned half-bridge signal
  The half-bridge sensor signal can be used to validate the bridge sensor signal output at the AOUT1 pin (see Table 18). If the filter function is used for the bridge sensor signal, setting the coefficients for filtering the half-bridge signal to the same value is recommended. Note, that validating the main signal channel by the half-bridge sensor signal disables the analog front-end BIST functionality (AFEBIST, see Table 1 and Figure 1).
- Continual output of a function of bridge sensor signal
  Output of a function of the bridge sensor signal can be used to validate the bridge sensor signal output at the AOUT1 pin. Several functions are available and are calculated from the conditioned and filtered bridge sensor output value (see Table 18).
- Sequential Analog Output Mode (SEQAOUT)
  If the Sequential Analog Output Mode (SEQAOUT) is enabled, a configurable, continuous sequence is output on the AOUT2 pin (see Table 18 for the settings and section 3.3 for the order). The running sequence begins with the bridge signal or a function of the bridge signal; the Diagnostic Fault Band level driven by the DFBH pin; the inverted DFB level; and then the temperature or the half-bridge sensor. This allows validating the bridge sensor signal output at the AOUT1 pin. The Diagnostic Fault Band levels can be checked to ensure proper failure messaging.

3.2 Power-On Diagnostic Output

The ZSSC3154 provides a Power-On Diagnostic Output (PDO) wave. If enabled by EEPROM CFGSF:PDOENA, after power-on, the analog outputs at AOUT1 and AOUT2 run a one-time sequence of the upper and lower output limits followed by the diagnostic fault band output level (see Figure 4 and Figure 5). This can be used to check the operability of the chip and its output levels.

The upper and lower output limits are programmed in EEPROM independently for both output pins.

The diagnostic fault band output level depends on the DFBH pin. If the DFBH pin is open, both output pins AOUT1 and AOUT2 switch to the lower diagnostic fault band. If the DFBH pin is connected to VSSA, both output pins switch to the higher diagnostic fault band. Use the appropriate configuration for the user's application according to output pin loads.

Enabling the sequential analog output (SEQAOUT) for the AOUT2 pin with CFGAPP2:AOUT2MD disables PDO independently of control bit CFGSF:PDOENA.

If PDO is enabled, the startup window for one-wire communication via the AOUT1 pin is open during the two phases for the upper and lower output limits.

The duration T_{PDO} of each phase in the PDO sequence is 160ms at f_{OSC} = 2.6MHz. This timing can be shortened by setting the divider CFGAPP:TIMEDIV.

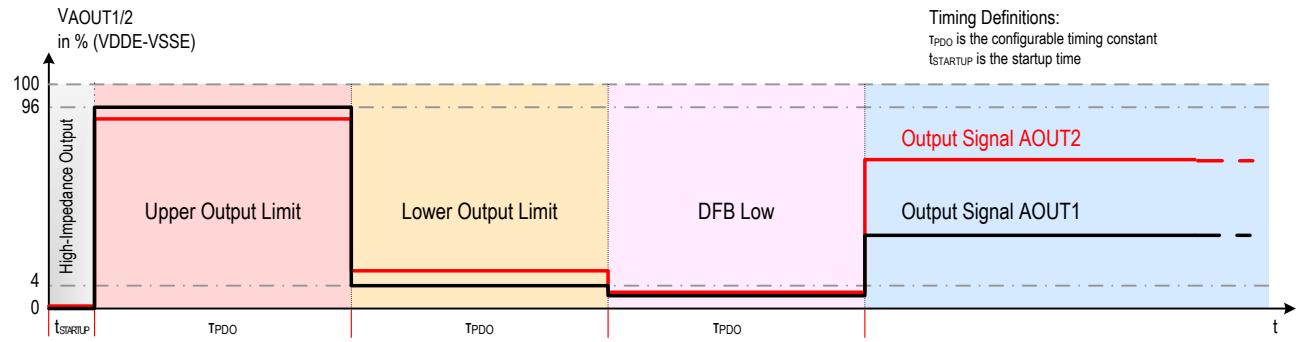


Figure 4. Power-On Diagnostic Output Wave with the DFBH Pin Open

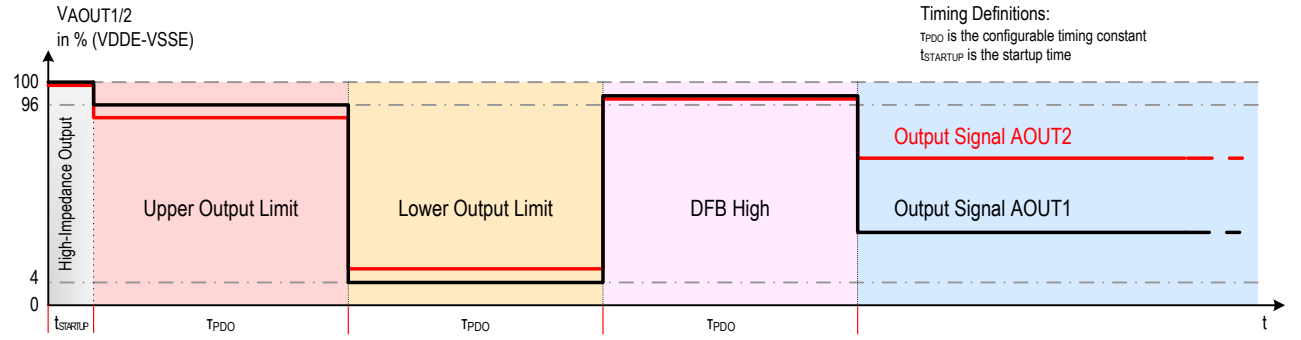


Figure 5. Power-On Diagnostic Output Wave with Pin DFBH Connected to VSSA

3.3 Sequential Analog Output Mode

The ZSSC3154 can provide the Sequential Analog Output Mode (SEQAOUT) at the AOUT2 pin if enabled by EEPROM CFAPP2:AOUT2MD. In this mode, the analog output at AOUT2 continuously runs a sequence of the bridge sensor signal followed by both diagnostic fault band output levels and by a 2nd configurable output signal (see Figure 6 and Figure 7). At the AOUT1 pin, the bridge sensor signal is continuously output.

The output of the diagnostic fault band levels can be used to check operability and proper failure messaging of the chip and to synchronize for evaluating both output signals. The actively driven diagnostic fault band level must be configured by connecting the DFBH pin to VSSA or by leaving it open. This actively driven diagnostic fault band level is output first in the SEQAOUT sequence; the reverse level follows.

The bridge sensor signal output in the SEQAOUT sequence can be manipulated by several functions selectable by CFGAPP2:AOUT2MD. This supports validating the bridge sensor signal output at pin AOUT1.

A half-bridge signal is selectable as the second signal output in the SEQAOUT sequence, which can also be used to validate bridge sensor signal.

Alternately the temperature signal can be selected as the second signal output. Depending on the selected temperature sensor (see Table 17, bits 5:3), this can be the sensor output used for calibration, which provides temperature compensation of the bridge sensor signal, or another temperature sensor.

The timing constant τ_{SEQ}, which determines duration of the individual phases in the SEQAOUT sequence, is 37ms at f_{OSC}=2.6MHz. This timing can be shortened by setting the divider CFGAPP:TIMEDIV.

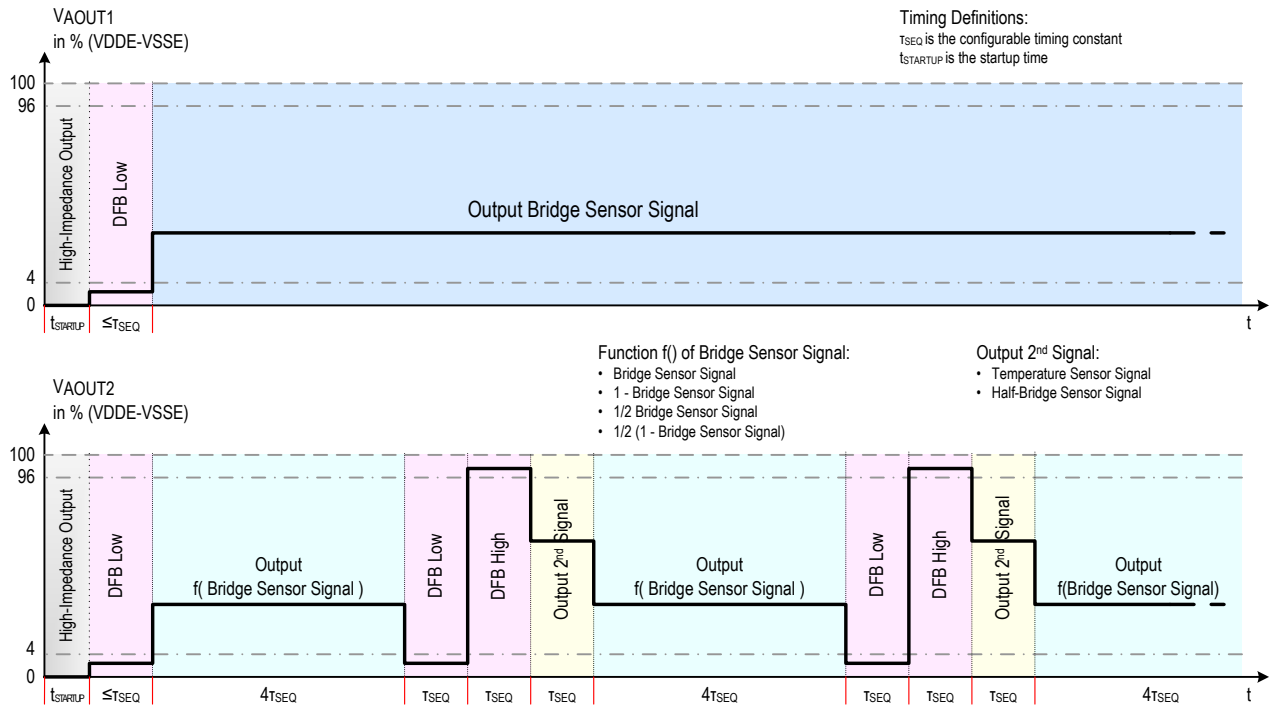


Figure 6. Sequential Analog Output with the DFBH Pin Open

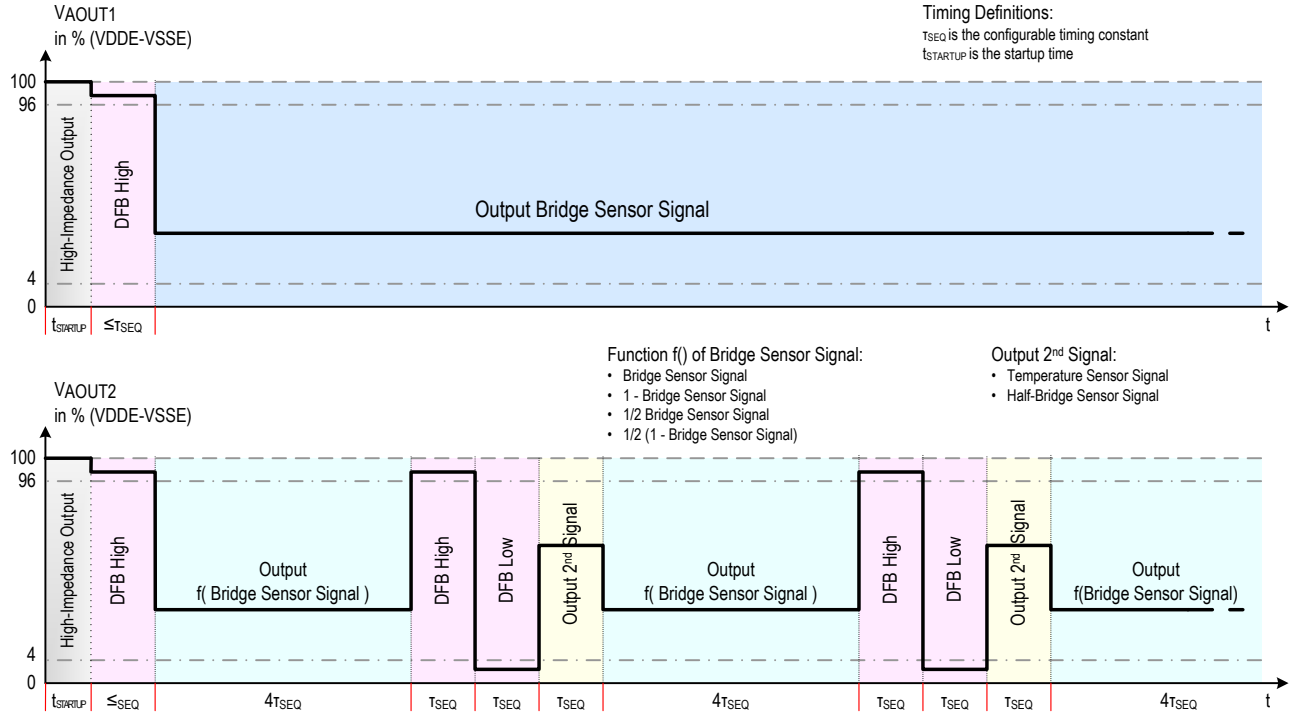


Figure 7. Sequential Analog Output with the DFBH Pin Connected to VSSA

4. Serial Digital Interfaces

4.1 General Description

The ZSSC3154 includes a serial digital I2C interface and a ZACwire™ interface for one-wire communication (OWI). The digital interfaces allow programming the EEPROM to configure the application mode for the ZSSC3154 and to calibrate the conditioning equations. It also provides the readout of the conditioning results as a digital value. The ZSSC3154 always functions as a slave.

I2C access to the ZSSC3154 is available in all operation modes independent of the programmed configuration. The I2C interface is enabled after power-on and a short initialization phase. In Normal Operation Mode (NOM), the result values for the bridge sensor signal and for the temperature or the half-bridge signal can be read out.

To access the ZSSC3154 by using OWI communication, the START_CM command must be transmitted in the startup window after power-on. For OWI communication, there are two possible startup window modes selectable by the CFGAPP2:OWIMD bit: with simultaneous analog output or without analog output during the startup window. The duration of the startup window depends on the selected analog output mode (refer to section 4.4.2). In NOM after the startup window, OWI communication is not applicable.

Transmitting the command START_CM enables the Command Mode (CM). In CM, either communication protocol can be used; all commands are available to process calibration. EEPROM write access via I2C is always available in CM. The EEPROM lock bit only affects EEPROM write access via OWI communication (refer to section 6.6).

In Diagnostic Mode (DM), both communication protocols can be used to read an error code to identify the error source. A non-configured device, identified by a non-consistent EEPROM signature, starts up in DM. Because the analog output pin AOUT1 is driven to the diagnostic range in DM, the analog output must be overwritten when starting communication using OWI communication. Starting CM from DM by transmitting the START_CM command is possible by using I2C or OWI communication.

In CM and DM, an alternating use of communication protocols is permitted.

4.1.1 Command Structure

A command consists of a device address byte and a command byte. Some commands (e.g. writing data into EEPROM) also include two data bytes. The command structure is independent from the communication protocol used. Refer to section 1.3 for details of working modes and section 5 for command descriptions.

4.1.2 Addressing

Addressing is supported by I2C and OWI communication protocol. Every slave connected to the master responds to a defined address. After generating the start condition, the master sends the address byte containing a 7-bit address followed by a data direction bit (R/W). A ‘0’ indicates a transmission from master to slave (WRITE); a ’1’ indicates a data request (READ). The addressed slave answers with an acknowledge bit (I2C only). All other slaves connected to the master ignore this communication.

The ZSSC3154 always responds to its general ZSSC3154 slave address, which is 28_{HEX} (7-bit). Via EEPROM programming, it is possible to allocate and activate an additional unique slave address within the range 20_{HEX} to $2F_{HEX}$ to the ZSSC3154. In this case, the device recognizes communication on both addresses, on the general one and on the additional one.

4.1.3 Read-Request

There are two general types of requests for reading data from the ZSSC3154:

- Digital read out: Continuously reading the conditioned result in NOM via I2C communication only.
  During the measurement cycle, the ZSSC3154 transfers the conditioned results for the bridge sensor signal and for the temperature or half-bridge signal (as configured by CFGAPP2:AOUT2MD[bit 13] in register 16_{HEX}; see Table 18) into the output registers of the I2C interface. These data will be sent if the master generates a read-request via I2C. The active measurement cycle is not interrupted by this.

- Calibration and/or configuration tasks via I2C or via OWI communication: Reading internal data (e.g., EEPROM content) or acquired measurement data in CM.
  To read internal and/or measurement data from the ZSSC3154 in CM, usually a specific command must be sent to transfer this data into the output registers of the digital interfaces. Thereafter the data will be sent if the master generates a read-request.

4.1.4 Communication Verification

In Normal Operation Mode (NOM) 16-bit data words are protected by even parity on the MSB (see section 4.2).

In Command Mode (CM) a read request is answered by the return of the data present in the digital interface output registers (2 bytes). Next a check sum is sent (1 byte) followed by the command which is answered (refer to section 4.2). The check sum and the returned command allow the verification of received data by the master. For details and exceptions, also see Table 12.

4.1.5 Communication Protocol Selection

Both available protocols, I2C and OWI, can be active simultaneously, but only one interface can be used at a time.

An OWI communication access is also possible if OWI communication is enabled and analog output is active at the same time (i.e. during the startup window, in Diagnostic Mode, or in Command Mode after START_CYCL commands). For this, the active output AOUT1 must be overwritten by the communication master, so generating a stop condition before starting the communication is recommended to guarantee a defined start of communication (refer to Figure 13).

4.2 Digital Output

A read request is answered by transmitting data from the digital interface output registers.

During the continuous measurement cycle (NOM, Temporary DM), the digital output via the I2C interface sends the 13-bit bridge sensor value and 13-bit temperature or half-bridge value (configured by the 16_{HEX} register CFGAPP2:AOUT2MD[bit 13], see Table 18), depending on the configured analog output mode. The diagnostic status (ERR) is included with 2 bits per 16-bit word. The MSB carries an even-parity (PAR). The data is updated continuously when a new conditioned value is calculated.

Table 3. I2C Read Request during NOM

Byte	Device Address		Bridge Sensor Signal				Temperature or Half-Bridge Signal			
			High Byte		Low Byte		High Byte		Low Byte	
	Address	R/W	PAR	ERR	Bridge signal (conditioned 13-bit value)		PAR	ERR	Temperature or Half-Bridge signal (conditioned 13-bit value)	
Value	28_{HEX}	1	P	00_{BIN}	MSB	LSB	P	00_{BIN}	MSB	LSB

During Temporary Diagnostic Mode (refer to section 1.3.3), the 2-bit diagnostic status ERR is set to 01_{BIN} for bridge sensor and main channel related failures and set to 10_{BIN} for temperature sensor related failures.

Table 4. I2C or OWI Read Request in Temporary DM

Byte	Device Address		Bridge Sensor Signal				Temperature or Half-Bridge Signal			
			High Byte		Low Byte		High Byte		Low Byte	
	Address	R/W	PAR	ERR	Possibly invalid Bridge signal (conditioned 13-bit value)		PAR	ERR	Possibly invalid Temperature or Half-Bridge signal (conditioned 13-bit value)	
Value	28_{HEX}	1	P	01_{BIN}/10_{BIN}	MSB	LSB	P	01_{BIN}/ 10_{BIN}	MSB	LSB

During Static Diagnostic Mode (DM), i.e., when a permanent failure has been detected, the diagnostic status ERR is set to 11_{BIN}. An error code is also transmitted to identify the failure source.

Table 5. I2C or OWI Read Request after Detecting an Error (Static DM)

Byte	Device Address		Error Code				Error Code			
			High Byte		Low Byte		High Byte		Low Byte	
	Address	R/W	PAR	ERR	Error code		PAR	ERR	Error Code	
Value	28_{HEX}	1	P	11_{BIN}	MSB	LSB	P	11_{BIN}	MSB	LSB

In Command Mode (CM) a 2-byte answer is generated for every received command. A 1-byte check sum is added followed by the command that is being answered. The check sum and the command echo allow verification of received data by the master. For details and exceptions, refer to section 5.3.

Table 6. I2C or OWI Read Request Answering a Command (CM)

Byte	Device Address		Answer		Verification	
			High Byte	Low Byte	High Byte	Low Byte
	Address	R/W	Response (2 byte)		Check Sum	Command Echo
Value	28_{HEX}	1	MSB LSB		MSB LSB	MSB LSB

4.3 I2C Protocol

For I2C communication, a data line (SDA) and a clock line (SCL) are required as illustrated in Figure 8.

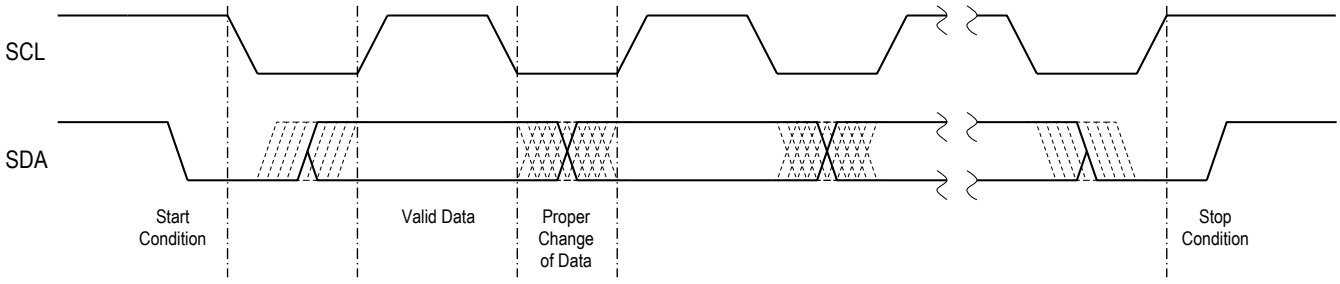


Figure 8. Principles of I2C Protocol

The I2C communication and protocol used are defined as follows:

- Idle period: When the bus is inactive, SDA and SCL are pulled-up to supply voltage VDDA.
- Start condition: A high-to-low transition on SDA while SCL is at the high level indicates a start condition. Every command must be initiated by a start condition sent by a master. A master can always generate a start condition.
- Stop condition: A low-to-high transition on SDA while SCL is at the high level indicates a stop condition. A command must be closed by a stop condition for the ZSSC3154 to start processing the command routine. The ZSSC3154 changes to inactive interface mode during processing of internal command routines started by a previously sent command.
- Valid data: Data is transmitted in bytes starting with the most significant bit (MSB). Each byte transmitted is followed by an acknowledge bit. Transmitted bits are valid if after a start condition, SDA maintains a constant level during a high period of SCL. The SDA level must change only when the clock signal at SCL is low.
- Acknowledge: An acknowledge after a transmitted byte is required. The master must generate an acknowledge-related clock pulse. The receiver (slave or master) pulls-down the SDA line during the acknowledge clock pulse. If no acknowledge is generated by the receiver, a transmitting slave will remain inactive. A transmitting master can abort the transmission by generating a stop condition and can then repeat the command.
  A receiving master must signal the end of transfer to the transmitting slave by not generating an acknowledge bit and by transmitting a subsequent stop condition.

- Write operation: During transmission from master to slave (WRITE), the device address byte is followed by a command byte and depending on the transmitted command, up to 2 optional data bytes. The internal microcontroller evaluates the received command and processes the related routine. See Figure 9.
- Read operation: After a data request from master to slave by sending a device address byte including a set-data-direction bit of 1, the slave answers by sending data from the interface output registers. The master must generate the transmission clock on SCL, acknowledges after each data byte (except after the last one), and then the stop condition. See Figure 10.
  A data request is answered by the interface module itself and consequently does not interrupt the current process of the internal microcontroller.
  The data in the output registers is sent continuously until a missed acknowledge occurs or a stop condition is detected. After transmitting all available data, the slave starts repeating the data.
  During operation, measurement cycle data is continuously updated with conditioning results. To get other data from the slave (e.g., EEPROM content) a specific command must be sent before the data request to initiate the transfer of this data to the interface output registers. This command does interrupt the current process of the internal microcontroller, e.g. the active measurement cycle.

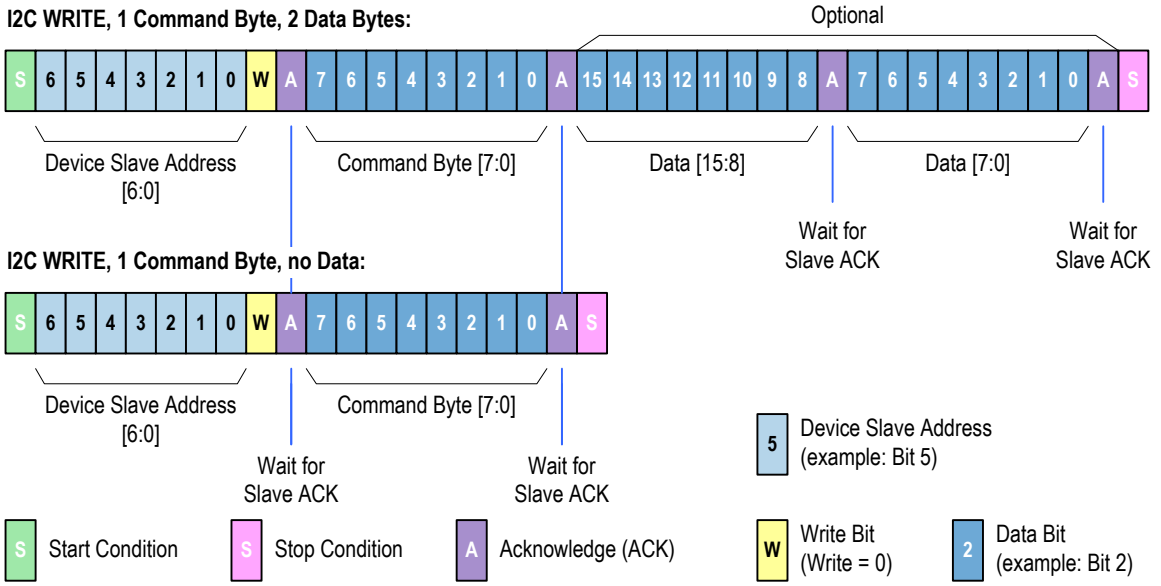


Figure 9. Write Operation I2C

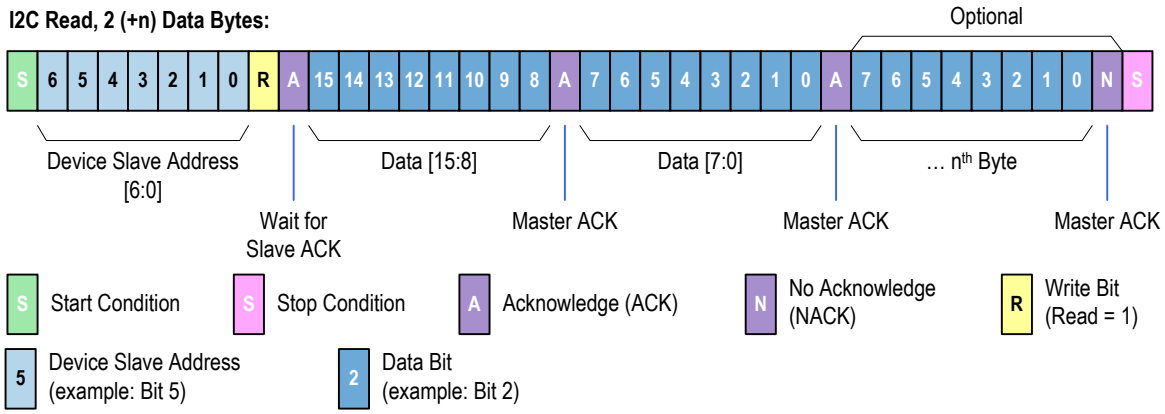


Figure 10. Read Operation I2C – (Data Request)

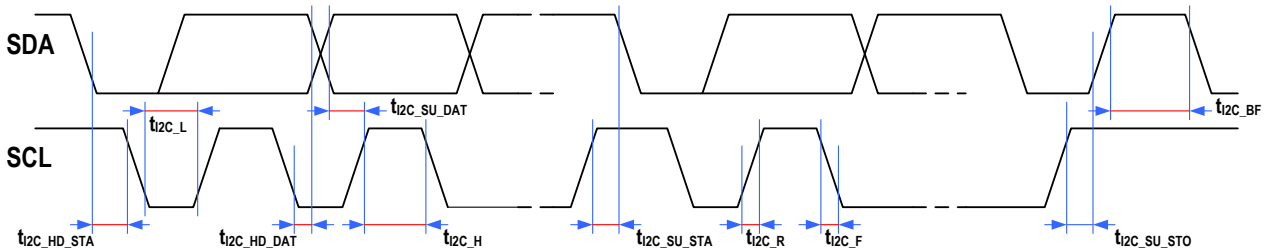


Figure 11. Timing I2C Protocol

Table 7. Timing I2C Protocol

No.	Parameter	Symbol	Min	Typical	Max	Unit	Conditions
1	SCL clock frequency	f_{SCL}			400	kHz	f_{OSC} ≥ 2MHz
2	Bus free time between start and stop condition	t_{I2C_BF}	1.3			µs	
3	Hold time start condition	$t_{I2C\_HD\_STA}$	0.6			µs	
4	Setup time repeated start condition	$t_{I2C\_SU\_STA}$	0.6			µs	
5	Low period SCL/SDA	t_{I2C_L}	1.3			µs	
6	High period SCL/SDA	t_{I2C_H}	0.6			µs	
7	Data hold time	$t_{I2C\_HD\_DAT}$	0			µs	
8	Data setup time	$t_{I2C\_SU\_DAT}$	0.1			µs	
9	Rise time SCL/SDA	t_{I2C_R}			0.3	µs	
10	Fall time SCL/SDA	t_{I2C_F}			0.3	µs	
11	Setup time stop condition	$t_{I2C\_SU\_STO}$	0.6			µs	
12	Noise interception SDA/SCL	t_{I2C_NI}			50	ns	Spike suppression

4.4 One-Wire Communication (OWI)

The ZSSC3154 utilizes a ZACwire™ interface, a digital interface concept for one-wire communication (OWI). It combines a simple and easy protocol adaptation with cost-saving pin sharing. The OWI communication principle is derived from the I2C protocol, so becoming familiar with the I2C protocol is recommended for an understanding of OWI communication.

Both the analog voltage output for normal operation and the one-wire digital interface for calibration use the same pin AOUT1. This enables “end of line” calibration; no additional pins are required to digitally calibrate a finished assembly.

4.4.1 Properties and Parameters

The ZSSC3154 functions as an OWI slave. An external master must control the communication by transmitting commands or data requests. Figure 12 explains the physical OWI connection in principle. Note that pulling up the OWI connection line must be done externally. There is no guarantee for using the ZSSC3154 internal pull-up. In addition, it might be necessary to implement a master push-pull driver to overwrite an analog output voltage at pin AOUT1 ($I_{OUT,max}$ = 20mA).

OWI communication is self-locking (synchronizing) on the master’s communication speed in the range of the defined OWI bit time, which is guaranteed for the ZSSC3154’s clock frequency in the range of 2 to 3MHz.

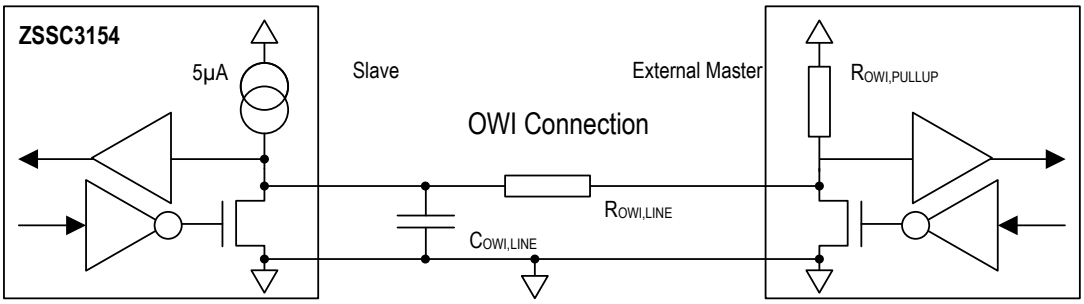


Figure 12. Block Schematic of an OWI Connection

Table 8. OWI Interface Basic Parameters

No.	Parameter	Symbol		Unit	Conditions
1	OWI bit time	$t_{OWI,BIT}$	0.04 to 4	ms	$t_{OWI,BIT} = 10 * R_{OWI,PULLUP} \times C_{OWI,LINE}$ Guaranteed for f_{OSC} = 2 to 3 MHz.
2	Pull-up resistance master	$R_{OWI,PULLUP}$	3.3 (typical)	kΩ	
3	OWI line resistance	$R_{OWI,LINE}$	< 0.01	$R_{OWI,PULLUP}$	
4	OWI load capacitance	$C_{OWI,LOAD}$	50 (typical)	nF	Total OWI line load.
5	Voltage level LOW	$V_{OWI,L}$	0.2	VDDA	Min VDDA is 4.2V @ 4.5V VDDE
6	Voltage level HIGH	$V_{OWI,H}$	0.75	VDDA	Max VDDA is 5.5V @ 5.5V VDDE

1. See Table 9 for additional specifications related to signal conditions and bit definitions.

4.4.2 OWI Startup Window

OWI communication must be started via the start command START_CM [72 74]$_{HEX}$ sent to the AOUT1 pin within a time window of 200ms at f_{OSC}= 2.6MHz after power-on. If this OWI startup window expires without the ZSSC3154 receiving a valid start command, OWI access is disabled.

The OWI startup window of 5ms at f_{OSC}= 2.6MHz is activated immediately after initialization.

OWI startup window is affected by several EEPROM configuration bits:

- CFGAPP2:OWIMD → OWI startup window mode
  Analog voltage output starts after expiration of the OWI startup window of 200ms at f_{OSC}= 2.6MHz. If CFGAPP2:OWIMD is set to 1, analog voltage output starts immediately after power-on, simultaneously with the OWI startup window. If CFGAPP2:OWIMD is set to 1, the OWI window is shortened to 50ms at f_{OSC}= 2.6MHz and the OWI master must overwrite the active analog voltage output on the AOUT1 pin to send the start command START_CM if OWI communication is needed.
- CFGSF:PDOENA → Power-on Diagnostic Output
  If the Power-on Diagnostic Output (PDO) is activated, a diagnostic sequence of the output limits and the diagnostic fault band (DFB) level is sent after power-on. The OWI startup window occurs simultaneously during the two PDO phases for the upper and lower analog output limits, so the startup window is 320ms at f_{OSC} = 2.6MHz. (Refer to section 3.2 for further details on the timing).
- CFGAPP2:AOUT2MD → Sequential Analog Output Mode (SEQAOUT) at AOUT2
  When Sequential Analog Output Mode (SEQAOUT; see AOUT2MD in Table 18) is enabled, the OWI startup window is activated immediately after initialization and remains open until the beginning of the first occurrence of the Second Analog Signal on the AOUT2 pin (refer to section 3.3).
  Note: Enabling SEQAOUT disables the Power-On Diagnostic Output (PDO) regardless of the setting for the control bit CFGSF:PDOENA.

In Command Mode (CM), OWI communication is always possible. After commands requesting an analog output at pin AOUT1, the OWI master must overwrite the analog voltage output for further communication.

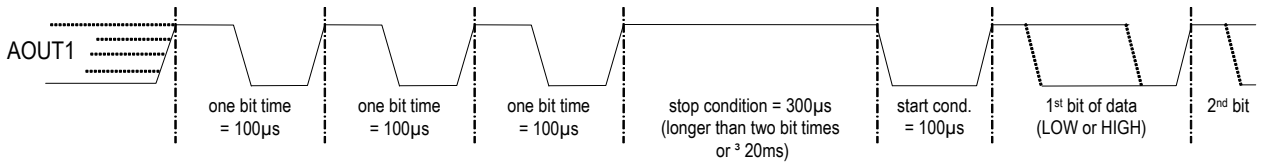
In Diagnostic Mode (DM), OWI communication is also possible. If the pin AOUT1 is driven to Diagnostic Fault Band Low (DFBL), again the OWI master must overwrite this voltage level for communication. Note that an unconfigured ZSSC3154 with an invalid EEPROM signature always starts in DM.

4.4.3 OWI Protocol

OWI communication is always initiated by a master. Transmission starts with an address byte including a read/write bit to define the direction of the following byte transfer.

The OWI protocol is defined as follows:

- Idle Period
  During inactivity of the bus, the OWI communication line is pulled-up to supply voltage V_{VDDE} by an external resistor.
- Start Condition
  When the OWI communication line is in idle mode, a low pulse with a minimum width of 10µs [1] and then a return to high indicates a start condition. Every command must be initiated by a start condition sent by a master. A master can generate a start condition only when the OWI line is in idle mode.
- Stop Condition
  A constant level at the OWI line (no transition from low to high or from high to low) for at least twice the period of the last transmitted valid bit indicates a stop condition. Without considering the last bit-time (secure stop condition), a stop condition is generated with a constant level at the OWI line for at least 20ms.
  The master finishes a transmission by changing back to the high level (idle mode). Every command (refer to the subsequent “Write Operation” section) must be closed by a stop condition to start the processing of the command. The master must interrupt a sending slave after it has completed a data request (refer to the subsequent “Read Operation” section) by clamping the OWI line to the low level for generating a stop condition.
  In the case of an active analog voltage output at pin AOUT1, the output level must be overwritten by the OWI master. For example, this can occur if the OWI communication is started in the OWI startup window with a simultaneous analog voltage output. To ensure correct communication, first generate a stop condition (see Figure 13) before sending the first command (e.g., START_CM). After the ZSSC3154 receives this first command, the analog output is disabled and OWI communication functions without sending additional sequences for this purpose.



Note: Bit times shown here are examples based on a given f_{OSC}.

Figure 13. OWI and Actively Driven AOUT1—Starting OWI Communication with a Stop Condition

- Valid Data
  Data is transmitted in bytes (8 bits) starting with the most significant bit (MSB). Transmitted bits are recognized after a start condition at every transition from low to high at the OWI line. The value of the transmitted bit depends on the duty ratio between the high phase and high/low period (bit period, $t_{OWI,BIT}$ in Figure 16). A duty ratio greater than 1/8 and less than 3/8 is detected as ‘0’, a duty ratio greater than 5/8 and less than 7/8 is detected as ‘1’. The bit period of consecutive bits must not change by more than a factor of 2 because the stop condition is detected in this case.
- Write Operation
  During transmission from master to slave (WRITE), the address byte including a set data direction bit (0 for WRITE) is followed by a command byte and, depending on the transmitted command, by an optional 2 data bytes. The internal microcontroller evaluates the received command and processes the requested routine.

[1] 10µs is the minimum t_{OWI_START} that guarantees the OWI start condition in the range of f_{OSC} = 2 to 3 MHz.

Figure 14 illustrates the writing of a command with two data bytes and a command without data bytes. A detailed description of the command set is given in section 5.1.

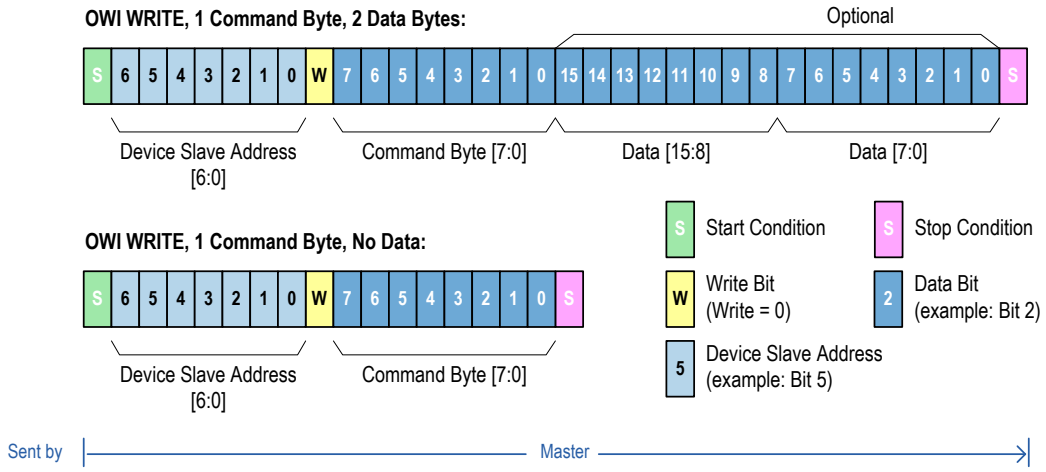


Figure 14. OWI Write Operation

- Read Operation
  After a data request from the master to the slave via sending an address byte including a set data direction bit (1 for READ), the slave answers by sending data from the interface output registers. The slave generates the data bits with a bit period equal to the last received bit (R bit). The master must generate a stop condition after receiving the requested data. (See Figure 15.)
  A data request is answered by the interface module itself and consequently does not interrupt the current process of the internal microcontroller.
  To get certain data from the slave (e.g. EEPROM content), the appropriate command must be sent before the data request to initiate the transfer of this data into the interface output registers. This command does interrupt the current operation of the internal microcontroller and consequently also an active measurement cycle.
  The data in the output registers is sent continuously until a stop condition is detected, after transmitting all available data, the slave starts repeating the data. Note that during the active measurement cycle, data is continuously updated with conditioned results.

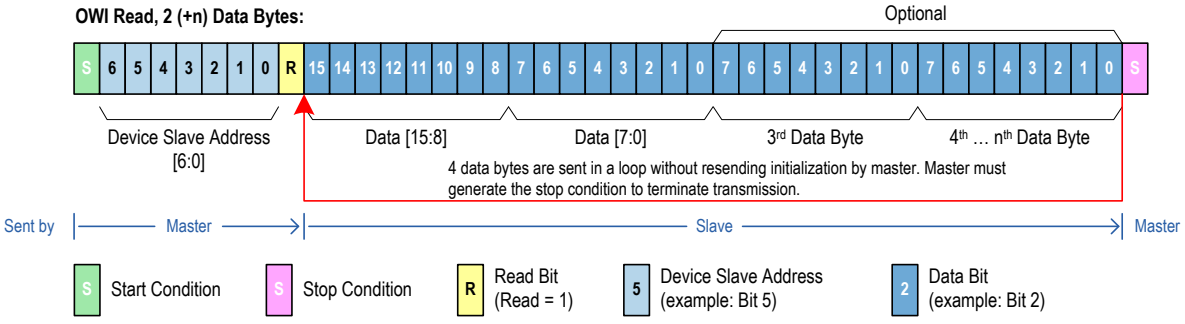


Figure 15. OWI Read Operation

OWI protocol timing and parameters are specified in Figure 16 and in Table 9.

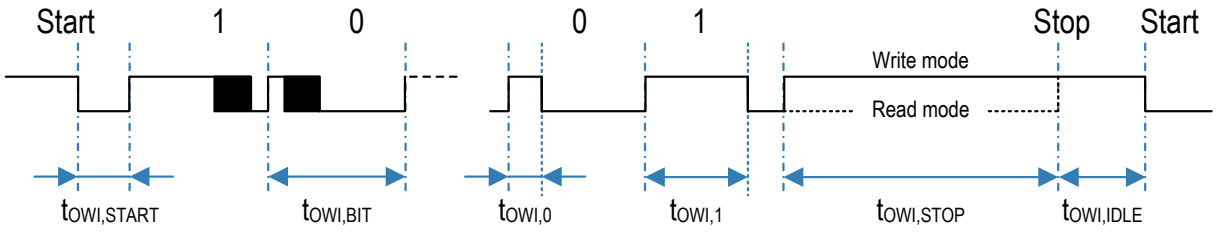


Figure 16. OWI Protocol Timing

Table 9. OWI Interface Signal Parameters

No.	Parameter	Symbol	Min	Typical	Max	Unit	Conditions
1	Bus free time	$t_{OWI,IDLE}$	25			µs	Between stop and start conditions
2	Hold time start condition	$t_{OWI,START}$	10			µs	
3	Bit time [2]	$t_{OWI,BIT}$	25		8000	µs	Min: f_{OSC} = 3.2MHz, max: f_{OSC} = 2MHz
4	Duty ratio bit ‘0’	$t_{OWI,0}$	0.125	0.25	0.375	$t_{OWI,BIT}$	
5	Duty ratio bit ‘1’	$t_{OWI,1}$	0.625	0.75	0.875	$t_{OWI,BIT}$	
6	Hold time stop condition	$t_{OWI,STOP}$	2.0	1.0		$t_{OWI,BIT}$	Depends on the bit time of the last valid transmitted bit
7	Bit time deviation	$t_{OWI,BIT,DEV}$	0.55	1.0	1.5	$t_{OWI,BIT}$	Current bit time to previous bit time

1. See Table 8 for basic OWI interface parameters.
2. This bit time range is achievable with different frequency adjustments for minimum and maximum values (see section 5.4.2).

5. Interface Commands

5.1 Command Set

All commands are available for I2C and OWI communication, but only in Command Mode (CM). CM is initiated by sending the command START_CM [72 74]$_{HEX}$.

Every received command is answered. The response consists of 2 bytes for the requested data or a validation code, 1-byte check sum, and 1-byte command echo. See Table 10 for exceptions (also refer to section 5.2).

EEPROM programming must be enabled first by sending the EEP_WRITE_EN command [6C F7 42]$_{HEX}$.

Table 10. Command Set

Com-mand	Data	Command	Notes	Processing Time @ f_{osc} = 2.6MHz
01HEX		START_CYC_EEP	Start measurement cycle including initialization from EEPROM or RAM. Analog output mode as configured. Note that selected analog output mode influences startup time.	500µs
02_{HEX}		START_CYC_RAM		
03_{HEX}		START_CYC_ EEP_OWI	Start measurement cycle including initialization from EEPROM or RAM. OWI communication remains enabled during the measurement cycle. No analog output is generated at AOUT1. Return conditioned but unfiltered conversion result values via OWI if requested. Analog output mode at AOUT2 as configured. Note that selected analog output mode influences startup time.	500µs
04_{HEX}		START_CYC_ RAM_OWI		
10_{HEX} to 27_{HEX}		READ_RAM	Read data from RAM addresses 00_{HEX} through 17_{HEX}.	100µs
30_{HEX} to $4B_{HEX}$		READ_EEP	Read data from EEPROM addresses 00_{HEX} through $1B_{HEX}$.	100µs

Com-mand	Data	Command	Notes	Processing Time @ f_{osc} = 2.6MHz
50_{HEX}		ADJ_OSC_ACQ	Use this command with OWI communication only! Acquire frequency ratio (f_{OSC} / f_{OWI}) where f_{OSC} is the frequency of internal oscillator f_{OWI} is the OWI communication frequency Use this for adjusting the internal oscillator frequency via CFGAPP2:OSCADJ (refer to section 5.4.2). Returns $CF50_{HEX}$ if command is received via I2C.	100µs
51_{HEX}		START_AD_BIST	Start cyclic A/D conversion for analog front-end BIST (internally generated differential input voltage).	500µs
52_{HEX}		START_AD_ BIST_AZC	Start cyclic A/D conversion for analog front-end BIST (internally generated differential input voltage) including auto-zero.	500µs
53_{HEX}		START_AD_SAC	Start cyclic A/D conversion for Sensor Aging Check (bridge common mode voltage measurement).	500µs
54_{HEX}		START_AD_SAC_AZC	Start cyclic A/D conversion for Sensor Aging Check (bridge common mode voltage measurement) including auto-zero.	500µs
56_{HEX}		RD_AD_CNT_1	Read result values of START_AD_CNT command: Read 1st result value (bridge or half-bridge) and 2nd result value (calibration temperature) Also see RD_AD_CNT_2.	100µs
57_{HEX}		RD_AD_CNT_2	Read result values of START_AD_CNT command: Read 3rd result value (half-bridge or temperature, or 00_{HEX}´if only two input channels were selected) and check sum (inverted sum of all 3 result values). Also see RD_AD_CNT_1.	100µs
58_{HEX}		GET_ERR_STATUS	Read and reset error code.	100µs
$5A_{HEX}$		GET_SENS_STATUS	Evaluate status information from Sensor Connection and Sensor Short Checks. Returns $C35A_{HEX}$ if check passed. Returns $CF5A_{HEX}$ if check failed. Read resulting error code with command GET_ERR_STAT to distinguish the root causes if check failed. Error code is reset before check.	3 ×A/D conversion time
$5B_{HEX}$		GET_BCC_STATUS	Evaluate status information from Broken Chip Check. Returns $C35B_{HEX}$ if check passed. Returns $CF5B_{HEX}$ if check failed.	100µs
$5C_{HEX}$		OUT_VDDB0	Output analog supply voltages at pin AOUT1: ▪ OUT_VDDB0 → 10% VDDB (±5%) ▪ OUT_VDDB1 → 90% VDDB (±5%) ▪ OUT_VDD → 100% VDD (±5%) ▪ OUT_VDDA → 50% VDDA (±5%) Returns $C35x_{HEX}$ if command is processed. Reset this output mode by command SET_AOUT1 $[60]_{HEX}$ or by commands START_CYC_* $[0*]_{HEX}$.	100µs
$5D_{HEX}$		OUT_VDDB1		
$5E_{HEX}$		OUT_VDD		
$5F_{HEX}$		OUT_VDDA		
60_{HEX}	2 bytes	SET_AOUT1	Set the analog output AOUT1 (DAC) to value defined by data bytes. Important note: If the data byte is outside the valid range of 0100_{HEX} to $14FF_{HEX}$, the ZSSC3154 will enter DM and output the DFB (Diagnostic Fault Band) level. The AOUT1 pin goes into tri-state during the command processing.	100µs

Com-mand	Data	Command	Notes	Processing Time @ f_{osc} = 2.6MHz
61_{HEX}	2 bytes	SET_AOUT2	Set the analog output AOUT2 (DAC) to value defined by data bytes. Important note: If the data byte is outside the valid range of 0100_{HEX} to $14FF_{HEX}$, the ZSSC3154 will enter DM and output the DFB (Diagnostic Fault Band) level. The AOUT2 pin goes into tri-state during the command processing.	100µs
62_{HEX}	2 bytes	START_AD_CNT	Process <n> times A/D conversion for main input signals including auto-zero compensation (refer to section 5.4.1). data[15:13] is digital Low Pass Filter averaging coefficient with range [0; 7] for the selected measurement (see section 2.6). data[12:11] selects the measured input channels: ▪ 00_{BIN} Bridge and Calibration Temperature ▪ 01_{BIN} Half-Bridge and Calibration Temperature ▪ 10_{BIN} Bridge, Calibration Temperature, and Temperature ▪ 11_{BIN} Bridge, Calibration Temperature, and Half-Bridge data[10:0] is the number <n> of measurements to process. Responses with the two most-recent result values (Bridge or Half-Bridge, Calibration Temperature) while processing measurement. Returns $C362_{HEX}$ if measurement is finished. Final measurement results can be read out using RD_AD_CNT_1 or RD_AD_CNT_2 commands or stored to EEPROM using STORE2_AD_CNT or STORE3_AD_CNT commands.	100µs + (4×n OR 6×n) ×A/D conversion time depending on the number of measurands
63_{HEX}	2 bytes	STORE2_AD_CNT	Write two result values (Bridge or Half-Bridge, Calibration Temperature) of START_AD_CNT to EEPROM addresses <data> to <data+1>. Refer to section 5.4.1 for details. Returns $C363_{HEX}$ if command is processed. Returns $CF00_{HEX}$ if EEPROM programming is disabled.	2 ×12.5ms
64_{HEX}	2 bytes	STORE3_AD_CNT	Write three result values (Bridge, Calibration Temperature, and Temperature or Half-Bridge) of START_AD_CNT to EEPROM addresses <data> to <data+2>. Refer to section 5.4.1 for details. Returns $C364_{HEX}$ if command is processed. Returns $CF00_{HEX}$ if EEPROM programming is disabled.	3 ×12.5ms
65_{HEX}	2 bytes	ADJ_OSC_WRI	Write to RAM and activate Oscillator Adjust value CFGAPP2:OSCADJ and Spread Spectrum enable CFGAPP2:OSCSS (see Table 18). Returns complete new configuration word CFGAPP2.	100µs
$6C_{HEX}$	2 bytes	EEP_WRITE_EN	Enable data write to EEPROM. To be sent with data $F742_{HEX}$. Other data disables EEPROM write. Returns $C36C_{HEX}$ if EEPROM programming is enabled. Returns $CF6C_{HEX}$ if EEPROM programming is disabled.	100µs
$6D_{HEX}$	2 bytes	CHECK_EEP	Calculate and return EEPROM signature. Low data byte is start address; high data byte is end address of evaluated area. Use [6D 17 00] for reading EEPROM signature of stored configuration.	250µs
72_{HEX}	1 byte	START_CM	Start Command Mode. To be sent with data 74_{HEX}. Returns $C372_{HEX}$ if Command Mode is enabled.	100µs

<table>
<tr><th>Com-mand</th><th>Data</th><th>Command</th><th>Notes</th><th>Processing Time @ f_{osc} = 2.6MHz</th></tr>
<tr><td>80_{HEX} to 97_{HEX}</td><td>2 bytes</td><td>WRITE_RAM</td><td>Write data to RAM addresses 00_{HEX} through 17_{HEX}.</td><td>100µs</td></tr>
<tr><td>$A0_{HEX}$ to BA_{HEX}</td><td>2 bytes</td><td>WRITE_EEP</td><td>Write data to EEPROM addresses 00_{HEX} through $1A_{HEX}$.
Note that there is no write access to Renesas word at address $1B_{HEX}$.
Returns $CF00_{HEX}$ if EEPROM programming is disabled.</td><td>12.5ms</td></tr>
<tr><td>$C0_{HEX}$</td><td></td><td>COPY_EEP2RAM</td><td>Copy content of EEPROM address 00_{HEX} through 17_{HEX} to RAM.
Restores EEPROM configuration in RAM.
Does not process EEPROM signature check.
Returns $C3C0_{HEX}$ if command is processed.</td><td>200µs</td></tr>
<tr><td>$C3_{HEX}$</td><td></td><td>COPY_RAM2EEP</td><td>Copy content of RAM address 00_{HEX} through 17_{HEX} to EEPROM.
Generates EEPROM signature; writes it to address 18_{HEX}.
Returns $C3C3_{HEX}$ if copy is successfully processed.
Returns $CFC3_{HEX}$ if copy failed.
Returns $CF00_{HEX}$ if EEPROM programming is disabled.</td><td>230ms</td></tr>
<tr><td>$C4_{HEX}$</td><td></td><td>LOAD_RAM_STD</td><td>Load RAM with default contents from ROM.
Returns $C3C4_{HEX}$ if load and signature check is successfully processed.
Returns $CFC4_{HEX}$ if load failed.
<table>
<tr><th colspan="4">RAM Contents with Default Values from ROM</th></tr>
<tr><td>c_0</td><td>4000_{HEX}</td><td>Upper Limit BIST</td><td>$FFFF_{HEX}$</td></tr>
<tr><td>c_1</td><td>$7FFF_{HEX}$</td><td>Lower Limit CMV</td><td>0000_{HEX}</td></tr>
<tr><td>c_2</td><td>0000_{HEX}</td><td>Upper Limit CMV</td><td>$FFFF_{HEX}$</td></tr>
<tr><td>c_3</td><td>0000_{HEX}</td><td>Lower Limit BR</td><td>0800_{HEX}</td></tr>
<tr><td>c_4</td><td>0000_{HEX}</td><td>Upper Limit BR</td><td>$A7F8_{HEX}$</td></tr>
<tr><td>c_5</td><td>0000_{HEX}</td><td>Lower Limit T</td><td>0800_{HEX}</td></tr>
<tr><td>c_6</td><td>0000_{HEX}</td><td>Upper Limit T</td><td>$A7F8_{HEX}$</td></tr>
<tr><td>c_7</td><td>0000_{HEX}</td><td>CFGAFE</td><td>0220_{HEX}</td></tr>
<tr><td>t_0</td><td>1800_{HEX}</td><td>CFGAFE2</td><td>0026_{HEX}</td></tr>
<tr><td>t_1</td><td>$7FFF_{HEX}$</td><td>CFGAPP</td><td>0000_{HEX}</td></tr>
<tr><td>t_2</td><td>0000_{HEX}</td><td>CFGAPP2</td><td>0018_{HEX}</td></tr>
<tr><td>Lower Limit BIST</td><td>0000_{HEX}</td><td>CFGSF</td><td>4000_{HEX}</td></tr>
</table></td><td>200µs</td></tr>
<tr><td>$C9_{HEX}$</td><td></td><td>GEN_EEP_SIGN</td><td>Calculate and return EEPROM signature and write it to EPROM address 18_{HEX}.
Returns $CF00_{HEX}$ if EEPROM programming is disabled.</td><td>12.7ms</td></tr>
<tr><td>CA_{HEX}</td><td></td><td>GET_RAM_SIGN</td><td>Calculate and return RAM signature.</td><td>250µs</td></tr>
<tr><td>CE_{HEX}</td><td></td><td>GET_ROM_STATUS</td><td>Check ROM Diagnostic Status.
Returns $C3CE_{HEX}$ if no failure is detected.
Returns $CFCE_{HEX}$ if a failure is detected.</td><td>10ms</td></tr>
<tr><td>CF_{HEX}</td><td></td><td>GET_REVISION</td><td>Get Hardware and ROM Revision.</td><td>100µs</td></tr>
</table>

1. Refer to Table 12 for a summary of responses to commands.

All Dx commands are used for the calibration process and write raw conversion result values to the digital output registers. No analog output is generated. OWI communication remains enabled during the measurement cycle.

Note: For the D0 to D7, DC, and DD commands, the processing time with f_{OSC} = 2.6MHz is 100µs plus the A/D conversion time. The processing time is 2 times this value for the D8 to DB and DE commands.

Note: Enabling the A/D converter clock divider (i.e., bit CFGAFE:ADCSLOW is set to 1) doubles only the A/D conversion time.

Table 11. Command Set – Data Acquisition Commands

Command	Command	Notes
$D0_{HEX}$	START_AD_P	Start cyclic A/D conversion at bridge sensor channel.
$D1_{HEX}$	START_AD_CT	Start cyclic A/D conversion at calibration temperature channel.
$D2_{HEX}$	START_AD_T	Start cyclic A/D conversion at temperature channel.
$D3_{HEX}$	START_AD_HB	Start cyclic A/D conversion at half-bridge channel.
$D4_{HEX}$	START_AD_PAZ	Start cyclic A/D conversion for auto-zero at bridge sensor channel.
$D5_{HEX}$	START_AD_CTAZ	Start cyclic A/D conversion for auto-zero at calibration temperature channel.
$D6_{HEX}$	START_AD_TAZ	Start cyclic A/D conversion for auto-zero at temperature channel.
$D7_{HEX}$	START_AD_HBAZ	Start cyclic A/D conversion for auto-zero at half-bridge channel.
$D8_{HEX}$	START_AD_P_AZC	Start cyclic A/D conversion at bridge sensor channel including auto-zero.
$D9_{HEX}$	START_AD_CT_AZC	Start cyclic A/D conversion at calibration temperature channel including auto-zero.
DA_{HEX}	START_AD_T_AZC	Start cyclic A/D conversion at temperature channel including auto-zero.
DB_{HEX}	START_AD_HB_AZC	Start cyclic A/D conversion at half-bridge channel including auto-zero.
DC_{HEX}	START_AD_SSCP	Start cyclic A/D conversion for positively biased Sensor Short Check.
DD_{HEX}	START_AD_SSCN	Start cyclic A/D conversion for negatively biased Sensor Short Check.
DE_{HEX}	START_AD_SSCP-SSCN	Start cyclic A/D conversion for positively biased Sensor Short Check minus negatively biased Sensor Short Check.

5.2 Command Processing

All implemented commands are available for both protocols – I2C and OWI. If Command Mode (CM) is active, a received valid command interrupts the internal microcontroller (CMC) and starts a routine processing the received command. During this processing time, the interfaces are disabled and transmitted commands are ignored. The processing time depends on the internal system clock frequency. A command always returns data (e.g., register contents, acquired measurement data) to interface output registers, which can be read by a read request.

5.3 Digital Output Data in Command Mode

Digital output data in CM consists of two 16-bit words that can be read by an I2C or OWI read request. Content of data words depends on the previously received command.

Table 12. Digital Output Data Resulting from Processed Commands

Mode/ Commands	Output Data Word 1		Output Data Word 2	
	High Byte	Low Byte	High Byte	Low Byte
Commands with data response	Requested data		Check sum [1]	Processed command
Commands without data response	Success code [C3 command]$_{HEX}$		Check sum [1]	Processed command
	Reject code [CF command]$_{HEX}$			
Unknown commands	Reject code [CF 00]$_{HEX}$		Check sum [1]	Received command
START_CYC [01]$_{HEX}$, [02]$_{HEX}$	Conditioned values, error status and parity as transmitted in NOM (see Table 3) or in DM (see Table 4 or Table 5)			
START_AD_CNT [62]$_{HEX}$ during measurement	1st measured raw value (Bridge or Half-Bridge)		2nd measured raw value (Calibration Temperature)	
RD_AD_CNT_1 [56]$_{HEX}$	1st measured raw value from START_AD_CNT command (Bridge or Half-Bridge)		2nd measured raw value from START_AD_CNT command (Calibration Temperature)	
RD_AD_CNT_2 [57]$_{HEX}$	3rd measured raw value from START_AD_CNT command (Temperature or Half-Bridge or 00_{HEX})		Check sum for all three measured raw values from START_AD_CNT command [1]	

1. The check sum for the two-byte digital output word is calculated with following formula:
   Check sum = FF_{HEX} – ($HighByte_{1st\_word}$ + $LowByte_{1st\_word}$)$_{8LSB}$.

5.4 Detailed Description for Particular Commands

5.4.1 Acquisition of Raw Measurement Data with START_AD_CNT [62]$_{HEX}$

The START_AD_CNT [62]$_{HEX}$ command is used for synchronized raw data acquisition during the calibration process (snapshot mode). Especially for mass calibration, it enables a raw data snapshot for all attached devices under temperature drift and pressure leakage conditions.

The command START_AD_CNT transmits two data bytes containing the following parameters:

- data[15:13] is the digital Low Pass Filter averaging coefficient LPAVRG for all measured values.

$$X_{OUT,i} = X_{OUT,i-1} + \frac{(X_i - X_{OUT,i-1})}{2^{AVRG}} \quad i > 0, \quad \text{AVRG} \in [0;7) \qquad \textbf{Equation 24}$$

- data[12:11] specifies the input channels to measure. Use appropriate selections for measuring the application-relevant input channels (see Table 13).
- data[10:0] is the A/D conversion cycle count to be processed. Recommended value is at least (2^{AVRG} + 8).

The A/D conversion is done cyclically over all selected input channels including adjustment for auto-zero for the selected channel. While measuring, the most recent result values for the bridge or half-bridge followed by the calibration temperature measurement can be read out by read request. No analog output is generated. OWI communication remains enabled during the measurement cycle. When finishing the A/D conversion cycles, the read request delivers the success code C362$_{HEX}$.

The commands RD_AD_CNT_1 [56]$_{HEX}$ and RD_AD_CNT_2 [57]$_{HEX}$ read the final result values of the A/D conversion initiated by the START_AD_CNT command. RD_AD_CNT_1 reads the first value and second value. RD_AD_CNT_2 reads the third value, if available, and a check sum calculated over all 3 values. If only two input channels were selected by START_AD_CNT, the third value is set to zero.

The check sum for the three values is calculated by [FFFF$_{HEX}$ – (Σ(Result Values))16LSB].

Alternatively, the final 2 or 3 A/D conversion result values of START_AD_CNT can be stored in EEPROM with commands STORE2_AD_CNT (63$_{HEX}$) or STORE3_AD_CNT (64$_{HEX}$), respectively. This can be done without prior reading of the values. The STORE*_AD_CNT command is transmitted with 2 data bytes that contain the EEPROM start address for storage. EEPROM programming must be enabled before sending STORE*_AD_CNT. Note that these commands need a processing time of 2 or 3 EEPROM programming cycles. For mass calibration, this enables data collection in the on-chip EEPROM and one-pass calibration as post-process.

Table 13. A/D Conversion Response Resulting from START_AD_CNT Command

Selected Input Channel	START_AD_CNT [62]$_{HEX}$ Response While Measuring		RD_AD_CNT_2 [57]$_{HEX}$ Response	
	RD_AD_CNT_1 [56]$_{HEX}$ Response			
	High 16-Bit Word	Low 16-Bit Word	High 16-Bit Word	Low 16-Bit Word
Bridge and Calibration Temperature data[12:11] = 00$_{BIN}$	Bridge	Calibration Temperature	Zero	Check Sum
Half-Bridge and Calibration Temperature data[12:11] = 01$_{BIN}$	Half-Bridge	Calibration Temperature	Zero	Check Sum
Bridge, Calibration Temperature, and Temperature data[12:11] = 10$_{BIN}$	Bridge	Calibration Temperature	Temperature	Check Sum
Bridge, Calibration Temperature, and Half-Bridge data[12:11] = 11$_{BIN}$	Bridge	Calibration Temperature	Half-Bridge	Check Sum

5.4.2 Oscillator Frequency Adjustment with ADJ_OSC_ACQ [50]$_{HEX}$ and ADJ_OSC_WRI [65 data]$_{HEX}$

ADJ_OSC_x commands are used to adjust the frequency of the internal oscillator. This frequency is adjustable in the range of 1.5MHz to 3MHz. It has a directly proportional effect on the A/D conversion time and on the timing of the Sequential Analog Output Mode (SEQAOUT) if enabled at the AOUT2 pin. The internal oscillator frequency can be adjusted by CFGAPP2:OSCADJ (refer to section 6.4 and Table 18). The frequency is adjusted by steps with one step equal to approximately -125kHz (frequency is decreased if CFGAPP2:OSCADJ is increased).

The ADJ_OSC_ACQ command is sent first. This command functions ONLY with one-wire communication (OWI). It returns a value that represents the ratio fOSC/fOWI of the internal oscillator frequency to the OWI communication frequency. After sending an ADJ_OSC_x command, the frequency ratio can be read with an I2C or OWI READ request (see Table 6).

The communication frequency fOWI is known, so the current internal oscillator frequency fOSC can be calculated. Note that the resolution of the frequency measurement is better when a lower OWI communication frequency is used. The required adjustment of CFGAPP2:OSCADJ to reach the target frequency can be calculated from the ratio fOSC/fOWI and the adjustment increment of -125kHz/step. The ADJ_OSC_WRI command is used to write CFGAPP2:OSCADJ to RAM and to activate the new adjustment. The command returns the complete configuration word CFGAPP2 (all other configuration bits retain their value).

Refer to the *ZSSC3154 Application Note—Oscillator Frequency Adjustment* for details and example code for an easy and accurate adjustment of the internal frequency during end-of-line calibration.

6. EEPROM and RAM

6.1 Programming the EEPROM

Programming the EEPROM is done using an internal charge pump to generate the required programming voltage. The timing of the programming pulses is controlled internally. The programming time for a write operation is typically 12.5ms independent of the programmed clock frequency (CFGAPP2:OSCADJ). Waiting a minimum of 15ms per write operation before starting the next communication is recommended.

To program the EEPROM, the ZSSC3154 must be set to Command Mode by the command START_CM [72 74]$_{HEX}$ and EEPROM programming must be enabled by the command EEP_WRITE_EN [6C F7 42]$_{HEX}$. Writing data to the EEPROM is done via the serial digital interface by sending specific commands (refer to section 5.1).

The WRITE_EEP command includes the address of the targeted EEPROM word and is followed by two data bytes. During EEPROM programming, the serial digital interface is disabled and no further commands can be recognized.

The COPY_RAM2EEP command writes the contents of the RAM mirror area to the EEPROM. This is to simplify the calibration process when the ZSSC3154 is configured iteratively. The EEPROM signature, which is not mirrored in RAM, is generated, written to EEPROM, and returned to the interface output register. This copy operation includes 25 EEPROM write operations and therefore typically requires 300ms (recommended wait time 375ms).

6.2 EEPROM and RAM Contents

The configuration of the ZSSC3154 is stored in 28 EEPROM 16-bit words.

Calibration coefficients for conditioning the sensor signal via conditioning calculations and output limits are stored in 19 words. There are 5 words for setting the configuration of the ZSSC3154 for the application. One register is used for storing the EEPROM signature, which is used in NOM to check the validity of the EEPROM contents after power-on. Two additional 16-bit words are available for optional user data. One additional word is reserved for Renesas use only.

After every power-on, the EEPROM contents are mirrored to RAM. After this read out, the contents of the RAM mirror are checked by calculating the signature and comparing it to the one stored in EEPROM. If a signature error is detected, the ZSSC3154 changes to Static DM . DM is indicated by setting both analog outputs AOUT1 and AOUT2 to the Diagnostic Fault Band (DFB). Subsequently the error code can be read via I2C or OWI.

The configuration of the device is done from the mirrored area in RAM, so the configuration words are subsequently transferred to the internal registers. The calibration coefficients for the conditioning calculations are also read from RAM. As a result, every change to the RAM mirror area impacts the configuration and behavior of the device after the next start of the measurement cycle.

After power-on, the contents of the RAM mirror area are determined by the EEPROM contents and can then be changed by specific commands writing to RAM. This new configuration can be activated by the START_CYC_RAM command or by the START_AD_x commands.

The EEPROM data are stored with Hamming distance of 3, which means that detection and correction of 1-bit or 2-bit errors is 100%. Detection of multi-bit-errors (>2 bit) is processed at a lower detection rate.

Table 14. EEPROM and RAM Contents

RAM and EEPROM Address	Write Command RAM/EEPROM	Description Note: The MSB is given first if an address has more than one assignment.	
Conditioning Coefficients – Conditioning Formula Bridge Sensor Signal (section 2)			
00_{HEX}	$80_{HEX}/A0_{HEX}$	c0 – Bridge offset	Bridge Signal
01_{HEX}	$81_{HEX}/A1_{HEX}$	c1 – Bridge gain	Bridge Signal
02_{HEX}	$82_{HEX}/A2_{HEX}$	c2 – Bridge non-linearity 2nd order	Bridge Signal
03_{HEX}	$83_{HEX}/A3_{HEX}$	c3 – Bridge non-linearity 3rd order	Bridge Signal
04_{HEX}	$84_{HEX}/A4_{HEX}$	c4 – Bridge temperature coefficient offset 1st order	Bridge Signal
05_{HEX}	$85_{HEX}/A5_{HEX}$	c5 – Bridge temperature coefficient offset 2nd order	Bridge Signal
06_{HEX}	$86_{HEX}/A6_{HEX}$	c6 – Bridge temperature coefficient gain 1st order	Bridge Signal
07_{HEX}	$87_{HEX}/A7_{HEX}$	c7 – Bridge temperature coefficient gain 2nd order	Bridge Signal
Temperature Measurement → CFGAPP2:AOUT2MD selects output of conditioned Temperature Signal			
Conditioning Coefficients – Conditioning Formula Temperature Signal (section 2.3)			
08_{HEX}	$88_{HEX}/A8_{HEX}$	t0 – Temperature offset	Temperature Signal
09_{HEX}	$89_{HEX}/A9_{HEX}$	t1 – Temperature gain	Temperature Signal
$0A_{HEX}$	$8A_{HEX}/AA_{HEX}$	t2 – Temperature non-linearity 2nd order	Temperature Signal
Analog Front-End Built-In Self-Test (AFEBIST) Limits			
$0B_{HEX}$	$8B_{HEX}/AB_{HEX}$	AFEBISTMIN – Lower limit analog front-end BIST Not used	[15:2] [1:0]
$0C_{HEX}$	$8C_{HEX}/AC_{HEX}$	AFEBISTMAX – Upper limit analog front-end BIST Not used	[15:2] [1:0]
Sensor Aging Check (SAC) Limits			
$0D_{HEX}$	$8D_{HEX}/AD_{HEX}$	CMVMIN – Lower limit common mode voltage (SAC) Not used	[15:2] [1:0]
$0E_{HEX}$	$8E_{HEX}/AE_{HEX}$	CMVMAX – Upper limit common mode voltage (SAC) Not used	[15:2] [1:0]
Half-Bridge Measurement → CFGAPP2:AOUT2MD selects output of conditioned half-bridge signal			
Conditioning Coefficients – Conditioning Formula Half-Bridge Sensor Signal (section 2.4)			
08_{HEX}	$88_{HEX}/A8_{HEX}$	h0 – Half-bridge offset	Half-Bridge Sensor
09_{HEX}	$89_{HEX}/A9_{HEX}$	h1 – Half-bridge gain	Half-Bridge Sensor
$0A_{HEX}$	$8A_{HEX}/AA_{HEX}$	h2 – Half-bridge non-linearity 2nd order	Half-Bridge Sensor
$0B_{HEX}$	$8B_{HEX}/AB_{HEX}$	h4 – Half-bridge temperature coefficient offset 1st order	Half-Bridge Sensor
$0C_{HEX}$	$8C_{HEX}/AC_{HEX}$	h5 – Half-bridge temperature coefficient offset 2nd order	Half-Bridge Sensor
$0D_{HEX}$	$8D_{HEX}/AD_{HEX}$	h6 – Half-bridge temperature coefficient gain 1st order	Half-Bridge Sensor
$0E_{HEX}$	$8E_{HEX}/AE_{HEX}$	h7 – Half-bridge temperature coefficient gain 2nd order	Half-Bridge Sensor

RAM and EEPROM Address	Write Command RAM/EEPROM	Description Note: The MSB is given first if an address has more than one assignment.
Analog Output Filter Coefficients and Limits		
$0F_{HEX}$	$8F_{HEX}/AF_{HEX}$	Bridge sensor signal analog output AOUTMINBR – Lower limit analog output [15:3] LPFAVRGBR – Digital LPF averaging coefficient [2:0] Note that f(AOUTMINBR) limits f(BR) at pin AOUT2 if selected.
10_{HEX}	$90_{HEX}/B0_{HEX}$	Bridge sensor signal analog output AOUTMAXBR – Upper limit analog output [15:3] LPFDIFFBR – Digital LPF differential coefficient [2:0] Note that f(AOUTMAXBR) limits f(BR) at pin AOUT2 if selected.
11_{HEX}	$91_{HEX}/B1_{HEX}$	Temperature or half-bridge signal analog output AOUTMINT, AOUTMINHB – Lower limit analog output [15:3] LPFAVRGT, LPFAVRGHB – Digital LPF averaging coefficient [2:0]
12_{HEX}	$92_{HEX}/B2_{HEX}$	Temperature or half-bridge signal analog output AOUTMAXT, AOUTMAXHB – Upper limit analog output [15:3] LPFDIFFT, LPFDIFFHB – Digital LPF differential coefficient [2:0]
Configuration Words (section 6.4)		
13_{HEX}	$93_{HEX}/B3_{HEX}$	CFGAFE – Configuration of analog front-end
14_{HEX}	$94_{HEX}/B4_{HEX}$	CFGAFE2 – Configuration of analog front-end
15_{HEX}	$95_{HEX}/B5_{HEX}$	CFGAPP – Configuration of target application
16_{HEX}	$96_{HEX}/B6_{HEX}$	CFGAPP2 – Configuration of target application
17_{HEX}	$97_{HEX}/B7_{HEX}$	CFGSF – Configuration of safety functions (Diagnostic function and bridge sensor signal filter function)
Calculated Signature Based on Register 00_{HEX} to 17_{HEX} Data		
18_{HEX}	$-/B8_{HEX}$	Signature
Free Memory Available for Optional Use by User Applications (not included in signature)		
19_{HEX}	$-/B9_{HEX}$	Free user memory, not included in signature (e.g., serial number)
$1A_{HEX}$	$-/BA_{HEX}$	Free user memory, not included in signature
Restricted		
$1B_{HEX}$	- / -	No user access - supplier restricted use

Note: The contents of the EEPROM registers at delivery are not specified and can be subject to changes. Particularly with regard to traceability, the contents can be unique per die. Note that contents at delivery might not have a valid signature. In this case, the ZSSC3154 would start in the Diagnostic Mode.

All registers must be rewritten during the calibration procedure.

Note that the LOAD_RAM_STD command can be used to load default values from ROM into RAM for registers 00_{HEX} to 17_{HEX}. See page 30 for defaults and command details.

6.3 Traceability Information

Renesas guarantees the EEPROM content only for packaged parts; on delivery, the EEPROM content of bare dice might be changed by flipped bits because of electrostatic effects might occur during the wafer sawing. Refer *ZSSC3154 Technical Note—Traceability Information* also.

6.4 Configuration Words

The data stored in EEPROM at addresses 13_{HEX} to 17_{HEX} determine the configuration of the ZSSC3154, as explained in the following tables.

Table 15. Configuration Word CFGAFE - EEPROM/RAM Address 13_{HEX}

<table>
<tr><th>Bit/Name</th><th>CFGAFE – Configuration of Analog Front-End (Part 1)</th><th>Failure detection relevant [1]</th></tr>
<tr><td>[15] / BRXZCPOL</td><td>BRidge sensor channel eXtended Zero Compensation POLarity (offset compensation by analog front-end; refer to section 2.1)
▪ 0 = negative – compensates positive offsets
▪ 1 = positive – compensates negative offsets
The bit is not relevant in failure detection.</td><td></td></tr>
<tr><td>[14:10] / BRXZC</td><td>BRidge sensor channel eXtended Zero Compensation value (offset compensation by analog front-end; refer to section 2.1)
Active only if BRXZC ≠ 0, one compensation step depends on the selected input span (refer to the “Analog Front-End Characteristics” section in the ZSSC3154 Datasheet).
The bit is not relevant in failure detection.</td><td></td></tr>
<tr><td>[9:6] / BRGAIN</td><td>BRidge sensor channel GAIN (a_{IN}—refer to section 2.1)
0000_{BIN} = 420 0100_{BIN} = 105 1000_{BIN} = 26.25 $11dd_{BIN}$ = 2.8
0001_{BIN} = 280 0101_{BIN} = 70 1001_{BIN} = 14
0010_{BIN} = 210 0110_{BIN} = 52.5 1010_{BIN} = 9.3
0011_{BIN} = 140 0111_{BIN} = 35 1011_{BIN} = 7
The bit is not relevant in failure detection.</td><td></td></tr>
<tr><td>[5:4] / BRADCRS</td><td>A/D Conversion input Range Shift regarding measured signal (rs_{ADC} – refer to section 2.1)
00_{BIN} = 1/16 → ADC range= [(–1/16 V_{ADC_REF}) to (+15/16 V_{ADC_REF})]
01_{BIN} = 1/8 → ADC range = [(–1/8 V_{ADC_REF}) to (+7/8 V_{ADC_REF})]
10_{BIN} = ¼ → ADC range = [(–1/4 V_{ADC_REF}) to (+3/4 V_{ADC_REF})]
11_{BIN} = ½ → ADC range = [(–1/2 V_{ADC_REF}) to (+1/2 V_{ADC_REF})]
The bit is not relevant in failure detection.</td><td></td></tr>
<tr><td>[3] / BRPOL</td><td>BRidge Signal POLarity (differential voltage at pins VBP, VBN)
▪ 0 = positive (VIN_DIFF = V_{VBP} – V_{VBN})
▪ 1 = negative (VIN_DIFF = V_{VBN} – V_{VBP})
The bit is not relevant in failure detection.</td><td></td></tr>
<tr><td>[2] / ADCSLOW</td><td>A/D Conversion SLOW mode
Doubles A/D conversion time (see ADCMD), Valid for all measurements.
▪ 0 = disabled
▪ 1 = enabled
The bit can be set as required by application constraints for failure detection. ffects OUR and FMT.</td><td>Yes, [x]
Affects OUR and FMT</td></tr>
<tr><td>[1:0] / ADCMD</td><td>A/D Conversion MODE
Resolution of A/D conversion integration phase. Adjust conversion and integration time.
Valid for all measurements.
<table>
<tr><th rowspan="2">ADCMD</th><th colspan="2">Resolution</th><th rowspan="2">Integration Time @ f_{osc} = 2.6MHz</th><th rowspan="2">A/D Conversion Time @ f_{osc} = 2.6MHz</th></tr>
<tr><th>A/D Conversion</th><th>Integration Phase</th></tr>
<tr><td>00_{BIN}</td><td rowspan="4">14-bit</td><td>10-bit</td><td>788µs</td><td>837µs</td></tr>
<tr><td>01_{BIN}</td><td>9-bit</td><td>394µs</td><td>443µs</td></tr>
<tr><td>10_{BIN}</td><td>8-bit</td><td>197µs</td><td>246µs</td></tr>
<tr><td>11_{BIN}</td><td>7-bit</td><td>98.5µs</td><td>197µs</td></tr>
</table></td><td>Yes, [xx]
Affects OUR and FMT</td></tr>
</table>

1. Yes, [1] means, that the bit must set to “1” Yes, [x] means, that the bit can be set as required by application constraints

Table 16. Configuration Word CFGAFE2 - EEPROM/RAM Address 14_{HEX}

Bit /Name	CFGAFE2 – Configuration of Analog Front-End (Part 2)	Failure detection relevant [1]
[15:12]	Not used The bit is not relevant in failure detection.	
[11] / HBXZCPOL	Half-Bridge channel eXtended Zero Compensation POLarity (offset compensation by analog front-end; refer to section 2.1) ▪ 0 = negative – compensates positive offsets ▪ 1 = positive – compensates negative offsets The bit can be set as required by application constraints for failure detection.	Yes, [x] Depends on application
[10:6] / HBXZC	Half-Bridge channel eXtended Zero Compensation value (offset compensation by analog front-end; refer to section 2.1) Offset compensation is only active if HBXZC ≠ 0. One compensation step depends on the selected input span (refer to the “Analog Front-End Characteristics” section in the ZSSC3154 Data Sheet).	Yes, [xxxxx] Depends on application requirements
[5:2] / HBGAIN	Half-Bridge channel GAIN (a_{IN}—refer to section 2.1) 0000_{BIN} = 420 0100_{BIN} = 105 1000_{BIN} = 26.25 $11dd_{BIN}$ = 2.8 0001_{BIN} = 280 0101_{BIN} = 70 1001_{BIN} = 14 0010_{BIN} = 210 0110_{BIN} = 52.5 1010_{BIN} = 9.3 0011_{BIN} = 140 0111_{BIN} = 35 1011_{BIN} = 7	Yes, [xxxx] Depends on application requirements
[1:0] / HBADCRS	Half-Bridge A/D Conversion input Range Shift (rs_{ADC}—refer to section 2.1) 00_{BIN} = 1/16 → ADC range = [(–1/16 V_{ADC_REF}) to (+15/16 V_{ADC_REF})] 01_{BIN} = 1/8 → ADC range = [(–1/8 V_{ADC_REF}) to (+7/8 V_{ADC_REF})] 10_{BIN} = ¼ → ADC range = [(–1/4 V_{ADC_REF}) to (+3/4 V_{ADC_REF})] 11_{BIN} = ½ → ADC range = [(–1/2 V_{ADC_REF}) to (+1/2 V_{ADC_REF})]	Yes, [xx] Depends on application requirements

1. Yes, [1] means, that the bit must set to “1” Yes, [x] means, that the bit can be set as required by application constraints

Table 17. Configuration Word CFGAPP

Bit / Name	CFGAPP – Configuration of Temp. Measurement and TIMEDIV	Failure detection relevant [1]
[15:8]	Not used The bit is not relevant in failure detection.	
[7:6] / TIMEDIV	Output TIMing DIVider: Power-On Diagnostic Output and Sequential Analog Output timing (refer to sections 3.2 and 3.3):	Yes, [xx] Affects startup time and AOUT2 update in sequential mode

@ fosc = 2.6MHz		Time base T_{PDO} Power-On Diagnostic	Time base T_{SEQ} Sequential Analog Output
TIMEDIV	Time Base		
00_{BIN}	Basic timing	160ms	37ms
01_{BIN}	Divide by 2	80ms	18ms
10_{BIN}	Divide by 4	40ms	9ms
11_{BIN}	Divide by 8	20ms	4ms

[5:3] / TS	Temperature Sensor select: $00d_{BIN}$ = on-chip diode $d10_{BIN}$ = external resistor on pin VTN1 100_{BIN} = external resistor on pin VTN2 $d11_{BIN}$ = external diode on pin VTN1 101_{BIN} = external diode on pin VTN2	
[2:0] / CTS	Calibration Temperature Sensor select: $00d_{BIN}$ = on-chip diode $d10_{BIN}$ = external resistor on pin VTN1 100_{BIN} = external resistor on pin VTN2 $d11_{BIN}$ = external diode on pin VTN1 101_{BIN} = external diode on pin VTN2	

1. Yes, [1] means, that the bit must set to “1” Yes, [x] means, that the bit can be set as required by application constraints

Table 18. Configuration Word CFGAPP2 - EEPROM/RAM Address 16_{HEX}

<table>
<tr><th>Bit / Name</th><th>CFGAPP2 – Configuration of Target Application</th><th>Failure detection relevant [1]</th></tr>
<tr><td>[15] / OWIMD</td><td>One-Wire Interface MoDe
▪ 0 = Analog output starts after OWI startup window
▪ 1 = Analog output starts simultaneously with OWI startup window
The bit is not relevant in failure detection.</td><td></td></tr>
<tr><td>[14] / AOUT2SEQ</td><td>Enable Sequential Analog OUTput MoDe at AOUT2 pin (SEQAOUT; refer to section 3.3.)
▪ 0 = Single Analog Output
▪ 1 = Sequential Analog Output
The bit is not relevant in failure detection.</td><td></td></tr>
<tr><td>[13:11] / AOUT2 MD</td><td>Select Analog Output Signal at the AOUT2 pin:
<table>
<tr><th rowspan="2">CFGAPP2[13:11]</th><th rowspan="2">CFGAPP2[14] = 0
Single Signal Analog Output</th><th colspan="2">CFGAPP2[14] = 1
Sequential Analog Output (see Figure 6)</th></tr>
<tr><th>1st Analog Output</th><th>2nd Analog Output</th></tr>
<tr><td>000_{BIN}</td><td>Temperature</td><td>Bridge</td><td>Temperature</td></tr>
<tr><td>001_{BIN}</td><td>(1 – Bridge)</td><td>(1 – Bridge)</td><td>Temperature</td></tr>
<tr><td>010_{BIN}</td><td>(½ ×Bridge)</td><td>(½ ×Bridge)</td><td>Temperature</td></tr>
<tr><td>011_{BIN}</td><td>(½ (1 – Bridge))</td><td>(½ (1 – Bridge))</td><td>Temperature</td></tr>
<tr><td>100_{BIN}</td><td>Half-Bridge</td><td>Bridge</td><td>Half-Bridge</td></tr>
<tr><td>101_{BIN}</td><td>Half-Bridge</td><td>(1 – Bridge)</td><td>Half-Bridge</td></tr>
<tr><td>110_{BIN}</td><td>Half-Bridge</td><td>(½ ×Bridge)</td><td>Half-Bridge</td></tr>
<tr><td>111_{BIN}</td><td>Half-Bridge</td><td>(½ (1 – Bridge))</td><td>Half-Bridge</td></tr>
</table>
Note: Bit 13 (AOUT2MD[2]) is also used for selecting the second signal sent by the digital output (I2C interface) during NOM and Temporary DM (see section 4.2). The second value sent in the digital output sequence can be either the 13-bit temperature or 13-bit half-bridge value: 0 = temperature; 1 = half bridge.
Update timing in sequential mode is defined by CFGAPP:TIMDEV.</td><td>Yes, [xxx]
Depends on application requirements</td></tr>
<tr><td>[10:5] / HBREF</td><td>REFerence Voltage for Half-Bridge Measurement
Single-ended Half-Bridge signal is measured against reference voltage VHB,REF.
Reference voltage is linearly adjusted in 63 steps from 0.3·VBR to 0.7·VBR.
$HBREF \in [0;31] \Rightarrow V_{HB,REF} = V_{BR} \cdot \frac{81+HBREF}{161}$ $HBREF \in [32;63] \Rightarrow V_{HB,REF} = V_{BR} \cdot \frac{81+31-HBREF}{161}$</td><td>Yes, [xxxxxx]
Depends on application</td></tr>
<tr><td>[4] / OSCSS</td><td>Enable OSCillator Spread Spectrum Mode
▪ 0 = disabled
▪ 1 = enabled
Reduces electromagnetic emission (EME).
Frequency of internal oscillator is linearly varied in 63 steps by nominal ±11%.
The bit is not relevant in failure detection.</td><td></td></tr>
<tr><td>[3:0] / OSCADJ</td><td>ADJust frequency fOSC of internal OSCillator
Refer to the ZSSC3154 Application Note—Oscillator Frequency Adjustment for details.</td><td>Yes, [xxxx]
Affects OUR, FMT and startup time</td></tr>
</table>

1. Yes, [1] means, that the bit must set to “1” Yes, [x] means, that the bit can be set as required by application constraints

Table 19. Configuration Word CFGSF - EEPROM/RAM Address 17_{HEX}

Bit	CFGSF – Configuration of Safety Functions	Failure detection relevant [1]
[15] / EEPLOCK	Enables the EEPROM Lock for OWI communication ▪ 0 = disabled ▪ 1 = enabled The bit is not relevant in failure detection.	
[14:11] / SLVADDR	Slave address for OWI and I2C communication Defines 4 LSB of a possible additional I2C slave address within the range 20_{HEX} to $2F_{HEX}$. Use 8_{HEX} to disable this second address by setting it to the general address 28_{HEX}. The bit is not relevant in failure detection.	
[10] / PDOENA	Enable the Power-On Diagnostic Output (PDO) ▪ 0 = disabled ▪ 1 = enabled Note: Sequential Analog Output at AOUT2 is dominant and disables PDO (Refer to section 3.2.) The bit is recommended to be set as required by application constraints for failure detection.	
[9] / CHKROM	Enable the ROM Check at power-on. Startup time is increased approximately 10ms. ▪ 0 = disabled ▪ 1 = enabled **Important**: the bit is relevant to failure detection and must be set to “1”.	
[8] / CHKTSC	Enable the Temperature Sensor Check Applies to temperature and calibration temperature: ▪ 0 = disabled ▪ 1 = enabled **Important**: the bit is relevant to failure detection and must be set to “1”.	
[7] / CHKMCCH	Enable the Main Channel A/D Conversion Result Check High Limit ▪ 0 = disabled ▪ 1 = enabled	Yes, [x] Recommended, depends on application
[6] / CHKMCCL	Enable the Main Channel A/D Conversion Result Check Low Limit ▪ 0 = disabled ▪ 1 = enabled	
[5] / CHKBCC	Enable the Broken Chip Check: ▪ 0 = disabled ▪ 1 = enabled **Important**: the bit is relevant to failure detection and must be set to “1”.	
[4] / CHKSSC	Enable the Sensor Short Check: ▪ 0 = disabled ▪ 1 = enabled Note that the Sensor Short Check is always disabled if the Half-Bridge measurement is enabled by the CFGAPP2:AOUT2MD setting. The bit is recommended to be set as required by application constraints for failure detection.	

Bit	CFGSF – Configuration of Safety Functions	Failure detection relevant [1]
[3] / CHKSCCHIC	Switch to the Sensor Connection Check High Capacitor Mode ▪ 0 = SCC Normal Mode ▪ 1 = SCC High Capacitor Mode The SCC High Cap Mode enables SCC diagnostics for input load capacities in range 1nF to 10nF. Note that for either mode, the Sensor Connection Check must be enabled by the CFGSF:CHKSCC setting. Note that the Sensor Connection Check is always disabled if the Half-Bridge measurement is enabled by the CFGAPP2:AOUT2MD setting. The bit can be set as required by application constraints for failure detection.	
[2] / CHKSCC	Enable the Sensor Connection Check: ▪ 0 = disabled ▪ 1 = enabled Note that the Sensor Connection Check is always disabled if the Half-Bridge measurement is enabled by the CFGAPP2:AOUT2MD setting. The bit can be set as required by application constraints for failure detection.	
[1] / CHKSAC	Enable the Sensor Aging Check: ▪ 0 = disabled ▪ 1 = enabled Note that the Sensor Aging Check is always disabled if the Half-Bridge measurement is enabled by the CFGAPP2:AOUT2MD setting. The bit can be be set as required by application constraints for failure detection.	
[0] / DMRES	Enables triggering a reset if the Diagnostic Mode (DM) occurs ▪ 0 = stop and DM ▪ 1 = reset and startup again If set to 1, reset is executed after timeout of watchdog. The bit can be be set as required by application constraints for failure detection.	

1. Yes, [1] means, that the bit must set to “1” Yes, [x] means, that the bit can be set as required by application constraints

6.5 EEPROM Signature

The EEPROM signature (address 18_{HEX}) is used to check the validity of the EEPROM contents. The signature is built using a polynomial arithmetic modulo 2. The following source code generates the signature if the field eepcont[ ] is allocated by the EEPROM content (addresses 00_{HEX} to 17_{HEX}). The parameter N is the count of applicable addresses and must be set as N = 24.

Figure 17. C Source Code Signature Generation

```
#define POLYNOM A005HEX
unsigned short signature(eepcont, N)
   unsigned short eepcont[], N;
   {
      unsigned short sign, poly, p, x, i, j;
      sign = 0; poly = POLYNOM;
      for (i=0; i<N; i++) {
          sign^=eepcont[i];
          p=0; x=sign&poly;
          for (j=0; j<16; j++, p^=x, x>>=1);
          sign<<=1; sign+=(p&1);
      }
      return(~sign);
   }
```

6.6 EEPROM Write Locking

The ZSSC3154 supports EEPROM write locking (EEPLOCK). If the EEPROM lock is active (i.e., CFGSF:EEPLOCK=1), it is not possible to enable EEPROM programming with the command EEP_WRITE_EN using one-wire communication (OWI); the ZSSC3154 answers the command EEP_WRITE_EN with the reject code $CF6C_{HEX}$, and a subsequent EEPROM write access is blocked.

An activated EEPLOCK does not block writing to the EEPROM using I2C and can always be reset using I2C.

EEPLOCK is active only if programmed into EEPROM and activated due to

- New power-on or
- Receiving the EEP_WRITE_EN command or
- Starting the measurement cycle by receiving the START_CYC_x command

The following write sequence is possible:

- Write calibration data including EEPLOCK to RAM mirror
- Enable EEPROM writing by sending the command EEP_WRITE_EN
- Copy the RAM mirror to EEPROM
- Write the EEPROM signature directly to EEPROM

If an invalid EEPROM signature is detected, the EEPROM lock is always deactivated.

7. Glossary

Term	Description
ADC	Analog-to-Digital Converter
AFE	Analog Front-End
AFEBIST	Analog Front-End Built-In Self-Test
BCC	Broken Chip Check
BIST	Built-In Self-Test
CM	Command Mode
CMC	Calibration Microcontroller
CMV	Common Mode Voltage
DFB	Diagnostic Fault Band
DFBH	Diagnostic Fault Band level High
DFBL	Diagnostic Fault Band level Low
DM	Diagnostic Mode
FB	Full Bridge
FDM	Failure Detection Mechanism
FMT	Fault Messaging Time
HB	Half Bridge
LSB	Least Significant Bit
MCCH	Main Channel Check High
MCCL	Main Channel Check Low
MSB	Most Significant Bit
NOM	Normal Operation Mode
OWI	One-Wire Interface
OUR	Output Update Rate
PDO	Power-On Diagnostic Output
SAC	Sensor Aging Check
SEQAOUT	Sequential Analog Output
SCC	Sensor Connection Check
SSC	Sensor Signal Conditioner
TSC	Temperature Sensor Check

8. Revision History

Revision	Date	Description
1.17	November 13, 2024	▪ AFEBIST and SAC description extended, AFEBIST LIMIT added ▪ 2xFB Mode AOUT output update information added
1.16	April 25, 2024	▪ Safe state definition added in chapter 1.3.3 and “Failure detection requested” added in chapter 1.3.4 ▪ Failure detetction relevance added to configuration words description in chapter 6.4 ▪ Refer to "Renesas ZSSC3154" for the latest version of related documents. ▪ Changed to Renesas branding
1.15	November 29, 2017	▪ Revisions for EEPROM signature section 6.5 regarding the setting for parameter N. ▪ Update for template. ▪ Removal of “Related Documents” section. ▪ Minor edits.
1.14	March 29, 2016	Changed to IDT branding. Revision is now the release date.
1.13	November 25, 2015	▪ CRC changed to check sum. ▪ Revision to Table 8 for OWI bit time equation. ▪ Revision to table note for Table 10 regarding Dx commands and timing. ▪ Additional information added for watchdog time in Table 1. ▪ Contact information updated. ▪ Related documents updated.
1.12	March 18, 2014	▪ Update for contact information and imagery for cover and header. ▪ Replacement of Table 5.4 with a referral to the ZSSC3154 Application Note—Oscillator Frequency Adjustment. ▪ Minor edits for clarity.
1.11	April 2, 2013	Updates for traceability information in new section 6.3 and “Related Documents” section.
1.10	June 7, 2012	Updates for revision B silicon, including addition of ADJ_OSC_WRI command.
1.00	June 4, 2012	Initial release.

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