EVK-UFT285-6-7 Evaluation Board User Guide

USER GUIDE

Introduction

The EVK-UFT285-6-7 is designed to help the customer evaluate the 8T49N285, 8T49N286, and 8T49N287 devices, members of IDT's 3rd generation Universal Frequency Translator family. When the board is connected to a PC running IDT Timing Commander™ software through USB, the device can be configured and programmed to generate frequencies with best-in-class performances.

Contents

The EVK-UFT285-6-7 evaluation board ships with the following:

- 1 – EVK-UFT285-6-7 Evaluation Board
- 1 – USB Cable

Requirements

1. PC Requirements:

- IDT Timing Commander software installed.
- USB 2.0 interface. The evaluation board USB module is not compatible with USB 3.0. If using a computer with high speed USB ports, please check if there's a standard USB 2.0 port available for use. The hardware drivers are automatically installed during the Timing Commander installation.
- Windows XP SP3 or later.
- Processor: Minimum 1GHz.
- Memory: Minimum 512MB, recommended 1GB.
- Available Disk Space: Min 600MB (1.5GB 64bit), recommended 1GB (2GB 64bit)
- Network access during installation if the .NET framework is not currently installed on the system.

2. Power Supply with 3.3V and 1000mA rating

3. Three banana plug cables to connect the power supply to the board.

Quick Start: Powering Up the Board

(1) Set 3.3V supply current limit to 500mA.

(2) Remove all output terminations.

(3) Set Dip Switch selectors to the middle position.

(4) Connect a cable from a PC to the USB port.

(5) Connect VEE to the black GND jack.

(6) Connect 3.3V to VCC_J and VDDO_J.

(7) Power on the Power Supply.

(8) Press the Reset Button.

Once correct operation is verified, set the power supply limit for the number of outputs to be active.

The USB port must be powered by the PC in order to have the correct I^2C bus voltage levels.

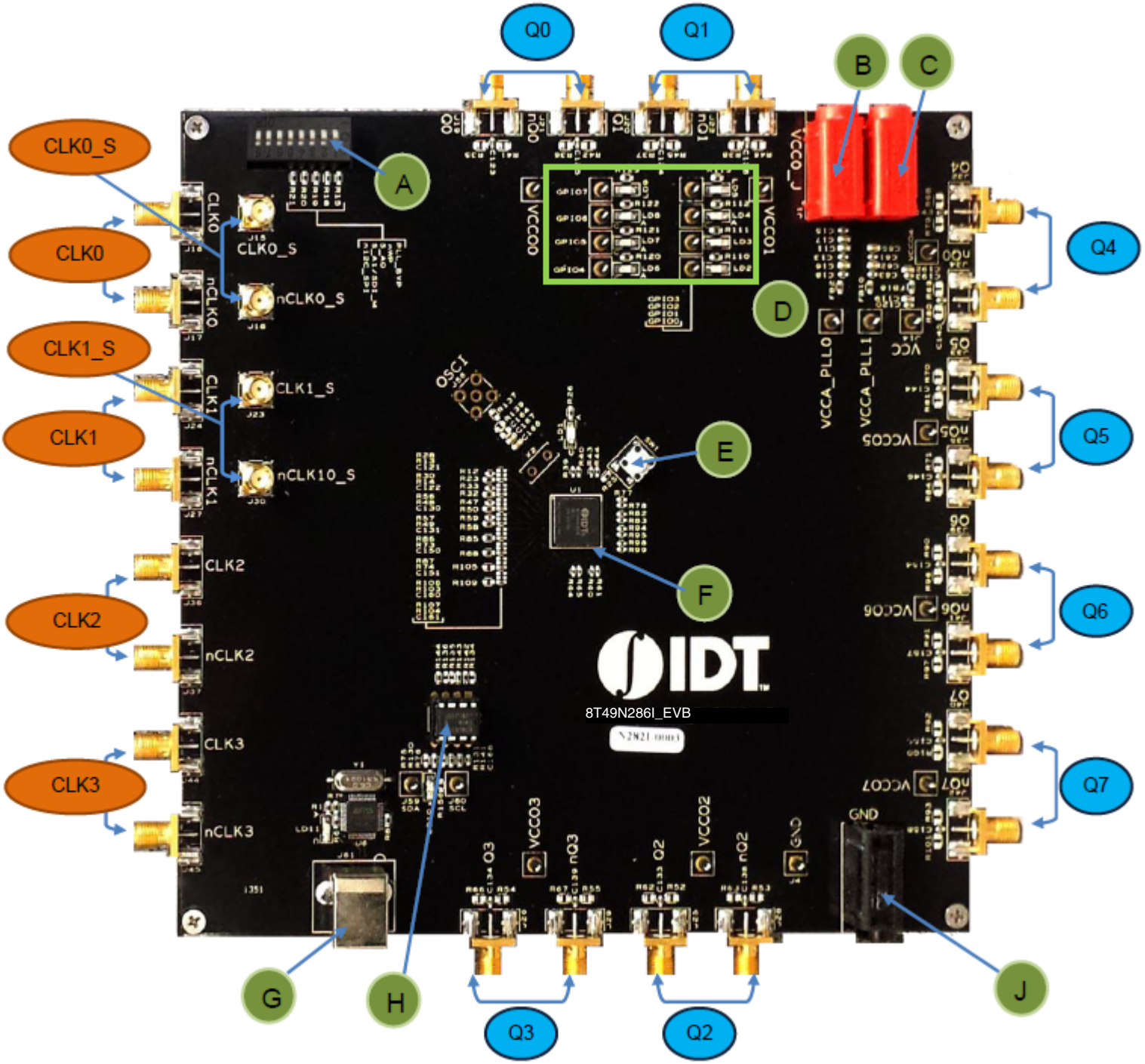
The board ships with a 38.88MHz crystal and will have a default frequency of 155.52MHz on Q0. If all outputs are unterminated, current should measure ~256mA with 3.3V on VCC_J and VDDO_J. If all outputs are terminated, current should measure ~262mA.

When evaluating performance with the default hardware configuration, it is recommended that all active outputs be terminated 50ohms to VEE by either terminator plugs or an instrument.

Board Overview

Use the following diagram to identify: power supply jacks, USB connector, input and output SMA connectors, reset button, EEPROM, etc.

Figure 1. Evaluation Board Top View



Legend–Evaluation Board Top View

Inputs

CLK0_S	Clock 0 sense lines.
CLK0	Clock 0 input lines. Can be configured for differential or single-ended input.
CLK1_S	Clock 1 sense lines.
CLK1	Clock 1 input lines. Can be configured for differential or single-ended input.
CLK2	Clock 2 input lines. Can be configured for differential or single-ended input.
CLK3	Clock 3 input lines. Can be configured for differential or single-ended input.

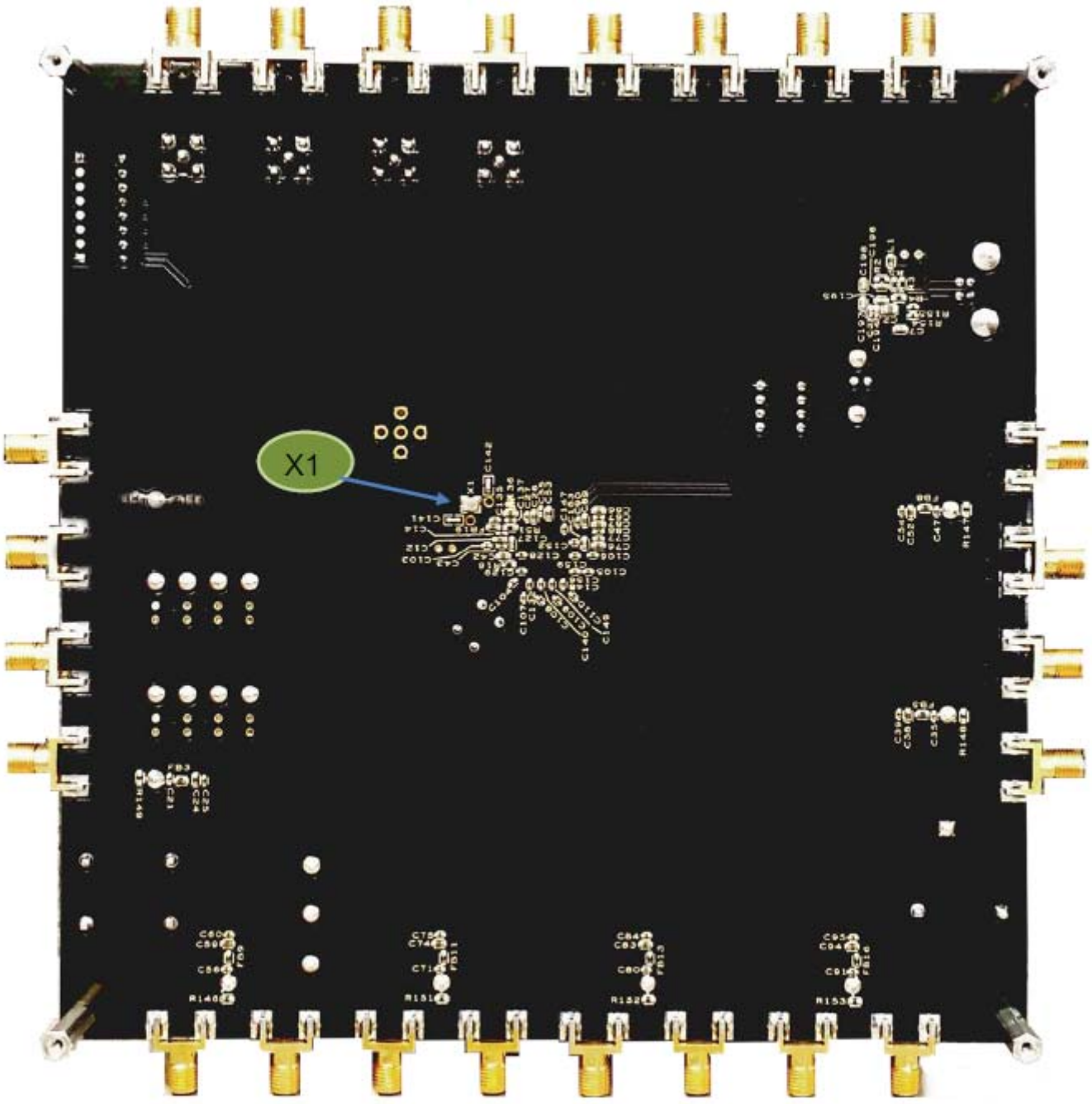
Outputs

Q0	Output Q0. Can be a differential pair or two individual single-ended outputs.
Q1	Output Q1. Can be a differential pair or two individual single-ended outputs
Q2	Output Q2. Can be a differential pair or two individual single-ended outputs.
Q3	Output Q3. Can be a differential pair or two individual single-ended outputs.
Q4	Output Q4. Can be a differential pair or two individual single-ended outputs.
Q5	Output Q5. Can be a differential pair or two individual single-ended outputs.
Q6	Output Q6. Can be a differential pair or two individual single-ended outputs.
Q7	Output Q7. Can be a differential pair or two individual single-ended outputs.

Other

A	Dip Switch for DC control signals (CLK_SEL, PLL_BYPASS, etc)
B	VCCO_J
C	VCC_J
D	GPIOs
E	RESET
F	IDT8T49N286 – the device to be evaluated
G	USB connector
H	EEPROM – AT24CO4C
J	Ground Jack

Figure 2. Evaluation Board Bottom View



Legend–Evaluation Board Bottom View

X1 3.2 x 2.5 mm SMD Fox-603-38.88-4 Crystal

Schematics

The following figures are schematics that are applicable to specific sections of this User Guide. The complete schematics are available in a separate document.

Figure 3. Inputs Schematic

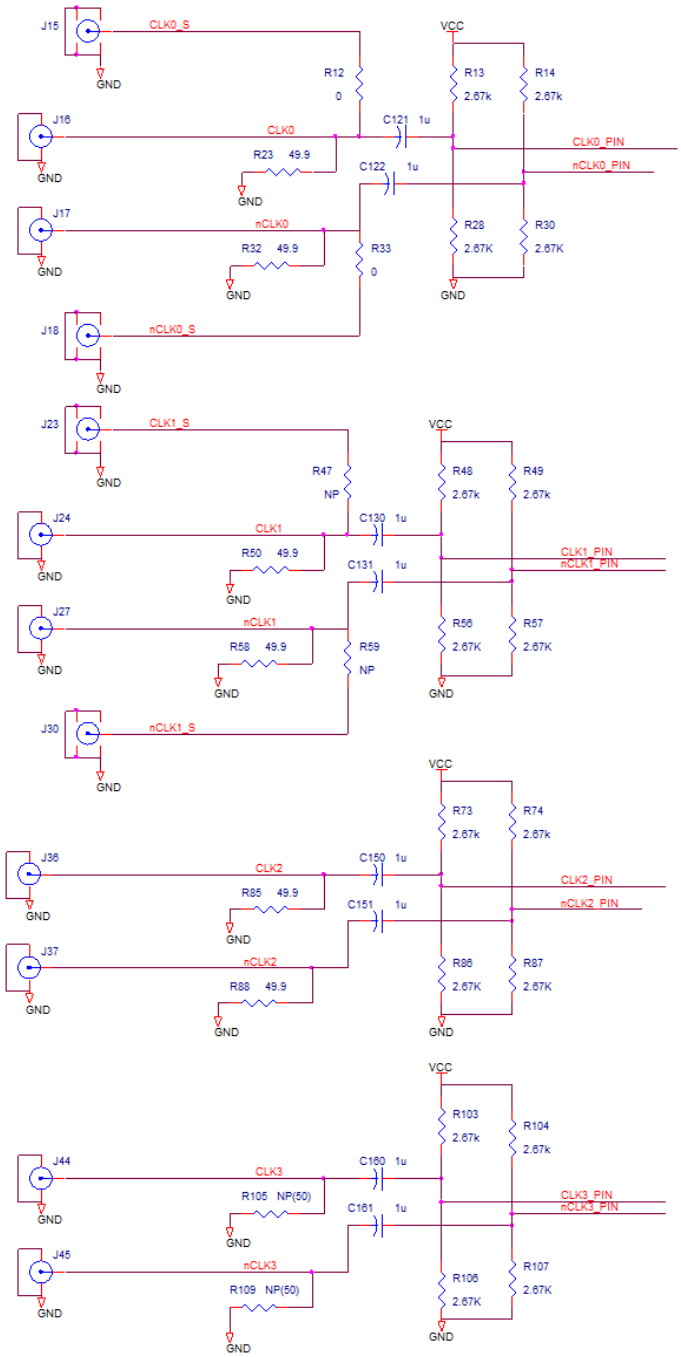


Figure 4. Output Termination Schematic

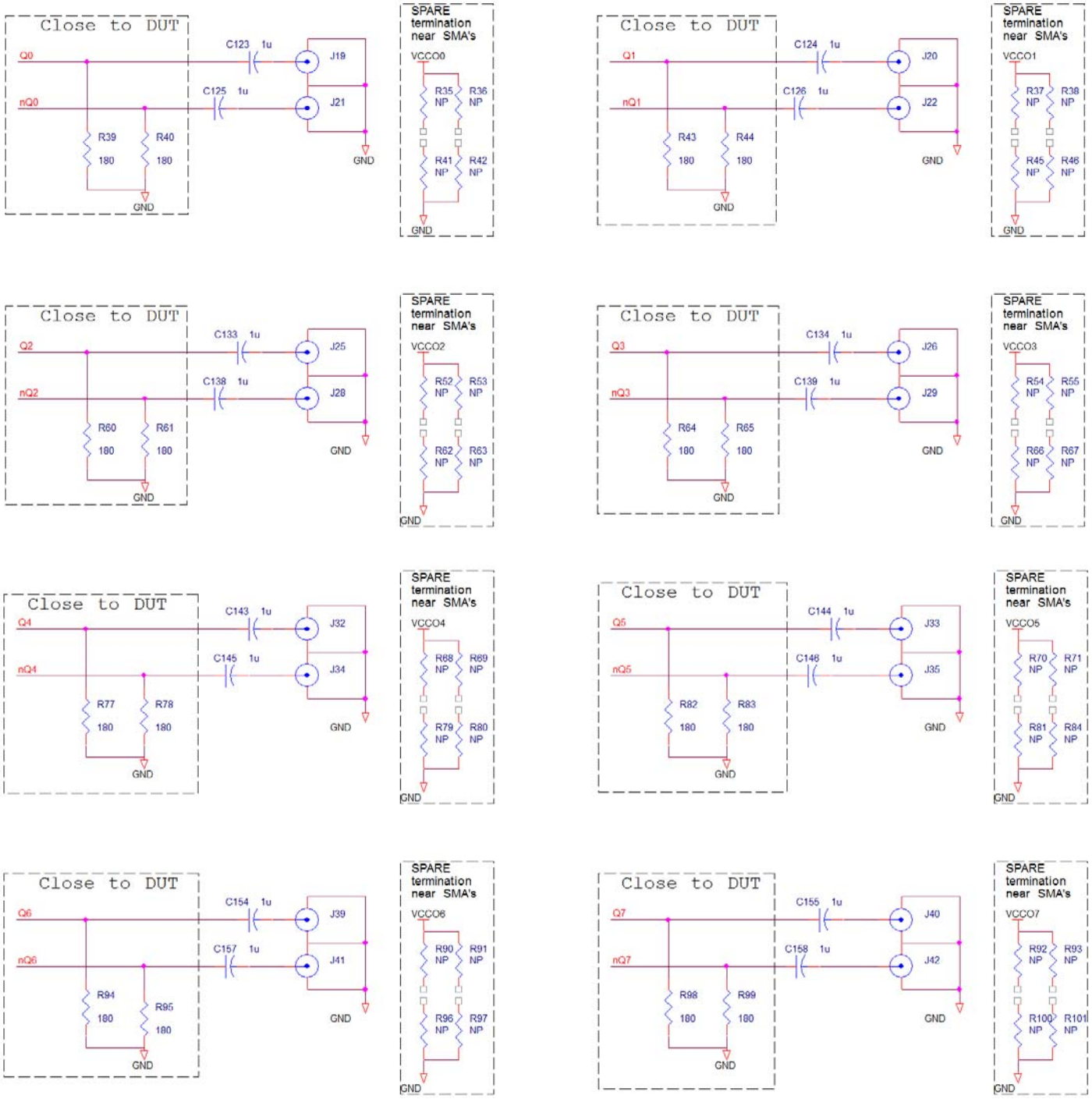


Figure 5. Crystal Interface Schematic

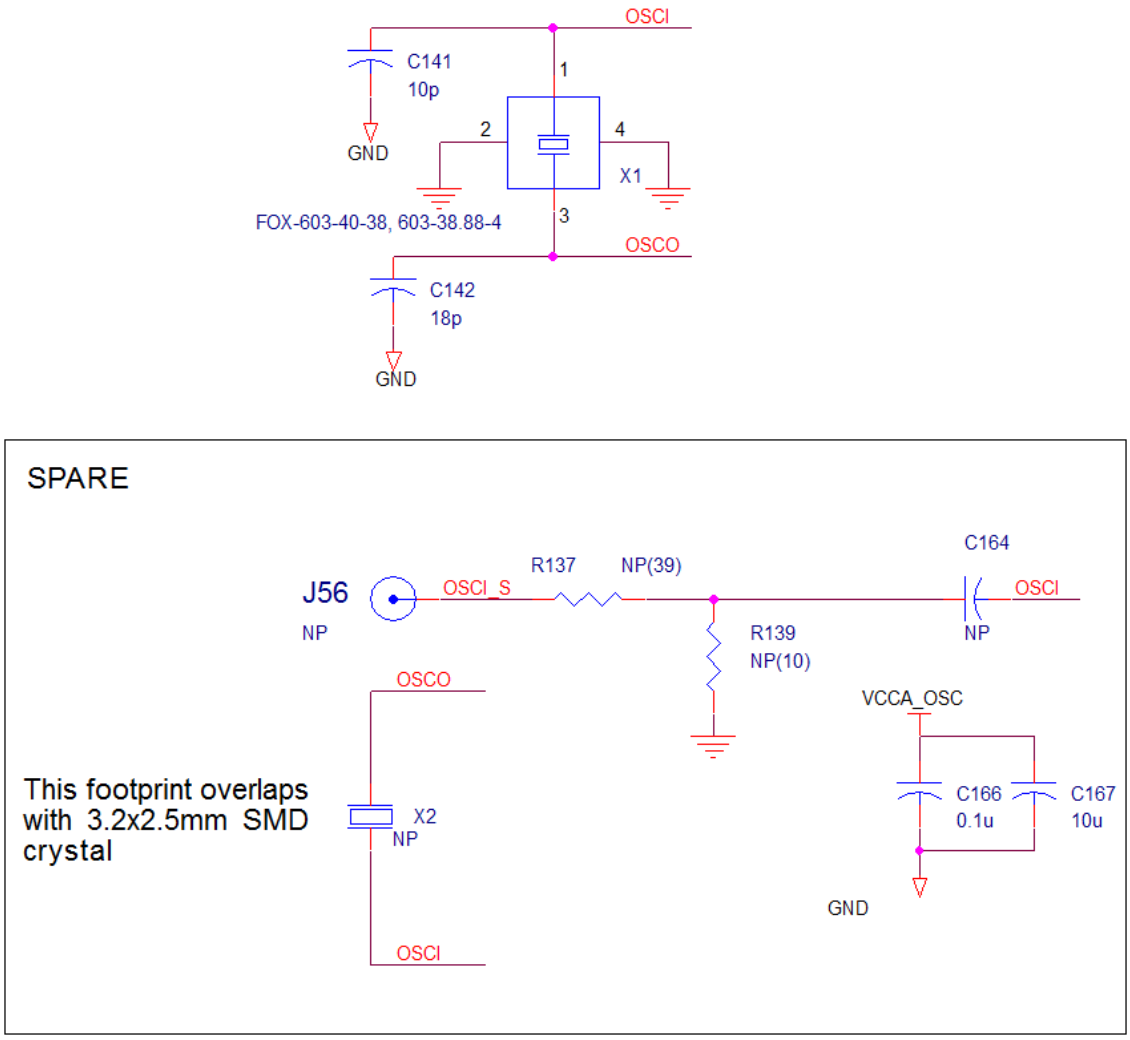


Figure 6. EEPROM/I²C Schematic

(If the device is programmed to boot from EEPROM, use R156=0ohm, R131=1Kohm, and do not populate LD10)

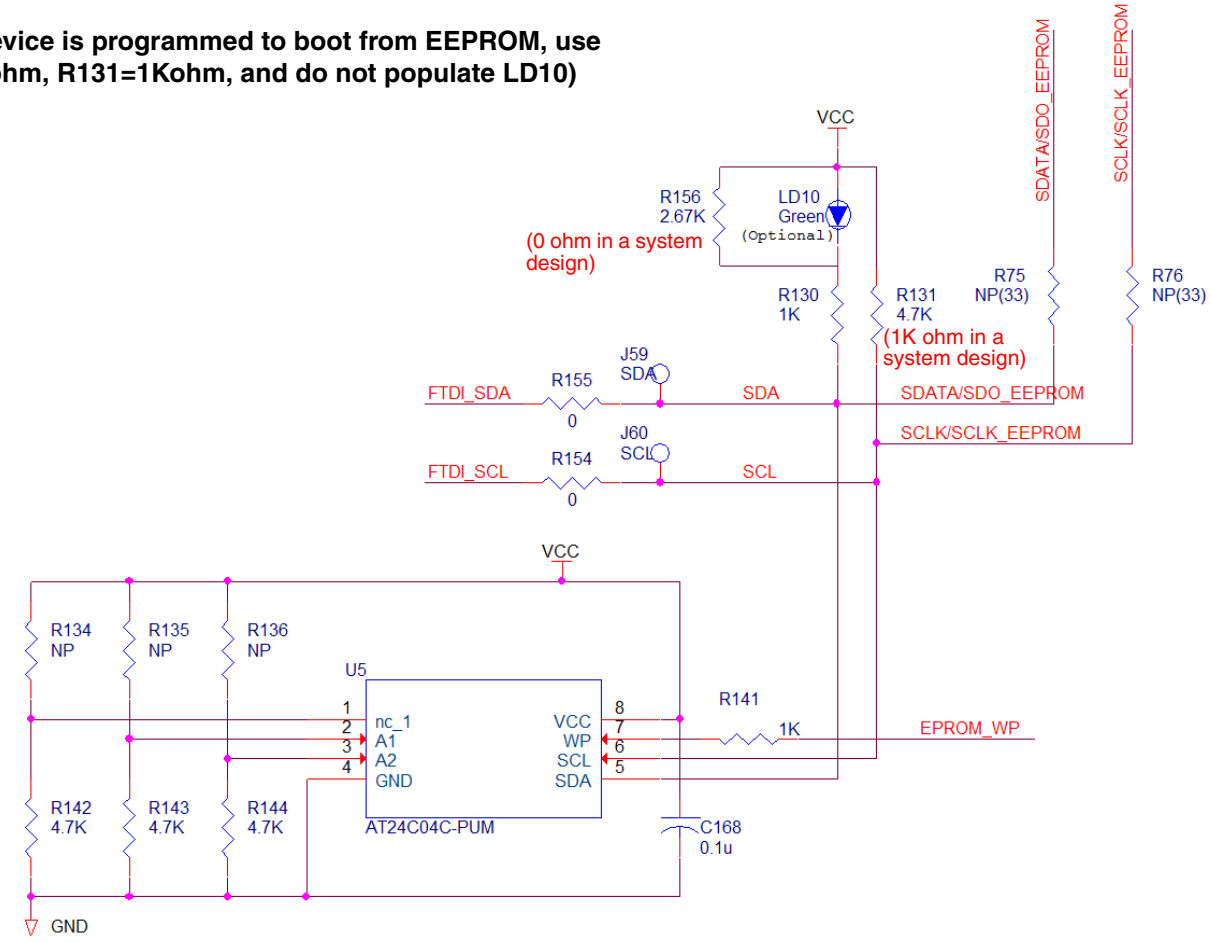


Figure 7. DC Control Schematic

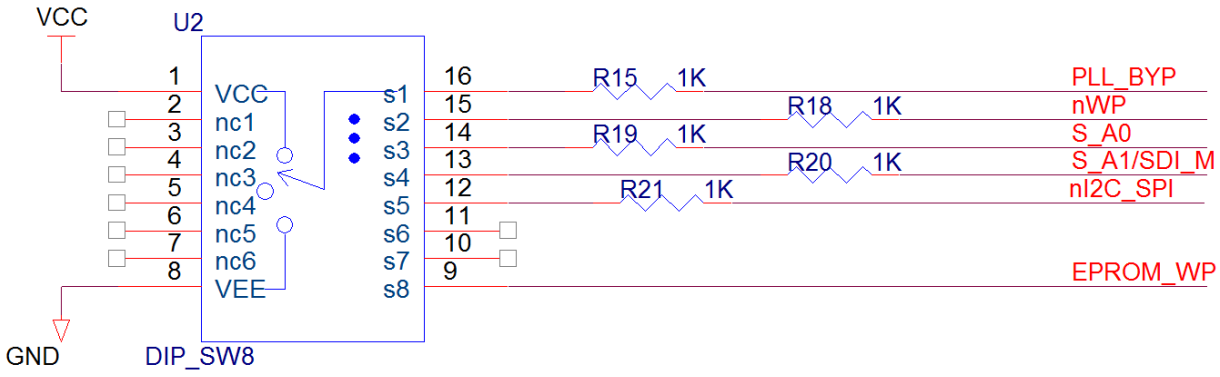


Figure 8. VCCO Power Filtering

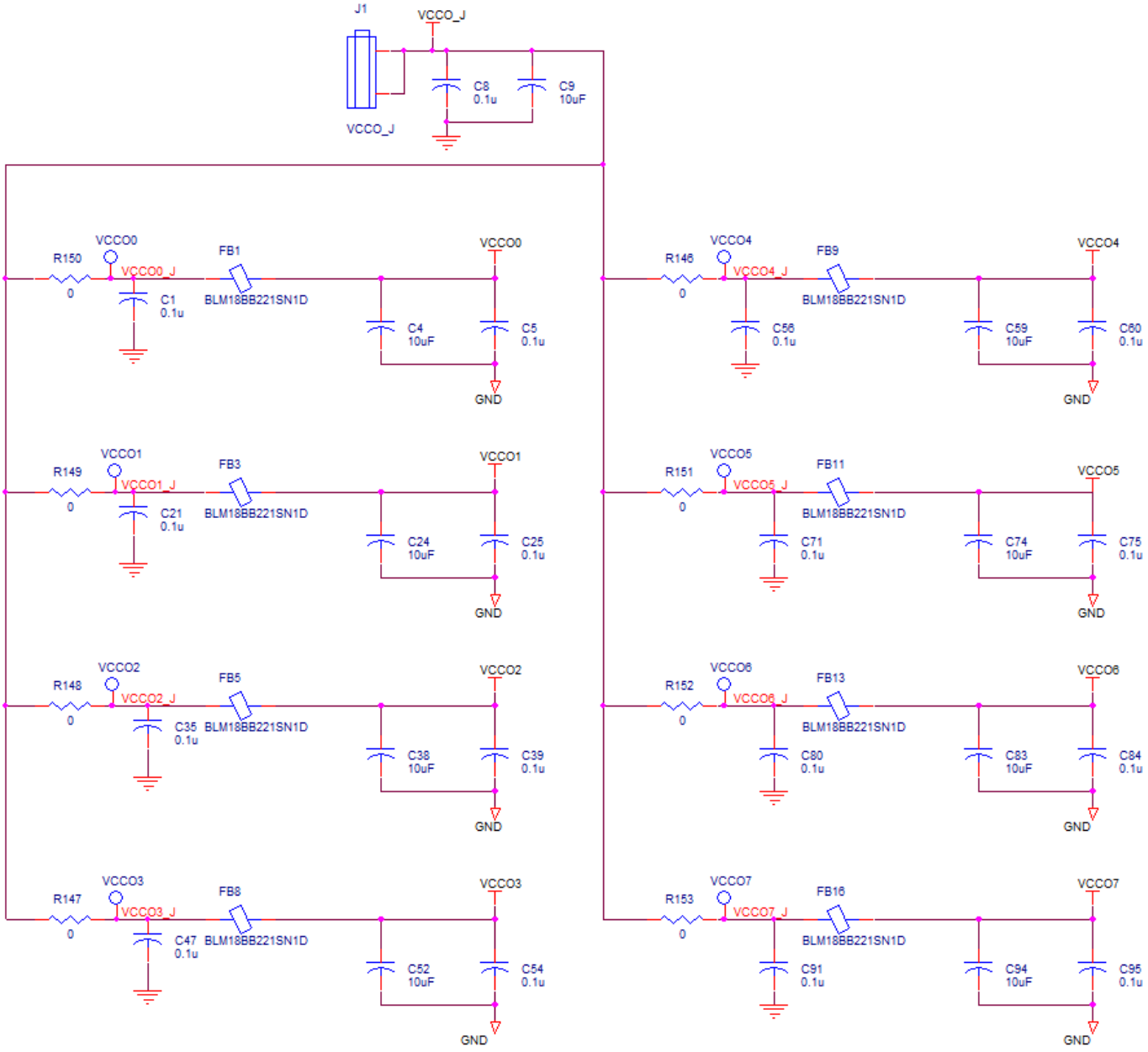
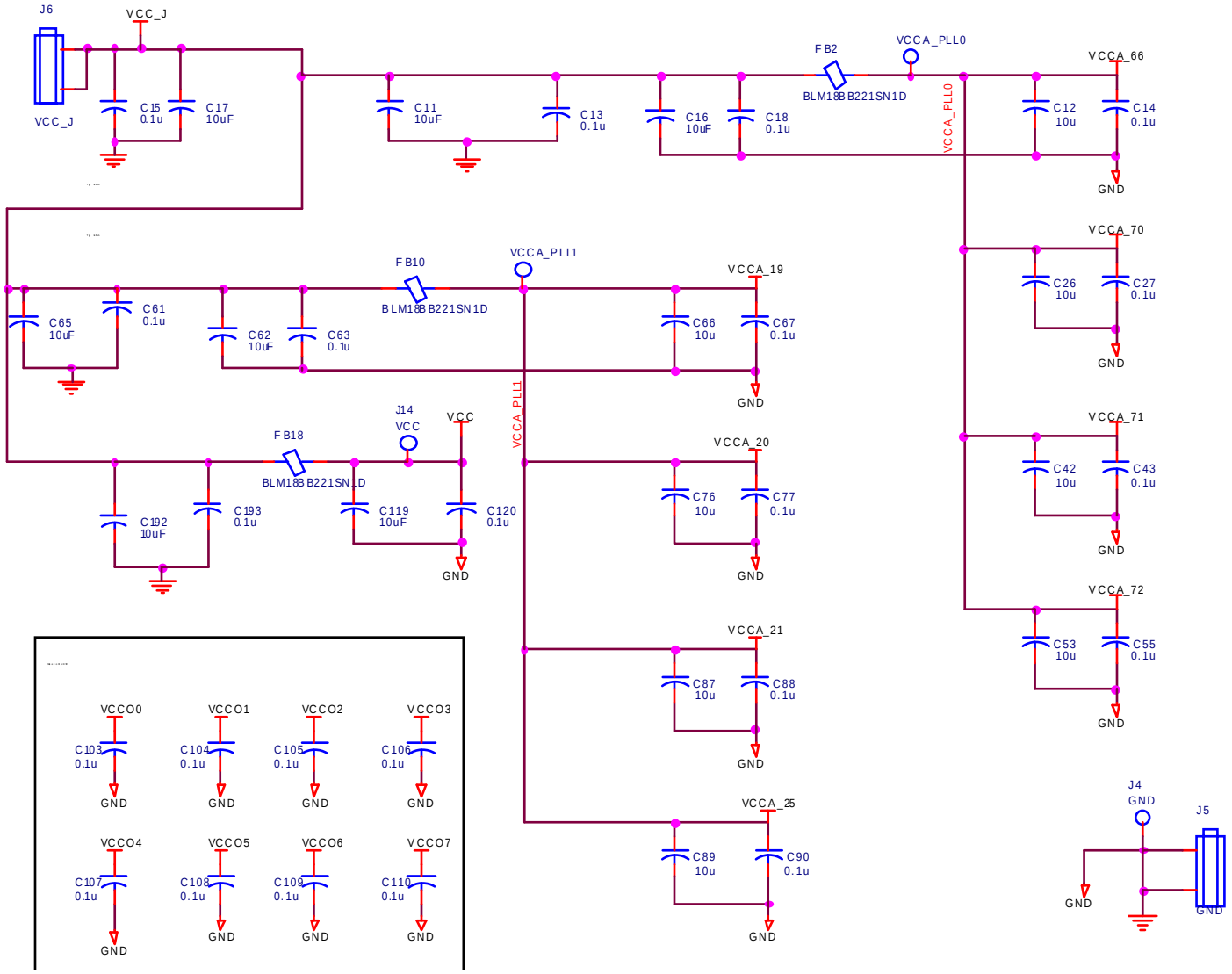


Figure 9. VCC Filtering



Board Power Supply

Core Voltages

The core voltage includes a digital voltage VDD and an analog voltage VDDA. Both core voltages are powered by the external bench power supply connected to J6 (VCC_J). See Figure 9 for details

Output Voltages

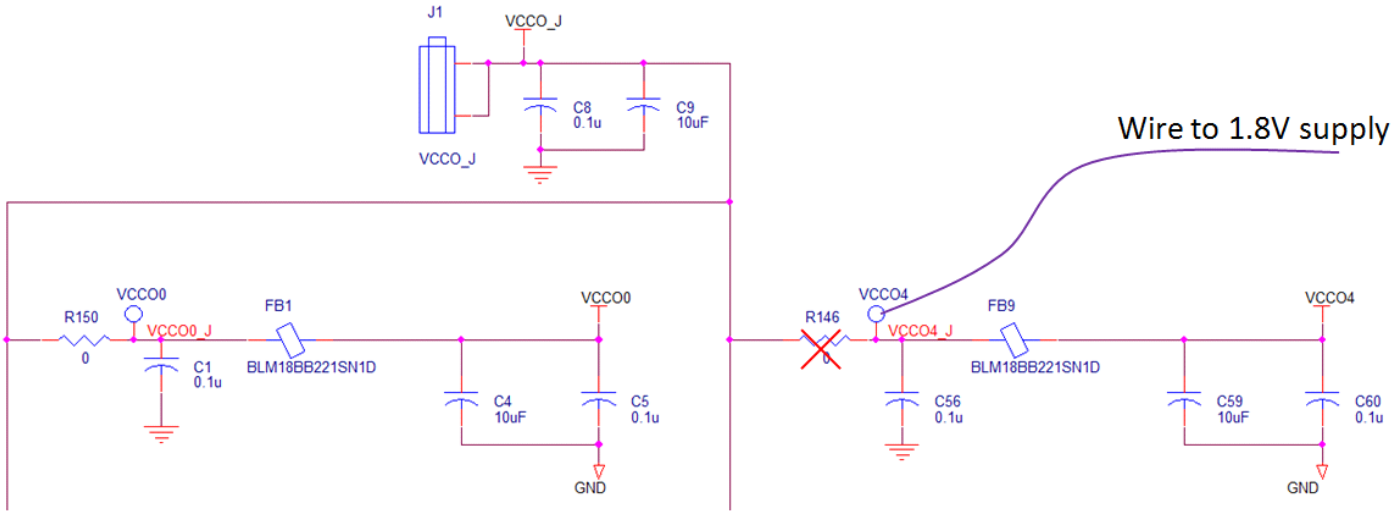
VDDO_J (J1) supplies the global voltage for the outputs and can be biased by the external power supply at 1.8V (all outputs LVCMOS), 2.5V, or 3.3V.

Mixed Voltage Operation

This board provides the option to operate the outputs with a mixed combination of output voltages. Refer to Figure 8 for a complete view of the VCCO schematic. Each VCCOx has a 0Ω resistor that connects it to the global VCCO_J power rail. This resistor can be removed and the voltage can be provided using the test point. For example, the schematic below can be configured so that Q0 (VCCO0) operates at 2.5V and Q4 LVCMOS (VCCO4) operates at 1.8V as follows:

1) Connect 2.5V to J1 (VCCO_J).
2) Remove R146. This isolates VCCO4 from global VCCO_J.
3) Solder a wire onto test point VCCO4 and bias with a 1.8V supply.

Figure 10. Mixed Output Voltage Operation



Input Configuration

The inputs are configured with an ac-coupling termination scheme. This scheme allows flexibility for either differential or single-ended inputs. The default configuration is as follows:

Table 1: Default Input Configuration

Input	Default Termination	Sense Lines
CLK0	50ohms to ground, ac-coupled into the device	Use SMAs J15/J18 for observation of the input signal
CLK1	50ohms to ground, ac-coupled into the device	Available but not connected. Populate R47 and R59 to observe input signal on SMAs J23/J30
CLK2	50ohms to ground, ac-coupled into the device	Not available
CLK3	50ohms to ground, ac-coupled into the device	Not available

Differential Input

Connect the input signal to CLKx and nCLKx. For CLK0, the CLK0_S and nCLK0_s sense lines are available for observation of the signal. They can be connected with 50ohm impedance cables to an oscilloscope with 50ohm termination, otherwise, they should be terminated with 50ohm plugs in order prevent reflections.

Single-ended Input

Connect the input signal to CLKx and float nCLKx. For CLK0, connect CLK0_S with a 50ohm impedance cable to an oscilloscope with 50ohm termination or terminate with a 50ohm plug.

Input Signals below 1MHz

For slow-frequency signals below 1MHz, we recommend that the coupling capacitors for the corresponding input be replaced with zero-ohm resistors and that the signal input dc-offset be set so that it meets the device's Vcmr requirements. Refer to Figure 3 to locate the components listed below.

Table 2: Input Termination Schemes

Signal Frequency	AC-coupling capacitors: CLK0 (C121, C122) CLK1 (C130,C131) CLK2 (C150,C151) CLK3 (C160,C161)	Input Signal DC Offset
>1MHz	1µF	Don't care
<1MHz	Ω	Must meet datasheet Vcmr specs

Output Configuration

The outputs are ac-coupled, allowing for maximum flexibility for observation of the output whether configured for LVPECL, LVDS, or LVCMOS levels. The default termination scheme can be used to measure either of the three output level-types but is not optimal. The optimal termination circuits are tabulated below. Refer to Figure 4 to locate the components listed below.

Table 3: Termination Outputs for Q0

Signal Type	180 ohm pull-down: R39, R40	Series capacitors: C123, C125	Resistor Network: R35, R36, R41, R42
LVPECL (Default)	Installed	1µF	Not installed
LVCMOS	Not installed	33 ohm	Not installed
LVDS	Not installed	1µF	Not installed

Table 4: Termination Outputs for Q1

Signal Type	180 ohm pull-down: R43, R44	Series capacitors: C124, C126	Resistor Network: R37, R38, R45, R46
LVPECL (Default)	Installed	1µF	Not installed
LVCMOS	Not installed	33 ohm	Not installed
LVDS	Not installed	1µF	Not installed

Table 5: Termination Outputs for Q2

Signal Type	180 ohm pull-down: R60, R61	Series capacitors: C133, C138	Resistor Network: R52, R53, R62, R63
LVPECL (Default)	Installed	1µF	Not installed
LVCMOS	Not installed	33 ohm	Not installed
LVDS	Not installed	1µF	Not installed

Table 6: Termination Outputs for Q3

Signal Type	180 ohm pull-down: R64, R65	Series capacitors: C134, C139	Resistor Network: R54, R55, R66, R67
LVPECL (Default)	Installed	1µF	Not installed
LVCMOS	Not installed	33 ohm	Not installed
LVDS	Not installed	1µF	Not installed

Table 7: Termination Outputs for Q4

Signal Type	180 ohm pull-down: R77, R78	Series capacitors: C143, C145	Resistor Network: R68, R69, R79, R80
LVPECL (Default)	Installed	1µF	Not installed
LVCMOS	Not installed	33 ohm	Not installed
LVDS	Not installed	1µF	Not installed

Table 8: Termination Outputs for Q5

Signal Type	180 ohm pull-down: R82, R83	Series capacitors: C144, C146	Resistor Network: R70, R71, R81, R84
LVPECL (Default)	Installed	1µF	Not installed
LVCMOS	Not installed	33 ohm	Not installed
LVDS	Not installed	1µF	Not installed

Table 9: Termination Outputs for Q6

Signal Type	180 ohm pull-down: R94, R95	Series capacitors: C154, C157	Resistor Network: R90, R91, R96, R97
LVPECL (Default)	Installed	1µF	Not installed
LVCMOS	Not installed	33 ohm	Not installed
LVDS	Not installed	1µF	Not installed

Table 10: Termination Outputs for Q7

Signal Type	180 ohm pull-down: R98, R99	Series capacitors: C155, C158	Resistor Network: R92, R93, R100, R101
LVPECL (Default)	Installed	1µF	Not installed
LVCMOS	Not installed	33 ohm	Not installed
LVDS	Not installed	1µF	Not installed

As noted, the 4-resistor network is not installed in Tables 3~10 because an oscilloscope with internal 50Ω termination is utilized for signal termination and measurement. If a DC-coupled, stand-alone LVPECL output is needed (without oscilloscope connections), the 4-resistor network needs to be installed accordingly. The table below provides the configuration for Q0:

Table 11: Resistor Termination Outputs for LVPECL for Q0

Signal Type	180 ohm pull-down: R39, R40	Series capacitors: C123, C125	Resistor Network: R35, R36, R41 R42
LVPECL (Default)	Not installed	0 ohm	R35=R36=125ohm R41=R42=84ohm

Output signals below 1MHz

For slow-frequency output signals below 1MHz, we recommend that the 1µF ac-coupling capacitors be replaced with 0ohm resistors and that the correct terminations be provided at the receiver.

EEPROM Boot

The evaluation board ships with an IDT8T49N286-997device, which will attempt to boot from the EEPROM at power-up. By default, the EEPROM boot is not enabled on the board. If use of the EEPROM boot is required, there are three options to enable this mode.

1) **No Rework Option.** This option will enable the EEPROM boot and does not require any soldering. This sequence must be performed each time the EEPROM needs to be reloaded into the device.
   a. Hold down the reset button.
   b. Unplug and then plug in the USB cable.
   c. Release the reset button.
2) **Rework Option.** This option will enable the EEPROM boot but requires soldering. It does not require continually unplugging/plugging-in the USB cable for reloading of the EEPROM into the device.
   a. Remove LD10 or replace R156 with a 1Kohm resistor. (See Figure 6).
   b. Power up the board with USB cable connected.
   c. Press and release the reset button.
3) **Stand-Alone Use.** Sometimes it's necessary to evaluate the device inside a temperature chamber, a system rack, or a Faraday cage where a USB connection to the device is impractical. For such cases contact IDT for further support.

For details on how to program the EEPROM, please refer to document *How to Program the 8T49N28x EEPROM*.

DC Controls

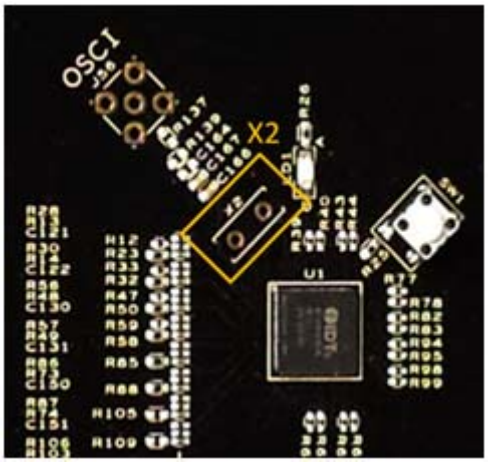
The Dip Switch has three settings: 0V, Float, and VCC. This board ships with all switches in the Float (middle) position. Refer to Figure 1, label "A" for the location of the Dip Switch.

Crystal Interface

By default, a 3.2x2.5mm SMD 38.88MHz crystal is installed on bottom side of the board. It provides the reference frequency for the device. This board supports other options for the XTAL_IN reference. If using one of the other options, the crystal on X1 must be removed.

1) **Through-hole crystal.** With this option, the device can be evaluated with different crystals without the need to solder each time the crystal is replaced:
   a. Remove the crystal from X1 on bottom-side of the board. (See Figure 2, "X1" for location of the component.)
   b. Solder in crystal sockets into the holes labeled X2. (See Figure 11 below for location of the component.)
   c. Place a crystal into the socket.

Figure 11. Crystal Interface PCB



2) **Crystal Overdrive.** With this option, the device can be evaluated with different sources, such as frequency generators, XO's, or other devices. Refer to Figure 5 and Figure 10 for identification of the components mentioned below.
   a. Remove the crystal from X1. (See Figure 2, "X1" for location of the component.)
   b. Populate SMA J56.
   c. Solder a 1µF capacitor onto C164. Note: the input **must** be ac-coupled
   d. R139 may be populated with a 50ohm resistor for input sources requiring such termination.
   e. R137 must be populated. It may be a 0ohm resistor for input sources or 33ohms for CMOS inputs.

IMPORTANT NOTICE AND DISCLAIMER

RENESAS ELECTRONICS CORPORATION AND ITS SUBSIDIARIES (“RENESAS”) PROVIDES TECHNICAL SPECIFICATIONS AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS OR IMPLIED, INCLUDING, WITHOUT LIMITATION, ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, OR NON-INFRINGEMENT OF THIRD-PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for developers who are designing with Renesas products. You are solely responsible for (1) selecting the appropriate products for your application, (2) designing, validating, and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. Renesas grants you permission to use these resources only to develop an application that uses Renesas products. Other reproduction or use of these resources is strictly prohibited. No license is granted to any other Renesas intellectual property or to any third-party intellectual property. Renesas disclaims responsibility for, and you will fully indemnify Renesas and its representatives against, any claims, damages, costs, losses, or liabilities arising from your use of these resources. Renesas' products are provided only subject to Renesas' Terms and Conditions of Sale or other applicable terms agreed to in writing. No use of any Renesas resources expands or otherwise alters any applicable warranties or warranty disclaimers for these products.

(Disclaimer Rev.1.01)

Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan
www.renesas.com

Contact Information

For further information on a product, technology, the most up-to-date version of a document, or your nearest sales office, please visit www.renesas.com/contact-us/.

Trademarks

Renesas and the Renesas logo are trademarks of Renesas Electronics Corporation. All trademarks and registered trademarks are the property of their respective owners.