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RENESAS

Design Manual

RENESAS

CMOS-N5 Series

CMOS Gate Array

Ver. 9.0

[MEMO]

NOTES FOR CMOS DEVICES

① **VOLTAGE APPLICATION WAVEFORM AT INPUT PIN**

Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (MAX) and V_{IH} (MIN) due to noise, etc., the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (MAX) and V_{IH} (MIN).

② **HANDLING OF UNUSED INPUT PINS**

Unconnected CMOS device inputs can be cause of malfunction. If an input pin is unconnected, it is possible that an internal input level may be generated due to noise, etc., causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND via a resistor if there is a possibility that it will be an output pin. All handling related to unused pins must be judged separately for each device and according to related specifications governing the device.

③ **PRECAUTION AGAINST ESD**

A strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it when it has occurred. Environmental control must be adequate. When it is dry, a humidifier should be used. It is recommended to avoid using insulators that easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors should be grounded. The operator should be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with mounted semiconductor devices.

④ **STATUS BEFORE INITIALIZATION**

Power-on does not necessarily define the initial status of a MOS device. Immediately after the power source is turned ON, devices with reset functions have not yet been initialized. Hence, power-on does not guarantee output pin levels, I/O settings or contents of registers. A device is not initialized until the reset signal is received. A reset operation must be executed immediately after power-on for devices with reset functions.

⑤ **POWER ON/OFF SEQUENCE**

In the case of a device that uses different power supplies for the internal operation and external interface, as a rule, switch on the external power supply after switching on the internal power supply. When switching the power supply off, as a rule, switch off the external power supply and then the internal power supply. Use of the reverse power on/off sequences may result in the application of an overvoltage to the internal elements of the device, causing malfunction and degradation of internal elements due to the passage of an abnormal current.

The correct power on/off sequence must be judged separately for each device and according to related specifications governing the device.

⑥ **INPUT OF SIGNAL DURING POWER OFF STATE**

Do not input signals or an I/O pull-up power supply while the device is not powered. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Input of signals during the power off state must be judged separately for each device and according to related specifications governing the device.

These commodities, technology or software, must be exported in accordance with the export administration regulations of the exporting country. Diversion contrary to the law of that country is prohibited.

M8E 02. 11-1

Major Revisions in This Edition

Page	Description
p.47	Modification of description in **2.4.1 (3) No connection (NC) pins**

**The revised points can be easily searched by copying an "<R>"
in the PDF file and specifying it in the "Find what:" field.**

To obtain the latest documents when designing, contact an NEC Electronics sales office or a distributer.

INTRODUCTION

This manual explains the restrictions and points to be noted when designing LSIs using NEC Electronics' CMOS-N5 Series of high-speed, high-density CMOS gate arrays.

In order to ensure smooth design of an LSI, read this manual carefully.

Be sure to follow the specifications described in this manual (including general information, cautions, and restrictions). Failure to do so may result in poor quality, poor performance, or operational faults in LSI products.

The following abbreviations are used for the package names in this manual.

Abbreviation	Standard Package Name
QFP	Plastic QFP
PBGA	Plastic BGA
TBGA	Tape BGA
FPBGA®	Fine pitch plastic BGA

Regarding the Order of Masters

Each of the information is described in gate size order, not in master order.

Target Readers　　　This manual is intended for user engineers who wish to design an LSI using the CMOS-N5 Series.

Purpose　　　This manual explains general information, limitations, and points to be noted when designing an LSI using the CMOS-N5 Series.

How to Read This Manual　　　It is assumed that the reader of this manual has general knowledge in the fields of electrical engineering, logic circuits, and microcomputers.

• To understand the overall functions of the CMOS-N5 Series:
  $\rightarrow$ Read this manual in the order of the contents.

See **CMOS Gate Array, Embedded Array Package Design Manual (A16400E)** for the following items.

- List of packages
- Maximum allowable power consumption
- Thermal resistance
- Assignment of V_{DD}, GND, NC, SCAN test pins
- Pins that can be used for oscillators
- Package drawings
- Package markings
- Mounting rank (Recommended soldering conditions)

Conventions　　　**Note**:　　Footnote for item marked with **Note** in the text
　　　　　　　　　　Caution:　　Information requiring particular attention
　　　　　　　　　　Remark:　　Supplementary information

Related Documents

The related documents indicated in this publication may include preliminary versions. However, preliminary versions are not marked as such.

- CMOS-N5 Series Design Manual   (This manual)
- CMOS-N5 Series (5.0 V) Block Library   (A13872E)
- CMOS-N5 Series (3.3 V) Block Library   (A15895E)
- CMOS-N5 Series Memory Block Library   (A14683E)
- CMOS-N5 Series Mega Macro Design Manual   (A14759E)
- CMOS Gate Array, Embedded Array Package Design Manual   (A16400E)
- NEC SYSTEM LSI DESIGN OPENCAD^{TM} OPC_VSHELL User's Manual   (A16306E)
- NEC SYSTEM LSI DESIGN Design For Test TESTACT, NEC_SCAN2 User's Manual   (A16437E)
- NEC SYSTEM LSI DESIGN Design For Test NEC_BIST, NEC_TESTBUS,
  NEC_SCAN/SCAN2, NEC_BSCAN/BSCAN2 User's Manual   (A15168E)
- SEMICONDUCTOR SELECTION GUIDE -Products and Packages-   (X13769X)

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LIST OF FIGURES (3/3)

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LIST OF TABLES (2/2)

CHAPTER 1 OVERVIEW

1.1 Features

The following table lists the CMOS-N5 Series features.

Very large-scale integration (VLSI) .... 3 K to 120 K gates

Process .... 0.5 μm rule Si gates, 2-layer metal routing

Input interface .... CMOS TTL compatible

Internal blocks .... More than 190 types of function blocks
Two types are available: high-speed and low-power
Scan path block
Driver for clock tree synthesis

Memory blocks .... Single-port RAM
Dual-port RAM

Variety of peripheral blocks .... CMOS TTL level input buffer
Input buffer with fail-safe function
CMOS level output buffer
High drive capability buffer (I_{OL} = 24.0 mA)
Low-noise output buffer
Buffer with internal pull-up resistor (5 kΩ/50 kΩ)
Buffer with internal pull-down resistor (50 kΩ)

Other .... High latch-up immunity

The features for each power supply voltage are as follows.

(1) V$_{DD}$ = 5.0 V $\pm$10%

High-speed operation .... t$_{PD}$ = 0.14 ns (2-input NAND (low power gate), fan-outs: 1, wiring length: 0 mm)

t$_{PD}$ = 0.21 ns (2-input NAND (low power gate), fan-outs: 1, standard wiring length)

t$_{PD}$ = 0.46 ns (2-input NAND (low power gate), fan-outs: 2, wiring length: 2 mm)

t$_{PD}$ = 0.16 ns (2-input NAND, fan-outs: 1, standard wiring length)

t$_{PD}$ = 0.30 ns (2-input NAND, fan-outs: 2, wiring length: 2 mm)

t$_{PD}$ = 0.18 ns (2-input NAND, fan-outs: 2, standard wiring length)

t$_{PD}$ = 0.33 ns (input buffer, fan-outs: 2, wiring length: 2 mm)

t$_{PD}$ = 0.23 ns (input buffer, fan-outs: 1, standard wiring length)

t$_{PD}$ = 1.30 ns (output buffer, C$_L$ = 15 pF, I$_{OL}$ = 9 mA)

Power consumption .... 1.35 μW/MHz/cell (internal gate, operating factor: 0.3)

Maximum clock frequency…..f$_{MAX}$ = 200 MHz (internal toggle F/F, fan-outs: 2, wiring length: 0 mm)

(2) V$_{DD}$ = 3.0 $\pm$0.3 V

High-speed operation .... t$_{PD}$ = 0.20 ns (2-input NAND (low power gate), fan-outs: 1, wiring length: 0 mm)

t$_{PD}$ = 0.30 ns (2-input NAND (low power gate), fan-outs: 1, standard wiring length)

t$_{PD}$ = 0.23 ns (2-input NAND, fan-outs: 1, standard wiring length)

t$_{PD}$ = 0.42 ns (2-input NAND, fan-outs: 2, wiring length: 2 mm)

t$_{PD}$ = 0.26 ns (2-input NAND, fan-outs: 2, standard wiring length)

t$_{PD}$ = 0.47 ns (input buffer, fan-outs: 2, wiring length: 2 mm)

t$_{PD}$ = 0.34 ns (input buffer, fan-outs: 1, standard wiring length)

t$_{PD}$ = 2.16 ns (output buffer, C$_L$ = 15 pF, I$_{OL}$ = 9 mA)

Power consumption .... 0.49 μW/MHz/cell (internal gate, operating factor: 0.3)

Maximum clock frequency….. f$_{MAX}$ = 120 MHz (internal toggle F/F, fan-outs: 2, wiring length: 0 mm)

(3) V$_{DD}$ = 3.3 $\pm$0.3 V

High-speed operation .... t$_{PD}$ = 0.18 ns (2-input NAND (low power gate), fan-outs: 1, wiring length: 0 mm)

t$_{PD}$ = 0.28 ns (2-input NAND (low power gate), fan-outs: 1, standard wiring length)

t$_{PD}$ = 0.22 ns (2-input NAND, fan-outs: 1, standard wiring length)

t$_{PD}$ = 0.39 ns (2-input NAND, fan-outs: 2, wiring length: 2 mm)

t$_{PD}$ = 0.24 ns (2-input NAND, fan-outs: 2, standard wiring length)

t$_{PD}$ = 0.44 ns (input buffer, fan-outs: 2, wiring length: 2 mm)

t$_{PD}$ = 0.31 ns (input buffer, fan-outs: 1, standard wiring length)

t$_{PD}$ = 2.02 ns (output buffer, C$_L$ = 15 pF, I$_{OL}$ = 9 mA)

Power consumption…............ 0.59 μW/MHz/cell (internal gate, operating factor: 0.3)

Maximum clock frequency….. f$_{MAX}$ = 130 MHz (internal toggle F/F, fan-outs: 2, wiring length: 0 mm)

1.2 CMOS-N5 Series Products

Table 1-1. Products

Master	Number of Row Gates	Number of Usable Gates
μPD65891	1920	1536
μPD65880	3456	2937
μPD65881	5880	4998
μPD65892	6692	5593
μPD65882	13952	11859
μPD65894	15232	12185
μPD65883	25344	21542
μPD65884	33864	28784
μPD65885	40768	30576
μPD65887	56496	41730
μPD65889	76000	57000
μPD65890	99528	74646
μPD65893	123384	92538

Remark Total number of gates integrated on the chip in terms of 2-input NAND
(1 cell = 1 gate)
Usable cell rate: μPD65880, 65881, 65882, 65883, 65884 ... 85%
μPD65891, 65892, 65894 ... 80%
μPD65885, 65887, 65889, 65890, 65893 ... 75%

1.3 Internal Structure of CMOS-N5 Series

Figure 1-1 shows the CMOS gate array internal structure, which is comprised of an internal cell region and an I/O cell region.

Figure 1-1. Gate Array Configuration
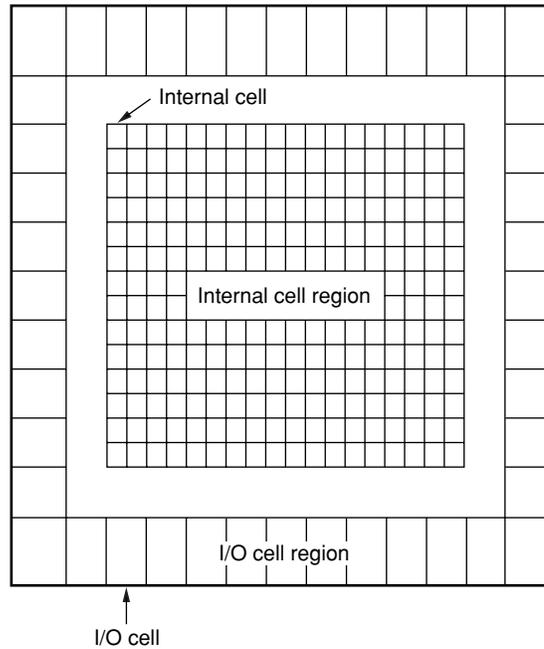
As shown in this figure, the CMOS-N5 Series does not have fixed routing regions in the internal cell region, and the entire surface of the internal cell region is filled with basic cells.

The internal cell region consists of various function blocks (such as NAND gates and D-F/F) and memory that are connected via routing layers to implement the desired circuit functions.

Input and output buffers are placed in the I/O cell region to adjust the input-level conversion and output drive capability. Some internal cells are also part of the I/O buffer implementation.

1.4 Internal Cell Structure

The circuit diagram in Figure 1-2 represents a CMOS-N5 Series internal cell.

Each cell of the CMOS-N5 Series can be configured as a device such as a two-input NAND/NOR gate, an inverter, or a buffer.

A CMOS circuit consists of a P-channel MOS transistor (P-ch. Tr) and an N-channel MOS transistor (N-ch. Tr). Normally, either the P-ch. Tr or the N-ch. Tr is in the OFF state.

Figure 1-2. Internal Cell Equivalent Circuit
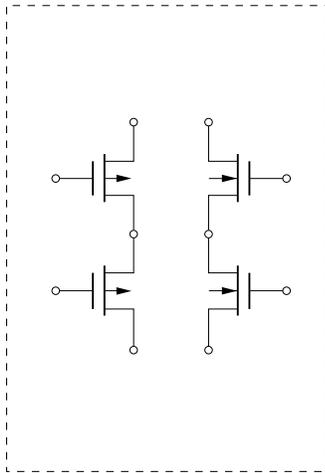
Because virtually no power flows in the steady state, the power consumption for a CMOS circuit is extremely low.

A CMOS circuit consumes current mostly during switching. Because a high transient current flows during switching, either a high-speed capacitor with a high capacitance must be inserted between the power supply and ground, or the impedance of the power supply lowered.

In addition, if a waveform with a slow rise/fall time is applied to a CMOS circuit, both the P-ch. Tr and N-ch. Tr will remain in the ON state for a period of time, causing a through current to flow between the P-ch. Tr and N-ch. Tr, resulting not only in increased current consumption but also possible malfunction.

Figure 1-3 (a) and (b) show the equivalent circuits of a 2-input NOR gate and a 2-input NAND gate. Because the ON resistance of the N-ch. Tr is about fifty percent less than that of the P-ch. Tr, a large current can be sent through the N-ch. Tr. Therefore, as shown in Figure 1-3 (a), the ON resistance of the output rise side at the NOR gate, which is serially connected to the P-ch. Tr, becomes larger, and the drive capability of the load drops.

In CMOS gate arrays, the NOR fan-out drive is slower than the NAND fan-out drive. Because of this, the NAND blocks should be used as much as possible to increase the speed and stability of the circuit.

For the same reason, complex gates that serially connect many transistors tend to be slow, and therefore should not be used in high-speed circuits. Use complex gates to improve cell utilization when speed is not as important.

Figure 1-3. Equivalent Circuits

(a) 2-Input NOR Equivalent Circuit **(b) 2-Input NAND Equivalent Circuit**
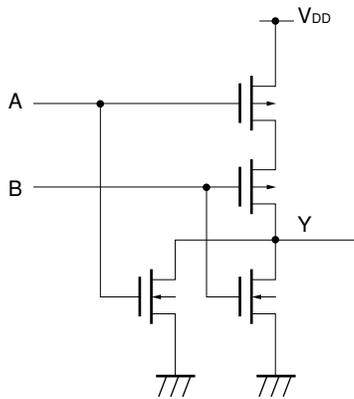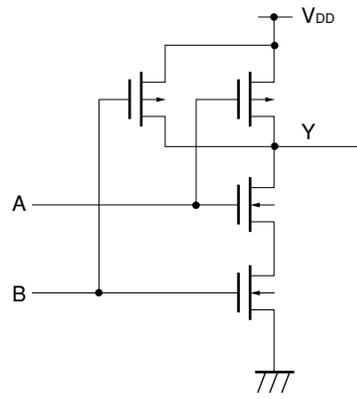
1.5 QFP Package

Figure 1-4 shows a cross-section of a normal QFP package. In a normal QFP package, the chip is placed on a metal plate called an island. The leads and chip are connected by fine bonding wires measuring only several 10 μm in diameter.

In a low thermal resistance type QFP package, the lead and island materials have increased thermal dissipation properties. The construction itself is the same as a normal QFP package.

Figure 1-4. Cross-Section of QFP Package
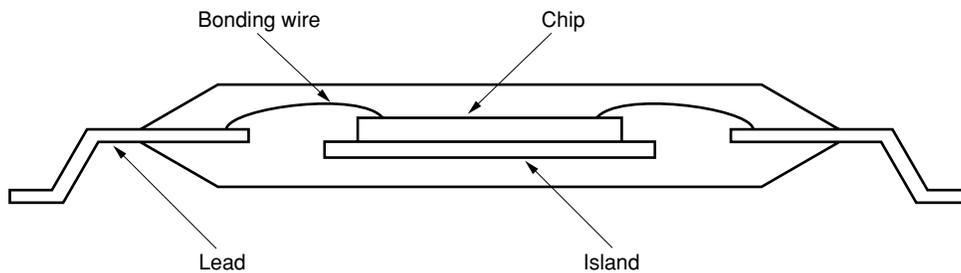
CHAPTER 2 IMPLEMENTING THE SYSTEM USING THE GATE ARRAY

Be sure to read this chapter since it describes the information that is important when starting design.

When using gate arrays to develop an LSI to implement some or all of a system designed by the user, the specifications must be determined so that the circuit scale and the number of I/O pins of the gate arrays are optimum.

As the circuit scale increases, designing the circuit becomes more difficult and the cost of the LSI increases. However, because the number of I/O pins can be reduced, so can the mounting area on a printed wiring board.

In addition, because the number of LSIs used decreases, the propagation delay time is shortened.

However, as the circuit scale decreases, many separate gate arrays are required to configure the system. This is disadvantageous in terms of printed circuit board mounting. Moreover, because signals are transferred between many LSIs, it is difficult to shorten the propagation delay time.

Therefore, when selecting a gate array, take into consideration the propagation delay time and circuit scale.

Select a gate array in the following steps.

[Circuit selection steps]

(1) Estimate circuit scale and master size
        ↓
(2) Select package
        ↓
(3) Verify power consumption
        ↓
(4) Verify pin placement
        ↓
(5) Verify I/O interface level
        ↓
(6) Design circuit
        ↓
(7) Interface
        ↓
(8) Check using the check items

2.1 Estimating Circuit Scale

2.1.1 Cell utilization rate, usable cell and pin-pair count limits

In a channel architecture gate array, the internal cell region is divided into two regions.

- Region where transistors that implement the function block are placed
- Routing dedicated region

In a channelless architecture gate array, the region for implementing the function blocks cannot be clearly distinguished from the routing region because the transistors that implement the function blocks are laid out over the entire internal cell region. Consequently, there is a stronger correlation between the number of cells utilized and the number of nets.

The CMOS-N5 Series uses a channelless architecture (sea-of-gates). This means that not all cells in the internal cell region can be used for function blocks such as gates, flip-flops, and memory. The number of cells actually used is the difference between the total number of cells and the routing cell region used by the number of wires between blocks (number of pin pairs).

The maximum cell utilization rate for the CMOS-N5 Series is as follows.

μPD65880, 65881, 65882, 65883, 65884 : 85%
μPD65891, 65892, 65894 :   80%
μPD65885, 65887, 65889, 65890, 65893 : 75%

However, if a large-scale block, such as memory, is placed, it may be that the total cell utilization rate is further limited, depending on the type of macro (see **2.1.3 Large-scale macro mounting** for details).

The pin-pair count is limited by the cell utilization rate and can be calculated by the following formula:

Pin-pair count = $150 \times$ number of raw cells $\times \{(100 -$ cell utilization rate$)/100\}^2/74.69$

[Pin-pair count] is the number of wires connecting the output pins and input pins between blocks (see **Figure 2-1**).

Figure 2-1. Pin-Pair Count
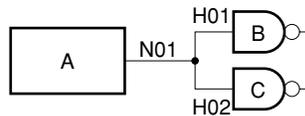
Block A N01-Block B H01
Block A N01-Block C H02

Total of 2 pairs (pin pair count = 2)

If many small-scale blocks such as inverters are used, routing between blocks increases compared with the number of cells used, which increases the number of routing channels.

Conversely, if many large-scale blocks such as memory are used, routing between blocks decreases compared with the number of cells used, which decreases the number of channels required.

Consequently, when placing large-scale blocks, such as memory, the cell utilization rate is further limited. Circuits that do not include memory are limited by the pin-pair count.

Table 2-1. Number of Cells Placed

Master	X	Y	Cells Placed
μPD65891	80	24	1920
μPD65880	108	32	3456
μPD65881	140	42	5880
μPD65892	152	46	6992
μPD65882	218	64	13952
μPD65894	224	68	15232
μPD65883	288	88	25344
μPD65884	332	102	33864
μPD65885	364	112	40768
μPD65887	428	130	55640
μPD65889	500	152	76000
μPD65890	572	174	99528
μPD65893	636	194	123384

Remark $X \times Y$ under the heading "Cells Placed" indicates that the master has a cell space of X in the horizontal direction and a cell space of Y in the vertical direction.

If the actual cell utilization rate and pin-pair count can be satisfied, placement and routing can be guaranteed in the standard schedule in most cases. On the other hand, in cases where the limits are exceeded, placement and routing requires a longer time and, in the worst case, becomes impossible.

Table 2-2 shows the number of usable gates and the corresponding pin-pair count with respect to the cell utilization rate.

Table 2-2. Usable Gates and Pin-Pair Count (1/2)

Master	40% Cell Utilization		50% Cell Utilization		60% Cell Utilization	
	Usable	Pin Pairs	Usable	Pin Pairs	Usable	Pin Pairs
μPD65891	768	1388	960	963	1152	616
μPD65880	1382	2498	1728	1735	2073	1110
μPD65881	2352	4251	2940	2952	3528	1889
μPD65892	2796	5055	3496	3510	4195	2246
μPD65882	5580	10087	6976	7004	8371	4483
μPD65894	6092	11012	7616	7647	9139	4894
μPD65883	10137	18323	12672	12724	15206	8143
μPD65884	13545	24483	16932	17002	20318	10881
μPD65885	16307	29474	20384	20468	24460	13099
μPD65887	22256	40227	27820	27935	33384	17878
μPD65889	30400	54947	38000	38157	45600	24420
μPD65890	39811	71957	49764	49970	59716	31981
μPD65893	49353	89205	61692	61948	74030	39646

Table 2-2. Usable Gates and Pin-Pair Count (2/2)

Master	70% Cell Utilization		75% Cell Utilization		80% Cell Utilization		85% Cell Utilization	
	Usable	Pin Pairs	Usable	Pin Pairs	Usable	Pin Pairs	Usable	Pin Pairs
μPD65891	1344	347	1440	240	1536	154	1632	86
μPD65880	2419	624	2592	433	2764	277	2937	156
μPD65881	4116	1062	4410	738	4704	472	4998	265
μPD65892	4894	1263	5244	877	5593	561	5943	315
μPD65882	9766	2521	10464	1751	11161	1120	11859	630
μPD65894	10662	2753	11424	1911	12185	1223	12947	688
μPD65883	17740	4580	19008	3181	20275	2035	21542	1145
μPD65884	23704	6120	25398	4250	27091	2720	28784	1530
μPD65885	28537	7368	30576	5117	32614	3274	34652	1842
μPD65887	38948	10056	41730	6983	44512	4469	47294	2514
μPD65889	53200	13736	57000	9539	60800	6105	64600	3434
μPD65890	69669	17989	74646	12492	79622	7995	84598	4497
μPD65893	86368	22301	92538	15847	98707	9911	104876	5575

2.1.2 Notes on estimating number of cells used

(1) Input/output/bidirectional buffer blocks

Not only I/O cells but also internal cells are used to configure external interface blocks such as input, output, and bidirectional blocks. Therefore, add the number of internal cells used for input, output, and bidirectional buffer blocks described in the **CMOS-N5 Series (5.0 V) Block Library (A13872E)** and **CMOS-N5 Series (3.3 V) Block Library (A15895E)** when calculating the total number of cells used.

(2) Critical paths

If there is a path in which speed is a problem, measures can be taken in some cases to shorten the propagation delay of that path. However, routability drops dramatically when such measures are taken. In such a case, the cell utilization rate and maximum pin-pair count should be reduced by about 10 to 20%.

(3) Macro configuration

Placement and routing are performed for each hierarchical macro (first hierarchy) in the circuit. Therefore, the hierarchical configuration calls for adequate consideration when a macro is created. Keep in mind the following points when performing hierarchical designing.

(a) Because the routing between macros of the first hierarchy is long, avoid hierarchical design that implements one function between macros.

(b) Avoid placing a small-scale macro used to facilitate circuit designing in the first hierarchy.

2.1.3 Large-scale macro mounting

Large-scale macro mountability is determined by whether or not it is possible to achieve the range $(X \times Y)$ of cells needed to implement the macros on the physical space of the internal cells indicated by $(X \times Y)$. For soft macros configured by small and medium-scale blocks, virtually no problems of mounting arise as long as the cell utilization rate is satisfied. However, there are cases in which large-scale hard macros such as RAM blocks (basic macro) and megamacros cannot be physically mounted due to the size of the master.

(1) Where only one large-scale macro is mounted

Table 2-3 shows the mountability of each large-scale macro on each master.

Table 2-3. List of Mountability (1/4)

(a) Single-Port RAM (1/2)

Master	RB47	RB49	RB4B	RB4D	RB4F	RB4H	RB4M	RB4S	RB87	RB89	RB8B	RB8D	RB8F	RB8H
μPD65891	√	√	√	×	×	×	×	×	√	√	×	×	×	×
μPD65880	√	√	√	√	×	×	×	×	√	√	√	×	×	×
μPD65881	√	√	√	√	×	×	×	×	√	√	√	×	×	×
μPD65892	√	√	√	√	√	×	×	×	√	√	√	√	×	×
μPD65882	√	√	√	√	√	√	×	×	√	√	√	√	√	×
μPD65894	√	√	√	√	√	√	×	×	√	√	√	√	√	×
μPD65883	√	√	√	√	√	√	√	×	√	√	√	√	√	√
μPD65884	√	√	√	√	√	√	√	√	√	√	√	√	√	√
μPD65885	√	√	√	√	√	√	√	√	√	√	√	√	√	√
μPD65887	√	√	√	√	√	√	√	√	√	√	√	√	√	√
μPD65889	√	√	√	√	√	√	√	√	√	√	√	√	√	√
μPD65890	√	√	√	√	√	√	√	√	√	√	√	√	√	√
μPD65893	√	√	√	√	√	√	√	√	√	√	√	√	√	√

Master	RB8M	RBAB	RBAD	RBAF	RBAH	RBC7	RBC9	RBCB	RBCD	RBCF	RBCH	RBCM	RBEB	RBED
μPD65891	×	×	×	×	×	×	×	×	×	×	×	×	×	×
μPD65880	×	√	×	×	×	√	√	×	×	×	×	×	×	×
μPD65881	×	√	×	×	×	√	√	√	×	×	×	×	×	×
μPD65892	×	√	√	×	×	√	√	√	×	×	×	×	√	×
μPD65882	×	√	√	√	×	√	√	√	√	×	×	×	√	√
μPD65894	×	√	√	√	×	√	√	√	√	×	×	×	√	√
μPD65883	×	√	√	√	×	√	√	√	√	√	×	×	√	√
μPD65884	√	√	√	√	√	√	√	√	√	√	√	×	√	√
μPD65885	√	√	√	√	√	√	√	√	√	√	√	×	√	√
μPD65887	√	√	√	√	√	√	√	√	√	√	√	×	√	√
μPD65889	√	√	√	√	√	√	√	√	√	√	√	√	√	√
μPD65890	√	√	√	√	√	√	√	√	√	√	√	√	√	√
μPD65893	√	√	√	√	√	√	√	√	√	√	√	√	√	√

Remark √: Mountable, ×: Not mountable

Table 2-3. List of Mountability (2/4)

(a) Single-Port RAM (2/2)

Master	RBEF	RBEH	RBH7	RBH9	RBHB	RBHD	RBHF	RBHH	RBKB	RBKD	RBKF	RBKH
μPD65891	×	×	×	×	×	×	×	×	×	×	×	×
μPD65880	×	×	×	×	×	×	×	×	×	×	×	×
μPD65881	×	×	√	×	×	×	×	×	×	×	×	×
μPD65892	×	×	√	√	×	×	×	×	×	×	×	×
μPD65882	×	×	√	√	√	×	×	×	√	×	×	×
μPD65894	×	×	√	√	√	×	×	×	√	×	×	×
μPD65883	×	×	√	√	√	√	×	×	√	×	×	×
μPD65884	√	×	√	√	√	√	√	×	√	√	×	×
μPD65885	√	√	√	√	√	√	√	×	√	√	×	×
μPD65887	√	√	√	√	√	√	√	×	√	√	√	×
μPD65889	√	√	√	√	√	√	√	√	√	√	√	√
μPD65890	√	√	√	√	√	√	√	√	√	√	√	√
μPD65893	√	√	√	√	√	√	√	√	√	√	√	√

Remark   √: Mountable, ×: Not mountable

Table 2-3. List of Mountability (3/4)

(b) Dual-Port RAM

Master	R947	R949	R94B	R94D	R94F	R94H	R987	R989	R98B	R98D	R98F	R9AB	R9AD	R9C7
μPD65891	√	√	×	×	×	×	√	×	×	×	×	×	×	×
μPD65880	√	√	√	√	×	×	√	√	√	×	×	√	×	√
μPD65881	√	√	√	√	×	×	√	√	√	×	×	√	×	√
μPD65892	√	√	√	√	×	×	√	√	√	×	×	√	×	√
μPD65882	√	√	√	√	√	×	√	√	√	√	×	√	√	√
μPD65894	√	√	√	√	√	√	√	√	√	√	√	√	√	√
μPD65883	√	√	√	√	√	√	√	√	√	√	√	√	√	√
μPD65884	√	√	√	√	√	√	√	√	√	√	√	√	√	√
μPD65885	√	√	√	√	√	√	√	√	√	√	√	√	√	√
μPD65887	√	√	√	√	√	√	√	√	√	√	√	√	√	√
μPD65889	√	√	√	√	√	√	√	√	√	√	√	√	√	√
μPD65890	√	√	√	√	√	√	√	√	√	√	√	√	√	√
μPD65893	√	√	√	√	√	√	√	√	√	√	√	√	√	√

Master	R9C9	R9CB	R9CD	R9CF	R9EB	R9ED	R9H7	R9H9	R9HB	R9KB
μPD65891	×	×	×	×	×	×	×	×	×	×
μPD65880	×	×	×	×	×	×	×	×	×	×
μPD65881	√	×	×	×	×	×	×	×	×	×
μPD65892	√	×	×	×	×	×	√	×	×	×
μPD65882	√	√	×	×	√	×	√	√	×	×
μPD65894	√	√	√	×	√	×	√	√	√	×
μPD65883	√	√	√	√	√	√	√	√	√	√
μPD65884	√	√	√	√	√	√	√	√	√	√
μPD65885	√	√	√	√	√	√	√	√	√	√
μPD65887	√	√	√	√	√	√	√	√	√	√
μPD65889	√	√	√	√	√	√	√	√	√	√
μPD65890	√	√	√	√	√	√	√	√	√	√
μPD65893	√	√	√	√	√	√	√	√	√	√

Remark √: Mountable, ×: Not mountable

Table 2-3. List of Mountability (4/4)

(c) Megamacro

Master	NA37A	NA51A	NA54A	NA55A	NA59A	NA16550A
μPD65891	×	×	×	×	×	×
μPD65880	×	×	×	√	×	×
μPD65881	×	√	×	√	√	×
μPD65892	√	√	√	√	√	×
μPD65882	√	√	√	√	√	√
μPD65894	√	√	√	√	√	√
μPD65883	√	√	√	√	√	√
μPD65884	√	√	√	√	√	√
μPD65885	√	√	√	√	√	√
μPD65887	√	√	√	√	√	√
μPD65889	√	√	√	√	√	√
μPD65890	√	√	√	√	√	√
μPD65893	√	√	√	√	√	√

Remark   √: Mountable, ×: Not mountable

(2) Where two or more large-scale macros are mounted

Whether two or more macros can be mounted is determined by the range of the cells necessary for implementing each macro on the chip, and the range of cells that can be implemented on the master.

(a) Range of cells occupied by each macro on chip (soft macro RAM)

An NEC Electronics RAM is implemented by soft macros that consist of a basic macro and a logic area. The shape of the cell area occupied to implement a macro depends on how the basic macro is placed. The cell area occupied is limited by the master selected.

Figure 2-2. Shape of Cell Range Occupied by Macros (with 4 Basic Macros)
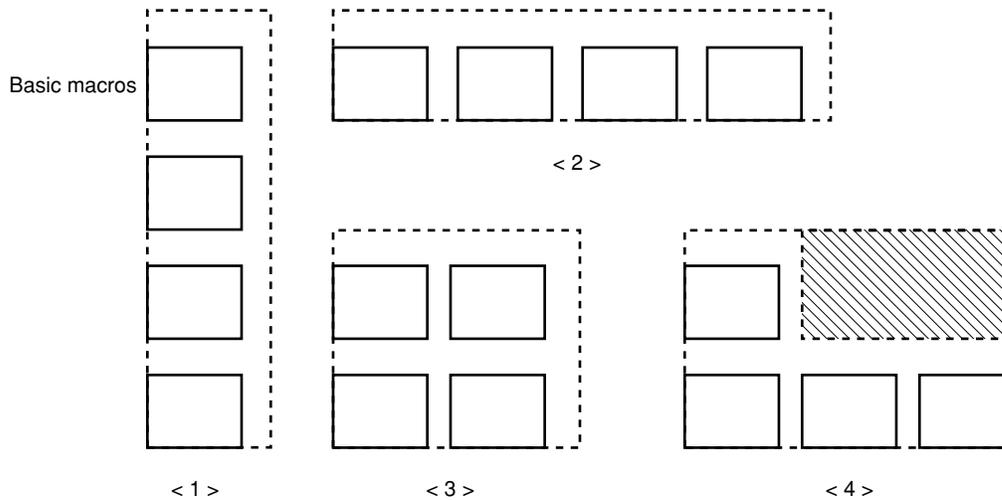
<1> Limited by the number of vertical cells of the master.
<2> Limited by the number of horizontal cells of the master.
<3> Effective if the number of basic blocks used becomes large.
<4> Physically possible but ineffective (because the placement range that can be set up during placement and routing is square or rectangular, the diagonally shaded area is wasted).

Table 2-5 lists examples of the cell ranges occupied by macros. However, it is possible to redefine cell ranges for a RAM outside those in Table 2-4.

To define cell ranges for soft macro RAM, first find the basic macro name and the number of cells required to configure the soft macro RAM in Table 2-5. Next, find the minimum number of cells occupied by the macro (X and Y values) in order to place one basic macro in Table 2-4. Then calculate the cell range by substituting in the variables in the following equation with the values from Tables 2-4 and 2-5.

Figure 2-3. Cell Range Occupied by Macro
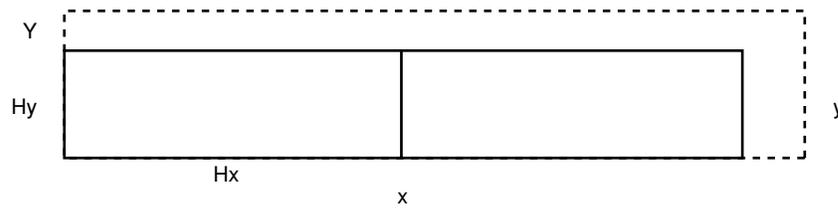
$y = 2^n \times Hy + Y$

$x = soft/uty/y$

In the above equation, $x \geq N/2^n \times Hx$ must be satisfied.

soft: Number of cells in the soft macro RAM

uty: 0.60

Hx: Minimum number of cells occupied in the horizontal direction needed for placing basic macros.

Hy: Minimum number of cells occupied in the vertical direction needed for placing basic macros.

N: Number of basic macros used

n When the number of basic macros is 1, n = 0

    When the number of basic macros is 2, n = 0, 1

    When the number of basic macros is 4, n = 0, 1, 2

    When the number of basic macros is 8, n = 0, 1, 2, 3

    When the number of basic macros is 16, n = 0, 1, 2, 3, 4

    When the number of basic macros is 32, n = 0, 1, 2, 3, 4, 5

Y: Arbitrary integer (Y = 0, 1, 2, ...)

(b) Array of internal cells of master selected (see Table 2-1)

Internal cells are also used for interface blocks and are limited as closely as possible to the I/O cell range in the CMOS-N5 Series. The area of internal cells used by the interface block is 17 internal cells from the left edge to the right edge and 2 cells from the top edge to the bottom edge. Therefore the cell area in which the macro can be placed must be within the 17×2 range (blank part).

Figure 2-4. Area Where Macros Cannot Be Implemented
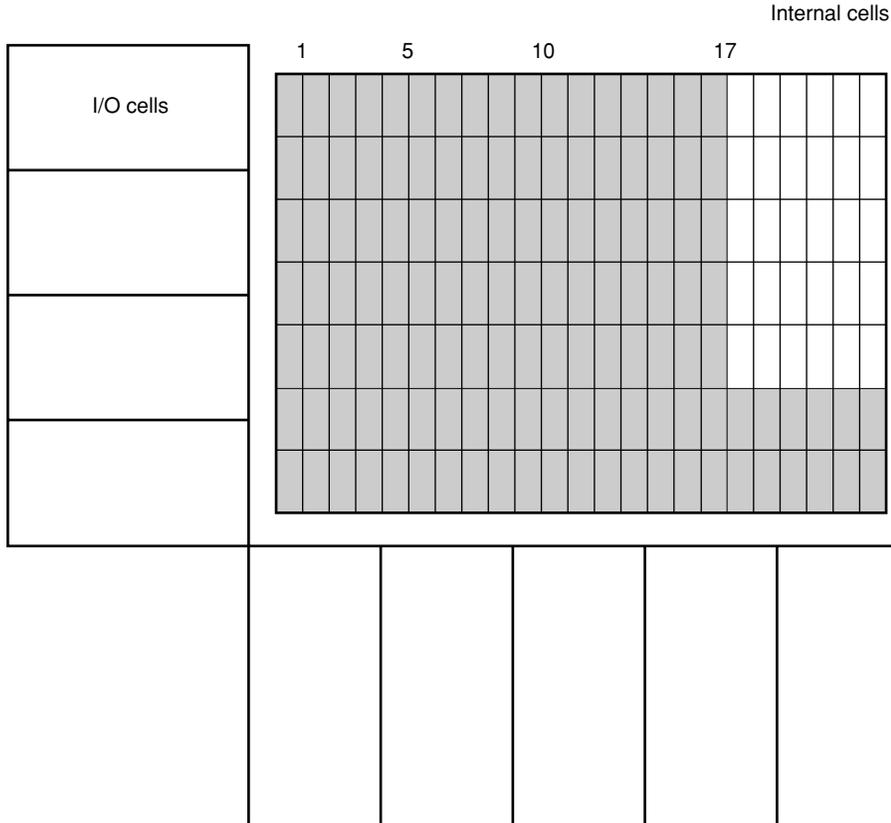
(c) Determining mountability

Macros are mountable if they can all be placed without overlapping, within the allowable area for implementing macros on the chip. If they are unmountable, modification of the shape of the macro-occupied area must be considered. If only a few cells overlap, contact NEC Electronics to determine mountability taking the pin configuration and macro placement position into consideration.

Table 2-4. Minimum Number of Cells Occupied by Basic Macro

(a) Single-Port RAM

Basic Macro Name	Words	Bits	X	Y
K147	16	4	29	12
K149	32	4	47	13
K14D	128	4	79	22
K18B	64	8	81	21
K18F	256	8	158	38
K1AB	64	10	81	25

(b) Dual-Port RAM

Basic Macro Name	Words	Bits	X	Y
K247	16	4	37	13
K249	32	4	63	15
K24D	128	4	112	24
K28B	64	8	113	24
K28F	256	8	224	41
K2AB	64	10	113	28

Table 2-5 shows the block names and cell ranges occupied by each RAM macro on the chip.

Table 2-5. Occupied Cell Ranges (1/8)

(a) Single-Port RAM (75% Cell Utilization)

Words × Bits	Soft Macro RAM	Basic Macro × Q'ty	Cell Ranges Occupied by RAM							
			Type A		Type B		Type C		Type D	
			X	Y	X	Y	X	Y	X	Y
16 × 4	RB47	K147 × 1	54	12						
32 × 4	RB49	K149 × 1	71	13						
64 × 4	RB4B	K149 × 2	61	26	122	13				
128 × 4	RB4D	K14D × 1	96	22						
256 × 4	RB4F	K14D × 2	89	44	177	22				
512 × 4	RB4H	K14D × 4	81	91	168	44	335	22		
1K × 4	RB4M	K14D × 8	78	185	159	91	328	44		
2K × 4	RB4S	K14D × 16	155	185	155	91				
16 × 8	RB87	K147 × 2	44	24	87	12				
32 × 8	RB89	K149 × 2	61	26	122	13				
64 × 8	RB8B	K18B × 1	100	21						
128 × 8	RB8D	K14D × 2	89	44	177	22				
256 × 8	RB8F	K18F × 1	170	38						
512 × 8	RB8H	K18F × 2	165	76	329	38				
1K × 8	RB8M	K18F × 4	159	155	323	76				
64 × 10	RBAB	K1AB × 1	98	25						
128 × 10	RBAD	K1AB × 2	91	50	181	25				
256 × 10	RBAF	K1AB × 4	84	103	173	50	346	25		
512 × 10	RBAH	K1AB × 8	164	103	338	50				
16 × 16	RBC7	K147 × 4	36	51	77	24	153	12		
32 × 16	RBC9	K149 × 4	53	55	112	26	224	13		
64 × 16	RBCB	K18B × 2	93	42	186	21				
128 × 16	RBCD	K14D × 4	82	91	170	44	340	22		
256 × 16	RBCF	K18F × 2	165	76	330	38				
512 × 16	RBCH	K18F × 4	159	155	324	76				
1K × 16	RBCM	K18F × 8	315	155						
64 × 20	RBEB	K1AB × 2	93	50	185	25				
128 × 20	RBED	K1AB × 4	85	103	175	50	350	25		
256 × 20	RBEF	K1AB × 8	165	103	339	50				
512 × 20	RBEH	K1AB × 16	324	103						
16 × 32	RBH7	K147 × 8	33	105	68	51	143	24	286	12
32 × 32	RBH9	K149 × 8	50	113	101	55	214	26	427	13
64 × 32	RBHB	K18B × 4	87	87	179	42	357	21		
128 × 32	RBHD	K14D × 8	79	185	161	91	333	44		
256 × 32	RBHF	K18F × 4	160	155	325	76				
512 × 32	RBHH	K18F × 8	315	155						
64 × 40	RBKB	K1AB × 4	87	103	179	50	357	25		
128 × 40	RBKD	K1AB × 8	167	103	343	50				
256 × 40	RBKF	K18F × 5	315	117	485	76				
512 × 40	RBKH	K18F × 10	474	155	624	117				

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Table 2-5. Occupied Cell Ranges (2/8)

(b) Single-Port RAM (70% Cell Utilization)

Words × Bits	Soft Macro RAM	Basic Macro × Q'ty	Cell Ranges Occupied by RAM							
			Type A		Type B		Type C		Type D	
			X	Y	X	Y	X	Y	X	Y
16 × 4	RB47	K147 × 1	56	12						
32 × 4	RB49	K149 × 1	73	13						
64 × 4	RB4B	K149 × 2	62	26	124	13				
128 × 4	RB4D	K14D × 1	97	22						
256 × 4	RB4F	K14D × 2	89	44	178	22				
512 × 4	RB4H	K14D × 4	82	91	168	44	336	22		
1K × 4	RB4M	K14D × 8	79	185	159	91	329	44		
2K × 4	RB4S	K14D × 16	155	185	314	91				
16 × 8	RB87	K147 × 2	45	24	89	12				
32 × 8	RB89	K149 × 2	62	26	124	13				
64 × 8	RB8B	K18B × 1	101	21						
128 × 8	RB8D	K14D × 2	89	44	178	22				
256 × 8	RB8F	K18F × 1	171	38						
512 × 8	RB8H	K18F × 2	165	76	330	38				
1K × 8	RB8M	K18F × 4	159	155	324	76				
64 × 10	RBAB	K1AB × 1	99	25						
128 × 10	RBAD	K1AB × 2	92	50	183	25				
256 × 10	RBAF	K1AB × 4	85	103	174	50	347	25		
512 × 10	RBAH	K1AB × 8	165	103	338	50				
16 × 16	RBC7	K147 × 4	37	51	78	24	156	12		
32 × 16	RBC9	K149 × 4	54	55	114	26	227	13		
64 × 16	RBCB	K18B × 2	94	42	187	21				
128 × 16	RBCD	K14D × 4	83	91	171	44	341	22		
256 × 16	RBCF	K18F × 2	166	76	331	38				
512 × 16	RBCH	K18F × 4	159	155	325	76				
1K × 16	RBCM	K18F × 8	315	155						
64 × 20	RBEB	K1AB × 2	93	50	186	25				
128 × 20	RBED	K1AB × 4	86	103	176	50	352	25		
256 × 20	RBEF	K1AB × 8	165	103	340	50				
512 × 20	RBEH	K1AB × 16	324	103						
16 × 32	RBH7	K147 × 8	34	105	68	51	145	24	289	12
32 × 32	RBH9	K149 × 8	50	113	102	55	216	26	431	13
64 × 32	RBHB	K18B × 4	87	87	180	42	359	21		
128 × 32	RBHD	K14D × 8	80	185	162	91	334	44		
256 × 32	RBHF	K18F × 4	160	155	326	76				
512 × 32	RBHH	K18F × 8	316	155						
64 × 40	RBKB	K1AB × 4	88	103	180	50	359	25		
128 × 40	RBKD	K1AB × 8	168	103	345	50				
256 × 40	RBKF	K18F × 5	315	117	485	76				
512 × 40	RBKH	K18F × 10	474	155	624	117				

Table 2-5. Occupied Cell Ranges (3/8)

(c) Single-Port RAM (60% Cell Utilization)

Words × Bits	Soft Macro RAM	Basic Macro × Q'ty	Cell Ranges Occupied by RAM							
			Type A		Type B		Type C		Type D	
			X	Y	X	Y	X	Y	X	Y
16 × 4	RB47	K147 × 1	61	12						
32 × 4	RB49	K149 × 1	77	13						
64 × 4	RB4B	K149 × 2	65	26	129	13				
128 × 4	RB4D	K14D × 1	100	22						
256 × 4	RB4F	K14D × 2	91	44	181	22				
512 × 4	RB4H	K14D × 4	82	91	170	44	339	22		
1K × 4	RB4M	K14D × 8	79	185	160	91	331	44		
2K × 4	RB4S	K14D × 16	155	185	316	91				
16 × 8	RB87	K147 × 2	47	24	94	12				
32 × 8	RB89	K149 × 2	65	26	129	13				
64 × 8	RB8B	K18B × 1	105	21						
128 × 8	RB8D	K14D × 2	91	44	182	22				
256 × 8	RB8F	K18F × 1	173	38						
512 × 8	RB8H	K18F × 2	166	76	332	38				
1K × 8	RB8M	K18F × 4	159	155	325	76				
64 × 10	RBAB	K1AB × 1	102	25						
128 × 10	RBAD	K1AB × 2	93	50	186	25				
256 × 10	RBAF	K1AB × 4	86	103	176	50	351	25		
512 × 10	RBAH	K1AB × 8	166	103	341	50				
16 × 16	RBC7	K147 × 4	39	51	81	24	162	12		
32 × 16	RBC9	K149 × 4	55	55	117	26	233	13		
64 × 16	RBCB	K18B × 2	96	42	191	21				
128 × 16	RBCD	K14D × 4	84	91	173	44	345	22		
256 × 16	RBCF	K18F × 2	167	76	334	38				
512 × 16	RBCH	K18F × 4	160	155	326	76				
1K × 16	RBCM	K18F × 8	316	155						
64 × 20	RBEB	K1AB × 2	95	50	190	25				
128 × 20	RBED	K1AB × 4	87	103	178	50	356	25		
256 × 20	RBEF	K1AB × 8	167	103	343	50				
512 × 20	RBEH	K1AB × 16	326	103						
16 × 32	RBH7	K147 × 8	35	105	71	51	150	24	299	12
32 × 32	RBH9	K149 × 8	51	113	104	55	220	26	440	13
64 × 32	RBHB	K18B × 4	89	87	183	42	365	21		
128 × 32	RBHD	K14D × 8	80	185	163	91	337	44		
256 × 32	RBHF	K18F × 4	161	155	328	76				
512 × 32	RBHH	K18F × 8	317	155						
64 × 40	RBKB	K1AB × 4	89	103	183	50	365	25		
128 × 40	RBKD	K1AB × 8	169	103	348	50				
256 × 40	RBKF	K18F × 5	317	117	487	76				
512 × 40	RBKH	K18F × 10	474	155	626	117				

Table 2-5. Occupied Cell Ranges (4/8)

(d) Single-Port RAM (50% Cell Utilization)

Words × Bits	Soft Macro RAM	Basic Macro × Q'ty	Cell Ranges Occupied by RAM							
			Type A		Type B		Type C		Type D	
			X	Y	X	Y	X	Y	X	Y
16 × 4	RB47	K147 × 1	67	12						
32 × 4	RB49	K149 × 1	83	13						
64 × 4	RB4B	K149 × 2	68	26	135	13				
128 × 4	RB4D	K14D × 1	104	22						
256 × 4	RB4F	K14D × 2	93	44	186	22				
512 × 4	RB4H	K14D × 4	83	91	172	44	344	22		
1K × 4	RB4M	K14D × 8	80	185	162	91	334	44		
2K × 4	RB4S	K14D × 16	156	185	156	91				
16 × 8	RB87	K147 × 2	51	24	101	12				
32 × 8	RB89	K149 × 2	68	26	136	13				
64 × 8	RB8B	K18B × 1	109	21						
128 × 8	RB8D	K14D × 2	93	44	186	22				
256 × 8	RB8F	K18F × 1	175	38						
512 × 8	RB8H	K18F × 2	168	76	336	38				
1K × 8	RB8M	K18F × 4	160	155	326	76				
64 × 10	RBAB	K1AB × 1	107	25						
128 × 10	RBAD	K1AB × 2	96	50	191	25				
256 × 10	RBAF	K1AB × 4	87	103	178	50	356	25		
512 × 10	RBAH	K1AB × 8	167	103	344	50				
16 × 16	RBC7	K147 × 4	41	51	86	24	171	12		
32 × 16	RBC9	K149 × 4	58	55	121	26	242	13		
64 × 16	RBCB	K18B × 2	99	42	197	21				
128 × 16	RBCD	K14D × 4	85	91	176	44	351	22		
256 × 16	RBCF	K18F × 2	169	76	337	38				
512 × 16	RBCH	K18F × 4	161	155	328	76				
1K × 16	RBCM	K18F × 8	317	155						
64 × 20	RBEB	K1AB × 2	98	50	196	25				
128 × 20	RBED	K1AB × 4	88	103	181	50	362	25		
256 × 20	RBEF	K1AB × 8	168	103	347	50				
512 × 20	RBEH	K1AB × 16	328	103						
16 × 32	RBH7	K147 × 8	36	105	74	51	156	24	312	12
32 × 32	RBH9	K149 × 8	52	113	107	55	226	26	452	13
64 × 32	RBHB	K18B × 4	91	87	187	42	373	21		
128 × 32	RBHD	K14D × 8	81	185	165	91	341	44		
256 × 32	RBHF	K18F × 4	162	155	330	76				
512 × 32	RBHH	K18F × 8	318	155						
64 × 40	RBKB	K1AB × 4	91	103	187	50	373	25		
128 × 40	RBKD	K1AB × 8	171	103	353	50				
256 × 40	RBKF	K18F × 5	318	117	490	76				
512 × 40	RBKH	K18F × 10	474	155	628	117				

Table 2-5. Occupied Cell Ranges (5/8)

(e) Dual-Port RAM (75% Cell Utilization)

Words × Bits	Soft Macro RAM	Basic Macro × Q'ty	Cell Ranges Occupied by RAM							
			Type A		Type B		Type C		Type D	
			X	Y	X	Y	X	Y	X	Y
16 × 4	R947	K247 × 1	63	13						
32 × 4	R949	K249 × 1	85	15						
64 × 4	R94B	K249 × 2	76	30	151	15				
128 × 4	R94D	K24D × 1	129	24						
256 × 4	R94F	K24D × 2	121	48	242	24				
512 × 4	R94H	K24D × 4	113	99	233	48	465	24		
16 × 8	R987	K247 × 2	56	26	111	13				
32 × 8	R989	K249 × 2	75	30	150	15				
64 × 8	R98B	K28B × 1	131	24						
128 × 8	R98D	K24D × 2	121	48	242	24				
256 × 8	R98F	K28F × 1	235	41						
64 × 10	R9AB	K2AB × 1	129	28						
128 × 10	R9AD	K2AB × 2	122	56	244	28				
16 × 16	R9C7	K247 × 4	44	55	93	26	186	13		
32 × 16	R9C9	K249 × 4	67	63	141	30	281	15		
64 × 16	R9CB	K28B × 2	124	48	247	24				
128 × 16	R9CD	K24D × 4	114	99	235	48	469	24		
256 × 16	R9CF	K28F × 2	230	82	460	41				
64 × 20	R9EB	K2AB × 2	123	56	246	28				
128 × 20	R9ED	K2AB × 4	116	115	237	56	474	28		
16 × 32	R9H7	K247 × 8	41	113	83	55	175	26	349	13
32 × 32	R9H9	K249 × 8	63	129	129	63	271	30	541	15
64 × 32	R9HB	K28B × 4	117	99	240	48	480	24		
64 × 40	R9KB	K2AB × 4	117	115	240	56	480	28		

Table 2-5. Occupied Cell Ranges (6/8)

(f) Dual-Port RAM (70% Cell Utilization)

Words × Bits	Soft Macro RAM	Basic Macro × Q'ty	Cell Ranges Occupied by RAM							
			Type A		Type B		Type C		Type D	
			X	Y	X	Y	X	Y	X	Y
16 × 4	R947	K247 × 1	65	13						
32 × 4	R949	K249 × 1	87	15						
64 × 4	R94B	K249 × 2	77	30	153	15				
128 × 4	R94D	K24D × 1	130	24						
256 × 4	R94F	K24D × 2	122	48	243	24				
512 × 4	R94H	K24D × 4	113	99	234	48	467	24		
16 × 8	R987	K247 × 2	53	26	105	13				
32 × 8	R989	K249 × 2	76	30	152	15				
64 × 8	R98B	K28B × 1	132	24						
128 × 8	R98D	K24D × 2	122	48	244	24				
256 × 8	R98F	K28F × 1	236	41						
64 × 10	R9AB	K2AB × 1	130	28						
128 × 10	R9AD	K2AB × 2	123	56	246	28				
16 × 16	R9C7	K247 × 4	45	55	95	26	189	13		
32 × 16	R9C9	K249 × 4	68	63	142	30	283	15		
64 × 16	R9CB	K28B × 2	125	48	249	24				
128 × 16	R9CD	K24D × 4	114	99	235	48	470	24		
256 × 16	R9CF	K28F × 2	230	82	460	41				
64 × 20	R9EB	K2AB × 2	124	56	248	28				
128 × 20	R9ED	K2AB × 4	116	115	238	56	476	28		
16 × 32	R9H7	K247 × 8	41	113	84	55	177	26	353	13
32 × 32	R9H9	K249 × 8	64	129	130	63	272	30	543	15
64 × 32	R9HB	K28B × 4	117	99	241	48	482	24		
64 × 40	R9KB	K2AB × 4	118	115	241	56	482	28		

Table 2-5. Occupied Cell Ranges (7/8)

(g) Dual-Port RAM (60% Cell Utilization)

Words × Bits	Soft Macro RAM	Basic Macro × Q'ty	Cell Ranges Occupied by RAM							
			Type A		Type B		Type C		Type D	
			X	Y	X	Y	X	Y	X	Y
16 × 4	R947	K247 × 1	69	13						
32 × 4	R949	K249 × 1	91	15						
64 × 4	R94B	K249 × 2	79	30	157	15				
128 × 4	R94D	K24D × 1	133	24						
256 × 4	R94F	K24D × 2	123	48	246	24				
512 × 4	R94H	K24D × 4	114	99	235	48	470	24		
16 × 8	R987	K247 × 2	56	26	111	13				
32 × 8	R989	K249 × 2	78	30	156	15				
64 × 8	R98B	K28B × 1	135	24						
128 × 8	R98D	K24D × 2	124	48	247	24				
256 × 8	R98F	K28F × 1	238	41						
64 × 10	R9AB	K2AB × 1	133	28						
128 × 10	R9AD	K2AB × 2	125	56	249	28				
16 × 16	R9C7	K247 × 4	47	55	98	26	196	13		
32 × 16	R9C9	K249 × 4	69	63	144	30	288	15		
64 × 16	R9CB	K28B × 2	127	48	253	24				
128 × 16	R9CD	K24D × 4	115	99	237	48	474	24		
256 × 16	R9CF	K28F × 2	231	82	462	41				
64 × 20	R9EB	K2AB × 2	126	56	251	28				
128 × 20	R9ED	K2AB × 4	117	115	240	56	480	28		
16 × 32	R9H7	K247 × 8	42	113	86	55	182	26	363	13
32 × 32	R9H9	K249 × 8	64	129	131	63	275	30	550	15
64 × 32	R9HB	K28B × 4	118	99	244	48	487	24		
64 × 40	R9KB	K2AB × 4	119	115	244	56	487	28		

Table 2-5. Occupied Cell Ranges (8/8)

(h) Dual-Port RAM (50% Cell Utilization)

Words × Bits	Soft Macro RAM	Basic Macro × Q'ty	Cell Ranges Occupied by RAM							
			Type A		Type B		Type C		Type D	
			X	Y	X	Y	X	Y	X	Y
16 × 4	R947	K247 × 1	75	13						
32 × 4	R949	K249 × 1	96	15						
64 × 4	R94B	K249 × 2	82	30	163	15				
128 × 4	R94D	K24D × 1	137	24						
256 × 4	R94F	K24D × 2	126	48	251	24				
512 × 4	R94H	K24D × 4	115	99	237	48	474	24		
16 × 8	R987	K247 × 2	59	26	118	13				
32 × 8	R989	K249 × 2	81	30	162	15				
64 × 8	R98B	K28B × 1	139	24						
128 × 8	R98D	K24D × 2	126	48	251	24				
256 × 8	R98F	K28F × 1	240	41						
64 × 10	R9AB	K2AB × 1	137	28						
128 × 10	R9AD	K2AB × 2	127	56	253	28				
16 × 16	R9C7	K247 × 4	49	55	103	26	205	13		
32 × 16	R9C9	K249 × 4	71	63	148	30	296	15		
64 × 16	R9CB	K28B × 2	129	48	258	24				
128 × 16	R9CD	K24D × 4	117	99	240	48	479	24		
256 × 16	R9CF	K28F × 2	233	82	465	41				
64 × 20	R9EB	K2AB × 2	128	56	256	28				
128 × 20	R9ED	K2AB × 4	119	115	243	56	485	28		
16 × 32	R9H7	K247 × 8	44	113	89	55	188	26	376	13
32 × 32	R9H9	K249 × 8	65	129	133	63	280	30	559	15
64 × 32	R9HB	K28B × 4	120	99	247	48	494	24		
64 × 40	R9KB	K2AB × 4	121	115	247	56	494	28		

2.1.4 Notes on mounting large-scale macros (memory)

The following points must be noted when mounting large-scale macros.

• External pin placement

• Block type used for circuits other than macros

(1) External pin placement

Place related external pins close to macros if two or more large-scale macros are mounted. If no consideration is given to pin placement, the routing of external pins may be long and routing channels wasted.

As a result, routing may not be completed. When mounting two or more large-scale macros, contact NEC Electronics for the macro placement method.

(2) Block type used for circuits other than macros

When the number of cells that can be used for logic is reduced because of large-scale macros, medium-scale macros, such as 8-bit latches, may not fit in the available space.

(3) Mountability based on power supply voltage

Megamacros and memory macros cannot be used with a power supply voltage specification of 3.3 V or 3.0 V.

2.2 Package Selection

The CMOS-N5 Series offer a variety of packages for each master. Base your package selection first on the number of I/O pins in the circuit specification.

The CMOS-N5 Series has no input-only or output-only pins. The number of I/O pins and the number of power supply pins differ depending on the master used.

See **CMOS Gate Array, Embedded Array Package (A16400E)** for details of package.

2.3 Verifying Power Consumption

Although CMOS gate arrays are of a low power consumption type, a considerable amount of power is consumed when they are operated at speeds greater than 30 MHz. The temperature of the LSI increases with the amount of power used. The reliability of the product is not guaranteed if the temperature increases beyond the maximum values specified here, therefore it is necessary to hold the power consumption of the LSI below these maximum values.

The maximum power consumption limit varies depending on the package type. To improve the allowable power consumption, special QFP packages with low thermal resistance heat spreaders are provided. Figure 2-5 shows the relationship between the QFP type and the allowable power consumption. For detailed data, see **4.3 Power Consumption**.

Figure 2-5. Allowable Power Consumption vs. QFP Type
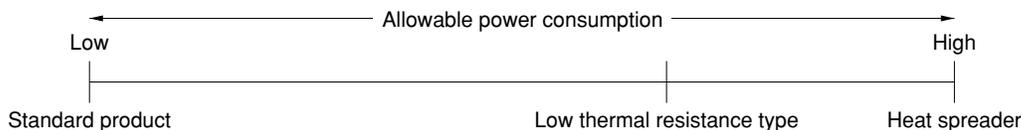
2.4 Pin Placement

The positions of the package power supply pins and NC pins are predetermined. The points noted below must be considered in determining the pin layout (pin placement).

There are cases where the power requirement will increase, <u>depending on the results of investigating items such as the number of simultaneously operating output pins.</u>

For details, see **4.6 Restrictions to Simultaneous Operation of Output Buffers**.

2.4.1 Notes on pin layout

(1) Clock pins, control (set, reset) pins

Because these pins are subject to noise, they must be placed close to ground (GND) pins.

(2) Output pins

Because output pins are subject to clock pin noise, they should be isolated as much as possible. If a large group of output pins has many simultaneously operating pins, the group should be surrounded by V_{DD} and GND pins.

(3) No connection (NC) pins

<R> Even in the case of unused pins, do not leave pins that are usable as signals unconnected, and be sure to process the following manner.

• Place an additional power supply or additional GND.

This is the rule not to leave NC pin open. So it is not necessary to connect the power supply or GND on the mounting board (it is enough to place them on LSI).

However, for a larger safety margin (simultaneous switching measure, etc.), it has naturally no problem to connect them to a power supply or GND on the mounting board.

(4) Scan path I/O pins

The placement of test pins for each package is predetermined. If scan path is used, be sure to specify scan path I/O pins for the specified pin number.

For details, see **NEC SYSTEM LSI DESIGN Design For Test User's Manual**.

(5) Placing oscillator

For details of the positions at which an oscillator can be placed, see the tables concerning pins that can be used for oscillators in **CMOS Gate Array, Embedded Array Package Design Manual (A16400E)**.

Do not place pins that may malfunction when noise is superimposed on them (such as a reset pin) in the vicinity of the oscillator.

2.5 I/O Interface

2.5.1 Input blocks

Signal Level
CMOS
TTL

Function
Buffer
Fail safe

Input Format
Normal
Schmitt trigger

Pull-Up/Pull-Down Resistor
No resistor
With 50 kΩ pull-up resistor
With 5 kΩ pull-up resistor
With 50 kΩ pull-down resistor

Signal Level
LVTTL

Function
Oscillator

Input Format
Special

There are two types of input interface blocks:

<1> CMOS level interface block

This block connects to the current CMOS LSI. Blocks with fail-safe functions are also available. A block with a fail-safe function has a protection function against over voltage. There is no continuity to the gate array power supply when the gate array power supply voltage is in the OFF state, even if a signal is applied.

<2> TTL level interface block

This block connects to the current TTL LSI. Blocks with fail-safe functions are available in this type as well.

2.5.2 Output blocks

Signal Level
CMOS

Function
Buffer
3-state
Open-drain

Output Format
Normal
Low noise

Pull-Up/Pull-Down Resistor
No resistor
With 50 kΩ pull-up resistor
With 5 kΩ pull-up resistor
With 50 kΩ pull-down resistor

Load Drive Capability I_{OL}
3.0 mA
6.0 mA
9.0 mA
12.0 mA
18.0 mA
24.0 mA

Signal Level
CMOS

Function
Oscillator

Output Format
Special

A CMOS-level interface block is available as an output interface-level block. This block connects to the current CMOS LSI, and outputs voltages of the same level as the power supply voltage. In addition, an N-ch open-drain block with a fail-safe function is also available. This block is provided with a function that protects against over voltage, ensuring there is no conduction to the power supply of the gate array even if signals are input when the power supply voltage of gate array is OFF. However, as with the current N-ch open-drain block, this block cannot be clamped with a voltage higher than that of the power supply voltage.

An oscillator and a low noise buffer for reducing noise generation are also available.

In a CMOS circuit, if an input signal is in a state whereby the level of input is unstable (floating level), excessive through current will flow, and a noise signal will be input into the circuit, resulting in malfunction. A buffer with a pull-up or pull-down resistor must be used for pins that may be open on the substrate. In the CMOS-N5 Series, 5 kΩ pull-up resistors are also available for TTL-type bus line.

2.6 Development Flow

The following figure shows the development flow of a CMOS gate array.

Flow 1: Development procedure and interfacing

NEC Electronics	User	Tools, Materials
	System planning	Pamphlets/ data sheets
1	Logic design Circuit design	Design manuals Block libraries Macro libraries
Circuit creation Logic synthesis Test pattern creation	Circuit creation Logic synthesis Test pattern creation	
Sign-off simulation	Simulation	TEG**Note**
2	Sign-off simulation	
Placement and routing		OPENCAD General-purpose EWS interface tools Interface manuals
Actual wiring simulation	Actual wiring simulation/ Simulation result check	
ES creation		
	ES evaluation	
CS creation		
	CS evaluation	
Mass production → Delivery		

1	Circuit diagram level interface	
2	Simulation level interface	• When using NEC Electronics' sign-off simulator, placement and routing is performed immediately after user confirmation. If another simulator is used, simulation will be executed again by NEC Electronics.

Note   Only when necessary.

Flow 2: Development flow

NEC Electronics   User

```
                                                    ┌─────────────────────────┐
                                                    │   Product planning      │
                                                    │ Functional specification│
                                                    └─────────────────────────┘
```

┌─────────────────────────┐
│   Logical design   │
│   (Circuit design)   │
│   (Test pattern design)│
└─────────────────────────┘

┌─────────────┐
│ Data input │
└─────────────┘

◇ Simulation results ◇ —— NG ——>

OK

┌─────────────────────────┐
│ Mask creation for routing│
└─────────────────────────┘

┌─────────────────────────┐
│ LSI prototype inspection│
└─────────────────────────┘

Evaluation sample (ES)

◇ Evaluation ◇ —— NG ——>

Specifications finalized

OK

┌─────────────────────────┐
│   LSI prototype   │
│ inspection for shipment │
└─────────────────────────┘

Mass production evaluation sample (CS)

◇ Evaluation ◇ —— NG ——>

OK

┌─────────────────┐
│ Mass production │
└─────────────────┘

Flow 3: Front-end detailed flow

```
┌─────────────────────┐        ┌─────────────────────┐
│   Circuit creation  │        │ Test pattern creation│
└─────────────────────┘        └─────────────────────┘
          │                              │
┌─────────────────────┐                  │
│  Design rule check  │                  │
│       GateDRC       │                  │
└─────────────────────┘                  ▼
          │                    ┌─────────────────────┐
┌─────────────────────┐        │  Pattern rule check │
│STA circuit configuration check  └─────────────────────┘
│     STADRC^Note     │
└─────────────────────┘
          │
          └──────┐
          ┌─────────────────────┐
          │  Delay simulation   │
          └─────────────────────┘
                  │
┌─────────────────────┐   Function verification
│        STA          │   Test pattern verification
└─────────────────────┘
          │
   Timing verification
- - - - - - - - - - - - - - - - - - - - - - - - - - - -  Interface
          ▼                       ▼
 Placement and routing          IC test
```
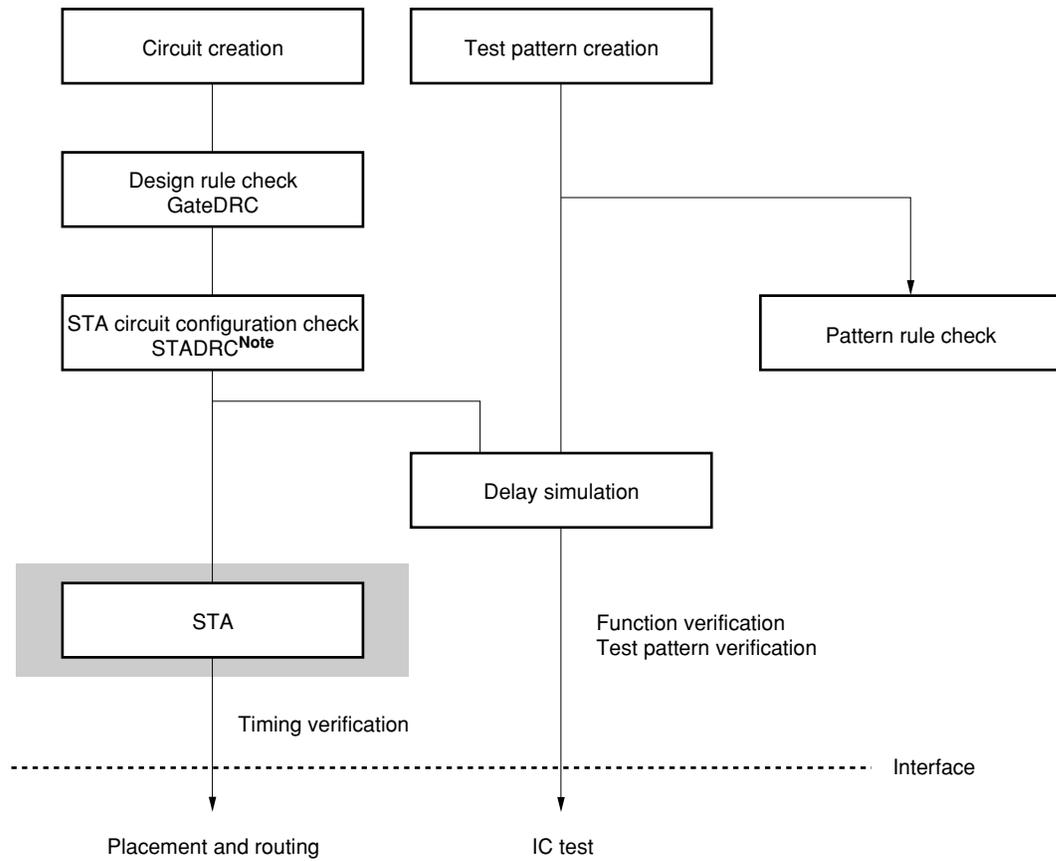
Note   STADRC is only required when sign-off performed by STA.

2.7 OPENCAD Configuration Tools

The following tools can be selected in accordance with the user environment.

Cautions 1. Refer to the user's manuals in the OPENCAD Series for the latest versions of the OPENCAD configuration tools.

2. Some functions may not be supported, so check before using OPENCAD.

Function	NEC Electronics Tools	I/F Data	Commercial Tools

Function simulator	—	• Netlist
		  PWC/
		  EDIF (2.0.0)/
		  Verilog™ HDL
		
		• Test pattern
		  ALBA
		
		• Delay data file
		
		• Constraint file
			ModelSim®/Verilog-XL™/
			NC-Verilog™/VCS™

Schematic editor	Vdraw		—
Logic synthesis	—		Design Compiler®
Gate-level simulator[Note 1]	V.sim		ModelSim/Verilog-XL/NC-Verilog/VCS
Formal verifier	—		Formality®/Tuxedo™-LEC/Conformal™-LEC
STA[Note 1]	Tiara		PrimeTime®
Fault simulator[Note 2]	C.FGRADE		—
Design for test	NEC_SCAN2/ NEC_BSCAN/NEC_BIST/ TESTBUS		DFTCompiler /TetraMAX®
Floorplanner[Note 3]	CBIC : ace_floorplan GA : Galet		—
Placement and routing[Note 3]	Galet		Silicon Ensemble™

Notes 1. Sign-off tool

2. Tool not supported in HP™ version

3. Tool supported individually

Remark Platform: Sun™ (Solaris™)/HP (HP-UX™)

GUI: X11R5/Motif™1, 2

Gate array development is a cooperative effort by the user and NEC Electronics. The user is responsible for the steps from system and circuit design through simulation. NEC Electronics is responsible for providing design information, supporting the user in designing the circuit, and the steps after simulation.

The transfer of development work from the user to NEC Electronics is called interfacing. The interface level is divided into the following two depending on what data is to be provided from the user to NEC Electronics.

(1) Circuit diagram level interface

A circuit diagram designed with 74LS or NEC Electronics' gate array blocks is submitted to NEC Electronics and NEC Electronics performs the steps after circuit simulation.

NEC Electronics will provide the user with the results of design rule checking and circuit simulation, which must be confirmed and approved by the user.

(2) Simulation level interface

The user performs circuit design and simulation work using various EWS (engineering work stations) and CAD system simulators, and NEC Electronics takes over the rest of the development work (such as automatic placement and routing and final simulation).

At either interface level, the user may consult NEC Electronics about items NEC Electronics has provided, as well as which tools are presently available.

2.8 List of Interface Data

Embedded array and cell-based IC descriptions should be disregarded when referencing this list.

Caution   There may be changes to the data depending on the edition of OPENCAD, so be sure to contact NEC Electronics before commencing design.

		File Type and Name	SIMULATOR	
			V.sim	Verilog
NETLIST		PWC (.pwc)	◎[Note 3] (t1)	◎[Note 3] (t1)
		Verilog HDL (.v)	—	◎[Note 3] (t1)
		EDIF (.edif)	◎[Note 3] (t1)	◎[Note 3] (t1)
PIN ASSIGN		DIF (.dif)	◎ (t1)	◎ (t1)
EMC Check	CB10, EA10 or later	EMC check file (.emc)	◎	◎
CROSS Talk	CB10 or later (except EA10)	pcs file (.pcs)	○	○
TEST Pattern	Without I/O modulation specification[Note 1]	ALBATROSS (.alb)	◎[Note 4] (t3)	◎[Note 6] (t3)
	With I/O modulation specification[Note 1]	ALBATROSS (.alb)[Note 2]	◎[Note 5] (t3)	◎[Note 7] (t3)
MACRO	RAM BIST	RAMPIN file (.rpi)	○	○
		BIST separation file (.bist.scn) (when used with SCAN)	○ (t1)	○ (t1)
	ROM	NINCF (.nin)	○ (t3)	○ (t3)
		ROM.cmd	○ (t3)	○ (t3)
	Mega macro	Megamacro unit test specifications	○	○
		Initial Pattern	○	○
	Digital PLL	Initial Pattern	○	○
DFT	BSCAN	SCAN+BSCAN Initial Pattern (scan.init.alb)	○	○
		SET file (.set)	○ (t1)	○ (t1)
		Circuit verification pattern (.bspat.alb)	◎	◎
		Order file (.bsorder)	○ (t1)	○ (t1)
		BSDL file (.bsdl)	○ (t1)	○ (t1)
	SCAN	User macro separation file	○ (t1)	○ (t1)
		Pin location file	○	○
Other	CRITICAL PATH	tiara command file	○ (t2)	○ (t2)
		Critical path guidelines (paper)	○ (t2)	○ (t2)
	Floorplan	Floorplan specification document (paper)	○[Note 8] (t1)	○[Note 9] (t1)
		Def file (.floorplan.def)	○[Note 8] (t1)	○[Note 9] (t1)
	CTS	CTS Check report (.rpt)	◎ (t1)	◎ (t1)

		File Type and Name	SIMULATOR							
			V.sim			Verilog				
Check result file	Netlist rule check	(.gatedrc)	◎ (t1)			◎ (t1)				
	alb check	(.ALBchk)	◎Note 10 (t3)			◎Note 11 (t3)				
	PIN check	"NO ERR" screen copy	◎ (t1)			◎ (t1)				
	SCAN check	(.scanchk)	○ (t1)			○ (t1)				
	BSCAN check	(.bscanchk)	○ (t1)			○ (t1)				
	Sim result MIN. & MAX. (fraction of pattern number)		.slg	.tpe	.iomoduchk	.log	.bus	.ovprd	.iochk	.trcpr
		DC test pattern (up to 32 K patterns)	◎Note 12	◎Note 12	◎Note 12	◎Note 15	◎Note 15	◎Note 15	◎Note 15	◎Note 15
		Function test pattern	○Note 13	○Note 13	○Note 13	○Note 16	○Note 16	○Note 16	○Note 16	○Note 16
		High-speed function test pattern	○Note 14	○Note 14	○Note 14	○Note 17	○Note 17	○Note 17	○Note 17	○Note 17
TESTACT	DFT database file	(dft_db)	○			○				
	DFT pin location file	(dft-set)	○			○				
	Test bus connection check pattern	testbus.cpt	○			○				
	BSCAN circuit verification pattern	bspat.cpt	○			○				

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Notes 1. There must be a description of I/O modulation in the timing of ALBATROSS.

2. Refers to input modulation and high-speed function test.

3 to 11. Select one for each.

12 and 14 or 15 and 17. Required if high-speed function test is requested.

12 and 13 or 15 and 16. Required if test patterns exceed 32 K.

Remarks 1. ◎: Required, ○: When necessary

2. (t1): When test run is requested (P&R → SDF)

(t2): When test run is requested ((t1) → Critical path confirmation)

(t3): When test run is requested ((t1) → Simulation)

2.9 ASIC Product Development Information

An example and the method for describing information related to ASIC product development is included here (as a checksheet).

Check (black out) the appropriate box. For items with only one box, check the box if your results agree with the statement.

Example There were no errors .... □

$\rightarrow$ Checked (blacked out) means that there were no errors.
$\rightarrow$ Unchecked (left white) means that there were errors.

Cautions 1. **Be sure to check with NEC Electronics that the ASIC product development information (checksheet) you are planning to use is the latest version. Do not use this description example for actual interfacing.**
2. **The ASIC product development information in this document includes descriptions for other series since this information is a common example for gate array products.**
3. **The ASIC product development information described here is provided to enable understanding of what kind of items should be checked, and is not intended to provide release-related information.**

2.9.1   ASIC product development information (checksheet)

1. Part number μPD6 **5944GM** – **XXX** – **JED**
2. Company **NEC Corporation**
   Department **Gate Array Development Department**   Contact details TEL **+81-3-XXXX-XXXX**
   Name of contact **N.E.C.Smith**   FAX **+81-3-XXXX-XXXX**
3. Specific information
   <1> Requested delivery date   ES: **2003** Year **6** Month **20** Day **10** Number
   <2> Application   **Personal Computer**
   <3> Interface level   Customer to distributor: **C2** , **C2** Distributor to D.C: **C2** , **C2**
   <4> Design tool to be used   Customer: **OPENCAD** Ver **5.4**   Distributor: **OPENCAD** Ver **5.4**
   <5> Hardware to be used   Customer: **SPARCstation**   Distributor: **SPARCstation**
   <6> Package   **160** pin **QFP**
   <7> Any special requirements?   ☐ No ■ Yes
   (Request No.: SBE-XXX-0001 Division Answer Date: April 15, 2003)
   In case of special request, please submit a special request form including division answer as the interface document.
   <8> Special signature   ☐ No ■ Yes
4. Interface materials

The materials required when interfacing are listed below.

<1> dif(Pin layout information)	dif file name: **top.dif**	Date: **2003** Year **4** Month **10** Day		
	Netlist file name: **top.pwc**	Date: **2003** Year **4** Month **10** Day		
<2> Netlist data	■ PWC ☐ EDIF ☐ VerilogHDL ☐ VHDL	Medium:	■ FD ☐ DAT	Format: ■ EWS
	■ ALB		☐ CGMT	☐ PC
<3> Test pattern data	–		☐ 8 mm tape	
<4> Timing file			☐ Network	
			☐ Other ( )	
<5> Design rule check results (GateDRC)		Date: **2003** Year **4** Month **10** Day		

<6> Delay simulation results, including timing check results. Be sure to submit both MIN and MAX in the result file.

■ V.sim	For V.sim, be sure to submit the pattern number fraction .slg/.tpe/.iomoduchk/.dpmodechk (when DPLL is incorporated)
☐ Verilog	For Verilog, be sure to submit the pattern number fraction verilog.log/.bus/.ovprd/.tpe/.iomoduchk/.dpmodechk (when DPLL is incorporated)
☐ Model-S	For Model-S, be sure to submit the pattern number fraction .*_report/.bus*/.dop/.tpe/.iomoduchk/.dpmodechk (when DPLL is incorporated)
☐ VCS	For VCS, be sure to submit the pattern number fraction .vcs.log/.bus/.ovprd/.tpe/.iomoduchk/.dpmodechk (when DPLL is incorporated)

<7> Simulation result check document (before placement and routing)	Date: **2003** Year **4** Month **10** Day
<8> Command file (When path analysis is required)	Date: **2003** Year **4** Month **10** Day
Tool used: **Tiara**	–
File name: **top.scr**	
<9> Name of net from clock input pin to CTS block (there is an adjacent placement prohibition specification, so only required for CMOS-10HD)	Net name: Or file name: **NET0001 or CTS.NET**

NEC Electronics distributor[Note]   NEC Electronics sales department[Note]

Distributor: **Distributor, Ltd.**   Sales department: **1st Sales Dept.**
Name of contact: **D.Smith**   Name of contact: **S.D.Smith**
TEL: **+81-3-XXXX-XXXX**   TEL: **+81-3-XXXX-XXXX**
FAX: **+81-3-XXXX-XXXX**   FAX: **+81-3-XXXX-XXXX**

Note   The names of the NEC Electronics distributor and sales department must be include

1. Enter the product name.
2. Enter the company, department, name of contact, and contact details.

3. Enter the following information.
    <1> Requested ES delivery date and number of samples
    <2> Application
    <3> Interface level.
    <4> Design tool to be used and its version
    <5> Hardware to be used
    <6> Package pin count and type
    <7> Select either the [Yes] or [No] check box for special request, and if [Yes] is selected, enter the request number and the division answer date.

    <8> Whether there is a special signature
4. Enter the file name and date for the following materials which are to be submitted when interfacing.
    Resubmit these materials whenever data is modified.
    <1> Enter the dif file name and creation date.
    <2> Enter the netlist data file name, data type, medium, format, and the creation date.
    <3> Since the only test pattern data type is ALB, nothing need be entered for this item.
    <4> There is no timing file, so this is not applicable (this information is included in ALB).
    <5> Enter the date that GateDRC was executed with the final netlist data.
    <6> Indicate the simulator type.
    <7> Enter the date the simulation result check document was created.
    <8> If performing path analysis, enter the analysis tool name, script file name, and script file creation date.
    <9> Name of net from clock input pin to CTS block or file name. This is required as there is an adjacent placement prohibition specification in CMOS-10HD.

    Remark   Enter the file name for <3> in the table under (b) Test pattern information in (23) Test pattern. For C3, confirm the necessary files later.

Enter the name of the NEC Electronics distributor and NEC Electronics sales department.

5. Product details (C2-level form)

Please fill out the following. This data will be used for designing LSIs and creating delivery specifications.

Note   If this item is satisfied, check the box. For any boxes left unchecked, please write proposed countermeasures.

(1) Are there any additional power supplies? .... ■ YES   ☐ NO

Additional V_{DD} __**1**__ Additional GND __**2**__ Additional $V_{D(D)5}$ __**3**__   (for other than CMOS-10HD)

Additional V_{D1} __**1**__   Additional V_{D2} __**0**__   Additional GND __**2**__   (for CMOS-10HD)

(2) Is there an oscillator block? .... ■ YES   ☐ NO

Block name: __**OS11, OS07, F093**__   Frequency: __**20**__ MHz

Oscillation input pin   (__**CIN**__)   Pin No. (__**110**__)

Oscillation output pin   (__**CEN**__)   Pin No. (__**112**__)

Oscillation enable input pin   (__**COUT**__)   Pin No. (__**111**__)

• If there is an oscillator block, an oscillation stop function is included .... ■

In the case of YES, for all user patterns, do not make the oscillation input signal the RZ signal and do not set the expected value "X" (undefined) for the oscillation output signal; fix the input of the stop control pin to 0.

(3) Conditions

(a) Simulation

☐ cmos_1.8 V ■ cmos_2.5 V ☐ cmos_3 V ☐ cmos_3.3 V ☐ cmos_5 V ☐ ttl_3.3 V ☐ ttl_5 V

(b) Electrical specifications

T_A ■ −40 to 85°C   ☐ 0 to 70°C   ☐ Other ( )

V_{DD} ■ 1.8 V ±0.15 V ☐ 3.3 V ±0.3 V ☐ 3.3 V ±0.165 V ☐ 5 V ±10% ☐ 5 V ±5% ☐ Other ( )

(4) Operating frequency

Input fmax.

Pin namae __**CLKIN**__   fmax. __**66**__ MHz   Duty __**50**__ ± __**10**__ %

Output fmax.

Pin name __**DAT (15:0)**__   fmax. __**33**__ MHz   Output load capacitance __**50**__ pF

Output minimum pulse width

Pin name __**DAT (15:0)**__   Pulse width __**15.2**__ ns   Output load capacitance __**50**__ pF

Direction ■ POS   ■ NEG

• Output buffer external load capacitance is within the recommended range**Note** .... ■

(5) Simultaneous operation

■ 3 GND pin determination method

☐ Total chip level determination method ☐ Simple determination method ☐ Detailed determination method

• According to the determination results, simultaneous operation was satisfied**Note** .... ■

(6) Power consumption

Calculation result Total power: __**523**__ mW Maximum allowable power consumption: __**680**__ mW

• The power consumption is within the allowable range**Note** .... ■

• When executing a detailed calculation (P_{WL}), calculation is made with T_J = 125 for T_A = −40°C to 85°C or T_J = 100 for T_A = 0°C to 75°C (($125 - T_{A(MAX)} \div \theta_{ja}$) or ($100 - T_{A(MAX)} \div \theta_{ja}$), $T_{A(MAX)} \geq 40°C$) .... ■

(Please answer when implementing detailed calculation (P_{WL}).)

(7) X-propagation simulation was performed**Note** .... ■

(8) There were no CTS Check result errors (for CTS-mounted products only)**Note** .... ■   ☐ No CTS

When CTS and a digital PLL are incorporated, submit the .rpt file.

• Are there no more than 4 CTS systems? (CMOS-10HD only. Excluding CTS for SCAN) .. ■

If there are more, contact NEC Electronics (submit a special request).

(9) There were no timing errors .... ■

Make checks based on the simulation result check document. If the X-propagation simulation item checkbox was unchecked, simulation will be performed with no effect on the output pins even if a timing error occurs, so be sure to execute simulation. If there is a timing error, it will be necessary to modify the circuits and the test pattern to avoid the output of such an error.

Note that although it is possible to accept only pseudo-errors, whose contents do not affect the output, it is anticipated that test bugs may be caused by check omissions. Bear in mind that in such cases, NEC Electronics may require users to investigate the origin of these bugs.

5. Enter the following information.

(1) Indicate whether there are any additional power supplies, and if YES, the number of additional V_{DD} or GND pins. The category is divided into either CMOS-10HD and other than CMOS-10HD. Please enter the answer in the correct category.

(2) Indicate whether there is an oscillator block, and if YES, the name, frequency, and input/output/enable pin names and numbers. In the case of YES, also indicate whether an oscillation stop function is included. For all user patterns, do not make the oscillation input signal the RZ signal and do not set the expected value "X" (undefined) for the oscillation output signal. Fix the input of the stop control pin to 0.

(3) Indicate the type of simulation, T_A (temperature range), and V_{DD} (supply voltage range).

(4) Enter the operating frequency.
    Input fmax.
        Enter the name of the pin at which the maximum operating frequency is input, the frequency, and the duty ratio.
    Output fmax.
        Enter the name of the pin at which the maximum operating frequency is output, the frequency, and the load capacitance.
    Output minimum pulse width
        Enter the name of the pin at which the maximum operating frequency is output, the minimum pulse width, and the load capacitance, and indicate whether the minimum pulse width is POS or NEG.
    • Check and indicate whether the output buffer external load capacitance is within the recommended range. The following restrictions apply for the maximum operating frequency.
        CMOS-10HD: 66 MHz (1.8 V), 133 MHz (2.5 V)
        CMOS-9HD, EA-9HD: 100 MHz
        CMOS-N5:   60 MHz (5 V), 33 MHz (3.3 V) , 25 MHz (3 V)
        Other series: fmax. of output buffer

(5) Check and indicate which determination method: 3 GND pin determination or total chip level simple determination/ detailed determination was used for simultaneous operation.
    Check and indicate whether simultaneous operation is satisfied according to the determination results. If it is not satisfied, list countermeasures.

(6) Calculate the power consumption using the design manual and enter the result. Also enter the maximum allowable power consumption of the package, based on the design manual, and indicate whether it is within the allowable range. If it is out of range, list countermeasures.
    For a detailed calculation, execute the calculation with the T_J value corresponding to T_A.
    $T_A = -40°C$ to $85°C$ $P_{WL} = 125 - T_{A(MAX)} \div \theta_{ja}$ Condition: $T_{A\,(MAX.)} \geq 40°C$
    $T_A = 0°C$ to $75°C$ $P_{WL} = (100 - T_{A(MAX)} \div \theta_{ja})$ Condition: $T_{A\,(MAX.)} \geq 40°C$

(7) Indicate whether X-propagation simulation was performed when executing simulation. Note that X-propagation simulation must be performed. If it was not performed, give reasons.

(8) For CTS-incorporated products, execute CTS Check and describe the confirmed results.
    • For CMOS-10HD, check that there are no more than 4 CTS systems (excluding CTS for SCAN).

(9) Based on the simulation result check document, indicate whether there were any timing errors.

(10) When bidirectional pins are used, there is no circuit designed in such a way that these signals enter the clock directly after the signals are re-input internally via a bidirectional pin input buffer in output mode
.... ☐　☐ No bidirectional pin

If this kind of circuit configuration exists, depending on the ringing, the internal circuit that receives these input signals may malfunction, causing testing problems. This is especially the case if these input signals directly enter the clock, so users are advised to take countermeasures in line with the specifications in the design manual.

- If this box is unchecked, countermeasures must be taken, and these measures must be checked and approved by NEC Electronics via a special request, etc.

(11) For CMOS-6, 6A, 6S, 6V, 6X, 8:
Is a TTL18 mA type output buffer used?
For CMOS-8L, 5 V interface:
Is an 18 mA, 24 mA type output buffer used [2-cell configuration]? ....☐ NO　■ YES
(12) Is there a RAM block? ....☐ NO　■ YES
- In the case of YES, please fill out **2.9.2 RAM block**.
(13) Is there a ROM block? ....☐ NO　■ YES
- In the case of YES, please fill out **2.9.3 ROM**.
(14) Is there a high-speed function test? ....☐ NO　■ YES
- In the case of YES, please fill out **2.9.4 High-speed function test**.
(15) Is there a GTL, PECL, HSTL, PCI, or LVDS block? ....☐ NO　■ YES
- In the case of YES, please fill out **2.9.5 GTL, PECL, HSTL, PCI, LVDS block**.
(16) Is there a digital PLL? ....☐ NO　■ YES
- In the case of YES, please fill out **2.9.6 DPLL block**.
(17) Is there a megamacro? ....☐ NO　■ YES
- In the case of YES, please fill out **2.9.7 Megamacro**.
(18) Use for both scan path and boundary scan ....☐ NO　■ YES
- In the case of YES, enter information regarding **2.9.8 Alternate use as scan path and boundary scan.**
(19) Is a scan path (SCAN) used? ....☐ NO　■ YES
- In the case of YES, please fill out **2.9.9 Scan path**. However, during alternate use as BSCAN, nothing need be entered.
(20) Is a boundary scan (BSCAN) used? ....☐ NO　■ YES
- In the case of YES, please fill out **2.9.10 Boundary scan**. However, during alternate use as SCAN, nothing need be entered.
(21) For EA-9HD, is a bus folder (F098) used for all internal 3-state output pins? ....☐ YES　■ NO
- In the case of NO, did you check beforehand with the person in charge of the EA-9HD Series in NEC Electronics whether the bus floating prevention circuit is properly configured and received OK? ....■
(22) Is an internal 3-state output block used (except EA-9HD)? ....☐ NO　■ YES
- In the case of YES, it has been confirmed that the bus floating prevention circuit has the correct configuration ....■

(10) Based on the design manual, confirm that there is no such circuit configuration.
If there is such a circuit configuration, the fact that countermeasures have been taken in line with the measures recommended in the design manual must be checked and approval given by NEC Electronics via a special request, etc., before interfacing.

(11) Indicate whether there is an output buffer with a 2-cell configuration.

(12) Indicate whether there is a RAM block.

(13) Indicate whether there is a ROM block.

(14) Indicate whether there is a high-speed function test.

(15) Indicate whether there is a GTL, PECL, HSTL, PCI, or LVDS block.

(16) Indicate whether there is a digital PLL.

(17) Indicate whether there is a megamacro.

(18) Select whether or not alternate use for both scan path and boundary scan.

(19) Indicate whether a scan path (SCAN) is used.

(20) Indicate whether a boundary scan (BSACN) is used.

(21) Indicate whether a bus folder (F098) is used (EA-9HD only).
In the case of YES, confirm that a bus folder (F098) is used for all internal 3-state output pins.
If [NO] is selected, check beforehand with the person in charge of the EA-9HD Series in NEC Electronics whether the bus floating prevention circuit is properly configured and receive OK.
(22) Indicate whether there is an internal 3-state output block (for other than EA-9HD).
In the case of YES, confirm that the bus floating prevention circuit has the correct configuration.
If the prevention circuit does not have the correct configuration, through current I_{DD} becomes abnormal when selecting the tester.
Be careful because this problem cannot be detected by the tool.

Note that because (11) to (20) in the page indicated on the left are examples, YES has been marked for all entries.

(23) Test pattern:

(a) The following restrictions have been satisfied[Note 1] .... ■

[CMOS-N5, 9HD, 10HD, EA]
[CMOS-8L] (OPENCAD V5.4 or earlier)
[CMOS-6, 6A, 6S, 6V, 6X, 8, 9] (OPENCAD V5.3 or earlier)

Number of Pins	Minimum Number of Test Patterns Per Pin (Patterns for DC Measurement Only)	Total Number of Test Patterns
Less than 145 pins	150 patterns	128 K patterns (with SCAN)[Note 2] 256 K patterns (without SCAN)[Note 2]
145 pins or more		512 K patterns[Note 2]

Notes 1. If this item is satisfied, check the box. For any boxes left unchecked, please write proposed countermeasures.

2. The number of DC patterns is 32K max. for all, except for 257 or more pins of EA-9HD.
If the DC pattern exceeds 32K, the patterns for DC measurement are up to 32K.
Therefore, create patterns so that DC measurement can be detected within 32K insofar as possible.
The pattern submitted to NEC Electronics can also be a single pattern exceeding 32K.

Example:
In the case of a 56K DC pattern, the pattern for DC measurement is 1 to 32K. Therefore, even if there are signal changes for 32001-56K, this is not reflected to DC measurement.
Patterns after 32K are handled as LFT (same as 1 to 56K LFT pattern).

In the case of 257 or more pins in EA-9HD, the number of DC patterns is 64K max.
If the DC patterns exceed 64K, the patterns for DC measurement are up to 64K.
Therefore, create patterns so that DC measurement can be detected within 64K insofar as possible.
The pattern submitted to NEC Electronics can also be a single pattern exceeding 64K.
Moreover, the number of patterns for (each) high-speed function test is 32K max. regardless of the series and pin count.

(23) Enter the following information about the test patterns.

(a) Indicate that the restrictions regarding the number of test patterns have been satisfied. If they are not, check with NEC Electronics as the tester restrictions may be unsupportable.

The restriction on the minimum number of test patterns per pin only applies to patterns for DC measurement.

Remark The number of DC patterns is a single pattern of 32K max., except for 257 or more pins of EA-9HD. If the DC pattern exceeds 32K, the pattern check is up to 32K.
Therefore, create patterns so that DC measurement can be detected within 32K insofar as possible.
The pattern submitted to NEC Electronics can also be a single pattern exceeding 32K.

Example
In the case of a 56K DC pattern, the pattern for DC measurement is 1 to 32K. Therefore, even if there are signal changes for 32001-56K, this is not reflected to DC measurement.
Patterns after 32K are handled as LFT (same as 1 to 56K LFT pattern).

In the case of 257 or more pins in EA-9HD, the number of DC patterns is a single one of 64K max.
If the DC patterns exceed 64K, pattern check is up to 64K.
Therefore, create patterns so that DC measurement can be detected within 64K insofar as possible.
The pattern submitted to NEC Electronics can also be a single pattern exceeding 64K.
Moreover, the number of patterns for (each) high-speed function test is 32K max. regardless of the series and pin count.

Pattern check up to OPENCAD V5.3 and patter check from OPENCAD V.5.4 or later differ.

Up to OPENCAD V5.3	LOGPAT	cptchk
	ALB	cptchk, albchk
From OPENCAD V5.4 or later	ALB only	albchk

(b) Test pattern information

<1> Please enter test pattern information in the following table (for OPENCAD V5.3 or earlier).

Test Pattern Data File Name	Timing Data File Name	Number of Patterns	Pattern Period(T) Strobe Position(ST)	Check One						
				DC	LFT	High-Speed[Note 2]	BSCAN [Note 3]	DPLL [Note 4]	Mega-macro[Note 4]	SCAN [Note 4]
DC.nlp	**DC.alb**	**20,000**	T = **200 ns** ST = **199.99 ns**	√[Note 1]						
LFT1.nlp	**LFT.alb**	**10,000**	T = ST =		√					
LFT2.nlp	**LFT.alb**	**10,000**	T = ST =		√					
FCT.nlp	**FCT.alb**	**20,000**	T = **300.00 ns** ST = **299.99 ns**		√					
			T = ST =							
			T = ST =							
			T = ST =							
			T = ST =							
			T = ST =							
			T = ST =							

Notes 1. Input the DC pattern in this column. In case of alternate use with LFT pattern, √ marks in LFT column are not required. If the pattern period is not 200 ns, enter the pattern period and reason for change below:

Pattern period:____**300**____ ns   Reason for change: **Because the MAX delay is 280 ns**

2. Check the High-Speed column for high-speed function test patterns.

3. Set the BSCAN pattern period to 300 ns or more.

4. Check these columns for the setting pattern and initialization pattern.

Remarks 1. The number of patterns is DC + LFT + High-Speed + BSCAN + DPLL + Megamacro, totaling no more than 20.

2. For the ALBATROSS interface, enter the ALBATROSS file name under File Name in the Test Pattern Data column. If there is an I/O modulation specification, enter the strobe file name for the timing data file name. Place a dash in this column if there is no I/O modulation specification.

(b) Test pattern information

<1> Enter test pattern information as shown below (for OPENCAD V5.3 or earlier)

Enter the file name and number of patterns for all test pattern data, and check the column corresponding to the pattern data type.

If the pattern period and strobe position are other than 200 ns and 199.99 ns, respectively, enter the actual values.

If there is an I/O timing specification, also enter the name of the timing data file. Place a dash ("-") if there is no I/O timing specification.

Be sure to enter the DC pattern in the first row, and if its pattern period is not 200 ns, enter the pattern period and the reason for the change in the column indicated by Note 1.

For the ALBATROSS interface, enter the ALBATROSS file name for the test pattern data file name, and enter "-" in the Timing Data File Name column because the timing data is not necessary when I/O modulation is not specified. Note that the number of patterns, i.e. DC + LFT + high-speed function test + BSCAN + DPLL, is 20 max., including mega macro initialization patterns. Regarding the mega macro initialization patterns, timing specification is prohibited, so enter "-" In the timing data file name column.

Resubmit this information whenever data is modified.

<2> Please enter test pattern information in the following table (for OPENCAD V5.4 or later).

Test Pattern Data File Name	Number of Patterns	Pattern Period(T) Strobe Position(ST)	DC	LFT	High-Speed[Note 2]	BSCAN [Note 3]	DPLL [Note 4]	Mega-macro[Note 4]	SCAN[Note 4]
DC.nlp	**20,000**	T = **200 ns** ST = **199.99 ns**	√[Note 1]						
LFT1.nlp	**10,000**	T = ST =		√					
LFT2.nlp	**10,000**	T = ST =		√					
FCT.nlp	**20,000**	T = **300.00 ns** ST = **299.99 ns**		√					
		T = ST =							
		T = ST =							
		T = ST =							
		T = ST =							
		T = ST =							
		T = ST =							

Notes 1. Input the DC pattern in this column. In case of alternate use with LFT pattern, √ marks in LFT column are not required. If the pattern period is not 200 ns, enter the pattern period and reason for change below:

Pattern period: ___**300**___ ns   Reason for change: **Because the MAX delay is 280 ns**

2. Check the High-Speed column for high-speed function test patterns.

3. Set the BSCAN pattern period to 300 ns or more.

4. Check these columns for the setting pattern and initialization pattern.

Remark The number of patterns is DC + LFT + High-Speed + BSCAN + DPLL + Megamacro, totaling no more than 20.

<2> Enter test pattern information as shown below (for OPENCAD V5.4 or later)

Enter the file name and number of patterns for all test pattern data, and check the column corresponding to the pattern data type.

If the pattern period and strobe position are other than 200 ns and 199.99 ns, respectively, enter the actual values.

Be sure to enter the DC pattern in the first row, and if its pattern period is not 200 ns, enter the pattern period and the reason for the change in the column indicated by Note 1.

Note that the number of patterns, i.e. DC + LFT + high-speed function test + BSCAN + DPLL, is 20 max., including mega macro initialization patterns.

Resubmit this information whenever data is modified.

(c) and (24) to (27) below are for OPENCAD V5.3 or earlier, and (28) and (29) are for OPENCAD V5.4 or later.

(c) Is there a timing specification? .... ■
If there isn't, <1> to <6> below do not need to be checked.
<1> The specified number of timing phases is 6 or less, including the basic timing**Note** .... ■
<2> The timing variation (time difference at the change point) of each phase is 10 ns
or more**Note** .... ■
<3> The I/O switching of the bidirectional buffer is performed at the basic timing
(Not applicable when I/O modulation is used)**Note** .... ■
<4> There is no contention when the time change is identical for each timing phase**Note** .... ■
<5> When there is an RZ signal specification, the clock is not output directly to
external pins**Note** .... ■
<6> When there is an RZ signal specification, there are no parts in which I/O switching of the
bidirectional buffer is performed by this signal
(Not applicable when I/O modulation is used)**Note** .... ■

(24) There are no errors in CPTchk**Note** .... ■

Bear in mind that because the tester cannot measure the level of pins at which an "HL" or "input change" error occurs in the DC pattern, defective products may be mixed in the samples at shipment. However, the above messages do not apply for the test pins of NEC Electronics that are not used alternately as user pins.
For the Verilog products, be sure to correct the "Hi-Z input" error to either "1" or "0".

(25) For the ALBATROSS interface,

(a) albchk was executed**Note** .... ■
If the above is checked, there were no errors in the albchk execution**Note** .... ■
Be sure to provide the pattern number fraction .albchk file.

Bear in mind that because the tester cannot measure the level of pins at which an "Value (/Transition) is not appeared" or "Don't care PIN exist" occurs in the DC pattern, defective products may be mixed in the samples at shipment. However, the above messages do not apply for the test pins of NEC Electronics that are not used alternately as user pins.

(26) When I/O modulation is specified

(a) It is confirmed that I/O modulation is not specified for 2 phases or more**Note** .... ■
(b) There were no errors in the I/O modulation check**Note** .... ■
(c) "*ALBATROSS TOP cell name ver4.0 ;" was described in the start line of the strobe
ALBA file **Note** .... ■
Be sure to provide the strobe ALBA file.
(d) When clock or modulation is specified, it is reflected in the strobe ALBA**Note** .... ■
Be sure to provide the pattern number fraction .iomoduchk file.

(27) When DPLL is incorporated
There were no errors in the DPLL mode check**Note** .... ■
Please submit the file .dpmodechk, which contains all the patterns to be interfaced, to NEC Electronics.
Patterns output by Create DPLL Connection Pattern used for checking the connection of a DPLL do not have to be checked. However, be sure to check whether the initialization pattern input when the pattern for checking the connection of a DPLL is created has an error or not.

Note   If this item is satisfied, check the box. For any boxes left unchecked, please write proposed
countermeasures.

(c) If there is a timing specification, indicate whether the number of timing phases is 6 or fewer, including the basic timing, whether the timing variation of each phase is at least 10 ns, whether the bidirectional buffer I/O switching is carried out at the basic timing, and whether there is conflict when the time change is identical for each timing phase.
<1> to <6> must all be checked. If I/O modulation is used, <3> and <6> are not applicable.

(24) Indicate whether there are any errors in CPTchk, referring to the CPTchk execution results. If there are errors, correct them in line with the contents of the box at the bottom of the page.

(25) For the ALBATROSS interface, indicate whether albchk was executed, and if it is executed, whether any errors occurred. **If it is not executed, list the reasons why it is not necessary to execute.**

(26) When an I/O modulation is specified, check items (a), (b), (c), and (d). Moreover, these boxes must all be filled in.

(27) When a DPLL is incorporated, check that there are no errors in the DPLL mode check of Simulation.
If the box is left unchecked, list the reasons why the error(s) will cause no problem.

(28) ALBATROSS

(a) ALBA was created using Create Interface ALBA File of Pattern Utilities**Note** .... ■
   • If so, It is confirmed that there are no problems with the test type of the created ALBA**Note** .... ■
     Test type = DC only for DC measurement patterns.
(b) Is there an I/O modulation specification? [Must indicate] .... ■
   If there is, check <1> to <3> below.
   <1> It is confirmed that I/O modulation is not specified for 2 phases or more**Note** .... ■
   <2> The IO_MODULATION ALBA file was input when creating
       "create interface ALBA" **Note** .... ■
   <3> When clock or modulation is specified, it is reflected in the IO_MODULATION ALBA **Note** ... ■

(c) albchk was executed**Note** .... ■
   If the above box is filled in, there were no errors in the albchk execution**Note** .... ■
   Be sure to provide the pattern number fraction .albchk file.

Bear in mind that because the tester cannot measure the level of pins at which an "Value (/Transition) is not appeared" or "Don't care PIN exist" occurs in the DC pattern, defective products may be mixed in the samples at shipment. However, the above messages do not apply for the test pins of NEC Electronics that are not used alternately as user pins.

(d) Was an I/O modulation check executed?**Note** .... ■
   Required for I/O contention error even if I/O modulation is not specified.
   If the above is checked, there were no errors in the I/O modulation check execution .... ■
   Be sure to provide the pattern number fraction .iomoduchk file.

   Were any errors that occurred control modulation errors, and the circuit configuration not a
   configuration such as PCI?**Note** .... ■

Unless circuit configuration is a configuration such as PCI, control modulation errors are handled as pseudo errors in OPENCAD V5.4.1 or later.

(29) When DPLL is incorporated
   There were no errors in the DPLL mode check**Note** .... ■
   Please submit the file .dpmodechk, which contains all the patterns to be interfaced, to NEC Electronics. Patterns output by Create DPLL Connection Pattern used for checking the connection of a DPLL do not have to be checked. However, be sure to check whether the initialization pattern input when the pattern for checking the connection of a DPLL is created has an error or not.

   Note   If this item is satisfied, check the box. For any boxes left unchecked, please write proposed
             countermeasures.

(28) ALBATROSS

Check that ALBA was created using the Create Interface ALBA File function of Pattern Utilities. Patterns not created using this function cannot be interfaced.

Moreover, check if there is no test type problem. Test type = DC only for DC measurement patterns.

Indicate whether albchk was executed, and if it is executed, whether any errors occurred. **If it is not executed, list the reasons why it is not necessary to execute.**

Indicate whether the I/O modulation check was executed, and if it was, check and indicate that there were no errors.

Unless the circuit configuration is a configuration such as PCI, control modulation errors are handled as pseudo errors.

Check that all errors were control modulation errors and that the circuit configuration is not a configuration such as PCI.

(29) When a DPLL is incorporated, check that there are no errors in the DPLL mode check of Simulation. **If the box is left unchecked, list the reasons why the error(s) will cause no problem.**

2.9.2   RAM block

(1) About the RAM block

(a) Blocks used

Block Type (Function)	Number of Bits	Number of Words	Number of Blocks Used
RJ8F	**8**	**256**	**1**
RJ8H	**8**	**512**	**1**

(b) Compiled RAM is used .... ■
(c) If compiled RAM is used, there are an even number of words**Note** .... ■
(d) All RAMs used are RAM with BIST (use of basic RAM only is prohibited)**Note** .... ■
(e) The TE pin is directly accessed without inverting the logic from an external pin in the
case of G/A and connected to TEB via an inverter in the case of EA**Note** .... ■
(f)   In test mode (TE = L), the TIN and TOUT pins are directly accessed without inverting
the logic from external pins**Note** .... ■
(g) There is a test output pin (TOUT) provided for each of the RAMs used**Note** .... ■
(h) If multiple RAMs are used, the TE and TIN pins are common to all the RAMs**Note** .... ■
(i)   There are no patterns that access non-existent addresses**Note** .... ■
(This does not apply to cell-based type high-density synchronous compiled RAM)
(j)   TE/TEB of RAM for all test pattern data is not in test mode**Note** .... ■
(k) A high impedance prevention circuit for normal mode is included**Note** .... ■
If it is not included, be sure to include a prevention circuit, otherwise the tester may
malfunction due to current flow, which may adversely affect shipping (embedded array only).
(l)   The instance names of the metalization wafer and base wafer are the same .... ■
If they are not the same, submit the instance correspondence of the upper and base wafers
(embedded array only).
(m) Enter the names of the RAM test pins.
TE/TEB (1 pin)   **TENB**
TIN (1 pin)   **TESTI**
TOUT (number of RAMs used)   **TOUT0, TOUT1**
(n) There were no mismatches in the RAM check results**Note** .... ■

All the boxes from (c) to (n) should be checked. Be aware that if one or more of these items are not checked, you may be requested to modify the circuitry at the test program creation stage (final development stage).

(o) Interface data
Submit the .rpi file in addition to normal interface data.

Note   If this item is satisfied, check the box. For any boxes left unchecked, please write proposed
countermeasures.

(1) Enter the following information about the RAM block.

(a) Enter the RAM block type name, as well as the number of bits, number of words, and number of RAM blocks used.

(b) Indicate whether compiled RAM is used.

(c) Odd words are prohibited, so indicate that there is an even number of words.

(d) Check and indicate that all RAMs used are RAM with BIST.
Change to RAM with BIST because the use of basic RAM only is prohibited.

(e) Because the TE (TEB) pin must be directly accessed without inverting the logic from an external pin and connected via an inverter in the case of the EA-9, 9HD Series, indicate that this is the case.

(f) In test mode (TE = L), because the TIN and TOUT pins must be directly accessed without inverting the logic from external pins, indicate that this is the case.

(g) Because a test output pin (TOUT) must be provided for each of the RAMs used, indicate that this is the case.

(h) If multiple RAMs are used, because the TE and TIN pins must be common to all the RAMs, indicate that this is the case.

(i) In the EA-9, 9HD Series, because there can be no patterns that access non-existent addresses, indicate that this kind of pattern does not exist.

(j) Check whether TE/TEB is not in test mode for all patterns and mark accordingly.

(k) Check and indicate whether a high-impedance prevention circuit for normal mode is included. If it is not included, be sure to include a prevention circuit, otherwise the tester may malfunction due to current flow, which may adversely affect shipping (embedded array only).

(l) Check and indicate that instance names of metalization wafer and base wafer are the same.
If they are not the same, submit the instance correspondence of the upper and base wafers (embedded array only).

(m) Enter the names of the RAM test pins (TE, TIN, TOUT). (Enter one pin for TE and TIN. Because the TOUT pin cannot be shared in a gate array, enter one pin per RAM used.)

(n) Execute the RAM check and check and indicate that there were no mismatches in the result.

(2) RAM initialization pattern (pattern for RAM single-unit test)

If there were no mismatches in the RAM check results, you do not need to fill out (a) to (e).

(a) If signals pass between the test pins and RAM block via an internal gate, the logic of this internal gate is set to the RAM's test mode in the final pattern of the user-generated test pattern (Note that signals cannot pass through a sequential circuit.)**Note** .... ■

(b) If there are bidirectional or 3-state pins (this includes all bidirectional and 3-state pins), enable is secured for these pins in the final pattern of the user-generated test pattern**Note** .... ■

- If any bidirectional or 3-state pins are being used as test pins, set the TE and TIN pins to input mode (EN = L) and the TOUT pin to output mode (EN = H) in the initialization pattern.

(c) If there is an internal bus in the LSI (this includes all in-circuit internal buses), that bus is neither shorted nor in a floating state in the final pattern of the user-generated test pattern**Note** .... ■

(d) If there is a sequential circuit in the LSI (this includes all in-circuit sequential circuits), the output of that sequential circuit is stable in the final pattern of the user-generated test pattern**Note** .... ■

Remark Regarding (d), the output should be stable so as to stabilize the LSI's internal status and improve the accuracy of the RAM test.

> If any of (a) to (d) above were not checked, an initialization pattern will be required for that item.

(e) Is an initialization pattern required for any of the above items? .... ■ YES   □ NO

- In the case of YES, please enter the following information.

<1> Neither "X" nor "Z" has been entered for the input**Note** .... ■
<2> The expected output value is "don't care" **Note** .... ■
<3> Initialization pattern range _____**19,990**_____ Pattern to _____**20,000**_____ Pattern

Note If this item is satisfied, check the box. For any boxes left unchecked, please write proposed countermeasures.

(2) Enter the following information about the RAM initialization pattern (pattern for RAM single-unit test)

(a) The tester automatically inserts the RAM test pattern behind the DC pattern. Therefore, if signals pass between the RAM test pins and RAM block via an internal gate, because the logic of this internal gate must be set to the RAM's test mode, indicate that this is the case (for the RAM test mode pattern, refer to the design manual).

(b) If there are bidirectional or 3-state pins, because these pins' enable must be secured in the final test pattern of the DC pattern, indicate that this is the case.

(c) If there is an internal bus in the LSI, because bus short or floating states must be suppressed, indicate that the bus is neither shorted nor floating.

(d) If there is a sequential circuit in the LSI, because the RAM test may not be performed normally, indicate that the output of that sequential circuit is stable in the final pattern of the DC pattern.

(e) Indicate whether an initialization pattern is required for any of items (a) to (d). If YES, enter the following information (<1> to <3> below).
(If any of items (a) to (d) were not satisfied, then an initialization pattern is required.)

<1> If either X or Z is input for the RAM initialization pattern input, because a stable test may not be able to be performed, indicate that X or Z has not been input.

<2> Indicate that the status in the RAM initialization pattern is "don't care" (mask status). This must be satisfied, because if the initialization pattern is not masked, the test may be defective.

<3> Because the RAM initialization pattern must be added to the end of the DC pattern, check that this is the case, and enter the pattern range of the RAM initialization pattern (this is not the pattern for checking connection (8 patterns)).

2.9.3   ROM

(1)   Blocks used

Block Name (Instance Name)	Block Type (Function)	NINCF File
C$0010020	**J14F**	**NINCF0**
C$0020030	**J14H**	**NINCF1**

(2)   Interface data

Submit the .nincf file in addition to normal interface data.

Enter the following information about the ROM block.

(1)   The name (instance name) and type (function name) of the ROM block being used, and the name of the NINCF file corresponding to that block.

Remark   Note that in cases when there are multiple ROM blocks of the same type, if the name (instance name) and type (function name) of the ROM block is erroneous, the ROM code merge will not be executed correctly.

2.9.4　High-speed function test

(1)　Pattern for high-speed function test

　　(a)　The following conditions are all satisfied[Note 1] .... ■
　　　　<1>　The initialization pattern has been entered[Note 1] .... ■
　　　　<2>　The test rate (T) is as follows: $T \geq 50$ ns[Note 1] .... ■
　　　　<3>　There is a strobe at one point only[Note 1] .... ■
　　　　<4>　The following equation is true: 15 ns $\leq$ Strobe time $\leq T - 10$ ns[Note 1] .... ■
　　　　<5>　The specified number of timing phases is 6 or less, including the basic timing[Note 1] .... ■
　　　　<6>　The timing variation (time difference at the change point) of each phase is 10 ns
　　　　　　　or more[Note 1] .... ■
　　　　<7>　The I/O switching of the bidirectional buffer is performed at the basic timing[Note 1] .... ■
　　　　<8>　Each pattern is initialized within 32 K[Note 1] .... ■
　　　　<9>　The following restrictions are satisfied[Note 1] .... ■

Timing Limit \ Signal Type	Input Delay (t_D)		Input Pulse Width	
	MIN.	MAX.	MIN.	MAX.
Basic timing	0 ns		−	
NRZ signal	10 ns	T − 10 ns	−	
RZ signal (clock mode)	10 ns	T − 10 ns	144 pins or less: 15 ns 145 pins or more: 10 ns	T − t_D − 15 ns

　　(b)　How many test patterns are there? **1**

(2)　Details of simulation using pattern for high-speed function test

　　(a)　Simulation was performed under the following conditions[Note 1] .... ■

Simulation \ Condition	MIN.	MAX.
Test cycle (T)	User-specified value	User-specified value
Load capacitance value	50 pF[Note 2]	125 pF (bidirectional pins) 90 pF (output pins)
Strobe time	User-specified value + 5 ns	User-specified value − 5 ns

　　(b)　There were no mismatches in either MIN. or MAX. simulation[Note 1] .... ■

　　Notes 1. If this item is satisfied, check the box. For any boxes left unchecked, please write proposed
　　　　　　countermeasures.
　　　　　2. The load capacitance value may change in order to improve the accuracy of the actual wiring
　　　　　　length.

(1) Enter the following information about the high-speed function test pattern. All these items must be satisfied.

    (a) Indicate whether conditions <1> to <9> below are all satisfied.
      <1> Indicate that the initialization pattern has been entered in the high-speed function test pattern.
      <2> Indicate that the test rate (T) is 50 ns or more.
      <3> Indicate that there is a strobe at one point only.
      <4> Indicate that the strobe time is 15 ns or more and T – 10 ns or less.
      <5> Indicate that the specified number of timing phases is 6 or less, including the basic timing.
      <6> Indicate that the timing variation (time difference at the change point) of each phase is 10 ns or more.
      <7> Indicate that the I/O switching of the bidirectional buffer is performed at the basic timing.
      <8> Indicate that each pattern is initialized within 32 K.
      <9> Indicate that the restrictions in the table on the left are satisfied.

    (b) Enter the number of high-speed function test patterns.

(2) Enter details of simulation using the pattern for high-speed function test.

    (a) Simulation must be performed under the conditions in the table on the left, so indicate that this was the case.

    (b) Indicate that there were no mismatches in either MIN. or MAX. simulation. The occurrence of a mismatch changes the timing conditions, so ensure that no mismatch occurs.

2.9.5   GTL, PECL, HSTL, PCI, LVDS block

(1) Blocks used

Block Name	I/O	Number of Blocks Used
FIR1	**I**	**1**
EGTL	**O**	**1**
BGOW	**I/O**	**2**

If there are IEN pins, please enter (2) to (8).

(2) All the IEN pins are connected directly to an input buffer**Note** .... ■
Connect IEN directly to an external buffer (PCI is not a target).

(3) The IEN pins are connected via input buffers FIXA, FUXA, and FIZA**Note** .... ■
Use the dedicated buffers above for the IEN pins (PCI is not a target).

(4) Enter the name of the external pin that controls the IEN pins (PCI is not a target).   Pin name   **GTLIEN**

(5) There is at least one pattern in which all the IEN pins are L after pattern 51 of
the DC pattern**Note** .... ■
This pattern is required for I_{DD} measurement, so be sure to make at least one pattern L (PCI is not a target).

(6) If 5 V PCI is being used, a 5 V additional power supply specification (VD5-CMOS9HD,
VDD5-EA9HD) was made when the dif file was created**Note** .... ■
Be aware that this name differs from the usual additional power supply name.   Additional $V_{D(D)5}$ **3**
(For CMOS-9HD and EA-9HD, a 5 V additional power supply is required for each edge used)
Pin No.   **50, 55, 60**

(7) If modulation must be inserted in PCI pins when PCI pins are used, check either (a) or (b).

(a) Pattern was created in I/O modulation specification. .... ■
(b) Enter the pin names and delay values if modulation needs to be inserted in the waveform.

Pin Name	Delay Value	Pin Name	Delay Value	Pin Name	Delay Value
A01	30				
A02	30				
A03	30				
A04	30				
A05	30				

Note   If this item is satisfied, check the box. For any boxes left unchecked, please write proposed
countermeasures.

Enter the following information about the GTL, PECL, HSTL, PCI, and LVDS blocks.

(1) Enter the block name, buffer type (input = I, output = O, bidirectional = I/O), and number of GTL, PECL, HSTL, PCI, and LVDS blocks used.

(2) All the GTL IEN pins must be connected directly from outside to GTL input buffers, so indicate that this is the case (PCI is not a target).

(3) A dedicated control buffer must be used for the IEN pins, so indicate that this is the case (PCI is not a target).

(4) Enter the name of the external pin that controls the IEN pins (PCI is not a target).

(5) For I_{DD} measurement, there must be at least one pattern 51 patterns or more after the DC pattern in which all the GTL IEN pins are L. Indicate that there is a pattern in which all the IEN pins are L (PCI is not a target).

(6) When a 5 V PCI is included, a 5 V additional power supply ($V_{D(D)5}$) must be specified in the dif file, so indicate that this specification was made when the file was created.
Note that the specification method differs depending on the series. Specify VD5 for the CMOS-9HD Series, and VDD5 for the EA-9HD Series.

(7) When PCI pins are being used

(a) When using I/O modulation, in the case of OPENCAD V5.3, submit strobe ALB.
In the case of OPENCAD V5.4 or later, create ALBA by making the device read the IO_MODULATION file with the create interface ALBA function of the pattern utility.

(b) Enter the pin name and delay value for those PCI pins at which it is necessary to insert modulation.

2.9.6   DPLL block

(1)   Blocks used

Block Name	Instance name	Number of Blocks Used
F9E6	**DPLL1**	**1**

(2)   An initialization pattern has been created**Note** .... ■
        (Execute simulation using the initialization pattern and check that there were no mismatches.)
(3)   In the initialization pattern, all the I/O buffer modes have been secured**Note** .... ■

(4)   If the DPLL's external pins have I/O buffers, the input pins are fixed to input and the output
        pins are fixed to output when TMD0, TMD1, (TMD2) are in DPLL unit test mode**Note** .... ■
        (Ensure the 3-state buffer is ON.)
(5)   Clock (RZ) and modulation (NRZ) are not used for external pin connected to DPLL
        in the initialization pattern**Note** .... ■
        (Do not make a timing specification.)
(6)   All output pins of the initialization pattern except the TOUT pin are "don't care"
        (except oscillation output signal)**Note** .... ■
(7)   The DPLL's input and output pins can be accessed directly**Note** .... ■
        If not, verification and approval of special requests, etc., by NEC Electronics are required before interfacing.
(8)   The RCLK, TMD0, TMD1, TMD2, TMD3, and TOUT pins do not share signal lines with other
        signals**Note** .... ■
        (This does not apply to sharing TMD0 to TMD3 with pins with the same function when using multiple
        DPLLs)
        (a) When using a DPLL together with NEC_SCAN, can the above pins be accessed without being
             affected by other external pins? .... ■
             If not, add information to pin fixing file regarding **2.9.8 Alternate use as scan path and
             boundary scan** and **2.9.9 Scan path.**
        (b) It is confirmed that the output signal of the TOUT pin is not used in the internal circuit**Note** .... ■
             If not, verification and approval of special requests, etc., by NEC Electronics are required before interfacing.
(9)   The test pattern (DC, LFT) was generated in through path mode and reset mode only**Note** .... ■
(10) A dedicated buffer (FI0P/FI0Q) is used for RCLK (H01)**Note** .... ■
(11) A function error does not occur as a result of creating and simulating the pattern
        for checking DPLL connection**Note** .... ■
(12) Interface data
        Submit the .dpmodechk file and .slg file in addition to normal interface data.

    Note   If this item is satisfied, check the box. For any boxes left unchecked, please write proposed
                countermeasures.

Enter the following information about the DPLL block.

(1)   Enter the block names, Instance names and number of DPLL blocks used.

(2)   Indicate whether an initialization pattern has been created. An initialization pattern must be prepared.

(3)   In the initialization pattern, in order to perform a stable the DPLL test, it is necessary to fix the mode of the I/O buffers not related to the DPLL, so indicate that these buffers have been mode-fixed.

(4)   When testing the DPLL, the mode of the external pins must be fixed to input mode when connected to input pins and output mode when connected to output pins, so indicate that these pins are fixed to either input or output (Ensure the 3-state buffer is ON).

(5)   In the DPLL test initialization pattern, clock and modulation cannot be used for the external pin connected to DPLL.
      Indicate that a clock (RZ) or modulation (NRZ) is not being used (Do not make a timing specification).

(6)   The final patterns of output pins other than TOUT pin in the initialization pattern must all be "don't care" for performing DPLL test. Check if this is the case and mark accordingly.
      However, the oscillation output signal when the oscillator is included must not be "don't care".

(7)   To test the DPLL, the input control pin and TOUT pin must be accessed directly, so indicate whether the input and output pins can be accessed directly.

(8)   Indicate that the RCLK, TMD0, TMD1, TMD2, TMD3, and TOUT pins do not share signal lines with other signals (this does not apply to sharing TMD0, TMD1, TMD2, and TMD3 with pins with the same function when using multiple DPLLs).
      (a)   When using a DPLL together with NEC_SCAN, check and indicate that the above pins can be accessed without being affected by other external pins.
            If they can't, add the required level information of the other external pins to the scan path pin fix file.

      (b)   Check if the output signal of the TOUT pin is not used by the internal circuit, and mark accordingly.
            If not, verification and approval of special requests, etc., by NEC Electronics are required before interfacing.

(9)   Indicate that the PLL or NEC test mode is not being used in the test pattern (in the user pattern, this only applies to through-path mode or reset mode).

(10) A dedicated buffer must be used for the external pin connecting RCLK. Indicate that this is the case.

(11) Indicate that function errors do not occur when executing simulation after creating the pattern for checking DPLL connection. Use ALBATROSS for OPENCAD V5.4 or later and ALBATROSS or LOGPAT for OPENCAD V5.3 as the pattern format at this time.

(12) Please submit .dpmodechk and .sig for DPLL connection verification simulation, in addition to regular materials, as interface data.

(13) Pin correspondence table

    (a) Either submit the .pinf file, or enter (c) pin correspondence table.

    (b) If multiple DPLLs are included during .pinf file submission, enter the .pinf file correspondence.

        DPLL block name__**F9E6**__   Interface name__**DPLL1**__   .pinf file name__**F9E6.pinf**__

        DPLL block name__**F9E4**__   Interface name__**DPLL2**__   .pinf file name__**F9E4.pinf**__

    (c) Pin correspondence table (if multiple DPLLs are included, make several copies of this sheet and enter the information as required.)

DPLL block name ____**F9E6**____   Instance name ____**DPLL1**____

Pin Name	External Pin Name	Pin No.	Pin Name	External Pin Name	Pin No.
(H01)	**PLLRCLK**	**3**	(H15)		
(H02)	–	–	(H16)		
(H03)	**PLLTCK0**	**5**	(H17)		
(H04)	**PLLTCK1**	**6**	(H18)		
(H05)	**PLLTMD0**	**7**	(H19)		
(H06)	**PLLTMD1**	**8**	(H20)		
(H07)	**PLLTMD2**	**9**	(N01)	–	–
(H08)	**PLLTSMI**	**10**	(N02)	**PLLTOUT**	**12**
(H09)			(N03)		
(H10)			(N04)		
(H11)			(N05)		
(H12)			(N06)		
(H13)			(N07)		
(H14)			(N08)		

(13) Pin correspondence table

    (a) Either submit the .pinf file, or enter (c) pin correspondence table.

    (b) Enter the DPLL block name and interface name corresponding to the .pinf file.

    (c) Enter the required information in the pin correspondence table. If multiple DPLLs are included, make several copies of this sheet and enter the information as required.

2.9.7 Megamacro

(1) Blocks used

Block Name	Number of Blocks Used
NA54	**1**

Remark Always initialize the megamacro after inserting the initialization pattern in each megamacro into the start of test patterns such as DC and LFT.

(2) Which level the CSE pin is fixed? [Must indicate] .... □ H ■ L
(In the case of H, a BUS configuration for the megamacro outputs is not possible)
  • In the case of CSE = L, what is the circuit configuration of the megamacro outputs?
  (a) The megamacro outputs have a BUS configuration .... ■
  (b) Megamacro outputs are received via a gate and Hi-Z disappears. .... □
    (This is basically prohibited in EA-9HD. Use a bus holder in this case.)

(3) Direct signals have been added from input pins for all the inputs of the megamacro[Note] .... ■
(Do not invert signals or pass them through a sequential circuit)

(4) Direct monitoring is possible at output pins for all the outputs of the megamacro[Note] .... ■
(Do not invert signals or pass them through a sequential circuit)

(5) A megamacro single-unit test setting pattern has been generated[Note] .... ■
Ensure that the megamacro single-unit test pattern conforms to next (a) to (f) interface conditions.
  (a) All the final patterns of output pins other than those of megamacros are "don't care"
    (except for the oscillation output signal)[Note] .... ■
  (b) Neither clock (RZ) nor modulation (NRZ) is used[Note] .... ■
  (c) The I/O buffer mode has been secured[Note] .... ■
  (d) The internal circuits other than those of the megamacro have been initialized[Note] .... ■
  (e) There is no Hi-Z or unknown input[Note] .... ■
  (f) There were no mismatches as a result of the simulation before placement and routing[Note] .... ■

(6) Is a test pattern required for setting (3) and (4) above? .... ■ YES □ NO
In the case of YES, incorporate it in the single unit test setting pattern.

(7) The "Megamacro Single Unit Test Specification Document" from the megamacro design
manual has been submitted[Note] .... ■
(If not, include it with this manual)
  • The required items for the megamacro to be used should be included in the above document.

  Note If this item is satisfied, check the box. For any boxes left unchecked, please write proposed
     countermeasures.

  Remark If there are any details regarding the megamacro test circuit configuration that require special
      attention, please enter them here.

> **A bidirectional buffer is used and ID0 to ID7 and OD0 to OD7 are used in common.**

Enter the following information about megamacros.

(1)   Enter the name and number of the megamacro blocks used

(2)   The configuration of the megamacro output block differs depending on the level of the CSE pin, so indicate that the level of the CSE pin is fixed to either H or L.
In the case of CSE = L, indicate whether the megamacro outputs are configured as a BUS or as a gate (refer to the relevant design manual for details of the circuit configuration).

(3)   For the megamacro single-unit test using the tester, direct signals must be added from input pins for all the inputs. Check the circuit and indicate that this is the case.

(4)   For the megamacro single-unit test using the NEC tester, direct monitoring must be possible at output pins for all the outputs. Check the circuit and indicate that this is the case.

(5)   When creating a megamacro single unit test design pattern, check and indicate that items (a) to (f) are all checked.

(6)   When performing the megamacro single-unit test, in order to transfer external signals to megamacro inputs without inverting them when gates, etc., have been inserted into the signal lines of the test pins, a setting pattern is required. Indicate whether a test pattern for setting (3) and (4) is required.

(7)   Indicate whether the required sections of the "Megamacro Single Unit Test Specification Document" in the megamacro version of each design manual have been copied and submitted with the required items entered (items such as the instance names and pin reference table are required specifications and therefore must be prepared).

For example, if a specific method such as sharing the megamacro data input and output is being used, enter this information.

2.9.8 Alternate use as scan path and boundary scan

(1) Dedicated boundary scan pins were added to dif**Note** .... ■

(2) Have TDI (SIN) and TDO (SOT) been allocated to positions reserved for dedicated scan path pins in each package? (This does not apply to packages with 314 or more pins.)**Note** .... ■

 • Please enter the relevant pin numbers in the following table for confirmation.
  (This does not apply to packages with 314 or more pins.)

BSCAN Pin Name	SCAN Pin Name	Pin No.	BSCAN Pin Name	SCAN Pin Name	Pin No.
TMS	SMC	-	TRST	-	-
TDI	SIN	41	TCK	SCK	-
TDO	SOT	42			

(3) It is confirmed that no error occurred in scan rule check**Note** .... ■

 The scan rule check execution results have been submitted**Note** .... ■

 (If not, please submit them)

 • If there is a separate file, pin fix file, or scan bist file, please submit these at the same time.

 • Separate file name __BUNRI__   Pin fix file name __KOTEI__   Scan bist file name __TOP.bist.scn__

(4) TAP macros (SBCG, SBCL) are placed on top layer**Note** .... ■

(5) The dedicated boundary scan pins are fixed to the following values**Note** .... ■

 (These pins must be fixed; otherwise they will be in boundary scan mode)

  | TCK = 0, TMS = 1, TDI = 1, TRST = 0, TDO = Hi-Z |

  * The same applies for user patterns such as DC and LFT.

(6) Please enter below the DC measurement pattern of the TAP macro section in the DC test pattern.

 (Refer to the design manual for details of the TAP macro DC pattern.)

 From __100__ pattern to __115__ pattern

> Be aware that if the DC pattern is not described, the tester cannot measure the level, possibly causing defective products to be mixed in the samples at shipment.

(7) In all BSCAN test patterns, the final value of the patterns of all output pins (pins other than boundary scan dedicated pins) has been set to "1", "0", or "Hi-Z"**Note** .... ■

 (This is necessary because undefined is prohibited.)

(8) The following data has been prepared in addition to the usual interface data**Note** .... ■

  .bspat.alb, .bscanchk, .set, .bsorder, .bsdl, .scan.init.alb

   [Non Test External Pin]   → Required when DPLL or oscillator with oscillation stop function is incorporated

   [Non SCAN MACRO Specification] → Required when compiled memory, megamacro, and macro have been specified as separate

   [Non SCAN BIST]   → Specified only when required in an embedded array

(9) .scan.init.alb and .bspat.alb are created from the same boundary scan initialize pattern**Note** .... ■

(10) The following restrictions apply when designing the scan path.

 Are all the following restrictions observed?**Note** .... ■

  <1> Use of an internal bus configuration (F53X, F54X, etc.) is not possible.

  <2> External I/O pins and TAP macros must always be placed on the topmost layer.

  <3> Do not connect the scan output control buffers (SOEH, SOEL) to the TAP macro test data output (TDO) pin and pins that use the boundary scan register.

The standard fault coverage is 95%. If a fault coverage greater than 95% is required, please contact NEC Electronics prior to interfacing.

Note If this item is satisfied, check the box. For any boxes left unchecked, please write proposed countermeasures.

Enter the following information about the scan path and boundary scan.
   (1)   Indicate whether boundary scan-dedicated pins have been added to the dif file.
   (2)   When there are fewer than 314 pins, check and indicate that TDI (SIN) and TDO (SOT) have been allocated
         to positions reserved for dedicated scan path pins in each package. For confirmation, also enter the pin No.
         of the TDI and TDO pins.

   (3)   The scan rule check checks the adequacy of the scan circuits and therefore must be executed. Check the
         execution results and indicate that there were no errors. If an error occurred, fix it, re-execute the scan rule
         check, and confirm that the error did not reoccur. The execution results must be submitted.
         If there is a separate file, pin fix file, or scan bist file, please submit these.
         Enter each file name (also check that BUNRI and ATGNAME are both included in the separate file).
   (4)   Check if the TAP macros (SBCG, SBCL) are placed on the top layer.
   (5)   The dedicated boundary scan pins in the BSCAN pattern will be in boundary scan mode if they are not fixed,
         so indicate that these pins have been fixed to the values shown on the left.

   (6)   If DC patterns for TAP macro are not described in the DC pattern, the level of the TAP macro I/O pins cannot
         be set. It is therefore necessary to describe DC patterns for TAP macro in the DC pattern. Enter pattern range
         in which DC patterns for TAP macro will be described.

   (7)   Check if the final value of output pin patterns other than boundary scan dedicated pins has been set to "1",
         "0", or "Hi-Z", and mark accordingly.
         3-state outputs must not be undefined or Hi-Z, so be sure to set the pin level correctly.
   (8)   Check whether there are the files listed on the left in addition to the regular interface data.

   (9)   An BSCAN pattern is also necessary when creating circuit-name.scan.init.alb.
   (10) There are blocks that cannot be used when designing the scan path, so refer to the restrictions in <1> to <3>
         and indicate that these restrictions have been observed.

2.9.9   Scan path

(1) Scan path

This check is not required in case of alternate use as boundary scan.

(a) Is If there are 32,000 or more F/Fs, the scan becomes a multiscan. In this case, fill in (2) Multiscan. If there are less than 32,000 F/Fs, check the following items.

(b) SMC, SIN, and SOT are located in the positions reserved for dedicated scan path pins in each package (This does not apply to packages with 314 or more pins.)**Note** .... ■

(c) Dedicated scan path pins were added to dif **Note** .... ■
   • Please enter the relevant pin numbers in the following table for confirmation.

Pin Name	Pin No.	Pin Name	Pin No.
SMC	**45**	AMC	**8**
SIN	**46**	SCK	**38**
SOT	**44**		

(d) Do the following 3 pins function alternately as general pins?
   • SIN .... ■ Has alternate function   Pin name:___**AAA**___   ☐ Does not have alternate function
   • SOT .... ☐ Has alternate function   Pin name:_____   ■ Does not have alternate function
   • SCK .... ■ Has alternate function   Pin name:___**CCC**___   ☐ Does not have alternate function
   • If these pins have alternate functions, the circuits have been configured in accordance
      with the design manual**Note** .... ■
      Be sure to submit the .primpin file regardless of whether these pins function alternately as general pins.

(e) It is confirmed that no error occurred in scan rule check**Note** .... ■
   The scan rule check execution results have been submitted**Note** .... ■
   (If not, please submit them)
   • If there is a separate file, pin fix file, or scan bist file, please submit these at the same time
   • Separate file name ____**BUNRI**____   Pin fix file name ____**KOTEI**____   Scan bist file name ____**.bist.scn**

(f) The following restrictions apply when designing the scan path.
   Are all the following restrictions observed?**Note** .... ■
   <1> Use of an internal bus configuration (F53X, F54X, etc.) is not possible.
   <2> Be sure to configure the external I/O pins in the top layer.

The standard fault coverage is 95%. If a fault coverage greater than 95% is required, please contact NEC Electronics prior to interfacing.

Note   If this item is satisfied, check the box. For any boxes left unchecked, please write proposed countermeasures.

(1) Enter the following information about the scan path.

(a) If there are 32,000 or more F/Fs, the scan becomes a multiscan. In this case, fill in (2) Multiscan (the items below do not need to be checked).

(b) In packages of less than 314 pin, the SMC, SIN, and SOT pin configuration locations is set separately for each package, so check if the pins are placed at their assigned locations and mark accordingly.

(c) Indicate whether scan-dedicated pins have been added to the dif file. For confirmation, also enter the pin No. of the SMC, SIN, SOT, AMC, and SCK pins.

(d) SIN, SOT, and SCK can function alternately as general pins, so indicate whether these pins have general-pin alternate functions.
     If these pins have alternate functions, enter the pin names and indicate whether the circuits have been configured in accordance with the design manual.
     Be sure to submit the .primpin file regardless of whether these pins function alternately as general pins.

(e) The scan rule check checks the adequacy of the scan circuits and therefore must be executed. Check the execution results and indicate that there were no errors. If an error occurred, fix it, re-execute the scan rule check, and confirm that the error did not reoccur. The execution results must be submitted. If there is a separate file, pin fix file, or scan bist file, please submit these.
     Enter each file name (also check that BUNRI and ATGNAME are both included in the separate file).

(f) There are blocks that cannot be used when designing the scan path, so refer to the restrictions in <1> and <2> and indicate that these restrictions have been observed.

(2) Multiscan

(a) Enter a check mark in the following table for the number of scan chains.

Number of F/Fs	31999 or Less	32000 to 63999	64000 to 127999	128000 to 255999	256000 to 511999	512000 or More
Number of scan chains	1	2	4	8	16	32
		√				

(b) It is confirmed that no error occurred in scan rule check**Note** .... ■

   The scan rule check execution results have been submitted**Note** .... ■

   (If not, please submit them)

   • If there is a separate file, pin fix file, or scan bist file, please submit these at the same time.

   • Separate file name __**BUNRI**__   Pin fix file name __**KOTEI**__   Scan bist file name __**bist.scn**__

(c) Enter the pin names corresponding to the following pins when multiscan pins are used alternately as user pins.

   When SIN, SOT, and SCK pins are not used alternately, it is not necessary to enter this item.

Dedicated Pin Name	External Pin Name	Dedicated Pin Name	External Pin Name	Dedicated Pin Name	External Pin Name	Dedicated Pin Name	External Pin Name
SIN1	aa	SOT1		SIN17		SOT17	
SIN2	bb	SOT2		SIN18		SOT18	
SIN3		SOT3		SIN19		SOT19	
SIN4		SOT4		SIN20		SOT20	
SIN5		SOT5		SIN21		SOT21	
SIN6		SOT6		SIN22		SOT22	
SIN7		SOT7		SIN23		SOT23	
SIN8		SOT8		SIN24		SOT24	
SIN9		SOT9		SIN25		SOT25	
SIN10		SOT10		SIN26		SOT26	
SIN11		SOT11		SIN27		SOT27	
SIN12		SOT12		SIN28		SOT28	
SIN13		SOT13		SIN29		SOT29	
SIN14		SOT14		SIN30		SOT30	
SIN15		SOT15		SIN31		SOT31	
SIN16		SOT16		SIN32		SOT32	
SCK							

   • If these pins have alternate functions, the circuits have been configured in accordance

     with the design manual**Note** .... ■

(d) The following restrictions apply when designing the scan path.

   Are all the following restrictions observed?**Note** .... ■

   <1> Use of an internal bus configuration (F53X, F54X, etc.) is not possible.

   <2> Be sure to configure the external I/O pins in the top layer.

The standard fault coverage is 95%. If a fault coverage greater than 95% is required, please contact NEC Electronics prior to interfacing.

 Note   If this item is satisfied, check the box. For any boxes left unchecked, please write proposed

           countermeasures.

(2) Enter the following information about the multiscan.

(a) Enter the check mark in the following table for the number of scan chains.
Calculate the number of F/Fs from the result of GateDRC.
The number of scan chains is 1, 2, 4, 8, 16, and 32 only as shown in the table. The other numbers are not supported.

(b) The scan rule check checks the adequacy of the scan circuits and therefore must be executed. Check the execution results and indicate that there were no errors. If an error occurred, fix it, re-execute the scan rule check, and confirm that the error did not reoccur. The execution results must be submitted. If there is a separate file, pin fix file, or scan bist file, please submit these.
Enter each file name (also check that BUNRI and ATGNAME are both included in the separate file).

(c) The SIN, SOT, and SCK pins can function alternately as general pins, so if they are being used as such, check that the circuits have been configured in accordance with the design manual.

(d) There are blocks that cannot be used when designing the scan path, so refer to the restrictions in <1> and <2> and indicate that these restrictions have been observed.

2.9.10   Boundary scan

This check is not required in case of alternate use as scan path.

(1)   For boundary scan dedicated pins, enter the pin names corresponding to the following pins for verification purposes.

Pin Name	External Pin Name	Dedicated Pin Name	External Pin Name	Dedicated Pin Name	External Pin Name
TCK	**TCK**	TMS	**TMS**	TDO	**TDO**
TDI	**TDI**	TRST	**TRST**		

(2)   It is confirmed that no error occurred in boundary scan rule check (BSCHK)**Note** .... ■
       The BSCHK execution results have been submitted**Note** .... ■
       (If not, please submit them)

(3)   BSCAN pattern
       (a)   The dedicated boundary scan pins are fixed to the following values**Note** .... ■
             (These pins must be fixed; otherwise they will be in boundary scan mode)

             | TCK = 0, TMS = 1, TDI = 1, TRST = 0, TDO = Hi-Z |

             • The same applies for user patterns such as DC and LFT.

       (b)   Patterns in which the final value is fixed to 1, 0, or Hi-Z at each output pin have been
             prepared**Note** .... ■
             <1>   In the case of 2-state, N-ch open-drain output pin, at least 2 patterns have been
                     prepared**Note** .... ■
                     (The 2 states are "0" and "1", and N-ch open drain is "0" and "Hi-Z".)
             <2>   In the case of 3-state, bidirectional output pins, at least 3 patterns have been
                     prepared**Note** .... ■
                     (The 3 states are "0", "1", and "Hi-Z", and bidirectional is "0", "1", and "input mode".)

(4)   Please enter below the DC measurement pattern of the TAP macro section in the DC test pattern.
       (Refer to the design manual for details of the TAP macro DC pattern.)
             From   **100**   pattern to   **115**   pattern

> Be aware that if the DC pattern is not described, the tester cannot measure the level, possibly causing defective products to be mixed in the samples at shipment.

• Use either SBC4 or SBCJ as the TAP macro.

(5)   Interface data:
       The following data has been prepared in addition to the usual interface data**Note** .... ■
             .bspat.alb, .bscanchk, .bspat.albchk
             Result of simulation (MIN, MAX) using .bspat.alb   (.slg, .iomoduchk, .dpmodechk, .tpe)

       Note   If this item is satisfied, check the box. For any boxes left unchecked, please write proposed
                   countermeasures.

Enter the following information about the boundary scan.

(1) For confirmation, enter the names of the external pins corresponding to the dedicated boundary scan pins (ensure that the names of the dedicated boundary scan pins match those of the external pins).

(2) BSCHK checks the adequacy of the boundary scan circuits and therefore must be executed. Check the execution results and indicate that there were no errors. If an error occurred, fix it, re-execute BSCHK, and confirm that the error did not reoccur. The execution results must be submitted.

(3) Enter the following information about the BSCAN pattern.

   (a) The dedicated boundary scan pins in the BSCAN pattern will be in boundary scan mode if they are not fixed, so indicate that these pins have been fixed to the values shown on the left.

   (b) Check if patterns where the final pattern value has been set to "1", to "0", and "Hi-Z" have been prepared for each output pin, and mark accordingly.

      <1> At least 2 BSCAN patterns are required for 2-state and N-ch open-drain output pins.
          ("0" and "1" for 2-state; "0" and "Hi-Z" for N-ch open drain)

      <2> At least 3 BSCAN patterns are required for 3-state and bidirectional output pins.
          ("0", "1", and "Hi-Z" for 3-state, and "0", "1", and "input mode" for bidirectional pins)

(4) If DC patterns for TAP macro are not described in the DC pattern, the level of the TAP macro I/O pins cannot be set. It is therefore necessary to describe DC patterns for TAP macro in the DC pattern. Enter pattern range in which DC patterns for TAP macro will be described.

(5) Check whether there are the files listed on the left in addition to the regular interface data.
     Submit also information for results of MIN/MAX simulation execution with .bspat.alb.

CHAPTER 3 PRODUCT SPECIFICATIONS

To enable connection to both CMOS and TTL products, the CMOS-N5 Series is provided with two types of input/output interface blocks, each with a specified V_{IL} and V_{IH}: CMOS level and TTL level. In general, usable operating conditions differ between the CMOS products and TTL products. This chapter describes the recommended operating conditions and the DC and AC characteristics corresponding to the usable power supply voltage range and temperature range.

3.1 Terminology

Table 3-1. Terminology for Absolute Maximum Ratings

Parameter	Symbol	Definition
Power supply voltage	V_{DD}	Range of voltages which will not damage or reduce reliability when applied to the V_{DD} pin.
Input voltage	V_I	Range of voltages which will not damage or reduce reliability when applied to the input pin.
Output voltage	V_O	Range of voltages which will not damage or reduce reliability when applied to the output pin.
Input current	I_I	Maximum allowable current which will not cause latchup when applied to the input pin.
Output current	I_O	Maximum allowable DC current which will not cause damage or reduce reliability when flowing to or from the output pin.
Operating temperature	T_A	Range of ambient temperatures for normal logical operation.
Storage temperature	T_{stg}	Range of element temperatures which will not damage or reduce reliability in the state where neither voltage nor current is applied.

Table 3-2. Terminology for Recommended Operating Conditions

Parameter	Symbol	Definition
Power supply voltage	V_{DD}	Range of voltages for normal logical operation when V_{SS} = 0 V.
Input voltage, high	V_{IH}	For voltage applied to the input of the gate array, this value indicates the voltage of the high-level state in which the input buffer operates normally. • If voltage greater than the MIN. value is applied, the input voltage is assured to be high-level.
Input voltage, low	V_{IL}	For voltage applied to the input of the gate array, this value indicates the voltage of the low-level state in which the input buffer operates normally. • If a voltage less than the MAX. value is applied, the input voltage is assured to be low-level.
Positive trigger voltage	V_P	Input level that inverts the output level when the input of the gate array is changed from the low-level side to the high-level side.
Negative trigger voltage	V_N	Input level that inverts the output level when the input of the gate array is changed from the high-level side to the low-level side.
Hysteresis voltage	V_H	Difference between the positive- and negative-trigger voltage.
Input rise time	t_{ri}	Limit value for the rise time from 10% to 90% of the input voltage applied to the input of the gate array.
Input fall time	t_{fi}	Limit value for the fall time from 90% to 10% of the input voltage applied to the input of the gate array.

Table 3-3. Terminology for DC Characteristics

Parameter	Symbol	Definition
Static current consumption	I_{DDS}	In the state where there is no voltage change in the input and output pins, indicates the current that flows in from the power supply pin at the specified power supply voltage.
Off-state output current	I_{OZ}	For a 3-state output, this value indicates the current that flows through the output pin at the specified voltage when the output is at high impedance.
Output short-circuit current	I_{OS}	Current that flows out if the output pin is short-circuited to GND when output is at the high level.
Input leakage current	I_I	Current that flows through the input pin when voltage is applied to the input pin.
Output current, low	I_{OL}	Current that flows to the output pin at the specified low-level output voltage.
Output current, high	I_{OH}	Current that flows from the output pin at the specified high-level output voltage.
Output voltage, low	V_{OL}	Output voltage when output is open in the low-level state.
Output voltage, high	V_{OH}	Output voltage when output is open in the high-level state.

3.2 Absolute Maximum Ratings

Table 3-4. Absolute Maximum Ratings

Parameter	Symbol	Conditions	Ratings	Unit
Power supply voltage	V_{DD}		−0.5 to +6.0	V
Input voltage/output voltage	V_I/V_O		−0.5 to +6.0	V
Input current	I_I		20	mA
Output current	I_O	I_{OL} = 3.0 mA type	10	mA
		I_{OL} = 6.0 mA type	15	mA
		I_{OL} = 9.0 mA type	20	mA
		I_{OL} = 12.0 mA type	30	mA
		I_{OL} = 18.0 mA type	40	mA
		I_{OL} = 24.0 mA type	60	mA
Operating ambient temperature	T_A		−40 to +85	°C
Storage temperature	T_{stg}		−65 to +150	°C

Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

3.3 Standard Specification of CMOS Interface Conditions (V_{DD} = 5.0 V $\pm$10%, T_A = –40 to +85$°$C)

3.3.1 Recommended operating range

Table 3-5. Recommended Operating Range (V_{DD} = 5.0 V $\pm$10%, T_A = –40 to +85$°$C)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Power supply voltage	V_{DD}			4.5	5.0	5.5	V
Input voltage, high	V_{IH}	CMOS interface[Note 1]		$0.7V_{DD}$		V_{DD}	V
Input voltage, low	V_{IL}			0.00		$0.3V_{DD}$	V
Positive trigger voltage	V_P		Old-type Schmitt input [Note2]	0.80		3.90	V
Negative trigger voltage	V_N			0.60		3.10	V
Hysteresis voltage	V_H			0.20		0.80	V
Positive trigger voltage	V_P		New-type Schmitt input [Note 3]	2.85		3.75	V
Negative trigger voltage	V_N			1.15		1.75	V
Hysteresis voltage	V_H			1.30		2.07	V
Input voltage, high	V_{IH}	TTL interface[Note 1]		2.29		V_{DD}	V
Input voltage, low	V_{IL}			0.00		0.77	V
Positive trigger voltage	V_P		Old-type Schmitt input [Note2]	1.15		2.54	V
Negative trigger voltage	V_N			0.59		2.10	V
Hysteresis voltage	V_H			0.15		0.60	V
Positive trigger voltage	V_P		New-type Schmitt input [Note 3]	1.68		2.55	V
Negative trigger voltage	V_N			0.64		1.33	V
Hysteresis voltage	V_H			0.83		1.44	V
Input rise time	t_{ri}	Normal input		0		200	ns
Input fall time	t_{fi}			0		200	ns
Input rise time	t_{ri}	Schmitt input		0		10	ms
Input fall time	t_{fi}			0		10	ms

Notes 1. Use a new-type CMOS interface, which has W suffixed to the block name, for the Schmitt buffer.
2. Schmitt buffer without W suffixed to the block name.
3. Schmitt buffer with W suffixed to the block name.

Remark When inputting a slow signal with a long rise/fall time, noise on the signal line may affect the operation, so be sure to use a Schmitt trigger input buffer.
Because fluctuation on the power supply line due to simultaneous operation of output buffers reduces the capability of the Schmitt trigger input buffer, carefully determine pin placement.

3.3.2 DC characteristics

Table 3-6. DC Characteristics (V_{DD} = 5.0 V $\pm$10%, T_A = –40 to +85°C)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Static current consumption[Note 1]	I_{DDS}	V_I = V_{DD} or GND		0.1	100	μA
Off-state output current	I_{OZ}	V_O = V_{DD} or GND			$\pm$10	μA
Output short-circuit current[Note 2]	I_{OS}	V_O = GND			–250	mA
Input leakage current						
Normal input	I_I	V_I = V_{DD} or GND		$\pm10^{-5}$	$\pm$10	μA
With pull-up resistor (50 kΩ)	I_I	V_I = GND	45	131.0	319.7	μA
With pull-up resistor (5 kΩ)	I_I	V_I = GND	0.3489	1.00	2.2	mA
With pull-down resistor (50 kΩ)	I_I	V_I = V_{DD}	45	131.0	319.7	μA
Pull-up resistor (50 kΩ)[Note 3]	R_{PU}	V_I = GND	17.2	38.2	100	kΩ
Pull-up resistor (5 kΩ)[Note 3]	R_{PU}	V_I = GND	2.5	5.0	12.9	kΩ
Pull-down resistor (50 kΩ)[Note 3]	R_{PD}	V_I = V_{DD}	17.2	38.2	100	kΩ
Output voltage, low (CMOS-level output)	V_{OL}	I_{OL} = 0 mA			0.1	V
Output voltage, high (CMOS-level output)	V_{OH}	I_{OH} = 0 mA	V_{DD} – 0.1			V
Output current, low (CMOS-level output)						
3.0 mA type	I_{OL}	V_{OL} = 0.4 V	3.00[Note 4]			mA
6.0 mA type	I_{OL}	V_{OL} = 0.4 V	6.00			mA
9.0 mA type	I_{OL}	V_{OL} = 0.4 V	9.00			mA
12.0 mA type	I_{OL}	V_{OL} = 0.4 V	12.00			mA
18.0 mA type	I_{OL}	V_{OL} = 0.4 V	18.00			mA
24.0 mA type	I_{OL}	V_{OL} = 0.4 V	24.00			mA
Output current, high (CMOS-level output)						
3.0 mA type	I_{OH}	V_{OH} = V_{DD} – 0.4 V	–3.00			mA
6.0 mA type	I_{OH}	V_{OH} = V_{DD} – 0.4 V	–6.00			mA
9.0 mA type	I_{OH}	V_{OH} = V_{DD} – 0.4 V	–9.00			mA
12.0 mA type	I_{OH}	V_{OH} = V_{DD} – 0.4 V	–12.00			mA
18.0 mA type	I_{OH}	V_{OH} = V_{DD} – 0.4 V	–18.00			mA
24.0 mA type	I_{OH}	V_{OH} = V_{DD} – 0.4 V	–24.00			mA

Notes 1. Static current consumption increases when an I/O block with an on-chip pull-up/pull-down resistor and an oscillator are used. See **CHAPTER 4 ESTIMATING ELECTRICAL CHARACTERISTICS** for details.

    2. The output short-circuit time is less than one second and for only one LSI pin.

    3. The pull-up resistor and pull-down resistor values vary depending on the input and output voltages.

    4. This value is 2.0 mA if a pull-up resistor of 5 kΩ is connected.

Remark The + and – signs of the current values in the table indicate the direction of the current. Current flowing into a device is indicated by +; current flowing out is indicated by –.

3.3.3 AC characteristics

Table 3-7 shows the AC characteristics.

The maximum operating clock frequency (f_{MAX}) of the internal cell toggle flip-flop is the value of the toggle frequency (f_{tog}) in the table. Note that the f_{MAX} varies in the actual circuit according to the circuit configuration.

Table 3-7. AC Characteristics (V_{DD} = 5.0 V $\pm$10%, T_A = –40 to +85°C)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Maximum toggle frequency	f_{tog}	Internal toggle F/F				
		Fan-outs = 2, wiring length = 0 mm	200			
Propagation delay time	t_{PD}	Internal gate				
		Fan-outs = 2, wiring length = 2 mm		0.30		ns
		Fan-outs = 1, standard wiring length		0.16		ns
		Fan-outs = 2, standard wiring length		0.18		ns
		Internal gate (low power gate)				
		Fan-outs = 1, standard wiring length		0.21		ns
		Fan-outs = 1, wiring length = 0 mm		0.14		ns
		Input buffer				
		Fan-outs = 1, standard wiring length		0.23		ns
		Fan-outs = 2, wiring length = 2 mm		0.33		ns
		Output buffer (FO01)				
		C_L = 15 pF		1.30		ns
Output rise time	t_r	Output buffer (FO01)				
		C_L = 15 pF		1.23		ns
Output fall time	t_f	Output buffer (FO01)				
		C_L = 15 pF		1.62		ns

3.4 Specification 1 (V$_{DD}$ = 3.0 $\pm$0.3 V, T$_A$ = –40 to +85°C)

3.4.1 Recommended operating range

Table 3-8. Recommended Operating Range (V$_{DD}$ = 3.0 $\pm$0.3 V, T$_A$ = –40 to +85°C)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Power supply voltage	V$_{DD}$			2.7	3.0	3.3	V
Input voltage, high	V$_{IH}$	CMOS interface		0.8V$_{DD}$		V$_{DD}$	V
Input voltage, low	V$_{IL}$			0.0		0.2V$_{DD}$	V
Positive trigger voltage	V$_P$		Schmitt input	1.75		2.40	V
Negative trigger voltage	V$_N$			0.70		1.10	V
Hysteresis voltage	V$_H$			0.81		1.46	V
Input rise time	t$_{ri}$	Normal input		0		200	ns
Input fall time	t$_{fi}$			0		200	ns
Input rise time	t$_{ri}$	Schmitt input		0		10	ms
Input fall time	t$_{fi}$			0		10	ms

Remark When inputting a slow signal with a long rise/fall time, noise on the signal line may affect the operation, so be sure to use a Schmitt trigger input buffer.
Because fluctuation on the power supply line due to simultaneous operation of output buffers reduces the capability of the Schmitt trigger input buffer, carefully determine pin placement.

3.4.2 DC characteristics

Table 3-9. DC Characteristics (V_{DD} = 3.0 ±0.3 V, T_A = –40 to +85°C)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Static current consumption[Note 1]	I_{DDS}	V_I = V_{DD} or GND			54.7	μA
Off-state output current	I_{OZ}	V_O = V_{DD} or GND			±8	μA
Output short-circuit current[Note 2]	I_{OS}	V_O = GND			–200	mA
Input leakage current						
Normal input	I_I	V_I = V_{DD} or GND		±6×10^{-5}	±8	μA
With pull-up resistor (50 kΩ)	I_I	V_I = GND	10.5	40.8	110.0	μA
With pull-up resistor (5 kΩ)	I_I	V_I = GND	0.08	0.41	0.80	mA
With pull-down resistor (50 kΩ)	I_I	V_I = V_{DD}	10.5	40.8	110.0	μA
Pull-up resistor (50 kΩ)[Note 3]	R_{PU}	V_I = GND	24.5	73.5	314.0	kΩ
Pull-up resistor (5 kΩ)[Note 3]	R_{PU}	V_I = GND	3.4	7.4	41.3	kΩ
Pull-down resistor (50 kΩ)[Note 3]	R_{PD}	V_I = V_{DD}	24.5	73.5	314.0	kΩ
Output voltage, low (CMOS-level output)	V_{OL}	I_{OL} = 0 mA			0.1	V
Output voltage, high (CMOS-level output)	V_{OH}	I_{OH} = 0 mA	V_{DD} – 0.1			V
Output current, low (CMOS-level output)						
3.0 mA type	I_{OL}	V_{OL} = 0.4 V	3.00			mA
6.0 mA type	I_{OL}	V_{OL} = 0.4 V	6.00			mA
9.0 mA type	I_{OL}	V_{OL} = 0.4 V	9.00			mA
12.0 mA type	I_{OL}	V_{OL} = 0.4 V	12.00			mA
18.0 mA type	I_{OL}	V_{OL} = 0.4 V	18.00			mA
24.0 mA type	I_{OL}	V_{OL} = 0.4 V	24.00			mA
Output current, high (CMOS-level output)						
3.0 mA type	I_{OH}	V_{OH} = V_{DD} – 0.4 V	–3.00			mA
6.0 mA type	I_{OH}	V_{OH} = V_{DD} – 0.4 V	–6.00			mA
9.0 mA type	I_{OH}	V_{OH} = V_{DD} – 0.4 V	–9.00			mA
12.0 mA type	I_{OH}	V_{OH} = V_{DD} – 0.4 V	–12.00			mA
18.0 mA type	I_{OH}	V_{OH} = V_{DD} – 0.4 V	–18.00			mA
24.0 mA type	I_{OH}	V_{OH} = V_{DD} – 0.4 V	–24.00			mA

Notes 1. Static current consumption increases when an I/O block with an on-chip pull-up/pull-down resistor and an oscillator are used. See **CHAPTER 4 ESTIMATING ELECTRICAL CHARACTERISTICS** for details.

2. The output short-circuit time is less than one second and for only one LSI pin.

3. The pull-up resistor and pull-down resistor values vary depending on the input and output voltages.

Remark The + and – signs of the current values in the table indicate the direction of the current. Current flowing into a device is indicated by +; current flowing out is indicated by –.

3.4.3 AC characteristics

Table 3-10 shows the AC characteristics.

The maximum operating clock frequency (f_{MAX}) of the internal cell toggle flip-flop is the value of the toggle frequency (f_{tog}) in the table. Note that the f_{MAX} varies in the actual circuit according to the circuit configuration.

Table 3-10. AC Characteristics (V_{DD} = 3.0 $\pm$0.3 V, T_A = –40 to +85°C)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Maximum toggle frequency	f_{tog}	Internal toggle F/F				
		Fan-outs = 2, wiring length = 0 mm	120			
Propagation delay time	t_{PD}	Internal gate				
		Fan-outs = 2, wiring length = 2 mm		0.42		ns
		Fan-outs = 1, standard wiring length		0.23		ns
		Fan-outs = 2, standard wiring length		0.26		ns
		Internal gate (low power gate)				
		Fan-outs = 1, standard wiring length		0.30		ns
		Fan-outs = 1, wiring length = 0 mm		0.20		ns
		Input buffer				
		Fan-outs = 1, standard wiring length		0.34		ns
		Fan-outs = 2, wiring length = 2 mm		0.47		ns
		Output buffer (FO01)				
		C_L = 15 pF		1.92		ns
Output rise time	t_r	Output buffer (FO01)				
		C_L = 15 pF		1.76		ns
Output fall time	t_f	Output buffer (FO01)				
		C_L = 15 pF		2.16		ns

3.5 Specification 2 (V$_{DD}$ = 3.3 $\pm$0.3 V, T$_A$ = –40 to +85$\degree$C)

3.5.1 Recommended operating range

Table 3-11. Recommended Operating Range (V$_{DD}$ = 3.3 $\pm$0.3 V, T$_A$ = –40 to +85$\degree$C)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Power supply voltage	V$_{DD}$			3.0	3.3	3.6	V
Input voltage, high	V$_{IH}$	CMOS interface		0.8V$_{DD}$		V$_{DD}$	V
Input voltage, low	V$_{IL}$			0.0		0.2V$_{DD}$	V
Positive trigger voltage	V$_P$		Schmitt input	1.95		2.60	V
Negative trigger voltage	V$_N$			0.75		1.20	V
Hysteresis voltage	V$_H$			0.90		1.57	V
Input voltage, high	V$_{IH}$	TTL interface		2.0		V$_{DD}$	V
Input voltage, low	V$_{IL}$			0.0		0.8	V
Positive trigger voltage	V$_P$		Schmitt input**Note**	1.35		1.78	V
Negative trigger voltage	V$_N$			0.5		0.85	V
Hysteresis voltage	V$_H$			0.85		0.93	V
Input rise time	t$_{ri}$	Normal input		0		200	ns
Input fall time	t$_{fi}$			0		200	ns
Input rise time	t$_{ri}$	Schmitt input		0		10	ms
Input fall time	t$_{fi}$			0		10	ms

Note   Schmitt input cannot be used with specification 1 (V$_{DD}$ = 3.0 $\pm$0.3 V). When using the Schmitt buffer with specification 1 (V$_{DD}$ = 3.0 $\pm$0.3 V), use a CMOS type input.

Remark   When inputting a slow signal with a long rise/fall time, noise on the signal line may affect the operation, so be sure to use a Schmitt trigger input buffer.
Because fluctuation on the power supply line due to simultaneous operation of output buffers reduces the capability of the Schmitt trigger input buffer, carefully determine pin placement.

3.5.2 DC characteristics

Table 3-12. DC Characteristics (V_{DD} = 3.3 ±0.3 V, T_A = –40 to +85°C)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Static current consumption[Note 1]	I_{DDS}	$V_I = V_{DD}$ or GND			54.7	μA
Off-state output current	I_{OZ}	$V_O = V_{DD}$ or GND			±8	μA
Output short-circuit current[Note 2]	I_{OS}	V_O = GND			–200	mA
Input leakage current						
Normal input	I_I	$V_I = V_{DD}$ or GND		±6×10^{-5}	±8	μA
With pull-up resistor (50 kΩ)	I_I	V_I = GND	14.5	59.7	135.0	μA
With pull-up resistor (5 kΩ)	I_I	V_I = GND	0.10	0.49	0.95	mA
With pull-down resistor (50 kΩ)	I_I	$V_I = V_{DD}$	14.5	59.7	135.0	μA
Pull-up resistor (50 kΩ)[Note 3]	R_{PU}	V_I = GND	22.2	55.3	248.3	kΩ
Pull-up resistor (5 kΩ)[Note 3]	R_{PU}	V_I = GND	3.2	6.7	36.0	kΩ
Pull-down resistor (50 kΩ)[Note 3]	R_{PD}	$V_I = V_{DD}$	22.2	55.3	248.3	kΩ
Output voltage, low (CMOS-level output)	V_{OL}	I_{OL} = 0 mA			0.1	V
Output voltage, high (CMOS-level output)	V_{OH}	I_{OH} = 0 mA	V_{DD} – 0.1			V
Output current, low (CMOS-level output)						
3.0 mA type	I_{OL}	V_{OL} = 0.4 V	3.00			mA
6.0 mA type	I_{OL}	V_{OL} = 0.4 V	6.00			mA
9.0 mA type	I_{OL}	V_{OL} = 0.4 V	9.00			mA
12.0 mA type	I_{OL}	V_{OL} = 0.4 V	12.00			mA
18.0 mA type	I_{OL}	V_{OL} = 0.4 V	18.00			mA
24.0 mA type	I_{OL}	V_{OL} = 0.4 V	24.00			mA
Output current, high (CMOS-level output)						
3.0 mA type	I_{OH}	$V_{OH} = V_{DD}$ – 0.4 V	–3.00			mA
6.0 mA type	I_{OH}	$V_{OH} = V_{DD}$ – 0.4 V	–6.00			mA
9.0 mA type	I_{OH}	$V_{OH} = V_{DD}$ – 0.4 V	–9.00			mA
12.0 mA type	I_{OH}	$V_{OH} = V_{DD}$ – 0.4 V	–12.00			mA
18.0 mA type	I_{OH}	$V_{OH} = V_{DD}$ – 0.4 V	–18.00			mA
24.0 mA type	I_{OH}	$V_{OH} = V_{DD}$ – 0.4 V	–24.00			mA

Notes 1. Static current consumption increases when an I/O block with an on-chip pull-up/pull-down resistor and an oscillator are used. See **CHAPTER 4 ESTIMATING ELECTRICAL CHARACTERISTICS** for details.

    2. The output short-circuit time is less than one second and for only one LSI pin.

    3. The pull-up resistor and pull-down resistor values vary depending on the input and output voltages.

Remark The + and – signs of the current values in the table indicate the direction of the current. Current flowing into a device is indicated by +; current flowing out is indicated by –.

3.5.3 AC characteristics

Table 3-13 shows the AC characteristics.

The maximum operating clock frequency (f_{MAX}) of the internal cell toggle flip-flop is the value of the toggle frequency (f_{tog}) in the table. Note that the f_{MAX} varies in the actual circuit according to the circuit configuration.

Table 3-13. AC Characteristics (V_{DD} = 3.3 $\pm$0.3 V, T_A = –40 to +85°C)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Maximum toggle frequency	f_{tog}	Internal toggle F/F				
		Fan-outs = 2, wiring length = 0 mm	130			
Propagation delay time	t_{PD}	Internal gate				
		Fan-outs = 2, wiring length = 2 mm		0.39		ns
		Fan-outs = 1, standard wiring length		0.22		ns
		Fan-outs = 2, standard wiring length		0.24		ns
		Internal gate (low power gate)				
		Fan-outs = 1, standard wiring length		0.28		ns
		Fan-outs = 1, wiring length = 0 mm		0.18		ns
		Input buffer				
		Fan-outs = 1, standard wiring length		0.31		ns
		Fan-outs = 2, wiring length = 2 mm		0.44		ns
		Output buffer (FO01)				
		C_L = 15 pF		1.76		ns
Output rise time	t_r	Output buffer (FO01)				
		C_L = 15 pF		1.62		ns
Output fall time	t_f	Output buffer (FO01)				
		C_L = 15 pF		2.02		ns

3.6 Pin Capacitance

The pin capacitance is the sum of the interface block capacitance and the package characteristic capacitance. Table 3-14 shows the capacitance (C_B) of the interface blocks. Table 3-15 shows the capacitance (C_P) of each package.

The pin capacitance is calculated by the following formula:

Pin capacitance (C_T) = interface block capacitance (C_B) + capacitance of each package (C_P)

Table 3-14. Capacitance of Interface Block (C$_B$)

(a) Input buffer

Interface Level	C$_{B(MIN.)}$ (pF)		C$_{B(MAX.)}$ (pF)	
	Normal	With Failsafe	Normal	With Failsafe
CMOS	4.0	3.50	7.0	5.0
TTL	4.0	3.50	7.0	5.0

Remark   V$_{DD}$ = 0 V; T$_J$ = 25°C; f = 1 MHz

(b) Output buffer/bidirectional buffer

Interface Level		C$_B$ (pF)					
		3 mA	6 mA	9 mA	12 mA	18 mA	24 mA
CMOS	MIN.	4.0	4.0	4.0	4.0	4.0	4.0
	MAX.	7.0	7.0	7.0	7.0	7.0	7.0

Remark   V$_{DD}$ = 0 V; T$_J$ = 25°C; f = 1 MHz

Table 3-15. Capacitance of Packages (C$_P$) (Preliminary Values)

Package	Number of Pins	Lead Pitch	Chip Size	C$_P$ (pF)
QFP	160	0.5 mm	24 $\times$ 24 mm	1.5
(fine pitch)	208	0.5 mm	28 $\times$ 28 mm	1.9
	240	0.5 mm	32 $\times$ 32 mm	2.0
	304	0.5 mm	40 $\times$ 40 mm	2.8
TQFP	48	0.5 mm	7 $\times$ 7 mm	0.9
	64	0.5 mm	10 $\times$ 10 mm	0.9
	80	0.5 mm	12 $\times$ 12 mm	0.9
LQFP	44	0.8 mm	10 $\times$ 10 mm	0.7
	100	0.5 mm	14 $\times$ 14 mm	1.0
	160	0.5 mm	24 $\times$ 24 mm	1.5

CHAPTER 4 ESTIMATING ELECTRICAL CHARACTERISTICS

This chapter explains the methodology for calculating the power consumption and propagation delay time.

4.1 Estimating Static Current Consumption

4.1.1 Estimating static current consumption

In the CMOS gate array, only a minute leakage current flows from the power supply to GND in the standby state. If a dedicated oscillation block or an I/O buffer with an on-chip pull-up/pull-down resistor is not used, the static current consumption is equal to the leakage current. On the other hand, if an I/O buffer with an on-chip pull-up/pull-down resistor is used, the static current consumption increases due to direct current flowing through that resistor according to the signal level.

In addition, when an on-chip feedback resistor-type oscillator is used and the oscillation is stopped by clamping the input pin, direct current flows into the feedback resistor, and as a result the static current consumption increases.

To calculate static current consumption, use the following equation:

$$I_{DDS(MAX.)} = I_L + I_{PD} \times m + I_{PU} \times n + I_{RF} \times k \ (\mu A)$$

I_L: Leakage current (see **Figure 4-1**)

I_{PD}: Current consumption of 50 kΩ on-chip resistor (see **Figure 4-2**)

I_{PU}: Current consumption of 5 kΩ on-chip resistor (see **Figure 4-3**)

I_{RF}: Current consumption of the on-chip feedback resistor of the oscillator (under study)

m: Total of number of signal low levels in an I/O buffer with a 50 kΩ on-chip pull-up resistor and number of signal high levels in an I/O buffer with a 50 kΩ on-chip pull-down resistor

n: Number of signal low levels in an I/O buffer with a 5 kΩ on-chip pull-up resistor

k: Number of oscillators

Figure 4-1. Leakage Current
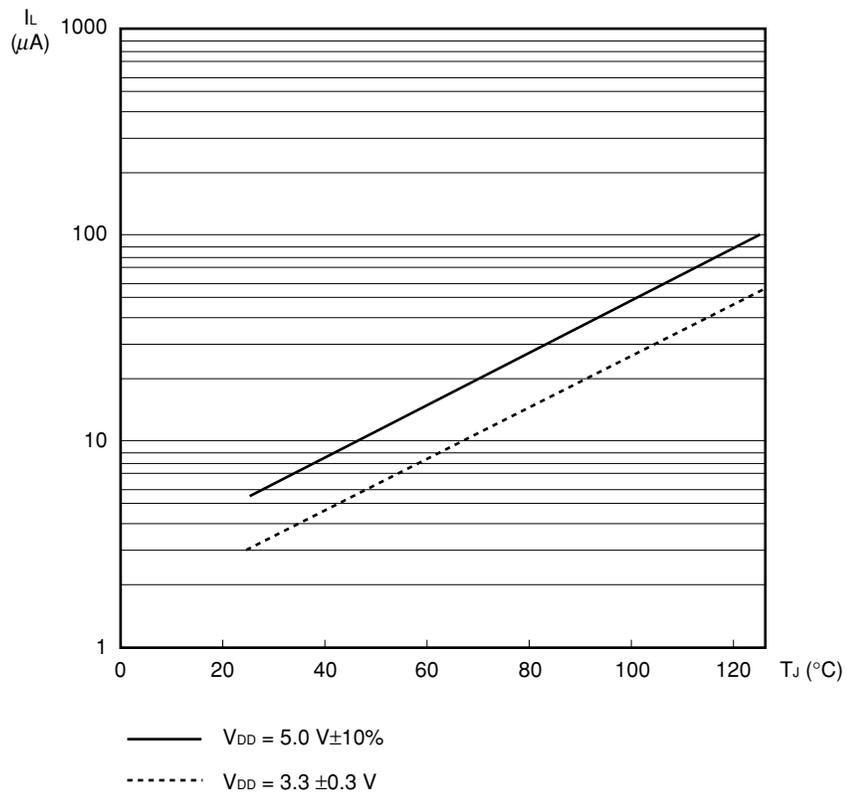
Figure 4-2. Current Consumption of On-Chip 50 kΩ Resistor (IPD)
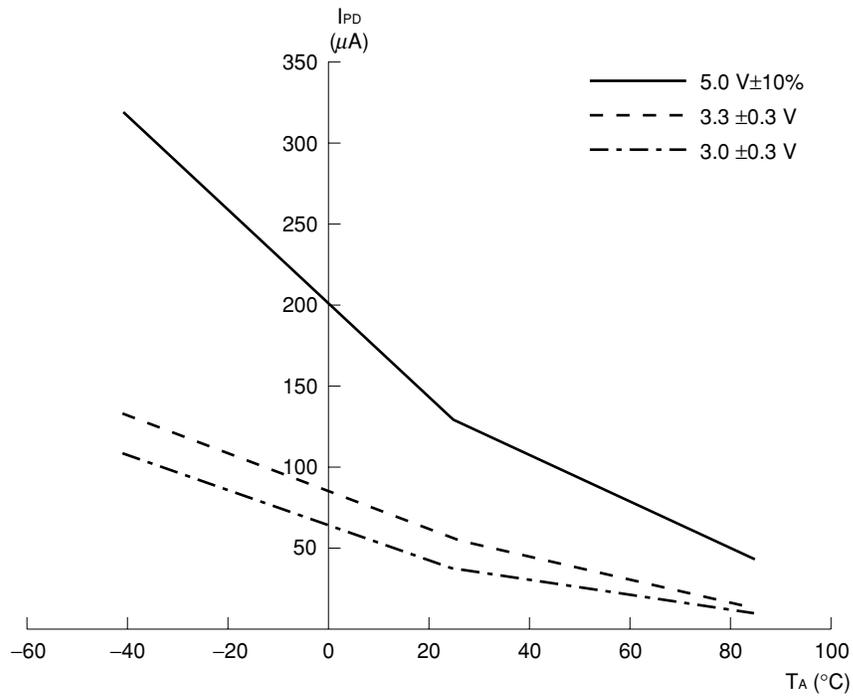
Figure 4-3. Current Consumption of On-Chip 5 kΩ Resistor (IPU)
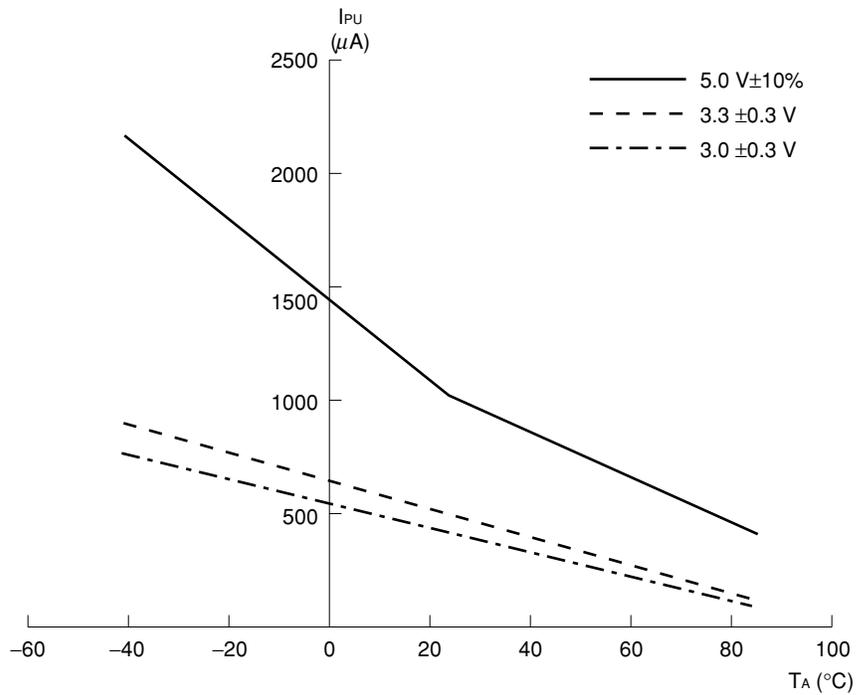
Calculation example

When V_{DD} = 5 V ±10%, T_A = 40°C, calculate the static current consumption under the following conditions.

External Pin	Signal Level	
	High	Low
Input with 5 kΩ pull-up resistor	2	0
Input with 50 kΩ pull-down resistor	2	8
Normal input	5	5
Normal output	8	2

From Figure 4-1, the leakage current is I_L = 8.6 μA.
From Figure 4-2, the current consumption in the 50 kΩ pull-down resistor is I_{PD} = 110 μA.
From the signal level, the current consumption in the 5 kΩ pull-up resistor is I_{PU} = 0.0 μA.

Therefore,

I_{DDS} = I_L + I_{PD} + I_{PU}

= 8.6 + 110 + 0.0 μA

= 118.6 μA

4.2 Input Through Current

If the input voltage (V_{IN}) is the same as the power supply voltage (V_{DD}), the input leakage current will be the same as the value listed in **CHAPTER 3 PRODUCT SPECIFICATIONS**. However, if the input voltage is lower than the power supply voltage, or if the input voltage is higher than the GND level, then a current will flow from the V_{DD} line via the P-ch transistor and N-ch transistor into the GND. This current is called the input through current. Figures 4-4 to 4-11 show the input through current (reference values) for each interface level.

Figure 4-4. Input Through Current

(V$_{DD}$ = 5.0 V CMOS Level)
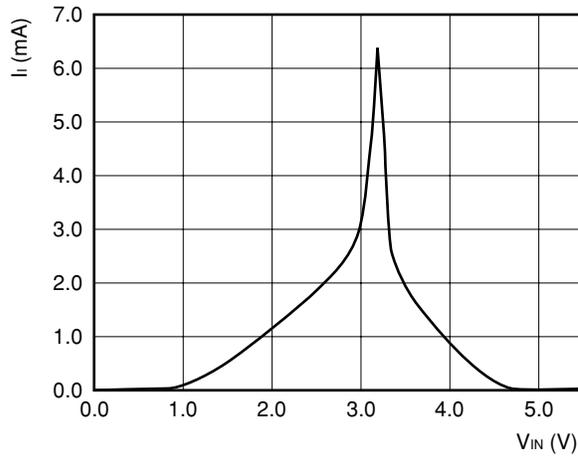
Figure 4-5. Input Through Current

(V$_{DD}$ = 5.0 V TTL Level)
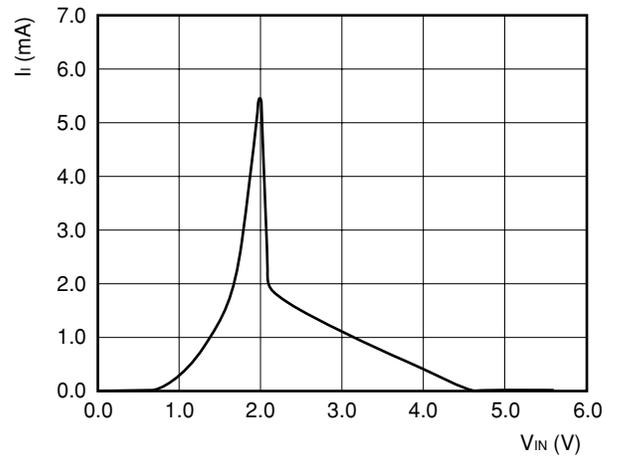
Figure 4-6. Input Through Current

(V$_{DD}$ = 5.5 V CMOS Level Schmitt[Note])

Figure 4-7. Input Through Current

(V$_{DD}$ = 5.5 V TTL Level Schmitt[Note])

Note This is a graph of the Schmitt buffer with
W in the last of the block name.
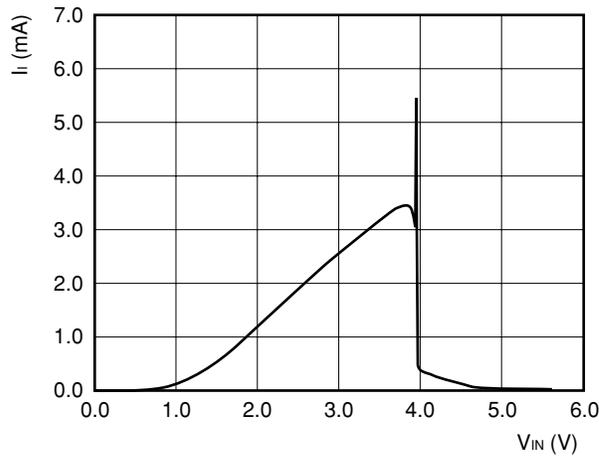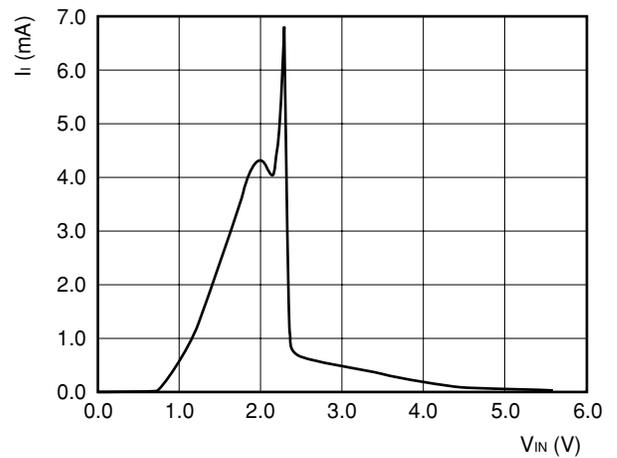
Note This is a graph of the Schmitt buffer with
W in the last of the block name.

Figure 4-8. Input Through Current
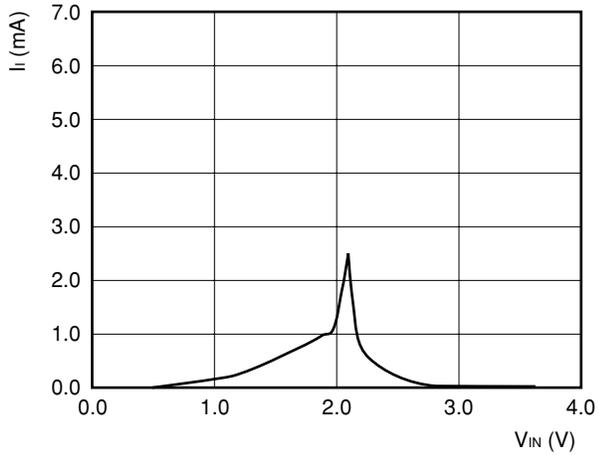
(V_{DD} = 3.6 V CMOS Level)

Figure 4-9. Input Through Current
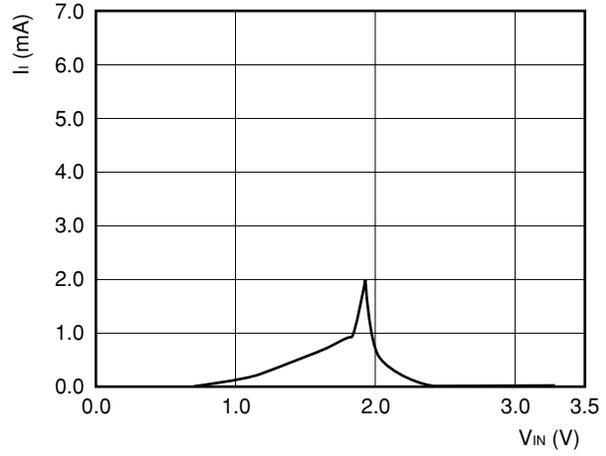
(V_{DD} = 3.3 V TTL Level)

Figure 4-10. Input Through Current

(V_{DD} = 3.6 V CMOS Level Schmitt[Note])
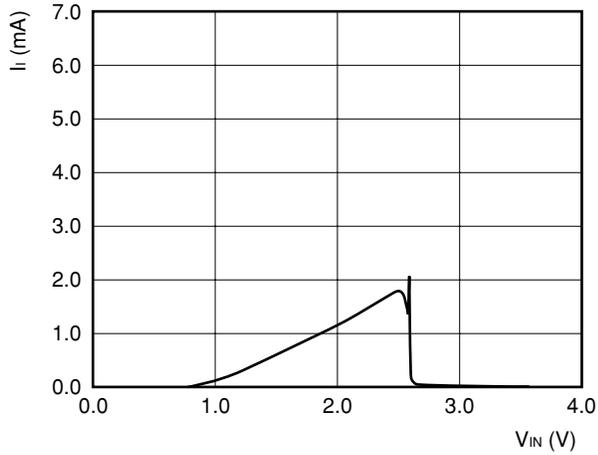
Figure 4-11. Input Through Current

(V_{DD} = 3.3 V TTL Level Schmitt[Note])
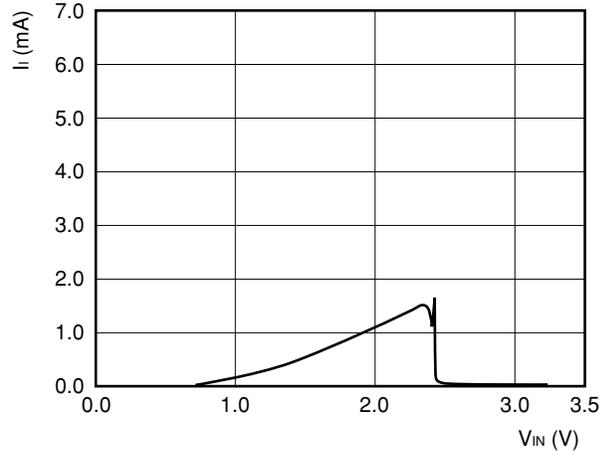
Note This is a graph of the Schmitt buffer with
W in the last of the block name.

Note This is a graph of the Schmitt buffer with
W in the last of the block name.

4.3 Power Consumption

   Although CMOS device transistors consume less power than bipolar devices, they still consume a considerable amount of power if the circuit scale is large and the operating frequency is high. Because the temperature of an LSI (chip), which has a significant influence on the reliability (life) of the LSI, rises with the power consumption, it is necessary to hold the power consumption of the LSI below a maximum.

4.3.1 Causes of power consumption

   As with standard CMOS devices, the current consumption is the sum of the following values:
   • Charge current of load capacitance connected to each transistor: i_c
   • Discharge current of load capacitance connected to each transistor: i_d
   • Through current when each transistor is switching: i_o
   • Leakage current of the device: I_L
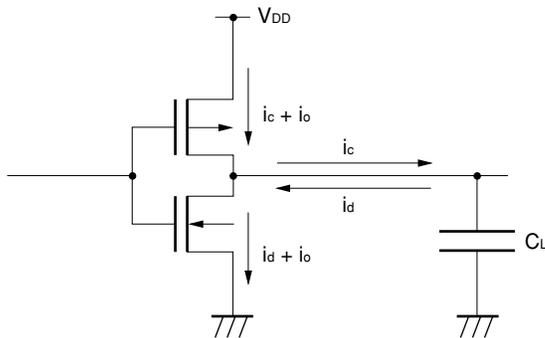
   Because there is no charge, discharge, or through current when the LSI is not operating, the power consumption of the chip is determined by the leakage current of the entire device. In as much as the charge, discharge, and through currents become extremely large compared with the leakage current when the LSI is operating, the effect of leakage current can be ignored in the chip power consumption. When the output rise (fall) time of each transistor is extremely fast compared with the input rise (fall) time, the through current increases greatly. However, the through current is normally proportional to the charge and discharge currents.

4.3.2 Estimating power consumption

Power consumption is determined by the charge, discharge, and through currents of each transistor.

However, as it is problematic to define each transistor state, a rough calculation of power consumption is made for each type of block.

The calculated results of the formulas shown below are values at $V_{DD} = 5$ V and $T_A = 85°C$; thus, adjustments must be made if the power supply or the temperature is different.

Total power consumption (P_D) $P_D = \Sigma P_{DCELL} + \Sigma P_{DM} + \Sigma P_{DI} + \Sigma P_{DO} + \Sigma P_{DCTS} + \Sigma P_{OSC}$

(1) ΣP_{DCELL} .... Internal cell power consumption (excluding the cells used by memory and interface block)

$\Sigma P_{DCELL} = \Sigma (4.52^{\textbf{Note 1}} \times f \times Cell \times A) (\mu W)$

f: Operating frequency (MHz)
$Cell$: Number of cells operating at frequency f
A: Gate operating factor[Note 2]

(2) ΣP_{DM} .... Memory block power consumption

RAM block power consumption

$\Sigma P_{DRAM} = \Sigma (P_{RM} \times f_{RM} \times R_{RM} + P_{WM} \times f_{WM} \times R_{WM}) (mW)$

P_{RM}: Unit power consumption during read (mW/MHz)[Note 3]
f_{RM}: Operating frequency during read
R_{RM}: Operating factor during read[Note 4]
P_{WM}: Unit power consumption during write (mW/MHz)[Note 3]
f_{WM}: Operating frequency during write
R_{WM}: Operating factor during write[Note 4]

(3) ΣP_{DI} .... Input buffer and bidirectional buffer input power consumption

$\Sigma P_{DI} = \Sigma (P_I \times f + P_{CONST}) \times Buffer (\mu W)$

P_I: Power consumption for each input buffer (μW/Buffer/MHz)
Refer to **Table 4-1**.
f: Operating frequency (MHz)
P_{CONST}: Constant power consumption[Note 6]
Buffer: Number of input buffers and bidirectional buffer inputs operating at frequency f
If input buffer operation is intermittent, use the average operating frequency (f_A)[Note 5]

Table 4-1. Power Consumption by Input Buffer

Block Type	P_I
FI01	16.8470
FI02	17.4223
FIS1	20.8117
FIS2	17.9722
FIA1	5.2705
FIA2	5.3776
FIE1	10.4223
FIE2	7.4192
FIS1W	12.3430
FIS2W	10.6810

Remark   The same power consumption value
is applied to the same type buffer.

(4) ΣP_{DO} .... Output buffer and bidirectional buffer output power consumption

$$\Sigma\ P_{DO} = \Sigma\ \{(P_O + P_{CO} \times C_L) \times f + P_{CONST}\} \times Buffer\ (mW)$$

P_O: Power consumption for each output buffer (without load) (mW/MHz)
Refer to **Table 4-2**.

P_{CO}: Power consumption for each output buffer (load dependent) (mW/MHz/pF)
Refer to **Table 4-2**.

C_L: Load capacitance

f: Operating frequency (MHz)
If output buffer operation is intermittent, use the average operating frequency (f_A)[Note 5]

P_{CONST}: Constant power consumption[Note 6]

Buffer: Number of output buffers and bidirectional buffer outputs operating at frequency f

Table 4-2. Output Buffer Power Consumption

Block Type	P_O	P_{CO}
FO09	0.2257	0.0264
FO04	0.2374	0.0268
FO01	0.2984	0.0271
FO02	0.3829	0.0272
FO03	0.6270	0.0263
FO06	1.0067	0.0254
FE09	0.1675	0.0271
FE04	0.1621	0.0275
FE01	0.2461	0.0266
FE02	0.2598	0.0265
FE03	0.4336	0.0266
FE06	0.7298	0.0255

(5) ΣP_DCTS .... Clock tree synthesis power consumption

$$\Sigma\ \mathrm{P_{DCTS}} = \Sigma\ \mathrm{P_{CTS}}\ (\mu W)$$

f: Operating frequency (MHz)
FF: Number of flip-flops

FC42: $\mathrm{P_{CTS}} = 6.73 \times (\mathrm{FF} \times 0.057) \times f$
FC82: $\mathrm{P_{CTS}} = 6.73 \times (\mathrm{FF} \times 0.114) \times f$
FC44: $\mathrm{P_{CTS}} = 6.73 \times (\mathrm{FF} \times 0.077) \times f$
FC84: $\mathrm{P_{CTS}} = 6.73 \times (\mathrm{FF} \times 0.154) \times f$

(6) ΣP_OSC .... Oscillator power consumption

$$\Sigma\ \mathrm{P_{OSC}} = \mathrm{P_{OSC1}} \times \text{number of oscillators (1 or 2) (mW)}$$

P_OSC1: Power consumption per one oscillator (mW/MHz)

The power consumption of the oscillator is shown in Table 4-3. The values in Table 4-3 are reference values because the power consumption of the oscillator varies greatly depending on the resonator and constant.

Table 4-3. Oscillator Power Consumption (Reference Values) (V_DD = 5.0 V ±10%, T_A = −40 to +85°C)

Frequency (MHz)	External Constant Used				Duty (%)	V_START (V)	V_HOLD (V)	P_OSCS (mW)
	C_in (pF)	C_out (pF)	LT (μH)	CT (pF)				
4	100	100			53.0	1.97	1.97	27.50
8	68	68			51.2	1.23	1.23	33.00
16	39	39			50.7	2.23	2.20	63.25
32	15	15			53.6	2.17	2.14	107.25

V_START: Oscillation start voltage
V_HOLD: Oscillation hold voltage

Evaluation using an evaluation sample is required to determine the power consumption.
The oscillator configuration diagram is shown in Figure 4-12.

Figure 4-12. Oscillator Configuration Diagram
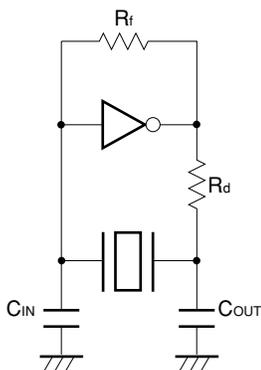
Notes 1. The power consumption per cell (μW/Cell/MHz) is specified under the following conditions:

<1> Assume that the ratio of combination circuits, flip-flops, and latches in the circuit is as follows: Gates : Flip-flops : Latches = 0.5 : 0.4 : 0.1.

<2> Assume that the data frequency of latches is 1 MHz and that they operate 40% of the total time that the gates are active.

<3> Assume that the clock frequency of flip-flops is 1 MHz and the data frequency is 0.25 MHz.

<4> Assume that the load of each output is Σ F/I = 2, L = 1.64 (F/I equivalent).

See **APPENDIX A POWER CONSUMPTION (PRELIMINARY)** if conditions have been modified to review the power consumption.

2. Gate operating factor

This is the percentage of the cells of the entire circuit that are operating in the same general time period.

For example, if 30% of the gates of a circuit are operating in the same period, the operating factor is 0.3.

3. Unit power consumption (under study)

The numerical values are listed in **4.3.3 Unit power consumption of memory**.

4. Write and read operating factors
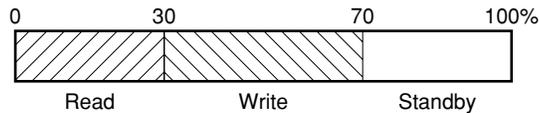
For example, if the RAM operating percentage is as shown in the figure above, then,
R_{RM} = 0.3 and R_{WM} = 0.4

5. Average operating frequency (f_A)

If operation is intermittent, the average operating frequency (f_A) can be investigated.

$$f_A = f_M \times T_M \div T_T$$

T_M: Actual operating interval

T_T: Intermittent operating cycle

f_M: Operating frequency of actual
operating interval
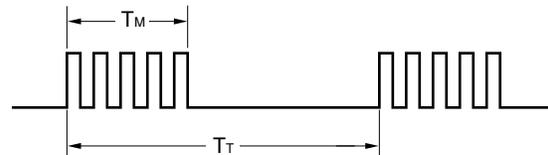
Notes 6. Constant power consumption
If direct current is flowing through the input, output, and bidirectional buffers, a constant power
consumption is added.

Example 1. Direct current via the pull-up/pull-down resistor

$$P_{CONST} = (V_{DD}^2/R) \times A$$

V_{DD}: Power supply voltage
  R: Pull-up/pull-down resistance
Use a typical value if the resistor
is incorporated in the LSI
  A: Operating factor
Low-level percentage when using a pull-up resistor, or high-level percentage
when using a pull-down resistor
The user should specify the operating factor based on the circuit specifications
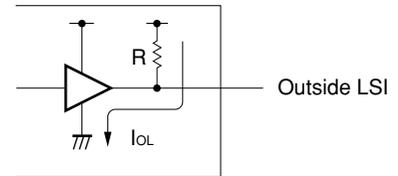
Example 2. To drive items that require a large current, such as LEDs

$$P_{CONST} = V_O \times I_O \times A$$

V_O: Output voltage
I_O: Output current
  A: Percentage of LED ON time
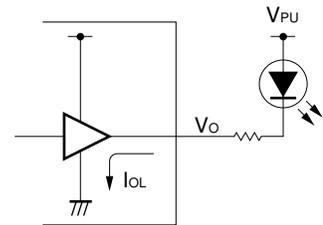
V_{PU}: Pull-up voltage

4.3.3 Unit power consumption of memory

In the calculation formula for memory block power consumption in **4.3.2 Estimating power consumption**, use the following values.

(1) Single-port RAM

Unit: mW/MHz

Unit: mW/MHz

RAM Name	P_{WM}	P_{RM}
RB47	0.261	0.188
RB49	0.285	0.198
RB4B	0.570	0.396
RB4D	0.336	0.191
RB4F	0.672	0.382
RB4H	1.344	0.764
RB4M	2.688	1.528
RB4S	5.376	3.056
RB87	0.522	0.376
RB89	0.570	0.396
RB8B	0.579	0.359
RB8D	0.672	0.382
RB8F	0.735	0.380
RB8H	1.470	0.760
RB8M	2.940	1.520
RBAB	0.689	0.420
RBAD	1.378	0.840
RBAF	2.756	1.680
RBAH	5.512	3.360
RBC7	1.044	0.752
RBC9	1.140	0.792
RBCB	1.158	0.718
RBCD	1.344	0.764
RBCF	1.470	0.760
RBCH	2.940	1.520
RBCM	5.880	3.04
RBEB	1.378	0.840
RBED	2.756	1.680
RBEF	5.512	3.360
RBEH	11.024	6.720
RBH7	2.088	1.504
RBH9	2.280	1.584
RBHB	2.316	1.436
RBHD	2.688	1.528
RBHF	2.940	1.520

RAM Name	P_{WM}	P_{RM}
RBHH	5.880	3.04
RBKB	2.756	1.680
RBKD	5.512	3.360
RBKF	2.895	1.795
RBKH	5.790	3.590

Remark P_{WM}: Power consumption during write operation

P_{RM}: Power consumption during read operation

(2) Dual-port RAM

Unit: mW/MHz

RAM Name	P_{WM}	P_{RM}
R947	0.256	0.079
R949	0.280	0.085
R94B	0.560	0.170
R94D	0.314	0.075
R94F	0.628	0.150
R94H	1.256	0.300
R987	0.512	0.158
R989	0.560	0.170
R98B	0.561	0.176
R98D	0.628	0.150
R98F	0.630	0.182
R9AB	0.654	0.211
R9AD	1.308	0.422
R9C7	1.024	0.316
R9C9	1.120	0.340
R9CB	1.122	0.352
R9CD	1.256	0.300
R9CF	1.260	0.364
R9EB	1.308	0.422
R9ED	2.616	0.844
R9H7	2.048	0.632
R9H9	2.240	0.680
R9HB	2.244	0.704
R9KB	2.616	0.844

Remark P_{WM}: Power consumption during write operation
  P_{RM}: Power consumption during read operation

4.3.4 Compensation method

The results calculated by the formulas in **4.3.2 Estimating power consumption** are values for V_{DD} = 5.0 V and T_A = 85°C. If different power supply or operating ambient temperature specifications are used, adjustments must be calculated using the following equation.

$$P_W = (P_D \times K_1 + \Sigma P_{CONST} \times K_2) \times K_3$$

P_D: Calculated result of total power consumption (including constant power consumption)
ΣP_{CONST}: Sum of constant power consumption only
K_1: Compensation coefficient (refer to **Table 4-4**)
K_2: Compensation coefficient (refer to **Table 4-4**)
K_3: Compensation coefficient (refer to **Table 4-4**)

The TYP. value is usually used to determine the power consumption.
However, the MAX. value is used when high reliability is demanded.
The MAX. value can also be used to calculate the maximum power consumption value in each power supply and temperature specification range.

Table 4-4. Compensation Coefficient (K_1, K_2, K_3)

(a) V_{DD} = 5.0 V $\pm$10%, T_A = –40 to +85°C

	TYP. Value	MAX. Value
Compensation coefficient (K_1)	1.00	1.40
Compensation coefficient (K_2)	0.00	0.15
Compensation coefficient (K_3)	1.00	1.00

(b) V_{DD} = 3.3 $\pm$0.3 V, T_A = –40 to +85°C

	TYP. Value	MAX. Value
Compensation coefficient (K_1)	1.0000	1.4000
Compensation coefficient (K_2)	0.0000	0.1500
Compensation coefficient (K_3)	0.4356	0.4356

(c) V_{DD} = 3.0 $\pm$0.3 V, T_A = –40 to +85°C

	TYP. Value	MAX. Value
Compensation coefficient (K_1)	1.00	1.40
Compensation coefficient (K_2)	0.00	0.15
Compensation coefficient (K_3)	0.36	0.36

4.3.5 Determining power consumption

The power consumption is determined on the basis of whether or not the calculated power consumption (P_D) is within the maximum allowable power consumption (P_{WL}) specified for each package and master.

The maximum allowable power consumption (P_{WL}) specified for each package and master is listed in **CMOS Gate Array, Embedded Array Package Design Manual (A16400E)**.

$$P_D \leq P_{WL}$$

The values in **CMOS Gate Array, Embedded Array Package Design Manual (A16400E)** are for $T_A = -40$ to $+85°C$ with natural convection. If a different maximum operating ambient temperature is used, the maximum allowable power consumption for the environment used must be calculated by means of the maximum junction temperature ($T_{J\,(MAX.)}$), the maximum ambient temperature ($T_{A\,(MAX.)}$), and the thermal resistance (θ_{ja}) specified for each package and master. The thermal resistance (θ_{ja}) for each package and master is listed in the tables concerning thermal resistance in **CMOS Gate Array, Embedded Array Package Design Manual (A16400E)**. Thermal resistance was measured under the conditions of a 90×90 mm by 1.6 mm thick sample mounted on a glass-epoxy circuit board.

$$P_{WL} = \frac{(T_{J\,(MAX.)} - T_{A\,(MAX.)})}{\theta_{ja}} \ (W)$$

Condition: $T_{A\,(MAX.)} \geq 40°C$

4.4 Propagation Delay Time

4.4.1 Accuracy of propagation delay time

The propagation delay time (t_{PD}) of a CMOS gate array fluctuates due to I/O buffers, internal function blocks, and the following factors:

Factors fluctuating propagation delay time
- Load capacitance (number of fan-outs, wiring capacitance)
- Power supply voltage
- Operating ambient temperature
- Manufacturing variation
- Other circuit-based factors

Circuit-based causes other than those related to power supply voltage, operating ambient temperature, and load capacitance include: fluctuation due to the input signal waveform, fluctuation in the equivalent input capacitance of the transfer gate, the Miller effect, and fluctuation in the input threshold voltage. NEC Electronics has introduced delay simulators and static delay calculators, taking these fluctuation factors into consideration as much as possible, so that a more precise propagation delay can be calculated. Thus, rough calculations of propagation delay time made by the user may not match the numerical values listed in the **CMOS-N5 Series (5.0 V) Block Library (A13872E)** and **CMOS-N5 Series (3.3 V) Block Library (A15895E)**.

4.4.2 Calculation in propagation delay time

The calculation formula shown below is rough and simplified. The calculation results are comparatively accurate for a load range that satisfies the following conditions. The larger the load capacitance, the larger the error becomes and the smaller the calculated numerical result of the simulator becomes. With this prior understanding, this formula can be used as a guide.

> Conditions   The sum of the prestage F/I of the block, which is the object of the delay calculation, is within 15% of the F/O limit of the prestage drive block.

Example
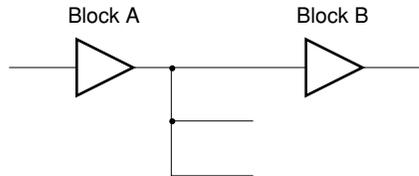
Let Block B be the object of the propagation calculation. The accuracy of the simplified calculation formula is high when the sum of the F/I connected to the output of block A is within 15% of the block A F/O limit.

If these details or the above conditions are not applicable, see **APPENDIX B PROPAGATION DELAY TIME** for methods to improve the calculation accuracy. The delay data for each block that is needed for the calculation is listed in the **CMOS-N5 Series (5.0 V) Block Library (A13872E)** and **CMOS-N5 Series (3.3 V) Block Library (A15895E)**.

(1) Input buffer and internal function block delay time

The delay time of the internal function block and memory blocks can be calculated roughly from the load (number of fan-outs) connected to that output pin and the wiring length (wiring capacitance).

$$t_{PD} = t_{LD0} + (\Sigma\ F/O + L) \times t_1\ \ (ns)$$

t_{LD0}: Delay time of the block itself with F/O = 0 and L = 0

$\Sigma F/O$: Number of fan-outs of the relevant output pins

L: Wiring capacitance connected to the relevant output pins

(see **4.4.3 Estimating wiring capacitance**)

t_1: Delay coefficient of the relevant output pins

(2) Internal bus delay time

$$t_{PD} = t_{LD0} + \{\Sigma\ F/O + L + (N - 1) \times 1.38\} \times t_1\ \ (ns)$$

t_{LD0}: Delay time of the block itself with F/O = 0 and L = 0

$\Sigma F/O$: Number of fan-outs connected to the bus

N: Sum of 3-state output buffers (F531, F532) connected to the bus

L: Wiring capacitance connected to the relevant output pins

(see **4.4.3 Estimating wiring capacitance**)

t_1: Delay coefficient of the relevant output pins

(3) Output buffer delay time

Using the following equation, the output buffer delay time can be roughly calculated from the load capacitance connected to the output pin.

$$t_{PD} = t_{LD0} + T \times C_L \quad (ns)$$

t_{LD0}: Delay time of the block itself with $C_L = 0$ pF
C_L: Load capacitance connected to the relevant output pin
T: Delay coefficient of the relevant output pin

The I/O buffer delay time is calculated under the following condition.
CMOS level interface: Threshold voltage = $1/2V_{DD}$

4.4.3 Estimating wiring capacitance

Since placement and routing is performed on the master based on the circuit connection information, the physical wiring length that is connected as a function block load is unknown before placement and routing of the gate array. Therefore, an estimation of the wiring lengths is made in order to calculate the propagation delay time before placement and routing. The wiring length estimation is calculated statistically based on the results of actual layouts, and most of the wiring length (70% of all routing) becomes shorter than the value specified as an assumed wiring length.

Table 4-5 shows estimated values of assumed wiring capacitances for the CMOS-N5 Series.

Placement and routing are executed for each hierarchical macro (top hierarchy). Consequently, wiring lengths within macros are shorter than wiring lengths between macros. The assumed wiring length is treated by the delay simulator in two categories: intramacro and intermacro. Table 4-5 shows top hierarchy intermacro estimates.

Table 4-5. Wiring Capacitance Estimate (Wiring Length Converted to F/I Value)

(1/2)

Master	Pin-Pair Count					
	1	2	3	4	5	6
μPD65891	1.297	2.613	3.929	5.245	6.560	7.876
μPD65880	1.621	3.266	4.911	6.556	8.200	9.845
μPD65881	1.641	3.356	5.070	6.785	8.500	10.214
μPD65892	1.674	3.423	5.171	6.921	8.670	10.418
μPD65882	1.684	3.552	5.421	7.289	9.158	11.027
μPD65894	1.718	3.623	5.529	7.435	9.341	11.248
μPD65883	1.730	3.767	5.803	7.840	9.876	11.913
μPD65884	1.757	3.892	6.026	8.161	10.295	12.430
μPD65885	1.780	3.997	6.213	8.430	10.647	12.863
μPD65887	1.819	4.175	6.532	8.889	11.245	13.602
μPD65889	1.861	4.372	6.883	9.393	11.904	14.414
μPD65890	1.904	4.569	7.233	9.897	12.562	15.226
μPD65893	1.943	4.747	7.552	10.356	13.160	15.965

(2/2)

Master	Pin-Pair Count					
	7	8	9	10	11 to 15	16 to 20
μPD65891	9.192	10.508	11.823	13.139	19.718	26.297
μPD65880	11.490	13.135	14.779	16.424	24.648	32.871
μPD65881	11.929	13.644	15.358	17.073	25.647	34.220
μPD65892	12.168	13.917	15.665	17.414	26.160	34.904
μPD65882	12.895	14.764	16.632	18.501	27.844	37.187
μPD65894	13.153	15.059	16.965	18.871	28.401	37.931
μPD65883	13.949	15.986	18.022	20.059	30.241	40.424
μPD65884	14.564	16.699	18.833	20.967	31.640	42.312
μPD65885	15.080	17.297	19.513	21.730	32.813	43.897
μPD65887	15.958	18.315	20.672	23.028	34.811	46.594
μPD65889	16.925	19.435	21.946	24.456	37.009	49.561
μPD65890	17.891	20.555	23.220	25.884	39.206	52.528
μPD65893	18.769	21.574	24.378	27.182	41.204	55.226

4.4.4 Fluctuation in propagation delay time

The propagation delay time (t_{PD}) fluctuates due to I/O buffers and internal function blocks, and a variety of other reasons, as described in **4.4.1 Accuracy of propagation delay time**. The **CMOS-N5 Series (5.0 V) Block Library (A13872E)** and **CMOS-N5 Series (3.3 V) Block Library (A15895E)** indicates the minimum and maximum values under the conditions:

V_{DD} = 5.0 V ±10%/V_{DD} = 3.3 ±0.3 V and T_A = −40 to +85°C (T_J = −40 to +125°C)

The difference between the typical value and these values is called the degrading factor. The propagation delay coefficient is listed for the minimum, typical, and maximum specifications in the CMOS-N5 Series.

With the CMOS-N5 Series, the degrading factor of each block is studied to improve the accuracy of calculation of the propagation delay time. Therefore, a uniform degrading factor cannot be used, unlike with conventional products. However, Figure 4-13 (a) through (c) shows, for reference, the dependency of the delay coefficient on the power supply voltage and operating junction temperature. The coefficient of the degrading factor can be recalculated by limiting the operating ambient temperature and power consumption (for example, by limiting the temperature rise due to power consumption to about 10°C). The operating junction temperature when the operating ambient temperature or power consumption is limited can be calculated by the formula below. The lower the operating junction temperature, the closer to 1 the coefficient of the degrading factor (if the operating junction temperature is limited to 100°C, the delay time is 5% shorter than when the operating junction temperature is limited to 125°C).

$$T_J = T_{A(MAX.)} + P_D \times \theta_{ja} \ \ (°C)$$

T_J: Operating junction temperature

$T_{A(MAX.)}$: Maximum value of operating ambient temperature

P_D: Power consumption estimated by the calculation formula in **4.3.2 Estimating power consumption**

θ_{ja}: Thermal resistance (See the tables concerning thermal resistance in **CMOS Gate Array, Embedded Array Package Design Manual (A16400E)**)

Please note that since Figure 4-13 (a) through (c) shows the average values of the delay distribution (variations in the process are already included in the value of the power supply voltage), **the guaranteed values are the result of simulation**.

Reference data

$$R_{MAX} = R_{V(MAX.)} \times R_{T(MAX.)}$$

$$R_{MIN} = R_{V(MIN.)} \times R_{T(MIN.)}$$

$$t_{PD(MAX)} = t_{PD(TYP.)} \times R_{MAX.}$$

$$t_{PD(MIN)} = t_{PD(TYP.)} \times R_{MIN.}$$

Standard specification: CMOS interface condition (V_{DD} = 5.0 V ±10%, T_A = −40 to +85°C (T_J = −40 to +125°C))

$R_{MAX.}$ = 2.05

$R_{MIN.}$ = 0.64

Calculation example

Derive $R_{MAX.}/R_{MIN.}$ for V_{DD} = 5.0 V ±10 % and T_A = −40 to +85°C (T_J = −40 to +120°C).

(1) Derive R_V from Figure 4-13 (a) and (b):

$R_{V\ (MAX.)}$ = 1.44

$R_{V\ (MIN.)}$ = 0.62

(2) Next, derive R_T from Figure 4-13 (c):

$R_{T\ (MAX.)}$ = 1.42

$R_{T\ (MIN.)}$ = 1.04

(3) Accordingly, it follows that,

$R_{MAX.}$ = $R_{V\ (MAX.)} \times R_{T\ (MAX.)}$ = 1.44 × 1.42

$R_{MIN.}$ = $R_{V\ (MIN.)} \times R_{T\ (MIN.)}$ = 0.62 × 1.04

$R_{MAX.}$ = 2.044

$R_{MIN.}$ = 0.645

Figure 4-13. Propagation Delay Time

(a) V$_{DD}$ dependency (MAX.)

Voltage coefficient R$_V$

$$R_{V\,(MAX.)} = 3.283 - 0.4094 V_{DD}$$

V$_{DD}$ (V)

(b) V$_{DD}$ dependency (MIN.)

Voltage coefficient R$_V$

$$R_{V\,(MIN.)} = 2.261 - 0.2978 V_{DD}$$

V$_{DD}$ (V)

(c) T$_J$ dependency

Temperature coefficient R$_T$

T$_J$ (°C)

| $-40 \leq T_J \leq 25°C$ | $R_{T\,(MIN.)} = 0.948 + 0.0021 T_J$ |
| $25 \leq T_J \leq 85°C$ | $R_{T\,(MAX.)} = 0.8879 + 0.0045 T_J$ |
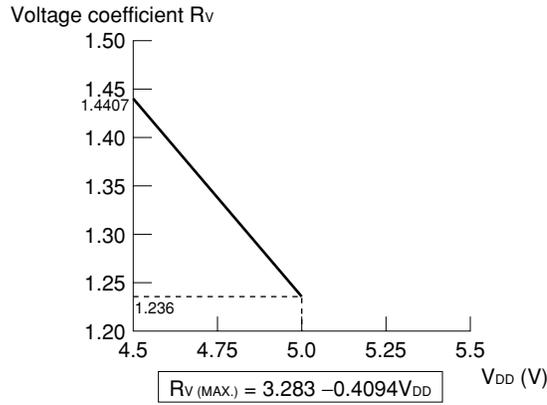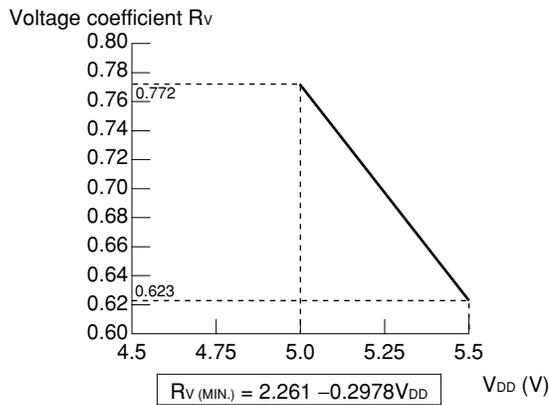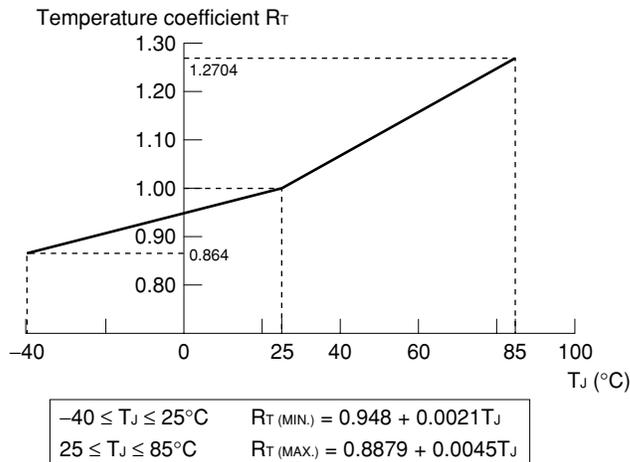
In addition to the degrading factor applicable from the device specification, there is also the relative variation generated by the chips internal paths and by the manufacture of the P-ch and N-ch transistors. This relative variation is an important factor in verifying the timing of the circuit. The CMOS-N5 Series's relative variation is as follows (this also applies when the power supply voltage specification is 3.3 V).

Relative variation α = 10%

Figure 4-14 shows the variation with $t_{PD(TYP.)}$ as the typical value.

Figure 4-14. t_{PD} Variation
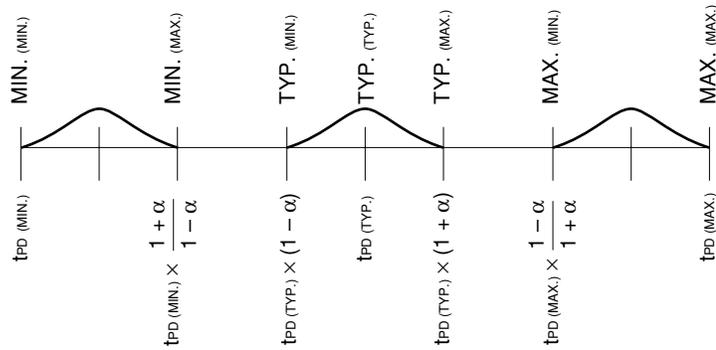
4.5 Output Buffer Characteristics

4.5.1 Output buffer rise and fall times

The rise and fall times of the output buffer vary greatly according to differences in the drive capability due to the output level and to the connected load capacitance. The output buffer rise and fall times (t_r, t_f) can be calculated as follows:

$$t_r = t_{r0} + F_{tr} \times C_L \text{ (ns)}$$

$$t_f = t_{f0} + F_{tf} \times C_L \text{ (ns)}$$

t_{r0}:   Reference rise time (load capacitance, C_L = 0 pF)

t_{f0}:   Reference fall time (load capacitance, C_L = 0 pF)

F_{tr}, F_{tf}: Load capacitance coefficient

C_L: Load capacitance (pF) ($0 < C_L \leq 300$ pF)

Refer to Tables 4-6 and 4-7 for output buffer coefficients.

Table 4-6. t_r and t_f Calculation Coefficients of Output Buffer (V_{DD} = 5.0 V, T_A = 25°C)

Buffer Type	Output Level	Drive Capability	t_{r0}	F_{tr}	t_{f0}	F_{tf}
Normal type	CMOS	I_{OL} = 3.0 mA	0.817	0.1562	1.279	0.2654
		I_{OL} = 6.0 mA	0.611	0.1035	0.716	0.1319
		I_{OL} = 9.0 mA	0.502	0.0611	0.603	0.0867
		I_{OL} = 12.0 mA	0.388	0.0510	0.443	0.0651
		I_{OL} = 18.0 mA	0. 394	0.0345	0.494	0.0426
		I_{OL} = 24.0 mA	0.413	0.0266	0.623	0.0305
Low-noise type	CMOS	I_{OL} = 3.0 mA	1.210	0.1532	1.554	0.2621
		I_{OL} = 6.0 mA	1.112	0.1018	1.118	0.1296
		I_{OL} = 9.0 mA	1.097	0.0631	0.990	0.0876
		I_{OL} = 12.0 mA	1.116	0.0542	0.938	0.0678
		I_{OL} = 18.0 mA	1.213	0.0415	0.935	0.0492
		I_{OL} = 24.0 mA	1.333	0.0352	1.013	0.0389

Remark The rise and fall times of the output buffer are specified by the following conditions:
CMOS level = $V_{DD} \times 10\%$ to $V_{DD} \times 90\%$, input signal t_r, t_f = 0.4 ns (V_{DD} = 5.0 V)

Table 4-7. t_r and t_f Calculation Coefficients of Output Buffer (V_{DD} = 3.3 V, T_A = 25°C)

Buffer Type	Output Level	Drive Capability	t_{r0}	F_{tr}	t_{f0}	F_{tf}
Normal type	CMOS	I_{OL} = 3.0 mA				
		I_{OL} = 6.0 mA	0.817	0.1562	1.279	0.2654
		I_{OL} = 9.0 mA	0.611	0.1035	0.716	0.1319
		I_{OL} = 12.0 mA	0.502	0.0611	0.603	0.0867
		I_{OL} = 18.0 mA	0.388	0.0510	0.443	0.0651
		I_{OL} = 24.0 mA	0. 394	0.0345	0.494	0.0426
Low-noise type	CMOS	I_{OL} = 3.0 mA				
		I_{OL} = 6.0 mA	1.210	0.1532	1.554	0.2621
		I_{OL} = 9.0 mA	1.112	0.1018	1.118	0.1296
		I_{OL} = 12.0 mA	1.097	0.0631	0.990	0.0876
		I_{OL} = 18.0 mA	1.116	0.0542	0.938	0.0678
		I_{OL} = 24.0 mA	1.213	0.0415	0.935	0.0492

Remarks **1.** The rise and fall times of the output buffer are specified by the following conditions:
CMOS level = $V_{DD} \times 10\%$ to $V_{DD} \times 90\%$, input signal t_r, t_f = 0.4 ns (V_{DD} = 3.3 V)
2. Blank: Under study

4.5.2 Recommended load capacitance range of output buffers

The maximum allowable load capacitance $C_{L(MAX.)}$ of the output buffer should be $C_{L(MAX.)} \leq 300$ pF. In addition, Tables 4-8 and 4-9 show the recommended load capacitance range for each drive capability of the output buffer. The optimal output buffer based on Tables 4-8 and 4-9 should be selected. In particular, if a load capacitance outside the recommended range is used, it must be noted that the overshoot and undershoot generated in the output signal increases if a lower load capacitance is used.

Table 4-8. Recommended Load Capacitance Ranges of Output Buffers (@5.0 V)

Buffer Type	Output Level	I_{OL} (mA)	Recommended Load Capacitance Range (pF)	Example of Corresponding Block
Normal type	CMOS	3.0	0 to 40	FO09
		6.0	0 to 110	FO04
		9.0	25 to 130	FO01
		12.0	100 to 210	FO02
		18.0	120 to 300	FO03
		24.0	170 to 300	FO06
Low-noise type	CMOS	3.0	0 to 40	FE09
		6.0	0 to 100	FE04
		9.0	15 to 150	FE01
		12.0	20 to 200	FE02
		18.0	50 to 200	FE03
		24.0	40 to 210	FE06

Table 4-9. Recommended Load Capacitance Ranges of Output Buffers (@3.3 V)

Buffer Type	Output Level	I_{OL} (mA)	Recommended Load Capacitance Range (pF)	Example of Corresponding Block
Normal type	CMOS	3.0	0 to 20	FO09
		6.0	0 to 40	FO04
		9.0	0 to 110	FO01
		12.0	25 to 130	FO02
		18.0	100 to 210	FO03
		24.0	120 to 300	FO06
Low-noise type	CMOS	3.0	0 to 20	FE09
		6.0	0 to 40	FE04
		9.0	0 to 100	FE01
		12.0	15 to 150	FE02
		18.0	20 to 200	FE03
		24.0	50 to 200	FE06

4.5.3 Maximum operating frequency of output buffers

The maximum operating frequency of the output buffer is determined by the drive capability and the load capacitance. As explained in **4.5.2 Recommended load capacitance range of output buffers**, there are recommended ranges for load capacitance. The shaded parts of the graphs in Figures 4-15 and 4-16 correspond to these ranges.

The parts to the right of the shaded part can be used if there are no problems with the propagation delay time, rise time, and fall time. On the other hand, be aware that the overshoot and undershoot in the parts to the left of the shaded part are large.

Figure 4-15. $f_{MAX.}$ vs. C_L Limit (CMOS Level Output) (1/2)

(a) I_{OL} = 3.0 mA (@3.3 V)

(b) I_{OL} = 3.0 mA (@5.0 V)
I_{OL} = 6.0 mA (@3.3 V)

(c) I_{OL} = 6.0 mA (@5.0 V)
I_{OL} = 9.0 mA (@3.3 V)

(d) I_{OL} = 9.0 mA (@5.0 V)
I_{OL} = 12.0 mA (@3.3 V)
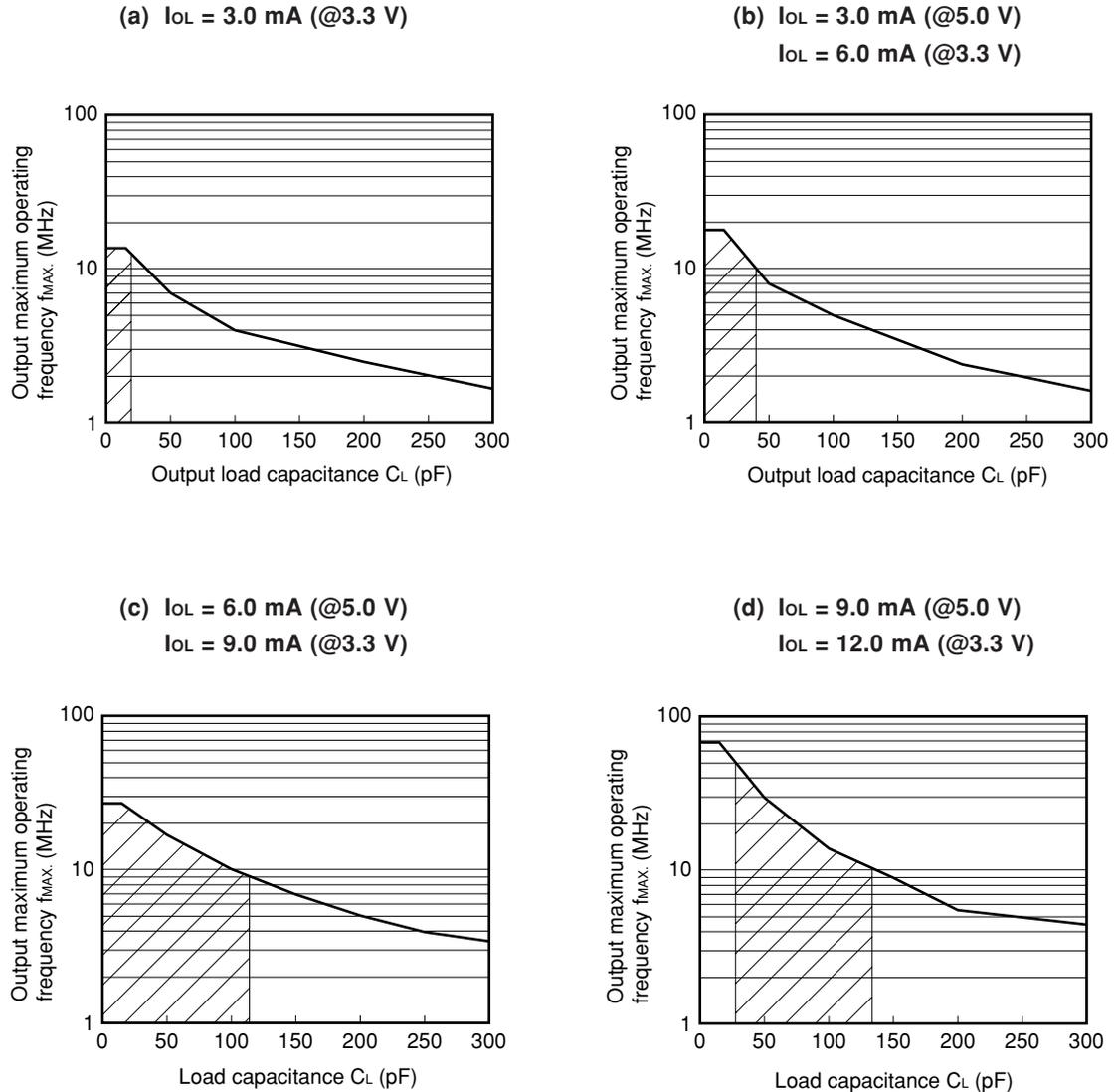
Figure 4-15. f$_{MAX.}$ vs. C$_L$ Limit (CMOS Level Output) (2/2)

(e) I$_{OL}$ = 12.0 mA (@5.0 V)
I$_{OL}$ = 18.0 mA (@3.3 V)
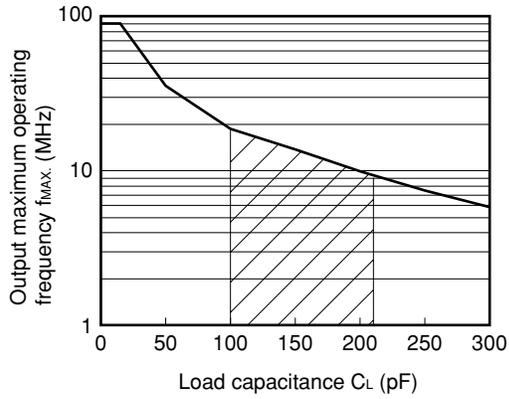
(f) I$_{OL}$ = 18.0 mA (@5.0 V)
I$_{OL}$ = 24.0 mA (@3.3 V)
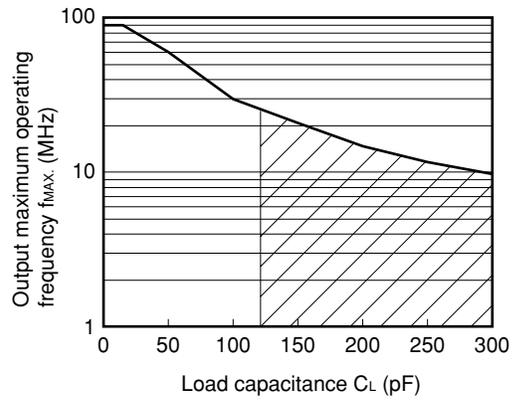
(g) I$_{OL}$ = 24.0 mA (@5.0 V)
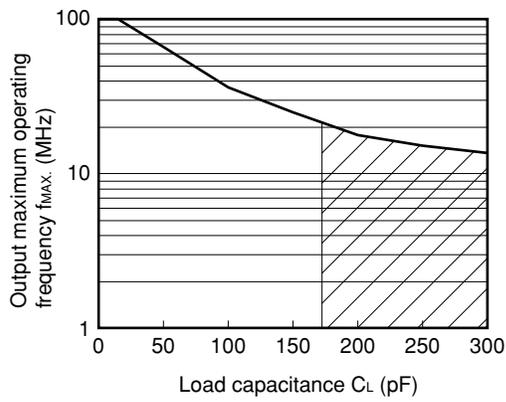
Figure 4-16. f$_{MAX.}$ vs. C$_L$ Limit (CMOS Level Low-Noise Output) (1/2)

(a) I$_{OL}$ = 3.0 mA (@3.3 V)
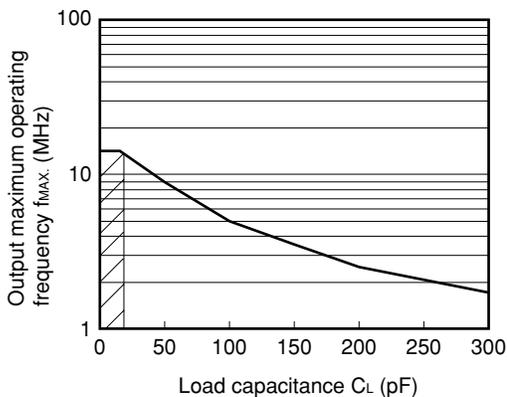
(b) I$_{OL}$ = 3.0 mA (@5.0 V)
I$_{OL}$ = 6.0 mA (@3.3 V)
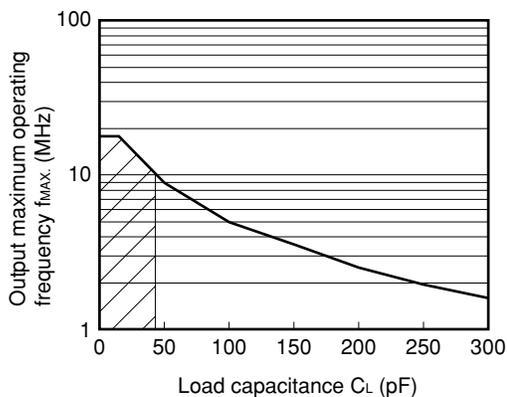
(c) I$_{OL}$ = 6.0 mA (@5.0 V)
I$_{OL}$ = 9.0 mA (@3.3 V)
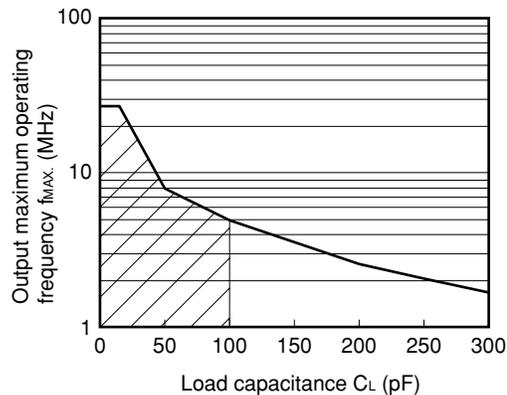
(d) I$_{OL}$ = 9.0 mA (@5.0 V)
I$_{OL}$ = 12.0 mA (@3.3 V)
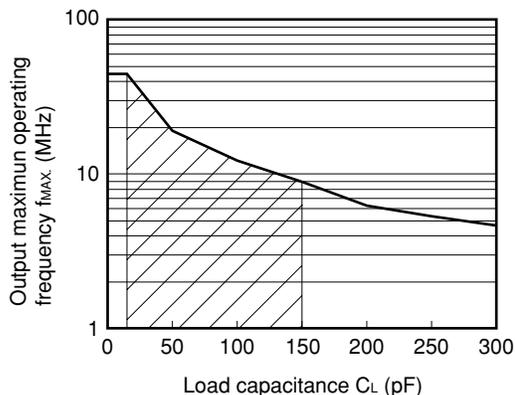
Figure 4-16. f$_{MAX.}$ vs. C$_L$ Limit (CMOS Level Low-Noise Output) (2/2)

(e) I$_{OL}$ = 12.0 mA (@5.0 V)
I$_{OL}$ = 18.0 mA (@3.3 V)
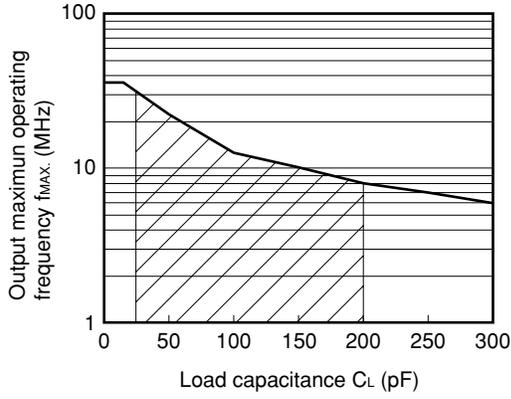
(f) I$_{OL}$ = 18.0 mA (@5.0 V)
I$_{OL}$ = 24.0 mA (@3.3 V)
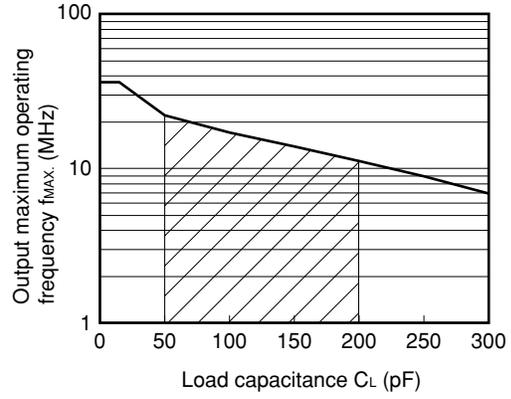
(g) I$_{OL}$ = 24.0 mA (@5.0 V)
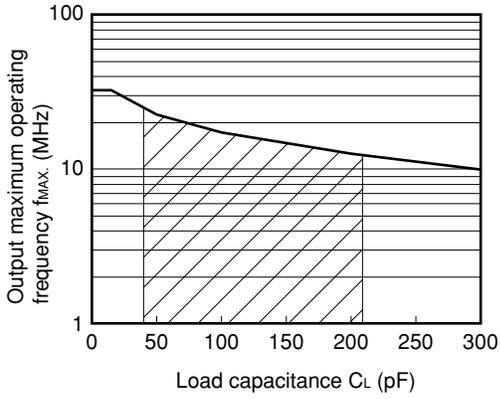
4.5.4 Output buffer output current (I_{OL}, I_{OH})

NEC Electronics defines the output current of a CMOS gate array at V_{OL} = 0.4 V and V_{OH} = V_{DD} – 0.4 V. However, there are cases in which the V_{OL} and V_{OH} that are used differ for actual applications. In such cases, the coefficients shown in (1) to (3) below should be used in estimating the I_{OL} and I_{OH} characteristics in accordance with the actual conditions.

Output current calculation

$$I_{OL'} = I_{OL} \times K_V \times K_T \ \ \text{(mA)}$$
$$I_{OH'} = I_{OH} \times K_V \times K_T \ \ \text{(mA)}$$

I_{OL}: I_{OL} specification when V_{OL} = 0.4 V

K_V: Voltage coefficient

K_T: Temperature coefficient

(1) Dependency on power supply voltage

The dependency on the power supply voltage is shown in Figure 4-17.

Figure 4-17. V_{DD} Dependency of I_{OL} / I_{OH}
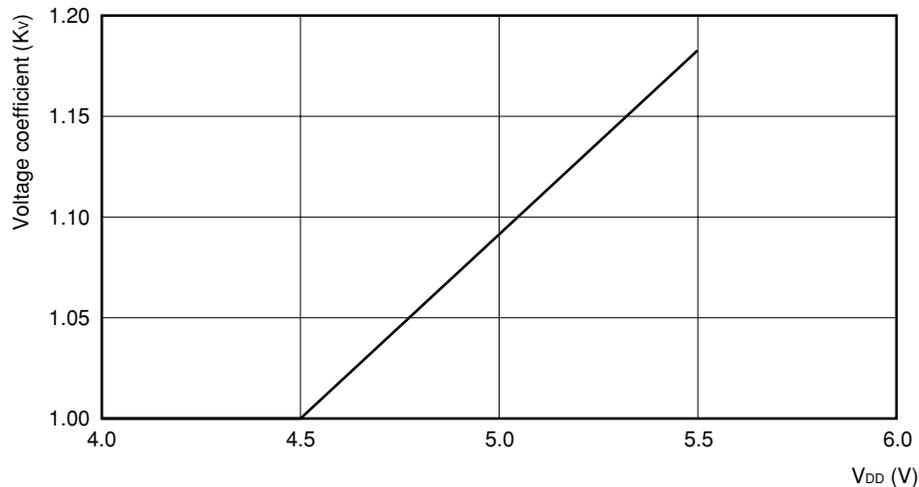
(2) Dependency on operating ambient temperature

The dependency on the operating ambient temperature is shown in Figure 4-18.

Figure 4-18. T$_A$ Dependency of I$_{OL}$ / I$_{OH}$
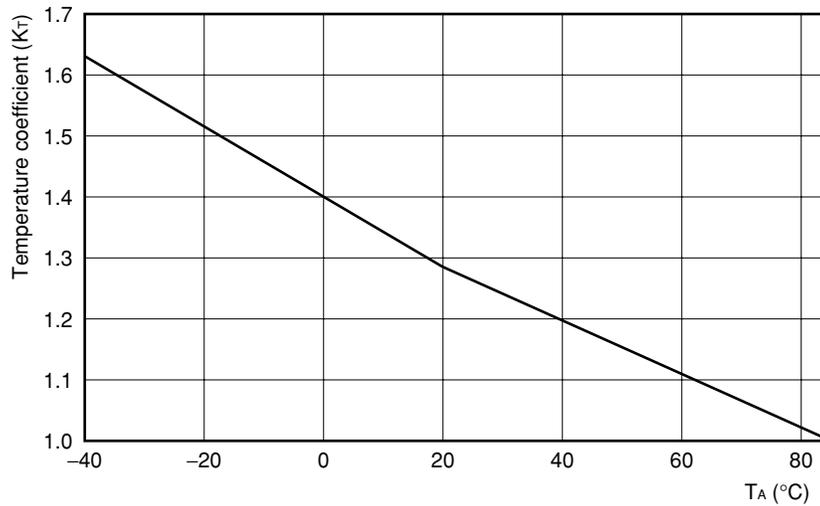
(3) Dependency on output voltage

V$_{OL}$ = 0.4 to 0.6 V, V$_{OH}$ = (V$_{DD}$ − 0.4 V) to (V$_{DD}$ − 0.6 V)

.... Because I$_{OL}$ and I$_{OH}$ vary almost proportionately to the output voltage, a direct approximation is possible. However, this excludes the I$_{OH}$ of the TTL level output buffer.

Equations for estimating the output buffer current

$$I_{OL'} = I_{OL} \times V_{OL}/0.4 \qquad \text{(mA)}$$
$$I_{OH'} = I_{OH} \times (V_{DD} - V_{OH})/0.6 \ \text{(mA)}$$

I$_{OL}$: I$_{OL}$ specification when V$_{OL}$ = 0.4 V

V$_{OL}$: V$_{OL}$ value used

I$_{OH}$: I$_{OH}$ specification when V$_{OH}$ = (V$_{DD}$ − 0.4 V)

V$_{OH}$: V$_{OH}$ value used

The I$_O$ vs. V$_O$ curves are shown in Figures 4-19 and 4-20. The MIN. curve is shown for the conditions V$_{DD}$ = 4.5 V and T$_J$ = 125°C. The TYP. curve is shown for the conditions V$_{DD}$ = 5.0 V and T$_J$ = 25°C. The MAX. curve is shown for the conditions V$_{DD}$ = 5.5 V and T$_J$ = −40°C. The direct currents I$_{OH}$ and I$_{OL}$ that can actually be used should be within the absolute maximum ratings.

Figure 4-19. I$_O$ vs. V$_O$ (@5.0 V) (1/2)

(1) I$_{OL}$ = 3 mA

(a) I$_{OL}$ vs. V$_{OL}$

(b) I$_{OH}$ vs. V$_{OH}$

(2) I$_{OL}$ = 6 mA

(a) I$_{OL}$ vs. V$_{OL}$

(b) I$_{OH}$ vs. V$_{OH}$
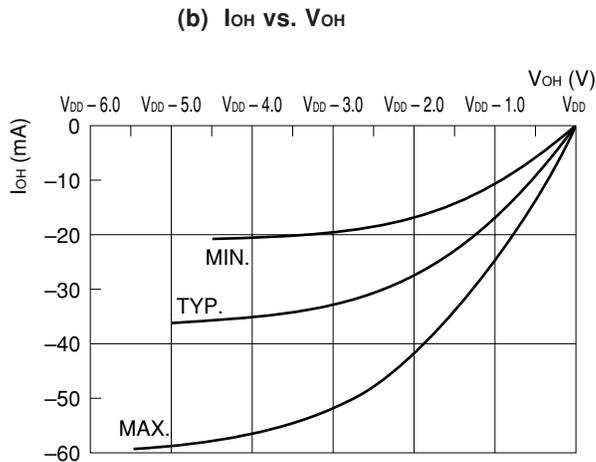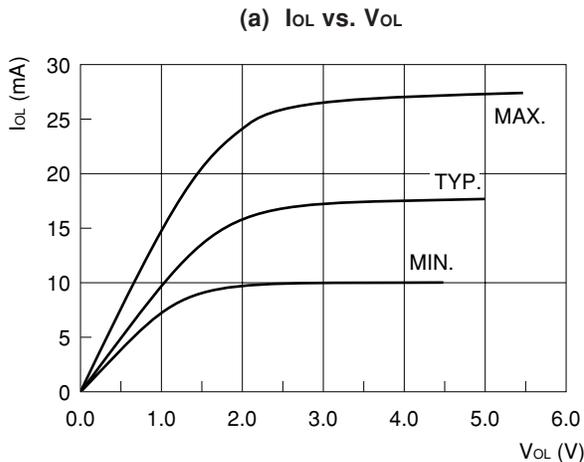
(3) I$_{OL}$ = 9 mA
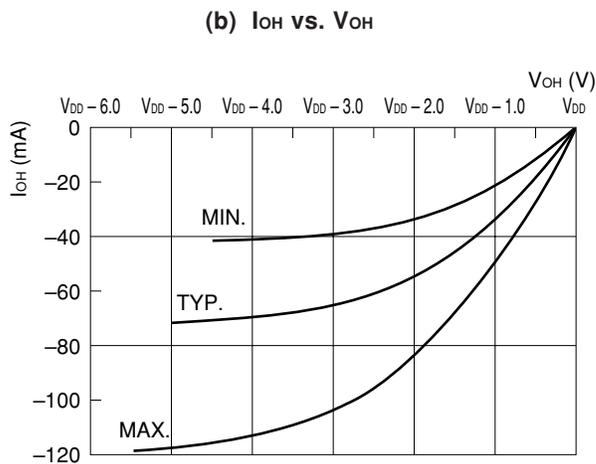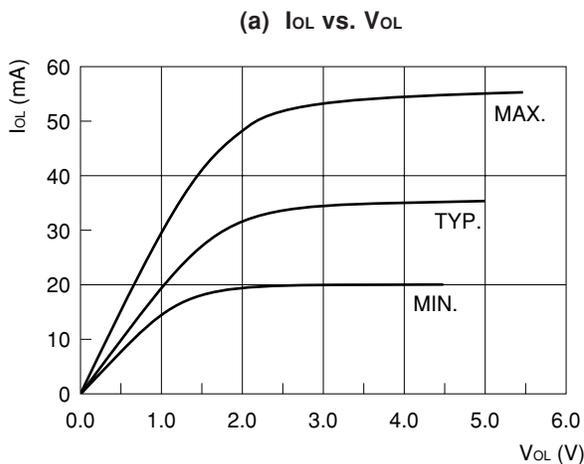
(a) I$_{OL}$ vs. V$_{OL}$
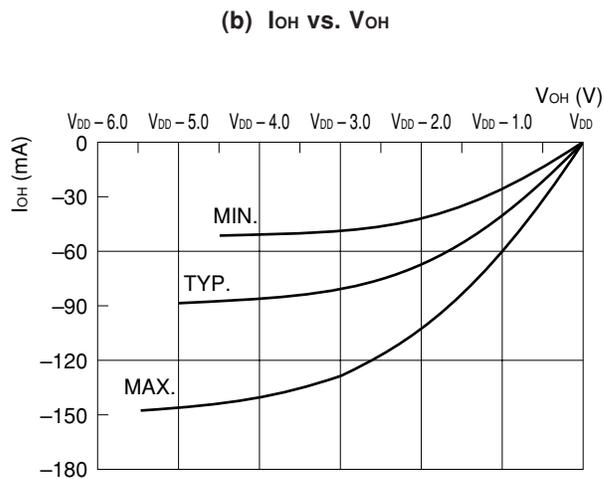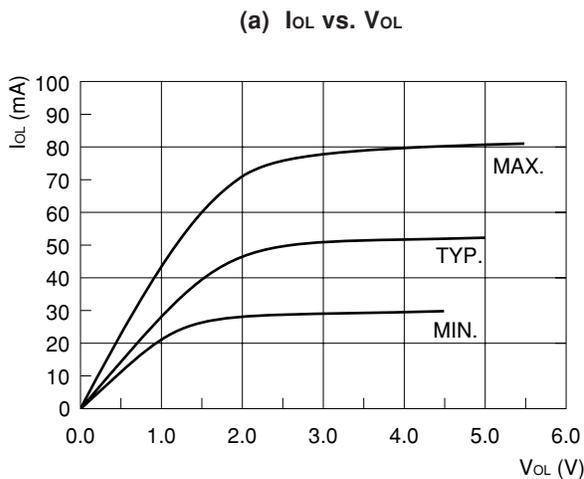
(b) I$_{OH}$ vs. V$_{OH}$

Figure 4-19. I$_O$ vs. V$_O$ (@5.0 V) (2/2)

(4) I$_{OL}$ = 12 mA

(a) I$_{OL}$ vs. V$_{OL}$
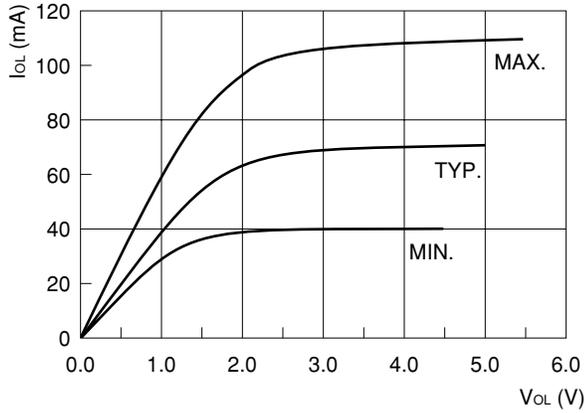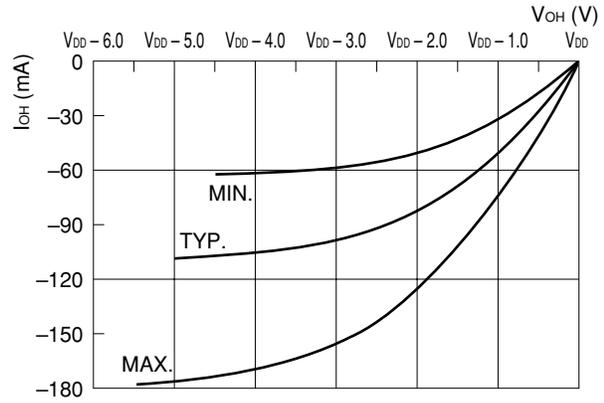
(b) I$_{OH}$ vs. V$_{OH}$

(5) I$_{OL}$ = 18 mA
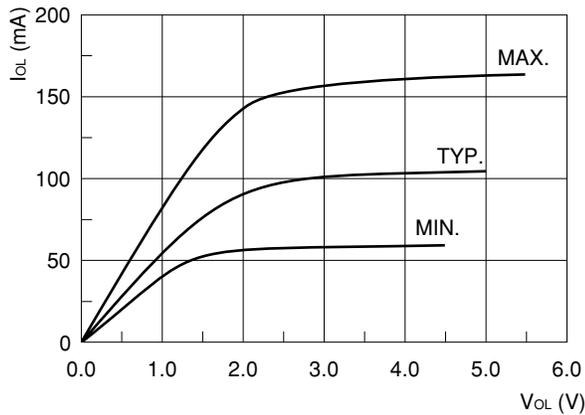
(a) I$_{OL}$ vs. V$_{OL}$
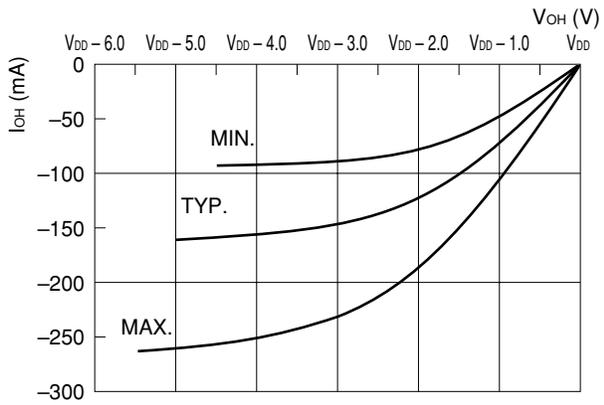
(b) I$_{OH}$ vs. V$_{OH}$

(6) I$_{OL}$ = 24 mA

(a) I$_{OL}$ vs. V$_{OL}$
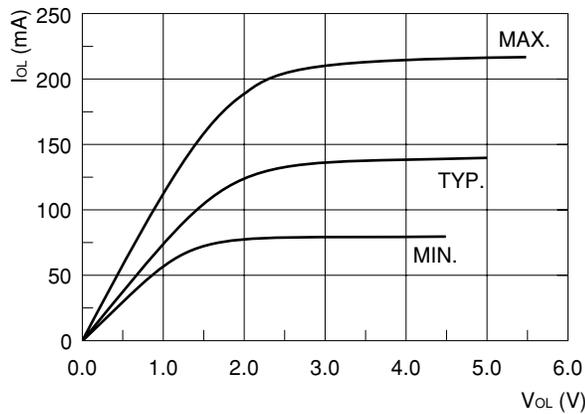
(b) I$_{OH}$ vs. V$_{OH}$
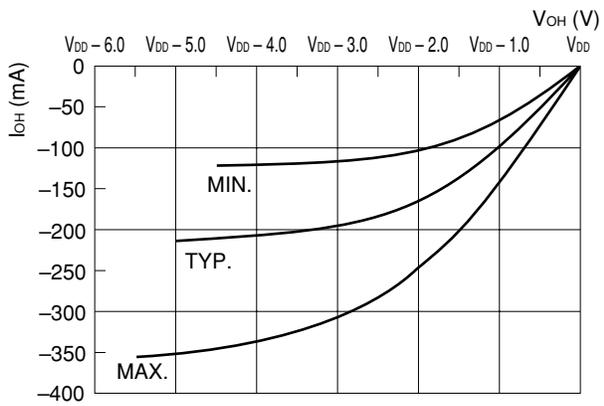
Figure 4-20. I$_O$ vs. V$_O$ (@3.3 V) (1/2)

(1) I$_{OL}$ = 3 mA

(a) I$_{OL}$ vs. V$_{OL}$

(b) I$_{OH}$ vs. V$_{OH}$

(2) I$_{OL}$ = 6 mA

(a) I$_{OL}$ vs. V$_{OL}$

(b) I$_{OH}$ vs. V$_{OH}$

(3) I$_{OL}$ = 9 mA

(a) I$_{OL}$ vs. V$_{OL}$

(b) I$_{OH}$ vs. V$_{OH}$
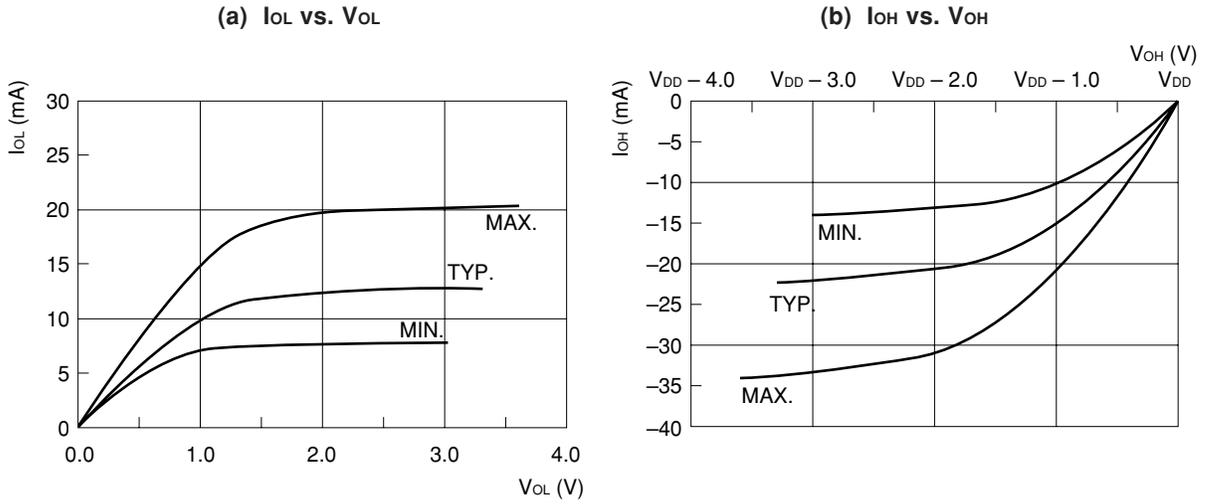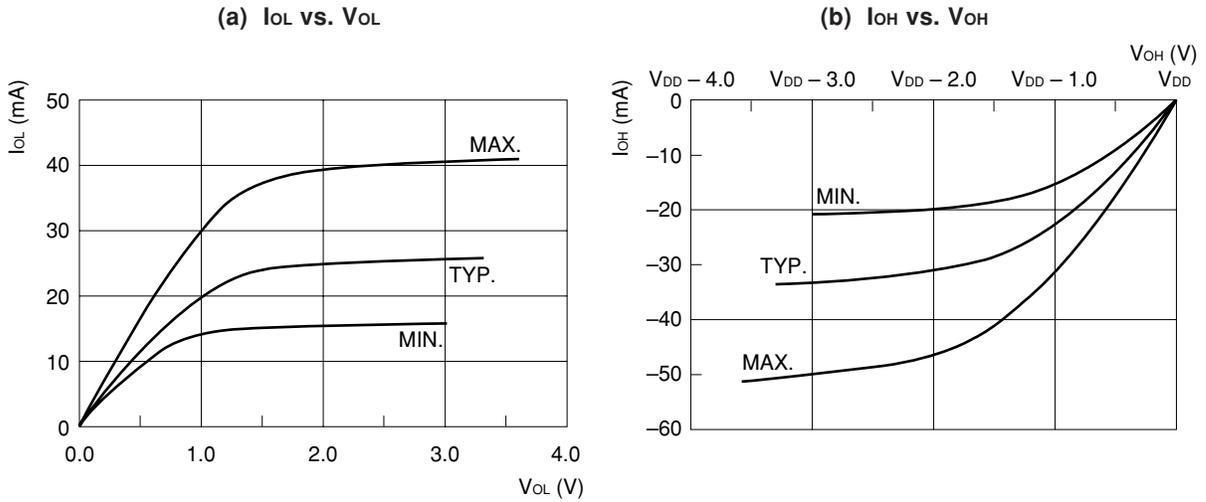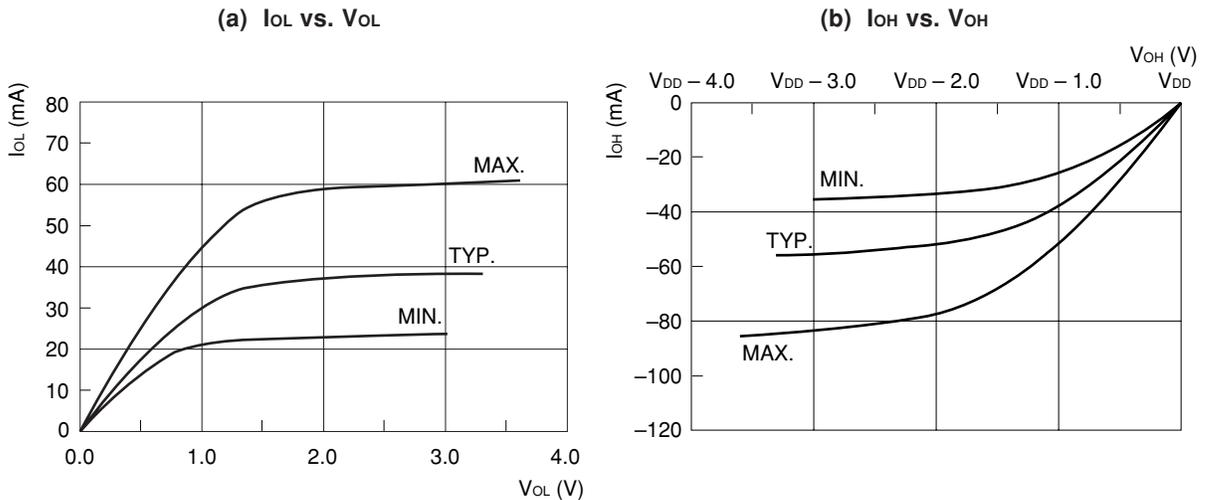
Figure 4-20. I$_O$ vs. V$_O$ (@3.3 V) (2/2)

(4) I$_{OL}$ = 12 mA

(a) I$_{OL}$ vs. V$_{OL}$

(b) I$_{OH}$ vs. V$_{OH}$

(5) I$_{OL}$ = 18 mA

(a) I$_{OL}$ vs. V$_{OL}$

(b) I$_{OH}$ vs. V$_{OH}$

(6) I$_{OL}$ = 24 mA

(a) I$_{OL}$ vs. V$_{OL}$

(b) I$_{OH}$ vs. V$_{OH}$
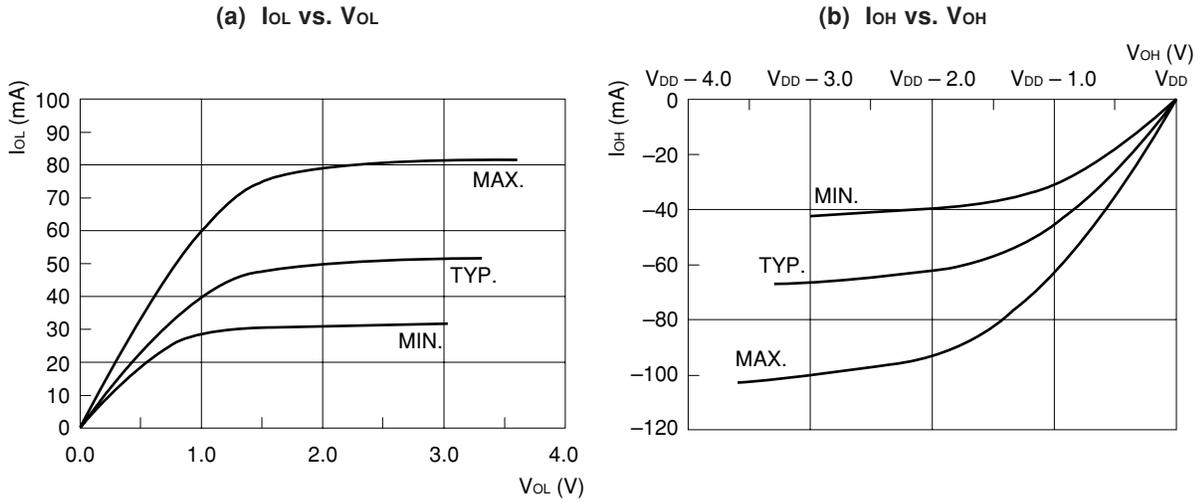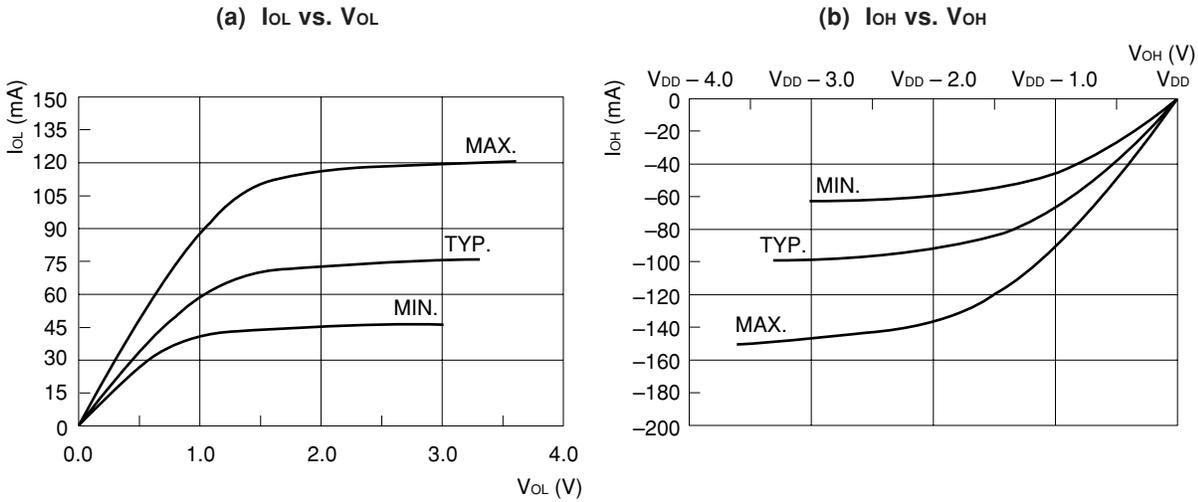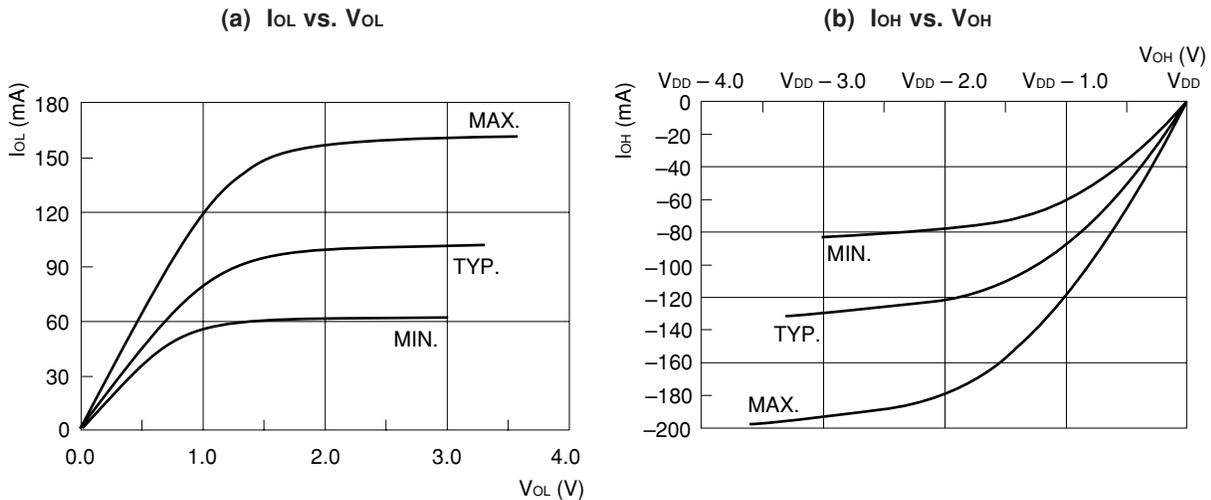
4.6 Restrictions to Simultaneous Operation of Output Buffers

4.6.1 Malfunction due to simultaneous operation of outputs

When the output buffer operates, a current that charges/discharges the output load capacitance flows between the load and LSI. If the current is too large, noise is generated in the power supply line, resulting in the malfunction of the system.

There are two types of malfunctions:

<1> The LSI malfunctions due to fluctuation in the LSI input threshold level
<2> The next stage circuit malfunctions due to noise appearing at the LSI output pin

The cause of malfunction due to simultaneous operation of output buffers is described as follows.

The circuit in Figure 4-21 (a) can be considered when LSI B's output buffer is switched from "H" to "L". When this happens, the current discharged from the load flows to GND via the power supply line of LSI B. As a result of this discharge current and the impedance of the GND line, the power supply to the GND line decreases and the GND level (V_G) inside LSI B increases. If the output buffer switches from "L" to "H", the current that charges the load capacitance flows, and noise is generated in the power supply line. As a result, V_{DD} temporarily decreases.

When many output buffers simultaneously operate, if the capacity of the load to be driven becomes large, the voltage level inside the LSI chip fluctuates due to the charge/discharge current, which may result in malfunction, as shown in Figure 4-21 (b) and (c).

To prevent such malfunctions, the number of simultaneously operating output buffers must be limited. The number of output buffers that can simultaneously operate differs depending on the following five factors:

<1> Numbers of V_{DD} and GND
<2> Load capacity (C_L)
<3> Load drive capability of the output buffer to be used (I_{OL})
<4> Type of input interface level
<5> Type of output interface level

Figure 4-21. Malfunction Caused by Simultaneous Operation

(a) Circuit diagram
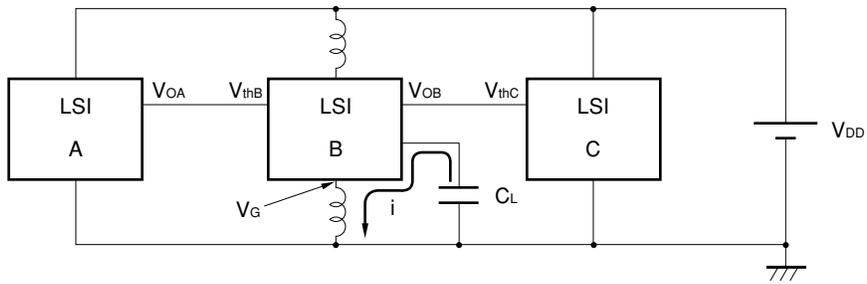
V_{OA}: Output level of LSI A
V_{OB}: Output level of LSI B
V_{thB}: Input threshold level of LSI B
V_{thC}: Input threshold level of LSI C
V_G: GND level of LSI B

(b) Fluctuation in input threshold level of LSI B

signal is input to LSI B
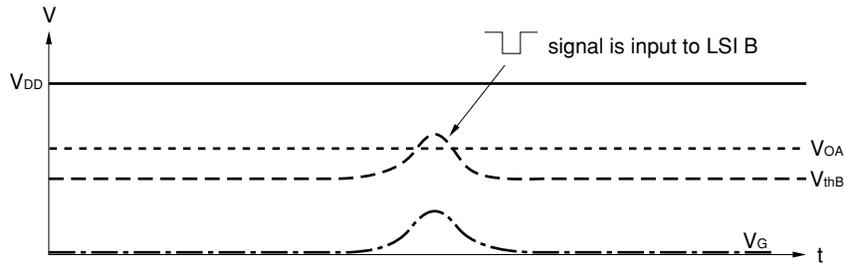
(c) Generated noise moving to the output pin of LSI B

signal is input to LSI C
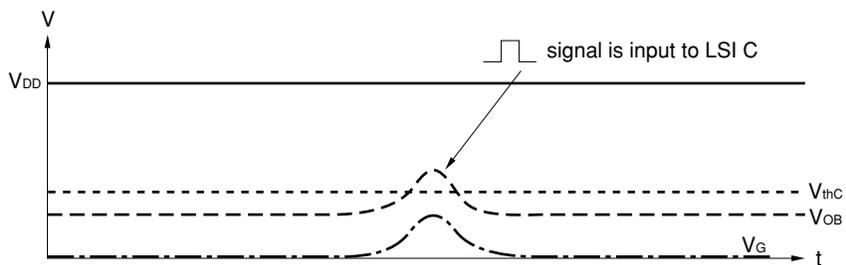
4.6.2 Definitions

Output simultaneous operation is the switching of multiple output buffers in the same direction (H → L, HZ → L or L → H, HZ → H) within a fixed time (see Table 4-10) as a result of conditions such as the buffer type and load capacitance. Output simultaneous operation is counted for each operation, and the respective simultaneous operation limits apply independently.

The following switching of signals is considered one output simultaneous operation group.

(1) Output signal switching from H → L, HZ → L, X → L, H → X
(2) Output signal switching from L → H, HZ → H, X → H, L → X

Remark HZ: High impedance, X: Undefined

Output signal switching from L → HZ and H → HZ is not counted as simultaneous operation. For bidirectional pins, operating that occurs during switching from input to output must also be considered.

Table 4-10. Reference Time Ranges for Simultaneous Operation (TYP.)

Buffer Type	Load Capacitance C_L (pF)		
	$0 \leq C_L \leq 50$	$50 < C_L \leq 200$	$200 < C_L \leq 300$
3.0 mA	≤ 2.5 ns	≤ 4.0 ns	≤ 6.0 ns
6.0 mA	≤ 3.0 ns	≤ 4.0 ns	≤ 6.0 ns
9.0 mA	≤ 3.0 ns	≤ 4.0 ns	≤ 6.0 ns
12.0 mA	≤ 3.0 ns	≤ 4.0 ns	≤ 6.0 ns
18.0 mA	≤ 3.0 ns	≤ 4.0 ns	≤ 6.0 ns
24.0 mA	≤ 3.0 ns	≤ 4.0 ns	≤ 6.0 ns

4.6.3 Factors for the determination of simultaneous operation

Because noise generated by charge/discharge currents is the cause of malfunction, the number of simultaneously operating output pins is limited by the following factors:

(1) Drive capability of the output buffers
(2) Load capacitance
(3) Number of output simultaneous operation pins
(4) Number of LSI power supply pins
(5) Routing pattern of GND and power supply on the circuit board
(6) Placement of the output simultaneous operation pins
(7) Input buffer types

Items (1), (2), and (3) specify the charge/discharge current, and item (7) specifies the LSI's noise margin using the input buffer interface. Items (4) and (5) restrict the inductance of the closed loop through which the charge/discharge current flows. Therefore, these items cannot be specified quantitatively. The simultaneous operation limit specified by NEC Electronics has a default value for the impedance of this loop. **It is therefore possible that noise will be generated, depending on the particular user's circuit board layout. Adequate noise countermeasures must be incorporated into the design of the circuit board**.

4.6.4 Simultaneous operation pins to be checked

Simultaneous operation of outputs should be checked for output buffer groups that meet the conditions explained below.

Conditions

(1) When buffers are driven in parallel by a shared internal block, or one signal output from a shared internal block is split into multiple buffers due to the fan-out limit, and the buffers are driven in parallel.
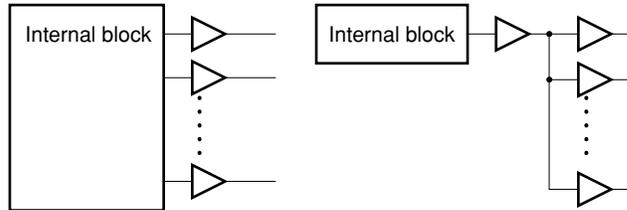
(2) When the output buffers are driven by sequential circuits operated by a shared control signal and when, due to the delay time of the combination circuits, the operation timing differential of the distributed output buffers is less than the simultaneous operation reference time for each buffer and load capacitance shown in **Table 4-10 Reference Time Ranges for Simultaneous Operation (TYP.)** .
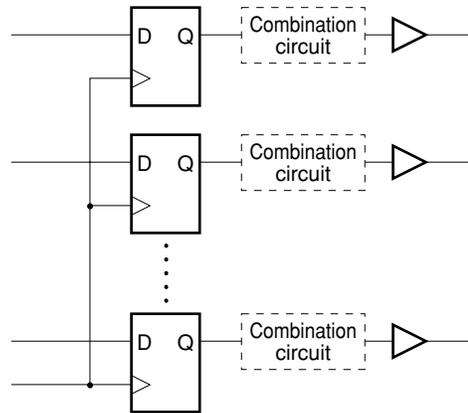
(3) When, due to identical timing of the external input, the timing differential of output buffer operation is less than the simultaneous operation reference time for each buffer and load capacitance shown in **Table 4-10 Reference Time Ranges for Simultaneous Operation (TYP.)**.
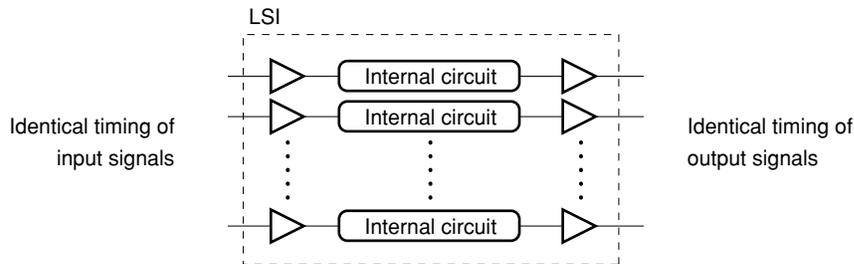
Determination of the simultaneous operation reference time (described in **Table 4-10 Reference Time Ranges for Simultaneous Operation (TYP.)**) is performed by the simple total of the t_{LD0} (TYP.) values listed in the **CMOS-N5 Series (5.0 V) Block Library (A13872E)** and **CMOS-N5 Series (3.3 V) Block Library (A15895E)**.

However, checking for simultaneous operation of outputs is not performed in those cases in which the following conditions apply:

* The operation timing differential of the output buffer is greater than the simultaneous operation reference time for each buffer and load capacitance shown in **Table 4-10 Reference Time Ranges for Simultaneous Operation (TYP.)**.
* Operation does not occur other than during initialization (set and reset).
   (Because malfunctions due to simultaneous operation are absorbed by initialization.)

4.6.5 Pin placement and simultaneous operation

The size of closed loop inductance, through which the charge/discharge currents of the output buffers flow, determines the size of the generated noise. The inductance of this closed loop depends on the LSI pin placement and the circuit board on which the LSI is mounted. Care must be taken in placing pins in order to control noise caused by simultaneous operation.

* As far as possible, avoid placing input pins in the output buffers that operate simultaneously.
* Locate input pins (especially clock input pins) susceptible to noise as close to the GND pin as possible. Separate these pins as far as possible from output buffers that operate simultaneously.
* Separate output buffers that operate simultaneously as far as possible from the input pins, and enclose them by GND pins.
* If it is difficult to enclose output buffers that operate simultaneously by GND pins, disperse the buffers as much as possible. In any case, separate the output buffers that operate simultaneously as far as possible from the input pins.
* Increase the number of GND/V_{DD} pins at a rate of one V_{DD} to two GND.

4.6.6 Three-GND-pin determination

By this method, a determination is made not for the number of GND and V_{DD} pins of the LSI, but for three GND pins. Therefore, locations at which simultaneous operation is concentrated can be taken into consideration.

Simultaneous operation is assessed by the output buffer type, output load capacitance, and the number of valid GND pins. Table 4-11 shows the number of pins that can operate simultaneously between three valid GND pins. Because the permissible number of simultaneous operation pins when a 12 mA output buffer is used is shown in this table, calculate the permissible number of pins by using the coefficient shown in Table 4-12 if a buffer with a different driving capability and output level is used.

If the driving capability is the same when I_{OL} is a value other than 12 mA, divide the values in Table 4-11 by the coefficient in Table 4-12.

> I_{OL} = Permissible number of simultaneous operation pins between 3GND pins with 12 mA/Coefficient

Criteria if drive capability or load capacitance is different

In the case of buffers with different driving capabilities, the following expression must be used to calculate the permissible number of simultaneous operation pins (M_i) in Table 4-11, taking the number of simultaneous operation pins (m_i) and coefficient (β_i) of each driving capability into consideration.

> $\Sigma \, (m_i \times \beta_i/M_i) \leq 1$

Calculation example	I_{OL} = 18 mA	CMOS level	30 pF	5 pcs.
	I_{OL} = 24 mA	CMOS level	50 pF	2 pcs.

$5 \times 1.189 \div 12.5 + 2 \times 1.266 \div 10 \leq 1$

BGA package determination

Determination is performed for the internal chip in the BGA package. For internal chip pin layout, see the tables concerning assignment of V_{DD}, GND, NC, and SCAN test pins in **CMOS Gate Array, Embedded Array Package Design Manual (A16400E)**.

Table 4-11. Permissible Number of Simultaneous Operation Pins Between 3 GND Pins (I_{OL} = 12 mA)

(1) 5.0 V

(a) When inputs are CMOS-level inputs only

Valid Number of GND	Output Load Capacitance (C_L)					
	15 pF	30 pF	50 pF	100 pF	150 pF	200 pF
1[Note]	13.0	8.5	6.3	4.8	4.3	3.8
3	19.5	12.5	10	7.5	6.5	6

(b) When inputs are TTL-level inputs only and when inputs are mixture of TTL-level inputs and CMOS-level inputs

Valid Number of GND	Output Load Capacitance (C_L)					
	15 pF	30 pF	50 pF	100 pF	150 pF	200 pF
1[Note]	5.2	4	2.8	1.9	1.6	1.5
3	8	5	4.5	3	2.5	2.5

(2) 3.0 V and 3.3 V

Valid Number of GND	Output Load Capacitance (C_L)					
	15 pF	30 pF	50 pF	100 pF	150 pF	200 pF
1[Note]	4.3	4.0	3.8	3.5	3.3	3.0
3	6.5	6	6	5.5	5	5

Note For a small-pin-count package

Remarks 1. Calculate the valid amount of capacitance not in the table by complementing linearly.
2. Count adjacent GND pins, including those sandwiching a corner on the layout, as one.

Table 4-12. Coefficient of Number of Simultaneous Operation Pins

(a) 5.0 V

Output Level	I$_{OL}$ (mA)	Coefficient	Example of Corresponding Block
CMOS normal type	3.0	0.467	FO09, B00T
	6.0	0.746	FO04, B00E
	9.0	0.757	FO01, B008
	12.0	1.000	FO02, B007
	18.0	1.189	FO03, B009
	24.0	1.266	FO06, B00H
CMOS low-noise type	3.0	0.287	FE09, BE0T
	6.0	0.465	FE04, BE0E
	9.0	0.483	FE01, BE08
	12.0	0.500	FE02, BE07
	18.0	0.530	FE03, BE09
	24.0	0.625	FE06, BE0H

(b) 3.0 V and 3.3 V

Output Level	I$_{OL}$ (mA)	Coefficient	Example of Corresponding Block
CMOS normal type	3.0	0.395	FO09, B00T
	6.0	0.575	FO04, B00E
	9.0	0.618	FO01, B008
	12.0	1.000	FO02, B007
	18.0	1.076	FO03, B009
	24.0	1.116	FO06, B00H
CMOS low-noise type	3.0	0.277	FE09, BE0T
	6.0	0.380	FE04, BE0E
	9.0	0.453	FE01, BE08
	12.0	0.500	FE02, BE07
	18.0	0.523	FE03, BE09
	24.0	0.533	FE06, BE0H

4.6.7 Assumptions for the determination method

The determination of simultaneous operation is also affected significantly by the power supply and GND pins of the circuit board.

It is assumed by the determination method that simultaneous operation is considered for comparative circuit board and LSI pin placements. The reference values are determined based on this assumption. Consequently, if the routing pattern of a circuit board is narrow (especially the power supply and GND routing), or if the closed loop from the power supply wiring on the circuit board through the LSI and GND wiring on the circuit board and back to the power supply wiring is long, and the impedance is large, then the noise generated by simultaneous operation will become greater than the noise level specified by the determination method. This must be kept in mind in order to avoid problems.

In such a case, it is effective to shorten the above closed loop by means of a bypass capacitor.

4.6.8 Other determination methods

The methods explained below must be used if the determination reference cannot be satisfied by the standard power supply and number of GND pins.

(1) Increasing V$_{DD}$ and GND pins

Increase the V$_{DD}$ and GND pins so that the condition of the number of simultaneous operation pins is satisfied. Increase the number of pins at a ratio of one V$_{DD}$ pin to two GND pins.

(2) Re-examine the applicable environment

<1> Reduction of output load capacitance

The size of the noise generated by charge/discharge currents that flow when the output changes depends on the size of the output load capacitance. Consequently, the size of the generated noise can be reduced by reducing the load capacitance, thereby increasing the allowable number of simultaneous operation pins.

<2> Modification of buffer type

The peak values of the output charge/discharge currents depend on the buffer drive capability and the buffer function. By changing to a buffer type with a lower drive capability or to a low-noise buffer, the generated noise can be controlled and the allowable number of simultaneous operation pins can be increased.

<3> Reduce simultaneous operation pins by adding delay time

Output simultaneous operation is the switching of multiple output buffers in the same direction (H $\rightarrow$ L, HZ $\rightarrow$ L or L $\rightarrow$ H, HZ $\rightarrow$ H) within a fixed time (see **Tables 4-8** and **4-9**), as determined by conditions such as the buffer type and load capacitance. Consequently, if delay time is added to the simultaneously operating output pins and the operating time does not fall within the time specified in **Table 4-10 Reference Time Ranges for Simultaneous Operation (TYP.)**, then it becomes unnecessary to consider these pins as operating simultaneously, and the number of simultaneous operation pins is thereby reduced.

Remark   HZ: High impedance

This chapter explains the points to be noted and limits to be applied in designing a circuit.

When designing an LSI using CMOS gate arrays, once a circuit has been designed it cannot be easily modified, unlike when designing a circuit using standard TTL or CMOS ICs.

It is therefore important to observe the limits and follow the design rules described in **CHAPTER 2 IMPLEMENTING THE SYSTEM USING THE GATE ARRAY**, **CHAPTER 4 ESTIMATING ELECTRICAL CHARACTERISTICS**, and this chapter to design an LSI without errors.

If an LSI is designed without observing the design rules, not only is the development period after interfacing with NEC Electronics extended, but also the product may need to be re-developed.

5.1 Basic Circuit Configuration

5.1.1 Using I/O buffers

When designing an LSI with gate arrays, place input/output buffers between the LSI and the input/output pins (see **Figure 5-1**).

Reasons: <1> To protect the LSI from destruction due to static electricity

              <2> To obtain sufficient output drive capability

Figure 5-1. Basic Circuit Configuration
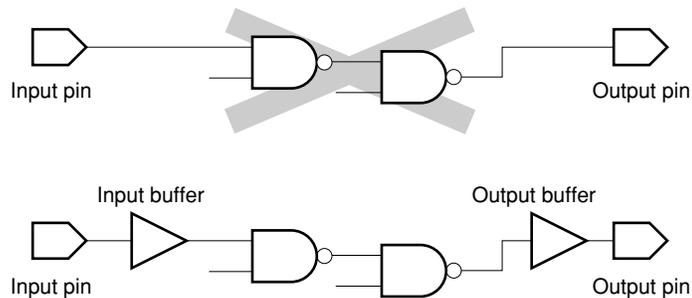
5.1.2 Unused pins

With gate arrays, <u>unused input pins cannot be left open (the state where they are not connected to anything)</u> in any block. The pins must be input at either a high or low level by using F091 (H- and L-level generator). If a block's input pins are left open, it cannot function correctly since the input level is undetermined. This condition also becomes a source of increased I_L (leakage current). In addition, large fan-outs should be avoided when F091 is used. If several blocks are clamped to a single block, the routing becomes concentrated, making placement and routing difficult. In such a case, divide the circuit by a certain unit to avoid routing concentration.

A warning error will be posted by the tester during a design rule check if the block's output pins have been left open. Discard unnecessary blocks.

5.1.3 Fan-out limitations

There are limitations on the number of charged gates that can be connected to a block's output pins (the fan-out number). The recommended fan-outs for each block (including the fan-in number) are given in the **CMOS-N5 Series (5.0 V) Block Library (A13872E)** and **CMOS-N5 Series (3.3 V) Block Library (A15895E)**.

Because signal rise and fall times increase when the number of charged gates increases, the estimation accuracy of the propagation delay time becomes lower. Moreover, if rise and fall times become very long, data-through develops in the flip-flops causing abnormal logic operation. <u>Therefore, do not exceed the fan-out restrictions when designing</u>.

Be sure also to design with fan-out numbers that are 1/3 of the limit in circuits that have strict speed specifications.

5.1.4 Wired logic circuit prohibitions

<u>Other than for the bus, do not configure wired logic as mutually connected block outputs</u>.

The P-ch transistors and the N-ch transistors become conductive at the same time as a function of the logic state if the outputs of the block are connected to each other. Pay attention to this since the steady low-power characteristics that are a feature of CMOS circuits can be lost when the output is at an intermediate level because current can flow from V_{DD} to GND.

Figure 5-2. Wired Logic Circuit Prohibitions
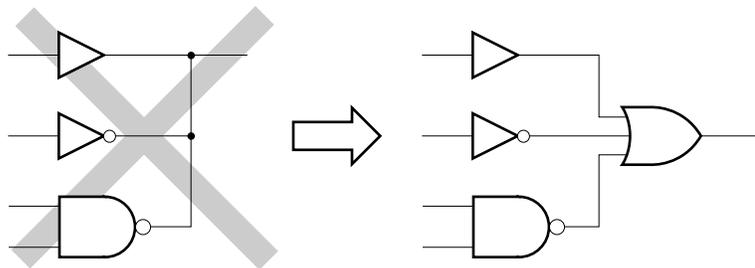
5.1.5 Notes on using bidirectional buffers

   If an output signal is input as is to an internal circuit with a bidirectional buffer, the internal circuit that receives this input signal may malfunction due to distortion of the output waveform and ringing as shown in Figure 5-3. Take special care to avoid inputting input signals to the clock of the flip-flop. In the output mode, make sure that the signal immediately before the output buffer is input to the internal circuit as shown in Figure 5-4.

Figure 5-3. Ringing
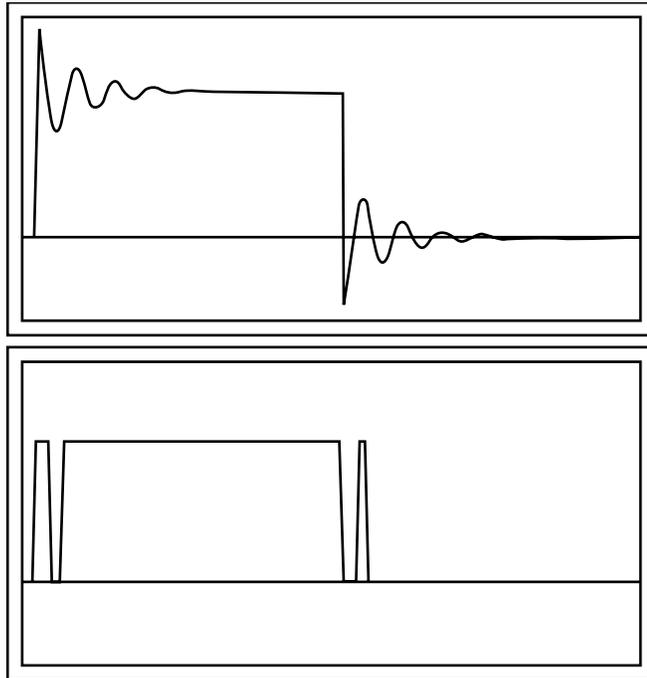
Figure 5-4. Example of Preventive Circuit
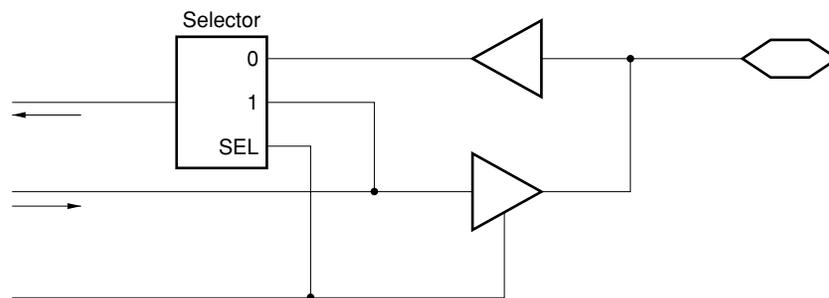
5.2 Differential Circuit Prohibition

As a rule, differential circuits should not be configured from gate arrays. Since gate-array placement and routing design is done automatically, the range of waveforms that are internally generated cannot be guaranteed with gate arrays, and the desired functions will not materialize. Therefore, avoid structuring the circuit shown in Figure 5-5 (a); instead structure the circuit as shown in Figure 5-5 (b).

Figure 5-5. Differential Circuit Prohibition

(a) Example of incorrect circuit
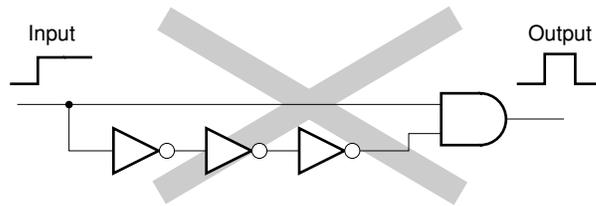
(b) Example of correct circuit
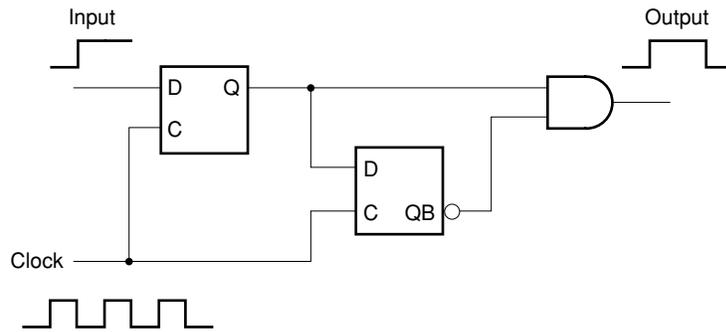
5.3 RS Latch and Loop Circuits

5.3.1 RS latch

Gate-configured asynchronous RS latches should not be used with gate arrays. This is not only because initialization may not be able to take place via simulation or high variation in circuit path speed due to routing location effects.

Figure 5-6. Asynchronous RS Latches
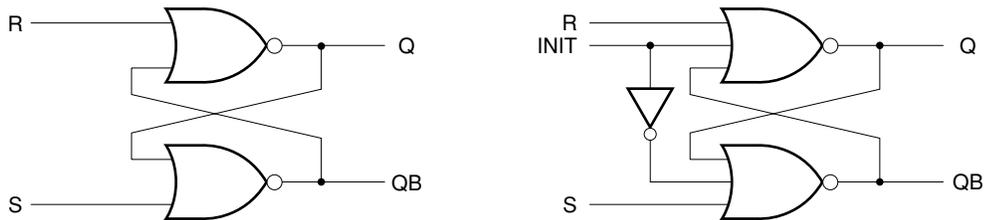
5.3.2 Loop circuit

The following points must be noted when loop circuits, such as feedback loops, are used.

(1)   As shown in Figure 5-7, if gates lie between feedback loops, such as divider circuits, the frequency characteristics will drop due to the delay time caused by these gates. The delay times of these loops must be determined beforehand and the frequency characteristics must be verified. See **5.6 Delay Time Margin** for the margin verification method.

Figure 5-7. Loop Circuit
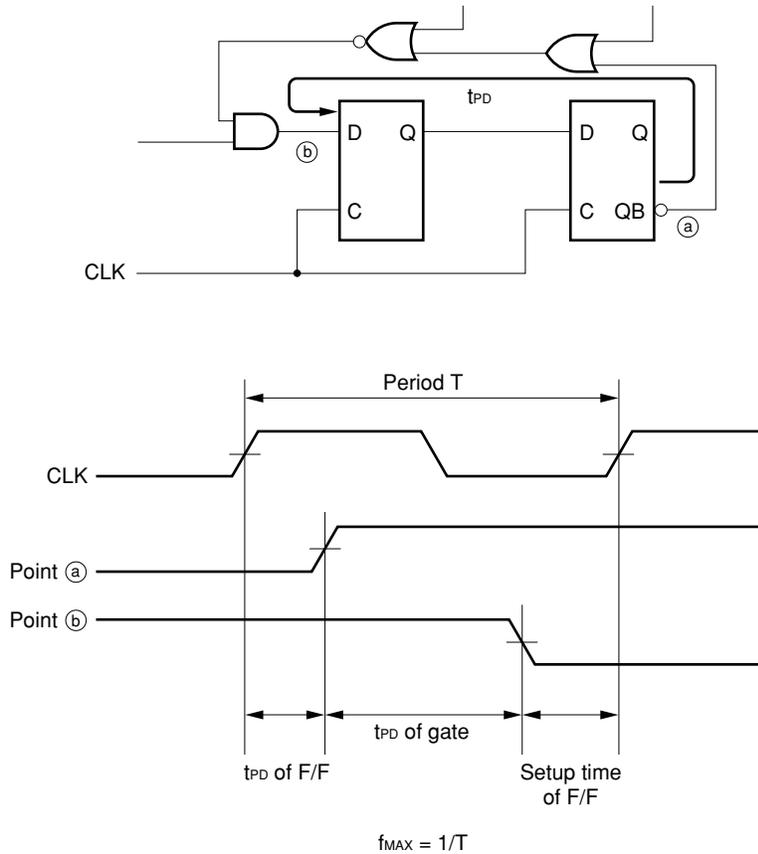
(2)   A loop circuit cannot be formed in a scan path configuration. In this case, employ a countermeasure such as isolating the loop circuit by using gates.

5.3.3 Prohibited state of flip-flops

The state in which both the set and reset inputs of an RS latch or flip-flop are enabled at the same time is prohibited. This is because the retained data becomes unstable if both the set and reset inputs are disabled simultaneously. What value the retained data will take is influenced by delicate timing such as the timing of the set and reset signal input and delay of the internal signal of the flip-flop and cannot be guaranteed.

Consequently, be aware of the following when using flip-flops with set/reset inputs.

<1> Do not enable set and reset inputs at the same time.

<2> When it is necessary to enable set and reset inputs simultaneously, disable one side first and then disable the other side. By doing this, the state that the flip-flop was in when it was disabled will be maintained.

Table 5-1. F617 (D-F/F with RB, SB)

D	C	RB	SB	Q	QB	
0	⤒	1	1	0	1	
1	⤒	1	1	1	0	
X	⤓	1	1	Hold	Hold	
X	X	0	1	0	1	
X	X	1	0	1	0	
X	X	0	0	0	0	←Use prohibited

X: Undefined

5.4 Clocked Signal Design

Gate arrays should basically be designed as synchronous circuits.

5.4.1 Synchronous circuit design

There are two techniques used for designing synchronous circuits: the single-phase synchronous circuit design technique normally used for circuits designed using general-purpose LSIs, and the multi-phase synchronous circuit design technique often used in CPU design.

The features of single-phase and multi-phase synchronous circuit design are shown in Table 5-2.

Table 5-2. Features of Single-Phase and Multi-Phase Synchronous Circuit Design

	Advantages	Disadvantages
Single-phase synchronous circuit design	• Circuit is simple. • Generally suited to high-speed circuits.	• Signal skew on the clock line must be considered in configuring shift registers
Multi-phase synchronous circuit design	• Timing tests for shift registers are unnecessary.	• A multi-phase clock signal must be generated. • Number of gates increases. • Generally unsuited to high-speed operation.

(1) Single-phase synchronous circuit design

Single-phase synchronous circuits should be designed when sequential circuits will operate with a single clock signal. This relatively simple design method is necessary to adjust timing such as clock skew between sequential circuits.

Figure 5-8. Clock Skew
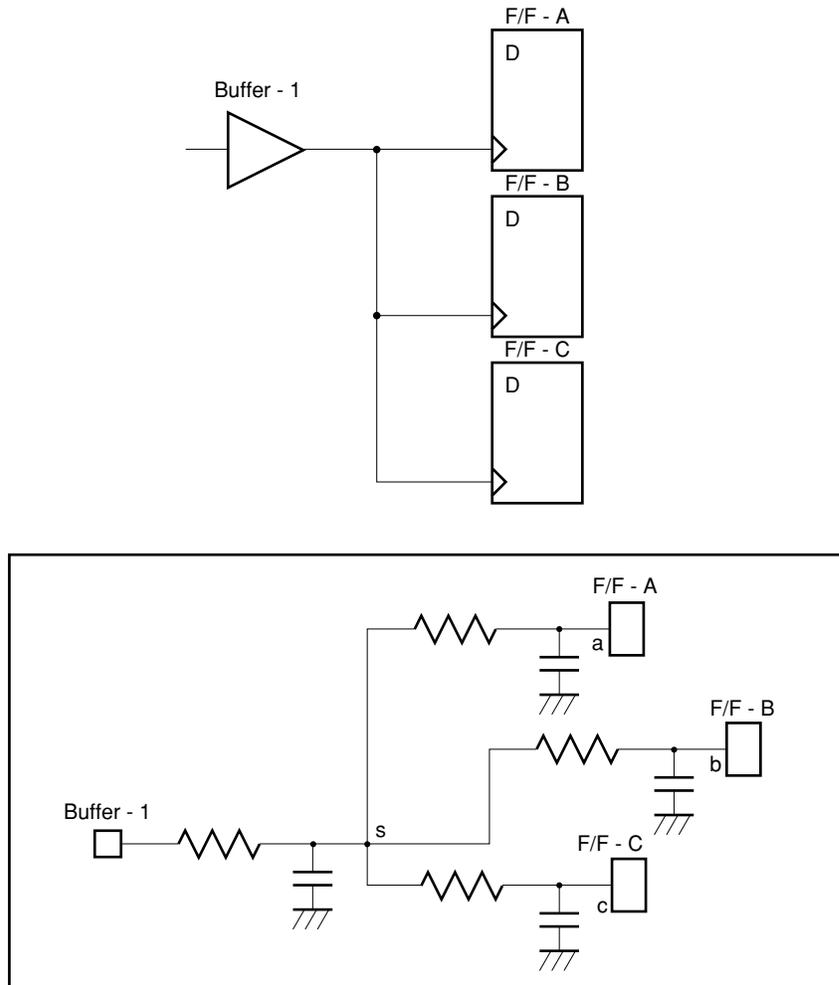
The s to a delay time differs from the s to b and s to c delay times due to wiring resistance.

Clock skew is a shift of the clock signal between sequential circuits.

This shift becomes greater if the wiring resistance becomes large and is also dependent on the wiring length from the point of divergence of the circuits. Follow the measures below to allow for clock skew when performing single-phase circuit design.

(a) Try to allocate similar clock lines in the same macro. (see **Figure 5-9 (a)**).
(b) When allocating a large number of clock lines, allocate the lines as shown in **Figure 5-9 (b)** so that errors due to clock skew do not occur.
(c) Accelerate the operation of the final-stage register by structuring the synchronous counters and shift registers (see **Figure 5-10**).
(d) Use clock tree synthesis (see **5.4.3 Clock tree synthesis**).

Figure 5-9. Clock Skew Countermeasure 1

(a)

(b)
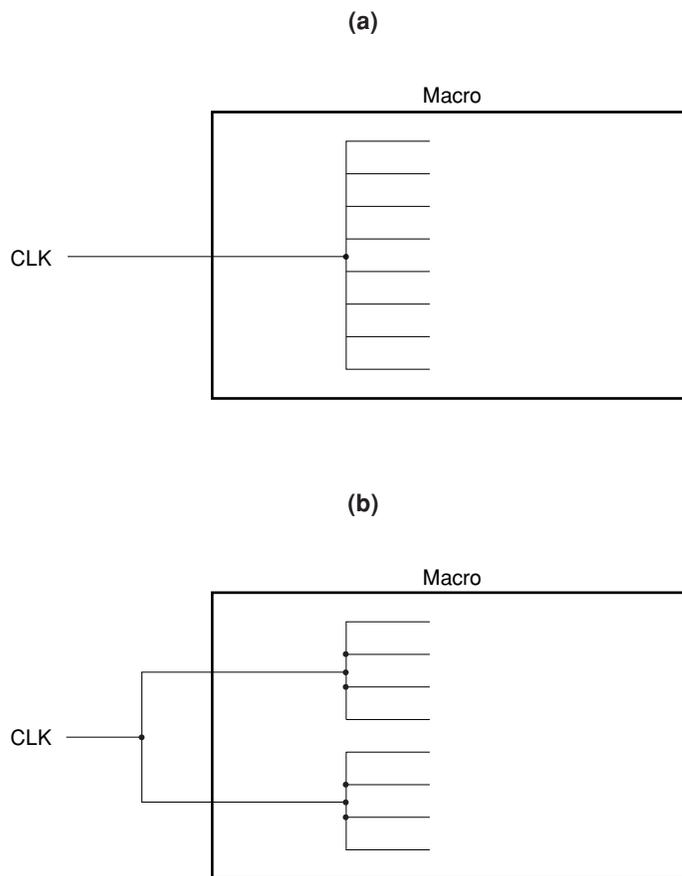
Figure 5-10. Clock Skew Countermeasure 2

(a) Circuits with potential for malfunction
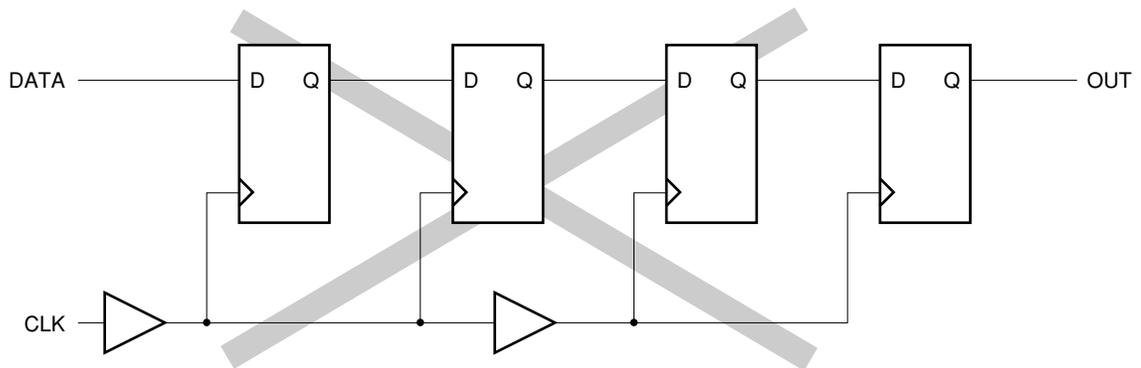
(b) Circuit with a clock skew countermeasure
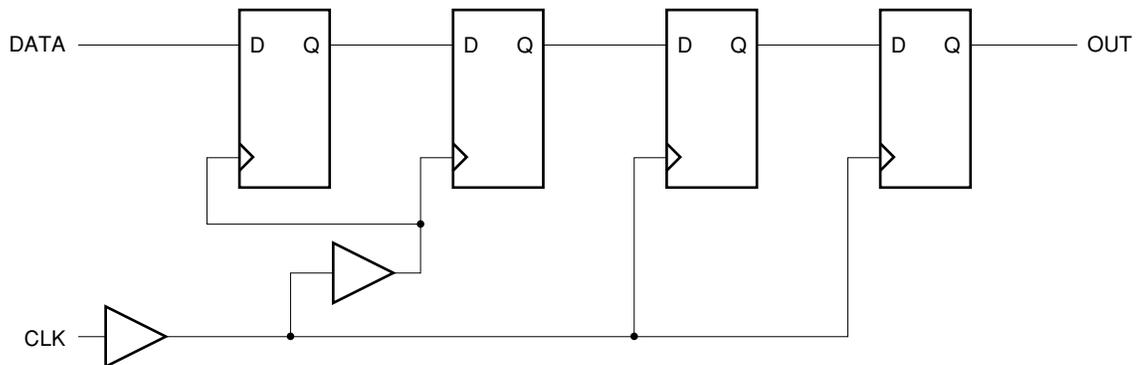
If buffers are inserted in the clock line due to the fan-out limitation, the countermeasures illustrated in Figure 5-10 (b) must be taken.

(2) Multi-phase synchronous circuit design

Operation of sequential circuits in multi-phase synchronous circuit design normally involves two or more clock signals with a constant relationship. This method avoids contention of clock operation between sequential circuits.

Figure 5-11. Double-Phase Synchronous Circuit
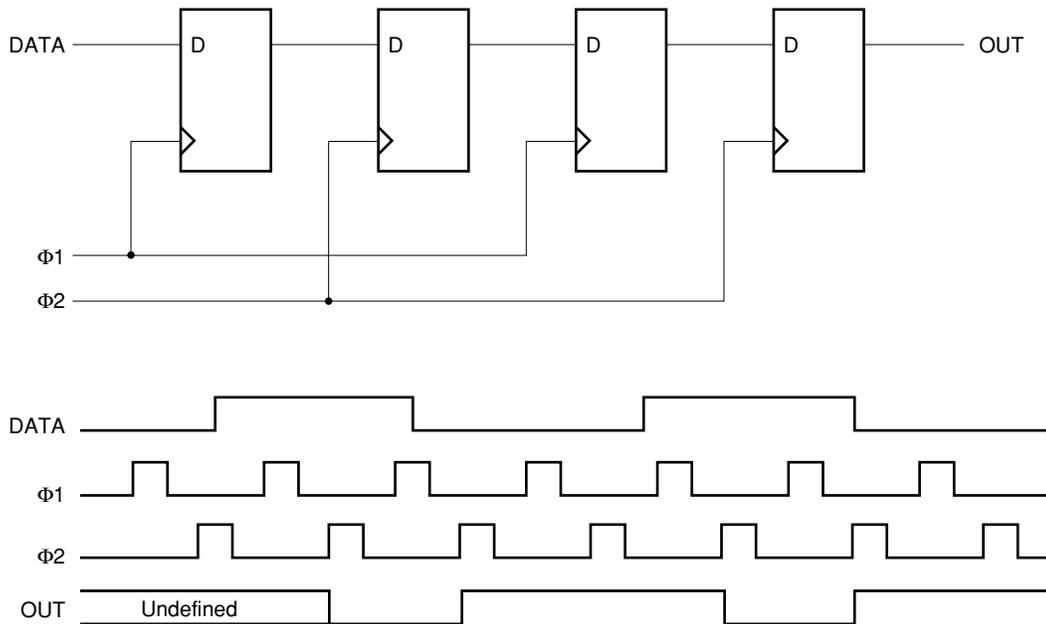
Figure 5-11 is an example of a double-phase clock circuit. The two clock signals ($\Phi1$ and $\Phi2$) vary in timing to avoid hold time errors between two sequential circuits. Even if there is interaction between complex sequential circuits, testing for timing contention can be curtailed by alternately operating sequential circuits. In addition, since the number of gates is reduced in this circuit example, a latch can be used instead of a flip-flop.

In multi-phase synchronous circuit design, configure the several clock signals from the basic clock signal. This will result in a lower clock frequency than that needed for a normal single-phase circuit (high speed is possible with a pipeline structure).

5.4.2 Clock skew

Clock skew is generated by wiring length variations in actual placement and routing. Hold time errors in sequential circuits can result from this clock skew. Normally, discrepancies due to these kinds of variations cannot be detected in the simulation that is performed before the placement and routing. The following guidelines are provided to minimize this problem.

(a) Clock line design in a macro

One clock line should be supplied in single-phase synchronous circuit design.

It is basically not necessary to test for clock skew in multi-phase synchronous circuit design. However, it is necessary to check the operating frequency.

(b) Clock line design between macros

There are clock skew problems especially between macros in single-phase synchronous design. Some examples of countermeasures are shown in Figure 5-12.

Figure 5-12. Countermeasures for Clock Lines Between Macros

(a) Insert delay gates

A delay gate must be inserted within macro B in order to gain flip-flop hold time.
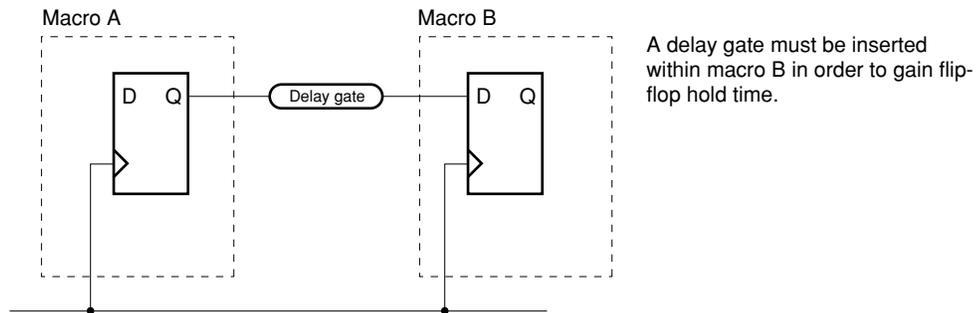
(b) Receive signal by inverse-phase clock
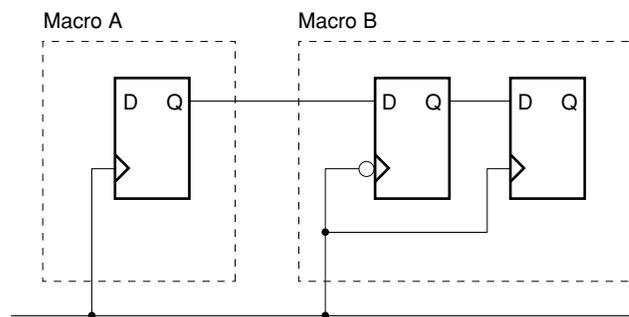
(c) Make circuit multi-phase
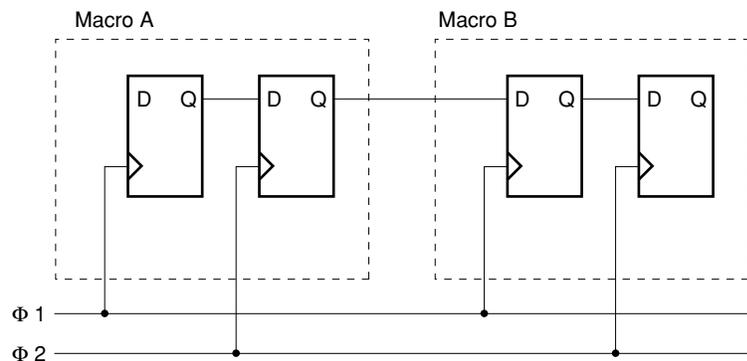
Figure 5-12 (b) uses the inverse phase of the clock to create a hold time margin. With this method, it is necessary to keep the clock frequency and duty cycle in mind.

Figure 5-12 (c) is a measure using a multi-phase clock. In this case, it is necessary to keep the clock frequency in mind.

5.4.3 Clock tree synthesis

Clock tree synthesis (CTS) is a technique that minimizes clock skew between flip-flops that are connected to the clock line. As shown in Figure 5-13 (a), the distance between the clock driver and each flip-flop is not constant. In addition, wiring resistance increases due to shrink processing. Because of this, the variations in wiring length are linked to clock skew. With CTS, a buffer is inserted in the clock line. This uniformly distributes the clock line, as shown in Figure 5-13 (b). Therefore, NEC Electronics recommends the use of the CTS instead of clock drivers.

Figure 5-13. Concept of CTS

(a) Conventional   **(b) CTS**

■ First-level driver
▦ Second-level driver
▨ Third-level driver
▯ Flip-flop
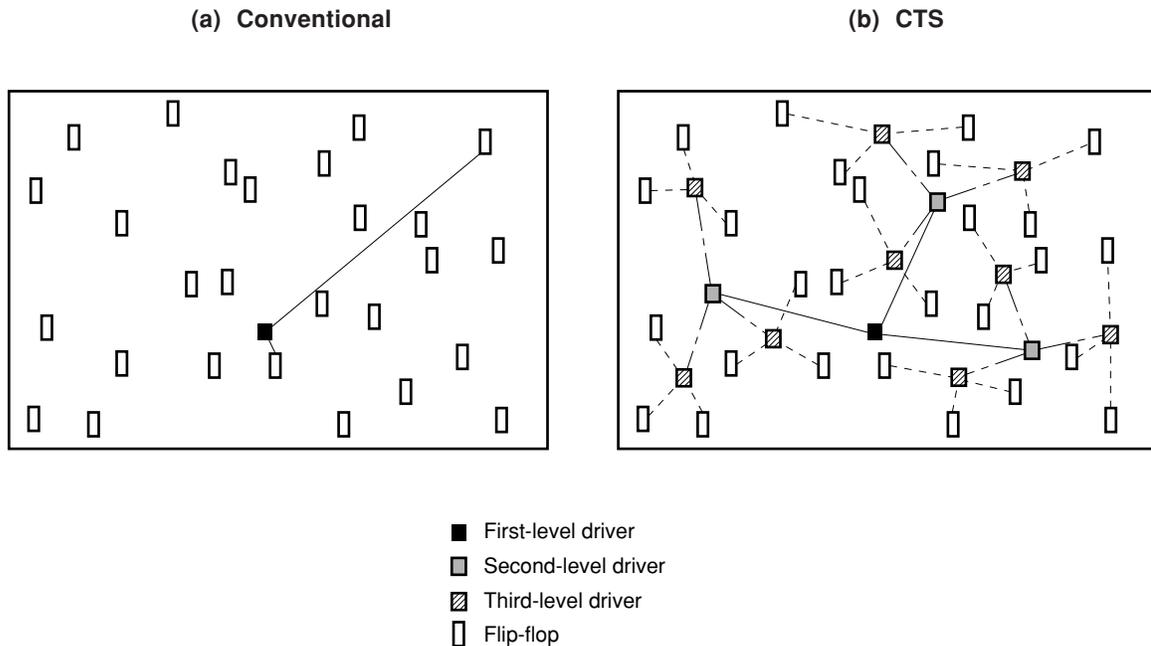
(1) Benefits of CTS

In CTS, a CTS block is substituted for the clock drivers (FCKA to E) that are usually used. Figure 5-14 shows how the clock line buffer is inserted. An inverter is used since the path delay time is shortened with actual CTS. This is how clock distribution is performed. As a result, the number of blocks that are inserted includes the number of CTS drivers. The block names and the number of stages of inserted block are shown in Table 5-3. The selection of the blocks to be used is based on the number of clock line branches.

Cautions 1. NEC Electronics recommends the use of only one CTS per chip. Using more than one CTS is possible, however, it may cause the cell usage rate to decrease and the clock skew to increase as the number of times CTS is used increases. In addition, because more time is needed for clock tree synthesis and placement and routing as the number of CTS operations is increased, users are advised to check their design schedule.

2. When an oscillator (resonator) is also being used, see 7.3.3 Using oscillator (resonator) and CTS together.

Table 5-3. CTS Blocks (Reference)

Block Name	Number of Stages	Block Inserted	Number of Branches on Clock Line				
			32 to 128	128 to 1280	1280 to 2560	2560 to 5120	5120 or more
FC42	2	F144	◎ (33:1.70) ±0.20 ns	○ (33:2.40) ±0.30 ns	×	×	×
FC82	2	F148	×	◎ (33:1.70) ±0.20 ns	○ (33:2.10) ±0.35 ns	×	×
FC44	4	F144	×	◎ (85:1.40) ±0.15 ns	○ (85:1.80) ±0.35 ns	×	×
FC84	4	F148	×	×	◎ (85:2.60) ±0.15 ns	◎ (85:3.00) ±0.25 ns	◎ (165:3.40) ±0.40 ns

Remark Each symbol has the following meaning.

×: Cannot be used

○: Can be used

◎: Preferred (recommended)

The values in parentheses represent the estimated number of inserted blocks (the first value), followed by the estimated delay time. The value on the next line is the estimated clock skew value, which varies slightly according to the conditions.

Cautions 1. FC42 or FC44 is recommended when using CTS in a chipset that is susceptible to EMI or noise.

2. If an OSOn oscillator block is directly connected to FC82, noise may occur, making stable oscillation impossible. Therefore, be sure to insert a gate between these blocks as shown in 7.3.3 Using oscillator (resonator) and CTS together.

Figure 5-14. Image of CTS Use (Example of FC44)

Total: 16 blocks   Total: 64 blocks
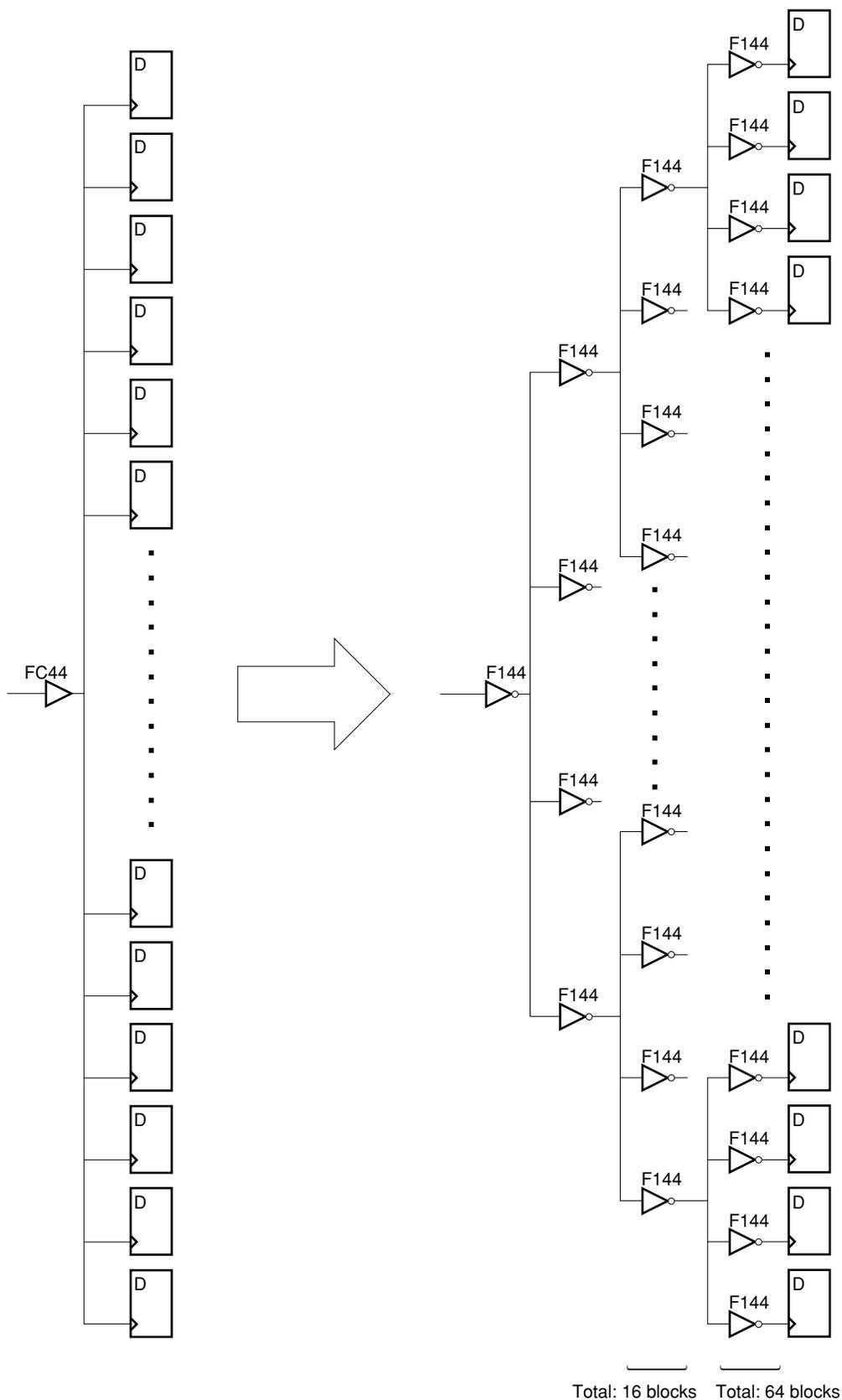
(2) Clock tree synthesis guidelines
The following precautions apply when using CTS.

(a) The section from the output of the clock tree synthesis block (FCTS) to the block that requires optimized clock skew must be described by one net.
If a function block is inserted in the path, the clock skew up to the function block is optimized.

Figure 5-15. Clock Skew Optimization

In clock tree synthesis, the clock skew is optimized as far as the thick wires.
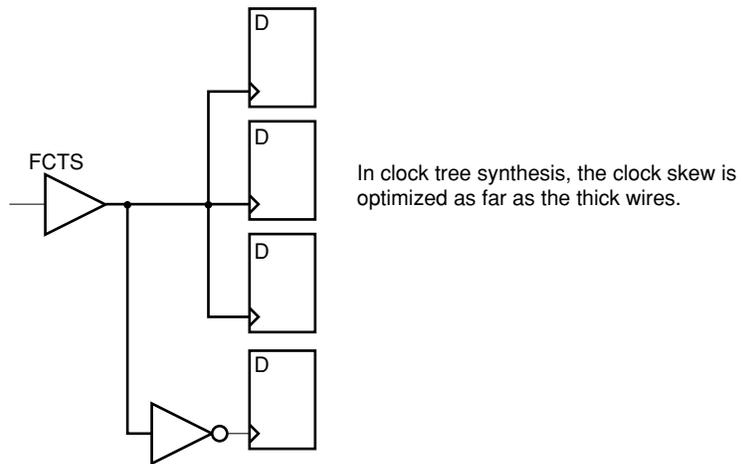
(b) The FCTS is described in the TOP level hierarchy and is not entered in the macro. This makes skew optimization difficult.

Figure 5-16. Example of CTS Block Description
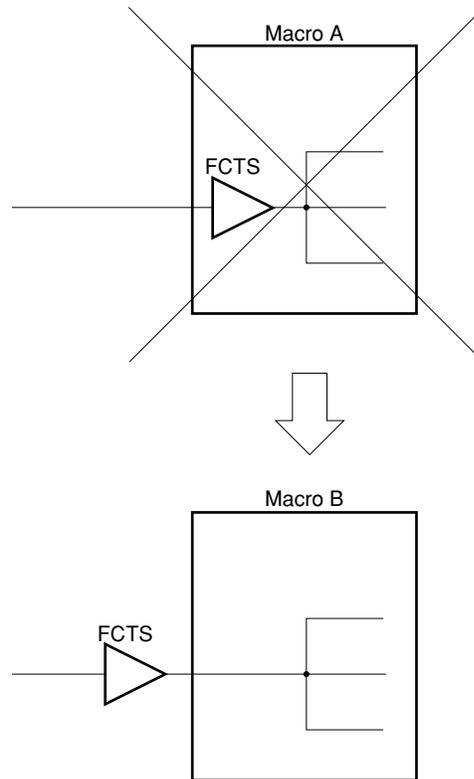
(c) Routing detours increase with large macros and high use rates, and there are cases where clock skew cannot be sufficiently optimized.

5.5 Notes on Configuring High-Speed Circuits

Generally, when comparing the characteristics of P-ch and N-ch transistors, an N-ch transistor can pass a higher current than a P-ch transistor. Therefore, a NOR gate consisting of P-ch transistors connected in series has a reduced load drive capability at the rising of the output. For example, a NOR block is slower than a NAND block, and has poor fan-out characteristics.

Guidelines to be followed when structuring a circuit that will run at high speed are shown below.

(1) Structure the circuit by using logic conversion techniques and standard NAND blocks.
  - The circuit's speed will improve, as will the circuit's stability (see **Figure 5-17 (a)**).

(2) Structure the circuit so that the fan-out is as small as possible to lighten the load.
  - In general, observe the 1/3 to 1/2 fan-out limit (see **Figure 5-17 (b)**).

(3) Convert from low-power blocks to standard blocks.

Figure 5-17. Configuring High-Speed Operational (Stable) Circuits
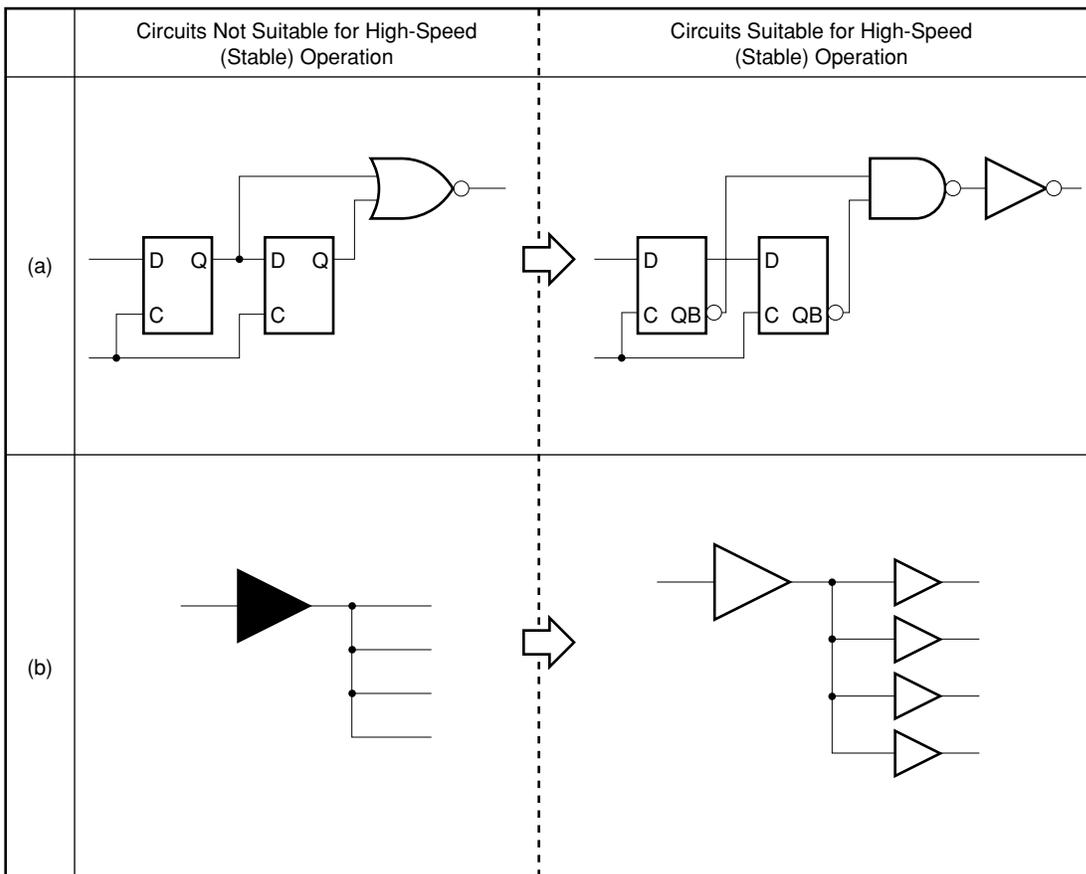
5.6 Delay Time Margin

Logic circuits consist of combination circuits whose output is determined simply by the state at their inputs and sequential circuits whose output is determined by the state at their inputs and their previous state. Specifically, sequential circuits consist of gate circuits with feedback, flip-flops, and latches.

Bearing in mind testability considerations and ease of design estimation for delay time, it is clear that individual combination and sequential circuits cannot be too large. Also, a majority of the sequential circuits are operated in synchronization with the system clock, which has an adequate margin with respect to the delay times of the combination circuits.

In the portion where adequate margin cannot be secured by the clock, timing of the entry of the sequential circuit, i.e., each input of flip-flops and latches, must be secured.

5.6.1 Timing definitions

(1) Setup time (t_{su})
In latches or flip-flops, the data setup time needed to read data at the active edge of the clock.

Figure 5-18. Setup Time
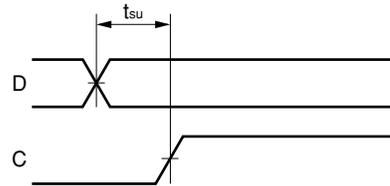
(2) Hold time (t_h)
In latches or flip-flops, the data hold time needed to read data at the active edge of the clock.

Figure 5-19. Hold Time
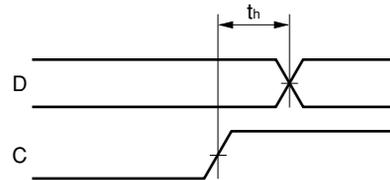
(3) Release time (t_{rel})
In latches and flip-flops, the time needed from release of the reset or set until the active edge of the next clock becomes valid.

Figure 5-20. Release Time
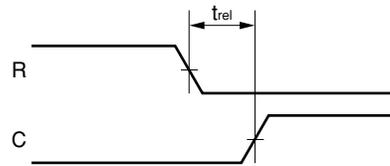
(4) Removal time (t_{rem})
In latches and flip-flops, the time needed to make the active edge of the clock invalid when the reset or set is cancelled.

Figure 5-21. Removal Time
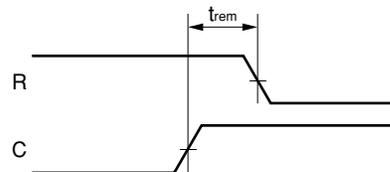
(5) Minimum pulse width (t_w)
In latches or flip-flops, the minimum time of the clock, reset, or set pulse width needed in order to read data correctly.

Figure 5-22. Minimum Pulse Width
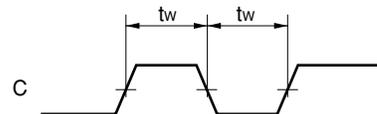
5.6.2 Delay time margin calculation (asynchronous circuits)

The setup time and the hold time for the circuit in Figure 5-23 are described as an example of calculating the delay time margin. Here, the variation and wiring length are set conditionally as to decrease the margin. If the specifications that are determined by each block (t_{su} and t_h) are satisfied, then decisions about normal operation can be ascertained.

Figure 5-23. Example of Delay Time Margin Calculation Circuit
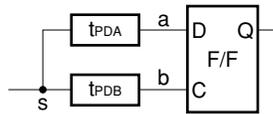
Figure 5-24. Timing Estimate

(a) Setup time (t_{su})
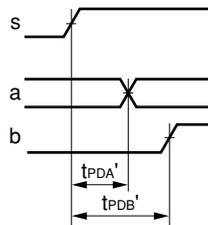
(b) Hold time (t_h)
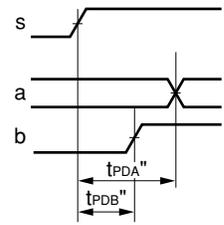
Calculation equations:

$$t_{su} < t_{PDB'} - t_{PDA'}$$

$$= t_{PDB(MIN.)} - t_{PDA}[MIN.(MAX.)]$$

$$= t_{PDB(MIN.)} - t_{PDA(MIN.)} \times \frac{1 + \alpha}{1 - \alpha}$$

$$t_h < t_{PDA''} - t_{PDB''}$$

$$= t_{PDA(MIN.)} - t_{PDB}[MIN.(MAX.)]$$

$$= t_{PDA(MIN.)} - t_{PDB(MIN.)} \times \frac{1 + \alpha}{1 - \alpha}$$

α: Distribution coefficient (0.1)

5.6.3 Delay time margin calculation (high-speed circuits)

In circuits operating at high frequencies, the operating margin for an internal functional block's delay time is small since the single-cycle time is short.

Here, the delay time margin calculation for both in-phase and inverse-phase circuits is described.

(1) In-phase clock

Consider the shift register operation containing delay between flip-flops F1 and F2 in Figure 5-25.

As shown in Figure 5-26, the points at which this circuit is inspected are where the output data (Q in F1) passes through delay A and is input to F2 (sampling timing <1>) and at sampling timing <2>, where a check is made to see if the data is read normally.

Therefore, the value resulting from adding the maximum delay at point a to the setup time of F2 must be obtained within one time period (T).

Figure 5-25. Example of In-Phase Clock Circuit
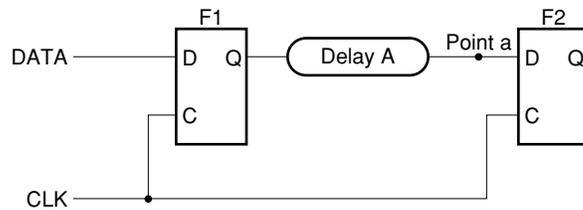
Figure 5-26. In-Phase Clock Timing
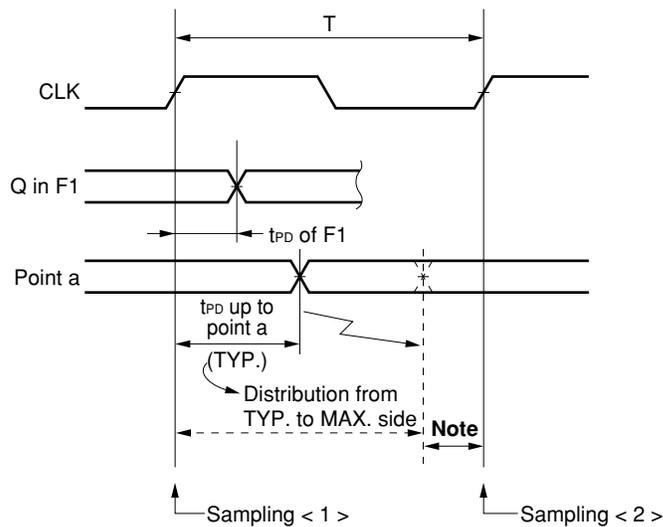
Note Do not cross into the next sampling timing with respect to the F2 setup time.

Calculation equation:

$$T - (t_{PD(F1)(MAX.)} + t_{PDA(MAX.)}) > t_{SU(F2)}$$

The following countermeasures are necessary if this relationship is not satisfied:

- Reduce the amount of delay of delay A
- Lower the operating frequency (lengthen period T)

(2) Inverse-phase clock

Figure 5-27 is an inverse modification of the F2 clock's active edge shown in Figure 5-25. Since both the rise and fall edges are used, the operating margin varies with the CLK duty. The circuit normally operates under the following conditions.

Figure 5-27. Example of Inverse-Phase Clock Circuit
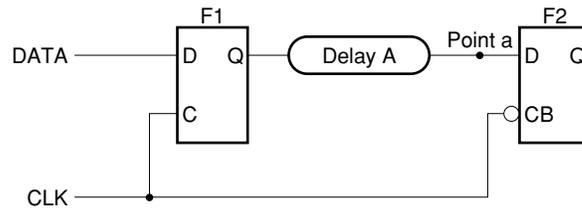
Figure 5-28. Inverse-Phase Clock Timing
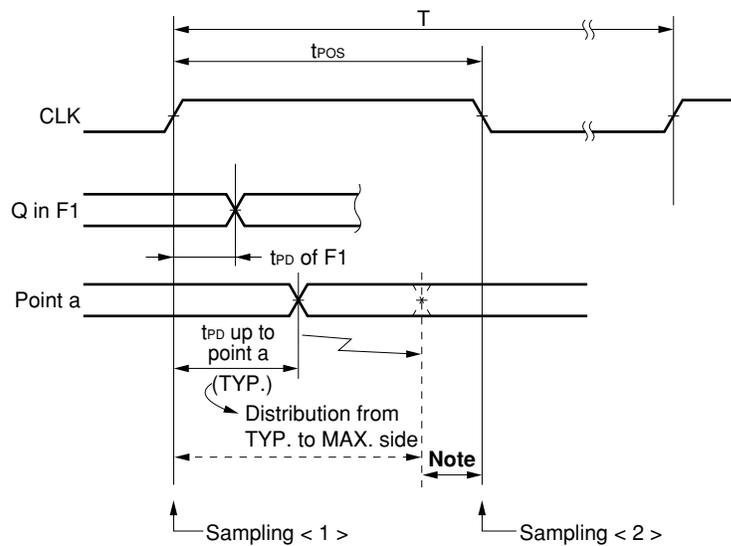
Note Do not cross into the next sampling timing with respect to the F2 setup time.

Calculation equation:

$t_{POS} - (t_{PD(F1)(MAX)} + t_{PDA(MAX)}) > t_{SU(F2)}$

The following countermeasures are necessary if this relationship is not satisfied:
- Reduce the amount of delay of delay A
- Lower the operating frequency (lengthen period T)
- Increase the CLK duty

5.6.4 Minimum pulse width

With circuits operating at high speed, there are cases when the minimum pulse width for a flip-flop input clock is not satisfied due to the delay difference between the rise and fall of the signal and the relative variation of an identical path.

For example, in Figure 5-29, the signal input by CLK passes through delay B and is input to the clock of the flip-flop. The timing is shown in Figure 5-30. In regard to delay B, when the fall time delay ($t_{PDB(LL)}$) is greater than the rise time delay ($t_{PDB(HH)}$), t_{NEG} becomes greater than $t_{NEG(MIN.)}$, and the pulse becomes narrow. $t_{NEG(MIN.)}$ is estimated by the conditional setting of $t_{PDB(LL)}$ to the maximum and $t_{PDB(HH)}$ to the minimum relative variation direction.

Figure 5-29. Minimum Pulse Width Estimate   **Figure 5-30. Pulse Narrowing**
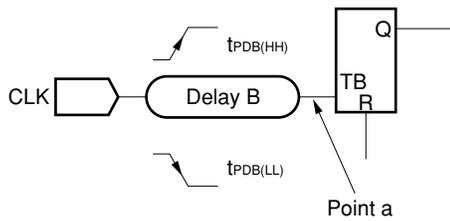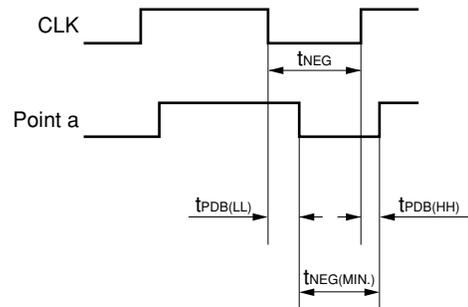
Calculation equations:

$$t_{NEG(MIN.)} = t_{NEG} + (t_{PDB(HH)(MAX.)} - t_{PDB(LL)[MAX.(min.)]}) > t_W$$

$$\rightarrow t_{NEG(MIN.)} = t_{NEG} + (t_{PDB(HH)(MAX.)} - t_{PDB(LL)(MAX.)} \times \frac{1 - \beta}{1 + \beta}) > t_W$$

β: Distribution coefficient (0.1)

The ratio $t_{PDB(HH)}/t_{PDB(LL)}$ is controlled in order to regulate the minimum pulse width of the signal that is input to the flip-flop clock. This increases the duty cycle. In the example above, if the functional block in delay B is changed to a type in which the fall delay ($t_{PDB(LL)}$) is fast and the rise delay ($t_{PDB(HH)}$) is slow, $t_{NEG(MIN.)}$ increases. In addition, it is necessary to be aware that the high-level pulse width must satisfy the minimum pulse width standard.

5.6.5 Metastable state (preliminary)

If the setup and hold time standards are not satisfied and the clock and data or clock and set/reset are changed simultaneously, the output may be oscillated at the flip-flop and latch and become an intermediate level that is neither high nor low. This unstable state is called a metastable state. The metastable state ends after a certain time, and the output settles into a high or low level. However, an unstable state results since the level that is defined has no relationship to the data input level.

In the cases where the setup, hold, release, and removal times cannot be satisfied, take the countermeasures shown below to prevent this unstable state from spreading over the entire circuit.

Setup time (t_{su}) .... Time that the data signal must secure before the clock changes
Hold time (t_h) .... Time that the data signal must hold after the clock changes
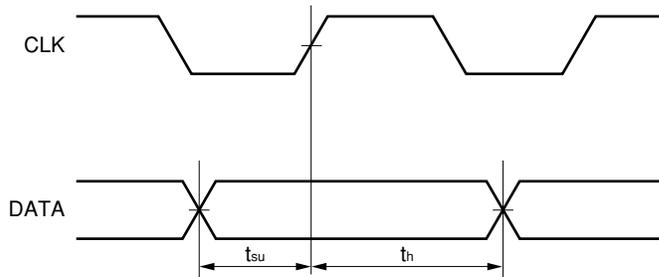
Caution The specified t_{su} and t_h must be satisfied (see the CMOS-N5 Series (5.0 V) Block Library (A13872E) and CMOS-N5 Series (3.3 V) Block Library (A15895E)).

Release time (t_{rel}) .... Time after the set/reset signal changes until the clock becomes valid
Removal time (t_{rem}) ..... Time needed in order to make the clock invalid
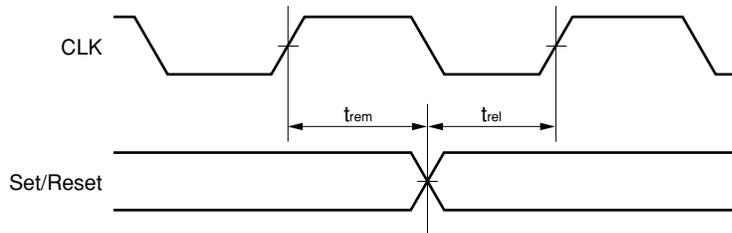
Caution The set or reset signals must not be cancelled in the vicinity of the active edge of the clock.

(1) Metastable state generation and recovery time
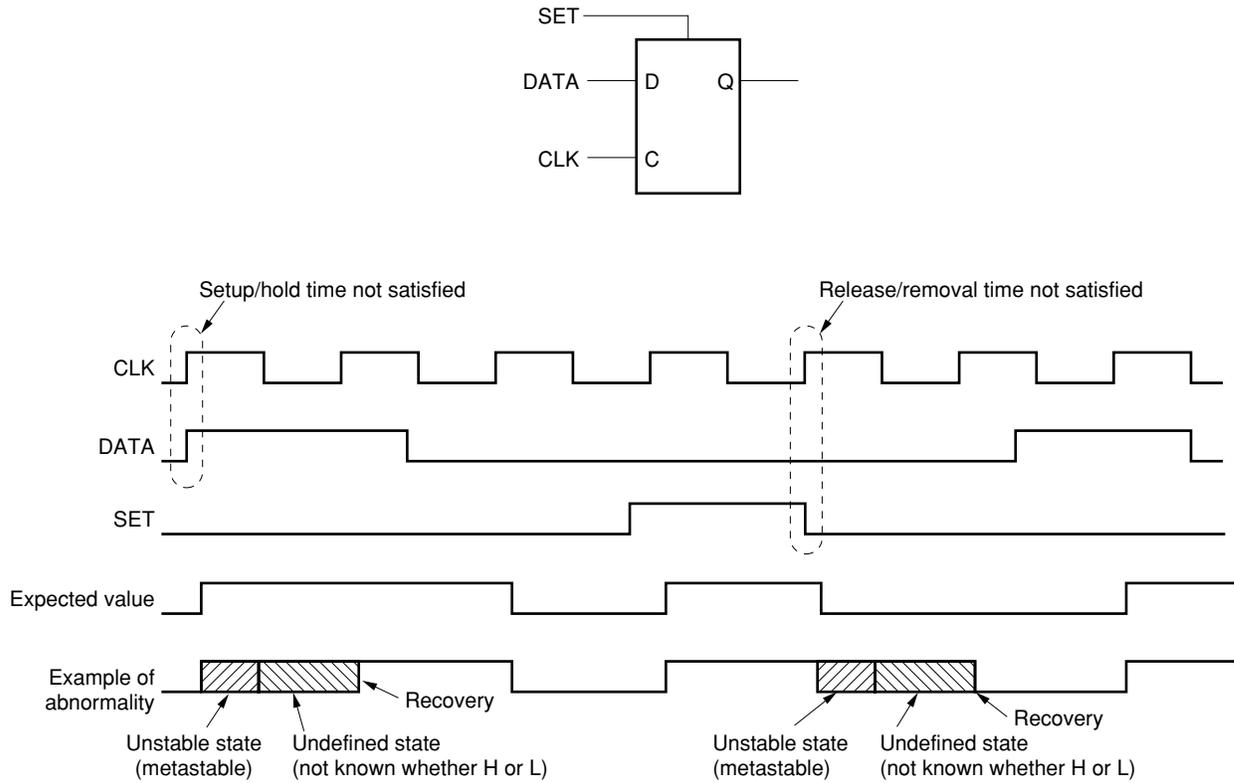
In the CMOS-N5 Series, the time of the metastable state is specified as shown below. After this time, the state is either H or L, but it is not clear which (shown as "undefined" in the above figure).

Metastable time = $t_{PD (MAX.)} \times 6$

$t_{PD (MAX.)}$ ...... Maximum value of the delay time from the active edge of the clock until the output changes (when the ratings of the setup/hold time could not be satisfied); or, release/removal time (when the ratings of the release/removal time could not be satisfied).
There is no problem even if $t_{PD0(MAX.)}$ is used in F×××-type sequential circuits. For the respective values, see the **CMOS-N5 Series (5.0 V) Block Library (A13872E)** and **CMOS-N5 Series (3.3 V) Block Library (A15895E)**.

(2) Avoiding a metastable state

When the stipulated times cannot be satisfied (asynchronous input signals), configure the circuit so that the occurrence of metastability will not affect the later stage. Examples of the abnormality and how to avoid it are shown below.

Example of abnormality

When the output from b in the figure below is input to the counter, an excess number of counts may occur.
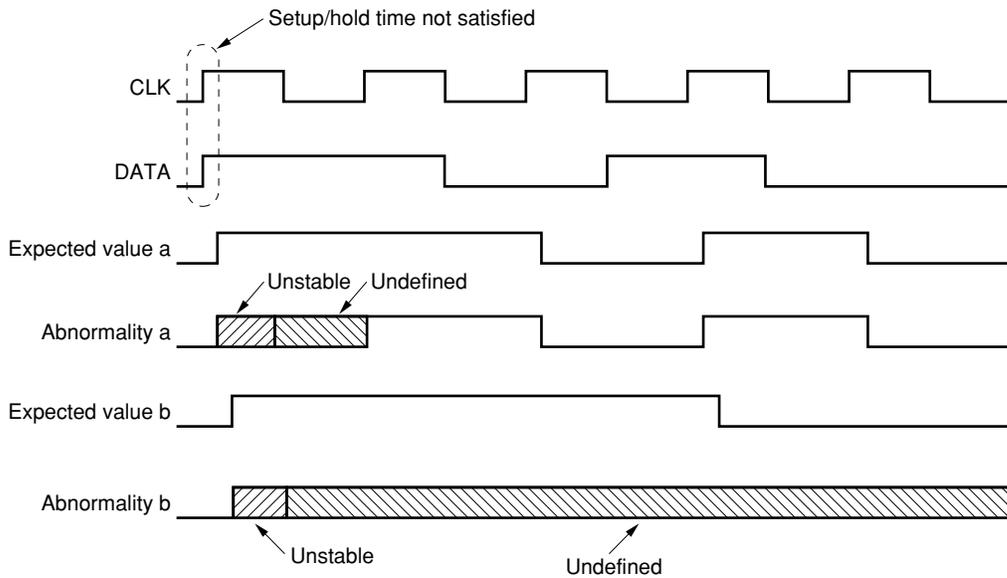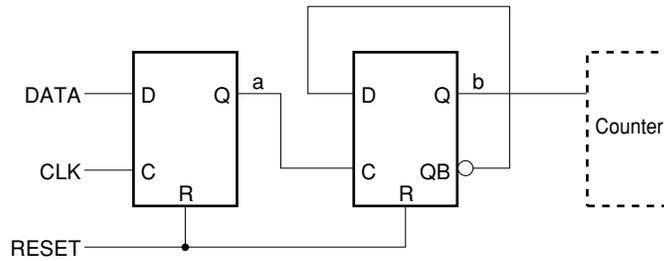
Example of avoiding abnormality

Output c is stable due to the insertion of the flip-flop. However, although the initial clock at c can have two values as a function of the instability of b, there is no effect on the counter in the following example.
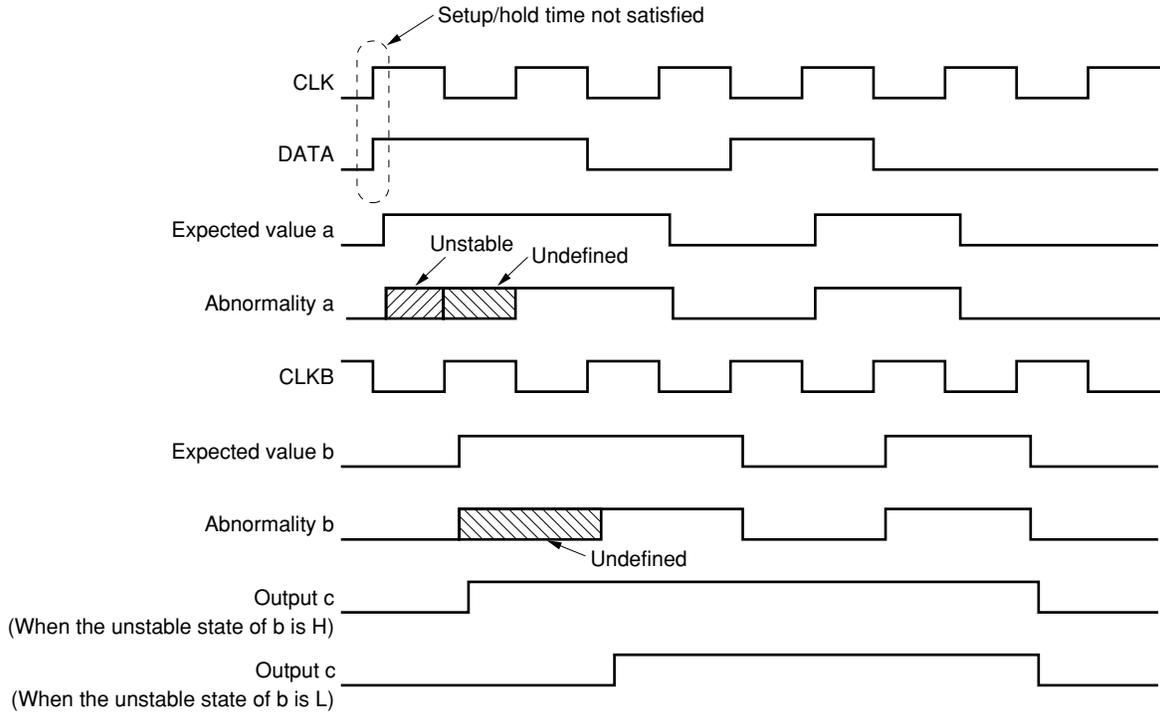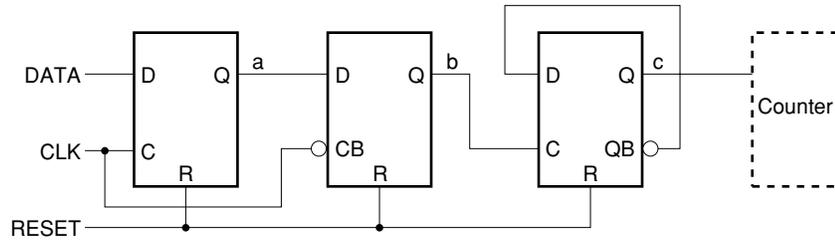
Remark   Clock width > $t_{PD(MAX.)} \times 6 + (t_{su}$ or $t_h)$

5.6.6 Critical paths

A critical path relates to the system timing contained in the gate array. It is the path that establishes the delay time for the gate array (see **Figure 5-31**). In this example, a detailed investigation of the paths A, B, and C (the critical paths) is necessary.

- Path A: Is the input timing of the device in the next stage satisfied for gate array output sampling by CLK?
- Path B, C: Is the sampling timing satisfied in the gate array by the controlling device's output timing?

Figure 5-31. System with Critical Paths
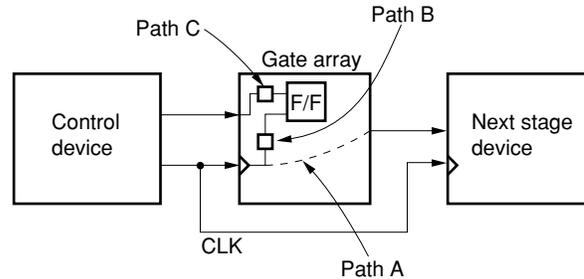
The following three types of critical paths are available:

<1> Input to output
<2> Input to input
<3> Output to output

The inspection and specification methods for these critical paths are explained in the following sections.

(1) Calculating and designing a critical path

As described in **4.4.3 Estimating wiring capacitance**, placement and routing are executed by determining the placement range for each macro hierarchy (first hierarchy only). Consequently, the intramacro and intermacro wiring lengths differ significantly. The following points must be noted when the propagation delay time of the critical path is estimated using the virtual wiring capacitance listed in Table 4-5.

<1> The critical path can be terminated in one macro hierarchy (first hierarchy) (excluding the I/O buffer).

<2> The load connected to the path can be reduced by making the critical path as simple as possible (limiting the fan-out value to 1/3).

<3> Except as given above, the input and output pins should be placed as close together as possible in regard to critical paths from the input to output pins.

<4> Circuits other than critical paths should not be included in macro hierarchy.

(2) Critical path between input and output

Path A in the circuit example of Figure 5-31 is not influenced by other inputs. The maximum t_{PD} value must be designed to be smaller than the value required by the system.

In addition, keep in mind the large dependency of the output buffer's delay time on the external load capacitance C_L.

Calculation equation:

$t_{PD(MAX.)}$ < System specification value

(3) Critical path between two inputs

The circuit configuration in Figure 5-32 will be calculated as an example to study the input sampling timing. Calculation will be made assuming that the timing of a signal input from outside is as shown in Figure 5-33, since the mutual timing specification between the input pins must be well defined in this timing verification.

Figure 5-32. Example of Input-Input Critical Path   **Figure 5-33. Verification of Setup Time**
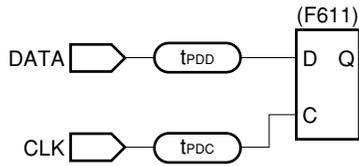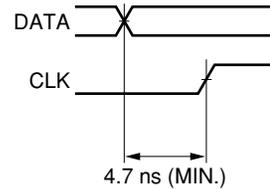
The following points must be taken into consideration with respect to the conditions used:

• Absolute variation is in the direction of the smallest margin
• Relative variation is in the direction of the largest t_{PDD} and the smallest t_{PDC}

The method for making these decisions is shown below.

Calculation equations:

DATA is assumed to be a time differential of 4.7 ns (MIN) from CLK, as shown in Figure 5-33.

$$t_{PDC(MIN.)} - t_{PDD}[MIN.(max.)] + 4.7 > t_{SU}$$

$$\rightarrow t_{PDC(MIN.)} - t_{PDD(MIN.)} \times \frac{1 + \alpha}{1 - \alpha} + 4.7 > t_{SU}$$

α: Distribution coefficient (0.1)

5.6.7 Ensuring operating margin

When a circuit lacks an operating margin as the result of a delay margin check and a critical path check, there are several things that can be done, depending on the circuit's configuration.

Generally, the following methods are used.

<1> Reassess input and output specifications
- Decrease the input $f_{MAX.}$ and lower the input $f_{MAX.}$ duty variation
- Ease the input and output timing and decrease the output's load capacitance

<2> Reassess pin placement
- Shorten the wiring length to decrease the delay between input and output (adjacent placement of pins)

<3> Modify the circuit
- Decrease the delay time by simplifying the circuit
- Decrease the delay time by decreasing the load on the circuit
- Obtain a margin by inserting a delay gate

Delay calculations (or recalculations) are necessary when modifying a circuit, so it is particularly important to estimate the inserted gate output wiring length as 0 mm in regard to delay gate insertion.

5.7 Internal Bus Configuration

5.7.1 Configuring internal bus

Typical data selection techniques include the data selector format and the bus format. The circuit configuration of a data selector (multiplexer) can become very complex. On the other hand, the bus format enables a comparatively simple circuit configuration that it is easier to understand and the number of cells used does not increase. However, the propagation delay time may increase. Therefore it is important to select the optimum format according to the circuit structure.

Figure 5-34. Bus Configuration
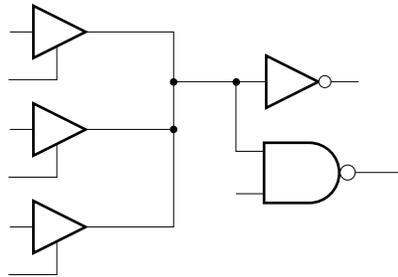
5.7.2 Preventing internal bus floating

As a basic rule when using an internal bus, **only one** block configured on the same bus line should be in the output enabled state. This is necessary to avoid the input of the next stage block being in a floating state. Examples of a good internal bus circuit structure are shown in Figure 5-35.

Figure 5-35. Examples of Internal Bus Floating Prevention Circuit

(a) Example 1   **(b) Example 2**
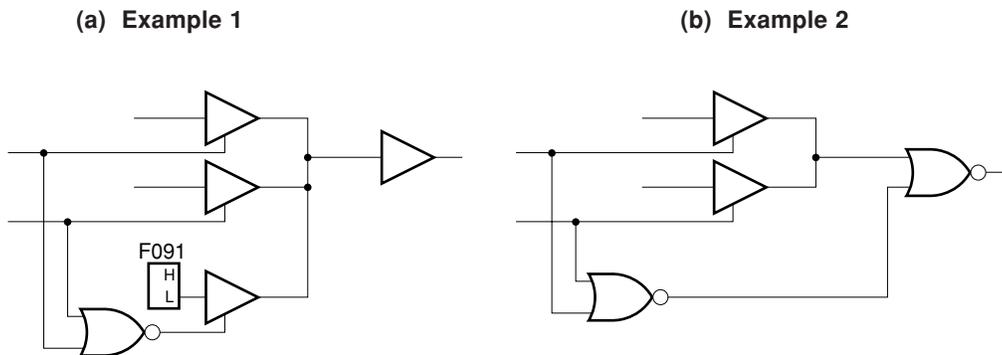
5.7.3 Precautions when using internal bus

Although the internal bus can operate with multiple blocks connected on the same bus line, the signal rise and fall times may increase due to an increase in wiring length and an increase in the fan-in loading of the previous block. Since problems in operating stability and reliability may result, the following constraints must be observed. For further information, see **5.8 Preventing Contention with External Bus**.

(1) Observe the bus constraints indicated by the following formula:

$$F/O + N \leq 50$$
$$(1.4 \times F/O + 1.1 \times N + 1.9) \times f < 410$$

F/O ... Sum of the fan-in loading (F/I) of the gates connected to the bus

N .... Sum of the 3-state output buffers (F531, F532) connected to the bus

f .... Operating frequency (MHz) of the bus

Contact NEC Electronics if it is required that the design exceeds the above conditions.

(2) Basically, the following states are prohibited on the bus line.

(a) More than two outputs are enabled on the same bus line.

(b) All outputs are disabled on the same bus line.

Consider enable-signal skew in order to converge the above states within no more than 20 ns.

5.8 Preventing Contention with External Bus

In addition to the explanation in **5.7.3 Precautions when using internal bus**, the two items below should be noted when connecting gate array and other LSIs in a system using a bus configuration.

(1) Bus contention
(2) Bus floating

Take measures via timing design and pull-up/pull-down resistors in order to avoid these problems.
In addition, in order to avoid external bus floating, I/O blocks with pull-up and pull-down resistors can also be used. For further information, see **CHAPTER 7 MULTIFUNCTION BLOCKS**.

Figure 5-36. External Bus Floating Prevention Countermeasure
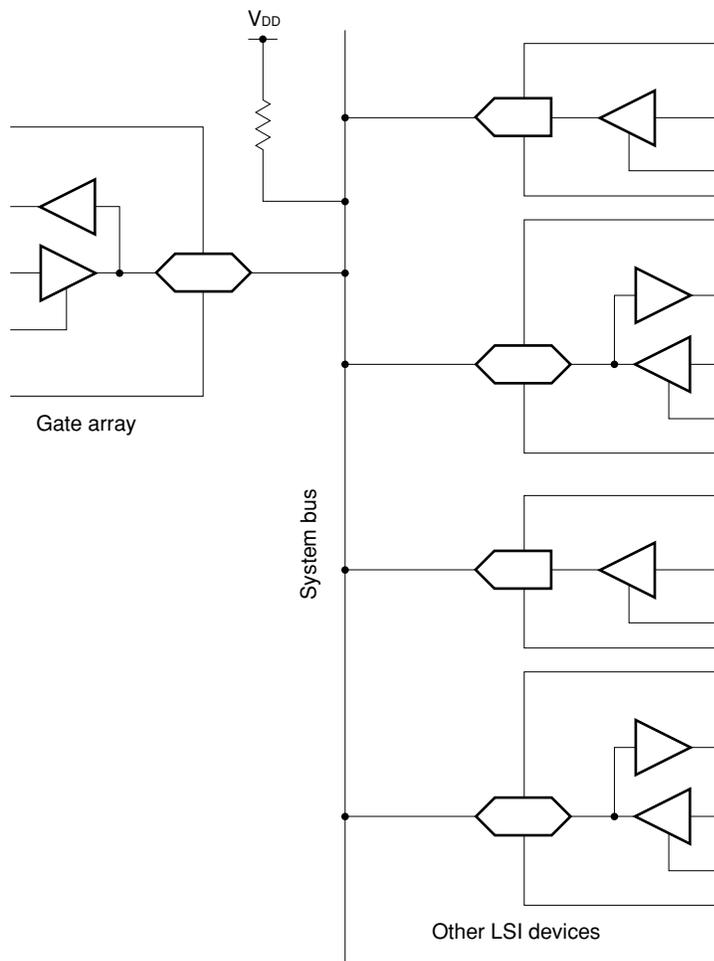
5.9 Testability

There is more than just logic design when designing a gate array. Testing and test circuits are also necessary. Consider the points shown below when designing the circuit and generating a test pattern. For more information, see **CHAPTER 6 TEST PATTERN GENERATION**.

- Flip-flop (F/F) initial setting
- Division of counters
- Addition of test pins
- Division (modularization) of internal circuits by test pins

5.9.1 Flip-flop initial setting

When the device is powered up, it is not known whether the output state of a block, such as a flip-flop or counter, is high level or low level. Consequently, the initial state must be set using the first few patterns during simulation.

In the design stage, the circuit should be configured so that an initial setting pattern is not too long, and blocks with reset inputs should be used as much as possible so that the initial state of the internal circuit can be reset.

Figure 5-37. Flip-Flop Initial Setting
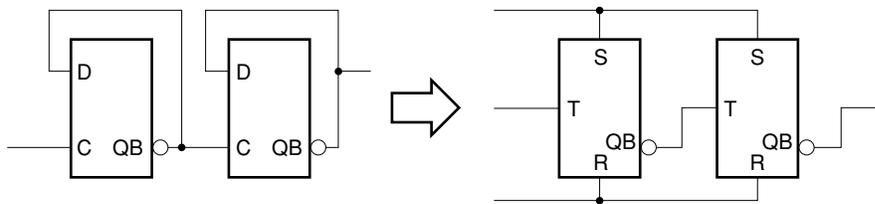
5.9.2 Counter division

With multi-bit counters, the effective test method is to divide the counters to reduce the number of test patterns.

For example, the number of pulses necessary until the final stage of a 16-bit counter operates is 2 to the 16th pulses. By dividing the 16-bit counter into two 8-bit counters as shown in Figure 5-38, however, the number of pulses can be cut by 1/100 to 1/200.

Figure 5-38. Counter Division
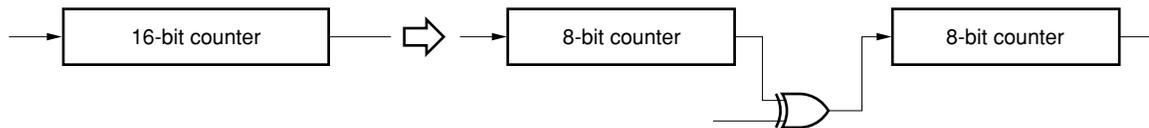
5.9.3 Adding test pins and dividing circuits

Similar to the case in **5.9.2 Counter division**, when testing multibit counters and large-scale macros, the LSI test can often be simplified and the number of test patterns reduced by setting up "test pins", which enable the operation mode to be set externally.

(1) An effective method to test LSIs when the circuit is internally divided into several operation modes is to set up pins (test pins) to enable the setting of a specific test mode.

(2) Large-scale circuits are often configured by several partitioned macros (modules), when testing such a circuit, an effective method is to set up specific test pins per partitioned module to enable testing of the circuit in a divided state.

5.10 Racing and Spike Noise

5.10.1 Racing (contention)

The state where the timing changes when there are more than two input signals in a logic block is called racing (contention).

If the test pattern shown in Figure 5-39 (b) is added to a circuit such as that in Figure 5-39 (a), a shift in flip-flop data and clock timing occurs due to the difference between the two delays in buffer 1 and 2 and the routing delay difference. The result of this is that the expected operation does not occur. In the case of Figure 5-39 (a), data is first set in the flip-flop, making it necessary to consider a change in the clock. The test pattern for this is shown in Figure 5-39 (c).

Figure 5-39. Racing

(a) Circuit with potential for racing
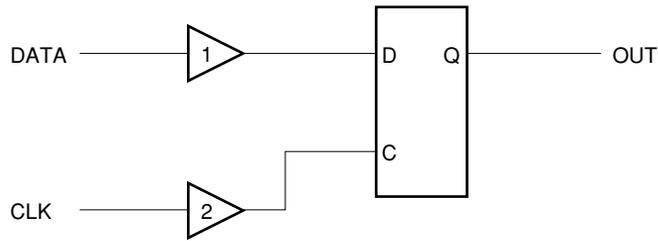
(b) Test patterns with potential for racing
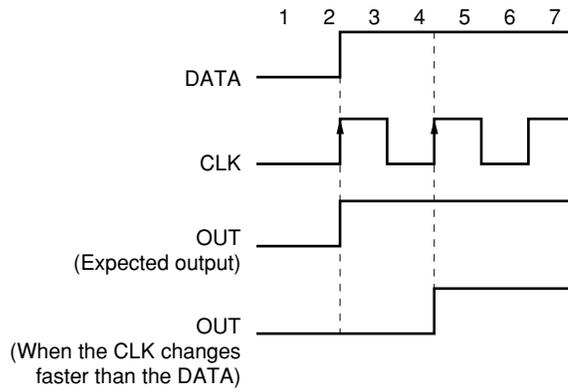
(c) Test patterns that do not cause racing
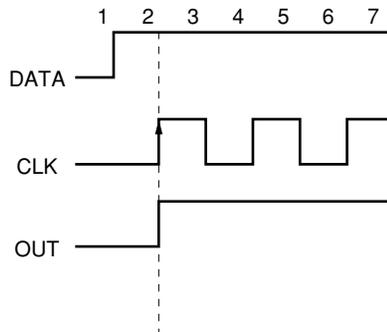
5.10.2 Spike noise

Spike noise is noise in a circuit that employs two or more gate inputs and is caused by a small input timing shift when the input signal timing changes. The time interval of this spike noise changes as a function of the size of the shift in timing. If the spike noise is input to the next-stage flip-flop clock or the set/reset, the affected signal path related to the flip-flop's output signal can generate errors in operation.

Consequently, when gates with two or more inputs are used, it must be checked whether an influence is exerted on the next-stage gates and the external output signals by spikes generated by changes occurring when the multiple inputs operate simultaneously. It must also be confirmed whether or not operating errors are occurring. If the spike noise cannot be ignored in the following stage, the test pattern and circuit need to be modified so as to not influence the following stage.

Following is an example of the generation of spike noise and measures that can be taken against it.

Figure 5-40. Example of Data Selector Circuit
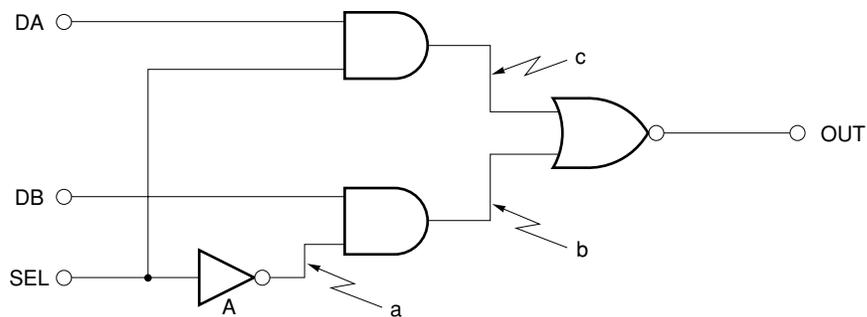
The AND-NOR data selector circuit shown in Figure 5-40 will generate the test pattern shown in Figure 5-41.

Figure 5-41. Example of Test Patterns (Before Improvement)
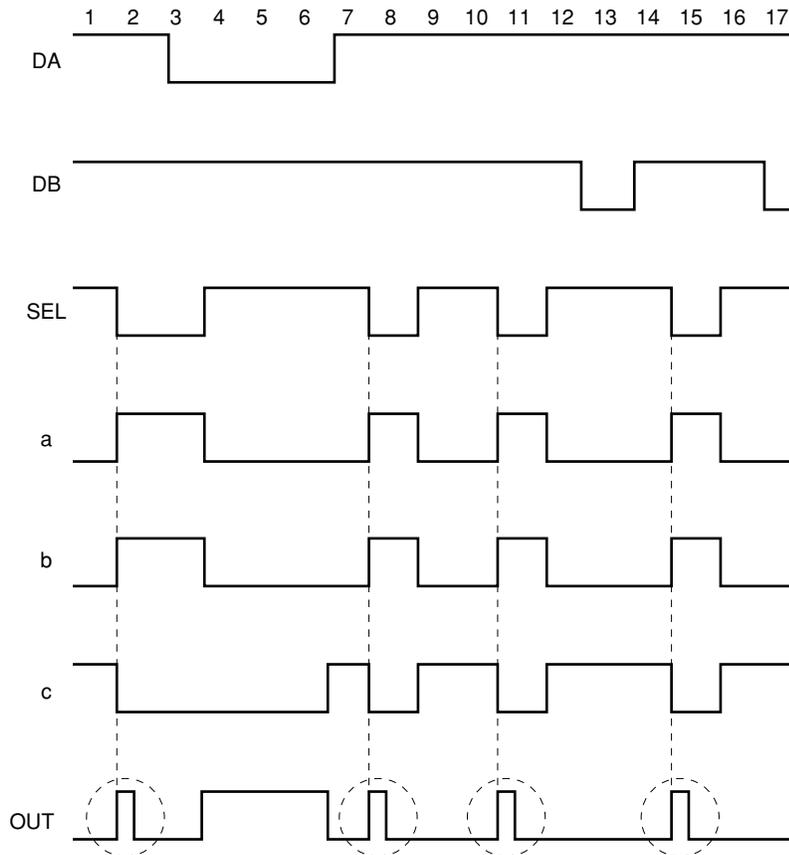
In this case, when both the DA and DB input data signals are in a high-level state, spike noise is generated at the output signal OUT since the SEL (select signal) changes from H to L. The pattern in Figure 5-41 generates spikes at pattern locations 2, 8, 11, and 15.

As is clear from the circuit diagram, when DA and DB are in the high-level state, the state of b and c are determined by the state of SEL. In addition, when SEL changes from H to L, b changes from L to H and c changes from H to L in the same pattern. Moreover, a changes when it goes through inverter A and the delay through A is greater than that of SEL. Because of this, b is delayed more than c for inverter A. Consequently, the state of b and c are simultaneously L and L at 2, 8, 11, and 15 of the test pattern, and L-to-H-to-L spike noise is generated for OUT.

Implement the following two measures if this spike noise is input to the flip-flop clock or the set/reset.

<1> Stop the flip-flop output changing due to spike noise by ensuring that the data is not changed, or by some other method at the spike noise generation timing.

<2> Modify the test pattern.

In the case shown in Figure 5-41, when SEL changes from H to L, make at least one of DA or DB change to L. There is no spike noise at the output OUT if the timing is designed as shown in Figure 5-42.

Figure 5-42. Example of Test Patterns (After Improvement)
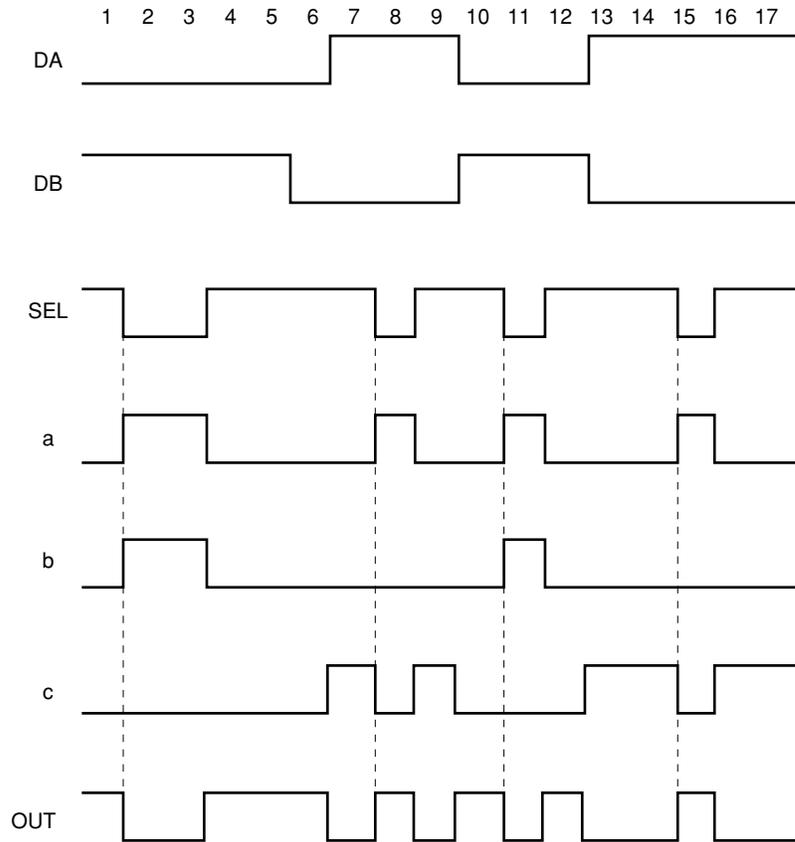
CHAPTER 6 TEST PATTERN GENERATION

When designing with gate arrays, the circuit's expected function and performance are verified through simulation on a computer. To execute the simulation, the user is requested to prepare a circuit diagram and test patterns.

These test patterns are also used for product inspection before shipment. During shipment inspection, the functions of the LSI are verified (test function) and the DC characteristics (such as power supply leakage current, input leakage current, and output current) are tested. Unless adequate consideration is given to the shipment inspection, therefore, the product is not thoroughly tested when shipped. Users are therefore requested to generate test patterns with which fault detection and DC testing can be performed.

During simulation, the conditions under which the LSI is actually used by the user can be realized relatively easily. The LSI tester, which tests the actual LSI, however, cannot completely reproduce the conditions under which the user actually uses the LSI, in many cases. The test patterns should therefore be generated in accordance with the capability of the LSI tester and by observing specified limits.

This chapter describes the points to be noted when generating test patterns.

6.1 Test Pattern Types

The types of test patterns available are shown in Table 6-1.

One DC test pattern is essential, but other test patterns may also be necessary depending on circuit or user requirements.   When the LSI tester is used to perform DC measurement, the measurement is carried out using up to the first 32,000 patterns of the DC test pattern.

Table 6-1. Test Pattern Types

Pattern Name	Purpose	Pattern Generator
DC test pattern	DC measurement, logic verification	User
Function test pattern	Logic verification	User
High-speed function test pattern	Logic verification (real time)	User
Megamacro initialization pattern	Initialization	NEC Electronics (inserted by user)
Megamacro single-unit test setting pattern	Setting megamacro peripheral values	User
Megamacro test pattern	Logic verification (megamacro single unit)	NEC Electronics
Scan test pattern	Fault detection	User or NEC Electronics
RAM test pattern	Logic verification (RAM single unit)	NEC Electronics
Digital PLL initialization pattern	Initialization	User
Boundary scan test pattern	Logic verification (boundary scan circuit)	User

Although the pattern length per pattern is not restricted (except for the high-speed function test), the total pattern length is. For details, refer to **6.2.2 Limitations on test pattern length**.

6.2 Notes from Viewpoint of Product Test (LSI Tester)

6.2.1 I/O pin naming conventions

(1) Maximum number of characters for I/O pins
64 characters MAX.

(2) Characters allowed
Some characters must not be used when specifying a pin name. The characters that can be used are listed in the table below.

Table 6-2. Restrictions on Pin Names

Usable characters	Alphabetic uppercase letters Numeric characters "_" (underscore)
Unusable characters	" / " (slash) and all other special characters other than the underscore Alphabetic lowercase letters

6.2.2 Limitations on test pattern length
The length of a test pattern is limited by the size of the LSI tester's memory.
The minimum and maximum lengths of test patterns (for DC test and for the function test) are listed in Table 6-3.

Table 6-3. Limitations on Number of Test Patterns

Number of Patterns Package[Note 1]	Minimum Number of Test Patterns (Applicable to DC Test Patterns)	Maximum Number of Test Patterns[Note 2]
144 pins or less: with SCAN	150 patterns	128 K patterns
144 pins or less: without SCAN		256 K patterns
145 pins or more		512 K patterns

Notes 1. The number of package pins includes the number of power supply pins (GND, V_{DD}, etc.).
2. The maximum length of test pattern does not need to be considered for the RAM test pattern, scan test pattern created by NEC Electronics, and high-speed function test pattern.
Examine each length of test pattern for the user-created test pattern and megamacro boundary scan, taking the limited pattern length above into consideration.

6.2.3 Number of test patterns

There can be more than one test pattern. The maximum number of patterns is 20, including all interface test patterns such as those for DC test and function test. In this case, the RAM test pattern, scan test pattern created by NEC Electronics, and high-speed function test pattern do not need to be considered.

However, the number of test patterns should be minimized as far as possible in order to increase efficiency. Even if the test pattern is divided for the sake of convenience of design, in principle, submit one test pattern to NEC Electronics (the test patterns can be easily combined by using the wave editor of the pattern utility or OPENCAD).

To divide the test pattern, initialize each pattern (see **6.3.1 Initializing circuit**). If this is not possible, be sure to inform NEC Electronics of the sequence of the test patterns (in writing).

The test pattern must be divided in the following cases.

- If the time conditions (input delay and pulse width) and output judge time (strobe time) of the input signals differ
   For details, see **6.3 Notes on Creating Test Pattern for Function Test**.

6.3 Notes on Creating Test Pattern for Function Test

6.3.1 Initializing circuit

Whether the output state of blocks, such as flip-flops and counters, is at the high level or low level immediately after power application is unknown (see **5.9.1 Flip-flop initial setting**). Consequently, the initial status of sequential circuits such as flip-flops and counters is "x" (undefined) during simulation. To verify operation of the circuit, it is necessary to change the internal function block state from an indeterminate state to a determinate state (circuit initialization).

When designing a circuit, prepare a pattern that can initialize the circuit at the beginning of the test pattern, and at the same time, consider use of a reset pin, so that the circuit can be easily initialized.

When preparing divided test patterns, in principle, initialization is necessary for each pattern (see **Figure 6-4 Test Pattern Example**).

6.3.2 Test cycle (test rate)

The test rate is referred to as the cycle of one test pattern.

Currently, the test cycle limitation at NEC Electronics for a general function test is as follows:

Test cycle: 200 ns

If a higher-speed test cycle than above is desired, perform the high-speed function test. For the high-speed function test pattern, refer to **6.6 High-Speed Function Test (Real-Time Test)**.

6.3.3 Output determination time (strobe time)

The output determination time (strobe time) refers to the time during which the output value of the product is referenced with the expected value on the test pattern. In the current normal function test pattern, this time is always the final time (199.99 ns) of the period, and anything outside of this becomes a high-speed function.

For details of the high-speed function test pattern, see **6.6 High-Speed Function Test (Real-Time Test)**.

6.3.4 Specification of timing phase

For the specification of timing phases currently supported, refer to **Table 6-4** (including the basic timing).

The skew among the pins of the LSI tester (specified as ± 5 ns) must be considered, and the time differential of each phase must be set to 10 ns or greater.

The basic timing phase indicates the NRZ signal when (Δt_D = 0 ns. NRZ signals with an equal delay time (Δt_D) are considered as in-phase and counted as one phase no matter how many input pins there are with the same timing.

Likewise, RZ signals with an equal delay time (Δt_D) and pulse width (Δt_W) are also considered as in phase.

Positive clocks and negative clocks with an equal Δt_D and Δt_W are also counted as one phase. However, NRZ signals and RZ signals with an equal Δt_D are in-phase.

Table 6-4. Timing Phase Number

PKG	Timing Phase Number[Note]
All packages	6

Note   Including basic timing phases.

Table 6-5. Timing Constraints

Signal Type \ Timing Limit	Input Delay (Δt_D)		Input Pulse Width (Δt_W)	
	MIN.	MAX.	MIN.	MAX.
Basic timing	0 ns		—	
NRZ signal	10 ns	$T - 10$ ns	—	
RZ signal (clock mode)	10 ns	$T - \Delta t_W - 10$ ns	145 pins or more: 10 ns 144 pins or less: 15 ns	$T - \Delta t_D - 15$ ns

Remarks 1. NRZ (No Return to Zero) signal: Indicates there is only one change within one test pattern (1 test rate).

2. RZ (Return to Zero) signal: A signal with a change of $0 \rightarrow 1 \rightarrow 0$ or $1 \rightarrow 0 \rightarrow 1$ within one test pattern.

Figure 6-1. Timing Phase
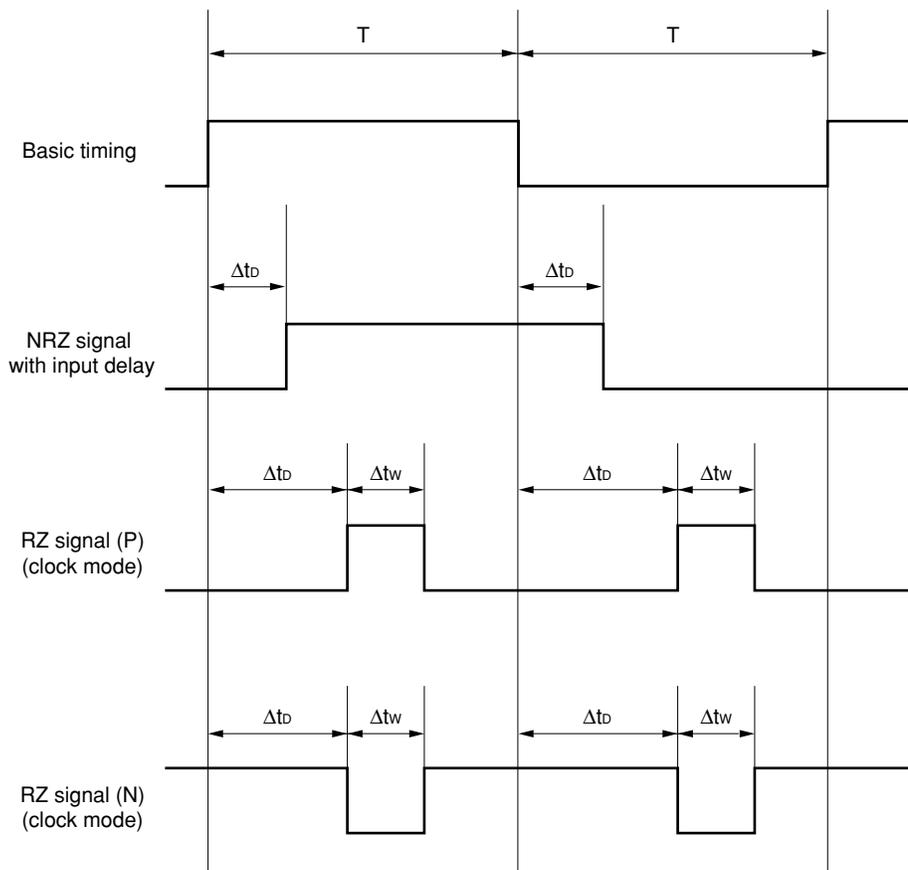
Cautions 1. At least 10 ns must remain between changes of each signal.

  2. RZ signal input to bidirectional pins is prohibited.

Remark   T: Test cycle (test rate)

The clock mode (RZ) signal of the input has two polarities, which determine how it is used.

Table 6-6. Clock Mode

Input Pattern	Definition	Operation	
		Positive Clock (P)	Negative Clock (N)
1 (H)	Clock generation	$0 \rightarrow 1 \rightarrow 0$ (positive clock generation)	$1 \rightarrow 0 \rightarrow 1$ (negative clock generation)
0 (L)	Clock stop	0 hold	1 hold

6.3.5 Skew

When two or more input signals are changed at the same time during simulation, no skew occurs between input signals. With an LSI tester that is used to check the quality of products, however, the input signals do not change at exactly the same time because of a skew of several ns that exists between input pins, even if it is specified that the signals change at the same time. Consequently, even if no problem is found during simulation, the product may not pass a quality test because of the skew between pins.

Therefore, take the following measures so that the product will operate normally even if there is an input skew when creating a test pattern.

(1) Do not change a flip-flop's data input and clock at the same time
$\rightarrow$ Instead, alternate by one pattern.

(2) Use a clock signal (RZ signal) and an input delay signal (NRZ signal).
$\rightarrow$ Stagger the input.
If it is assumed that the input skew is 10 ns and the setup time between data and clocks is 5 ns, then a 15 ns delay time is needed, as shown below.

LSI tester input skew	+	Setup time	=	Input delay time specified to clock signal
10 ns	+	5 ns	=	15 ns

6.3.6 Notes on switching I/O mode of bidirectional pin

(1) Although the switching of the bidirectional pins' I/O mode is generally carried out at the basic timing, for the DC test pattern and function test pattern, it is possible to shift the I/O switch timing of <u>a single set</u>. This is known as the I/O modulation function (refer to **6.3.7 I/O modulation function** for details).
Note, however, that the bidirectional pin I/O mode cannot be switched using the RZ signal (because the mode will change twice within 1 rate: input $\rightarrow$ output $\rightarrow$ input. See **Figure 6-2**.)

Figure 6-2. Example of Incorrect Bidirectional Pin Switch Timing
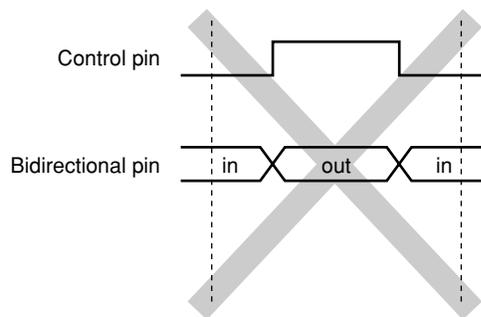
(2) In cases when an input delay has been added to the control pin in the bidirectional pin I/O mode, or when the I/O mode switch timing is different to the basic timing because there is a delay until the internal circuit is enabled, ensure that the input and output values match when switching the I/O mode. This processing prevents a current from flowing when the device's output signal conflicts with the LSI tester's driver (input), and is used to avoid power supply modulation or other such causes of malfunction. If it is not possible to match the input and output values, ensure that the conflict does not exceed 20 ns (see **6.3.8 I/O conflict**). Note that it is prohibited to input the RZ signal (clock waveform) to a bidirectional pin.

Figure 6-3. Contention During Input/Output Switching
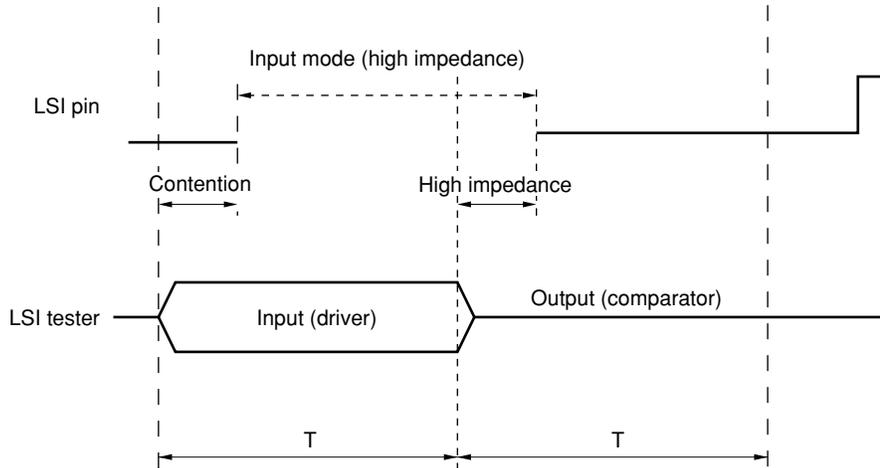
Remark   T: Pattern period

(3) In cases when due to the circuit specifications of PCI bus circuits, etc. the I/O mode switch timing differs from the basic timing, and the bidirectional mode is switched after the pre-switching value is fetched inside the circuit, use the I/O modulation function (refer to **6.3.7 I/O modulation function** for details).
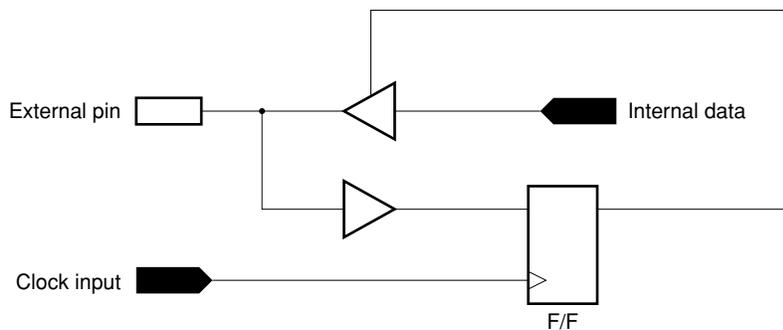
6.3.7 I/O modulation function

Although in the case of the DC test pattern and function test pattern it is possible to shift the I/O switch timing of a single set, the following restrictions apply.
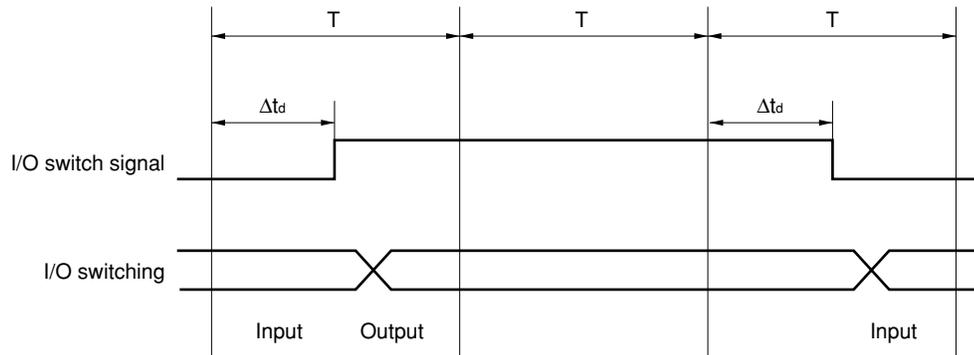
Remark T: Pattern period
Δt_d: Input delay of I/O switch signal

When shifting the I/O switch timing from the basic timing, the I/O switch time on the tester side is set as the I/O modulation.

The following expression must be satisfied, assuming Δt_{rmax} is the slowest time of all the pins and patterns among the bidirectional pin (simulation result) I/O switch times, and Δt_s is the I/O modulation time.

$$\Delta t_s \geq \Delta t_{rmax} + 5 \text{ ns}$$

The reason for this is that in cases when the bidirectional mode is switched after the pre-switching value is fetched inside circuits such as a PCI bus circuit, because it is necessary to hold the external (LSI tester) value until the pin's I/O mode has been switched, the circuit must be driven longer (I/O mode switching delayed longer) than in the simulation result: 5 ns of the skew between the LSI tester pins.
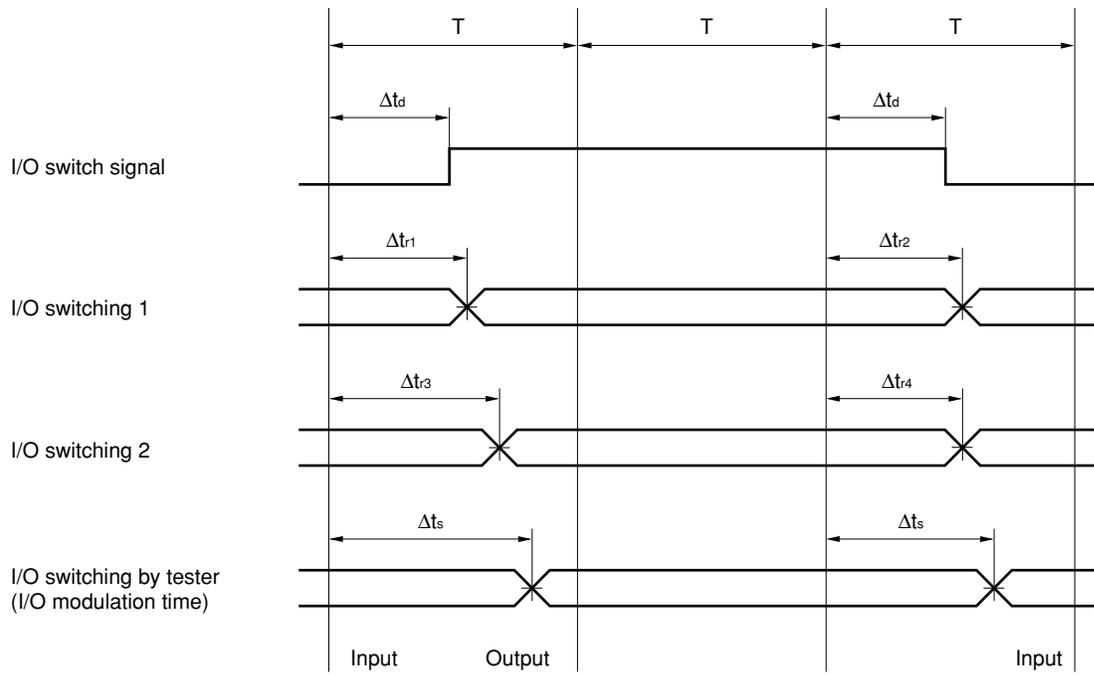
Remark T: Pattern period

Δt_d: Input delay of I/O switch signal

Δt_{r1} to Δt_{r4}: Bidirectional pins' I/O switch times

(Δt_{r3} in the above figure corresponds to Δt_{rmax} in the aforementioned equation.)

Δt_s: I/O modulation (I/O switching on the tester side) time

In addition to satisfying the above conditions, the following restrictions must be observed.

Item	I/O Modulation (Δt_s)		Interval Between I/O Modulation and Other Input Delay (Δt_p)
	MIN.	MAX.	MIN.
Restriction	10 ns	T – 10 ns	10 ns
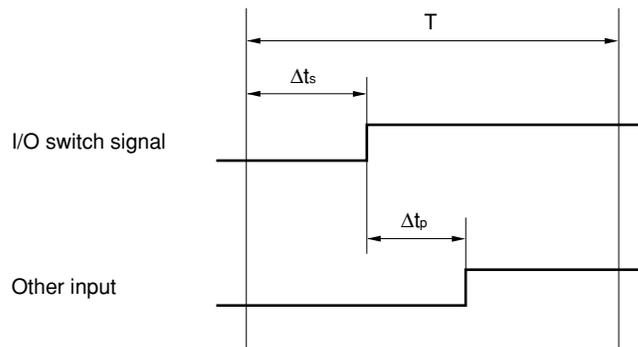
When setting both the input delay (Δt_d) and I/O modulation (Δt_s) for the same pin, ensure that either of the following is satisfied: $\Delta t_s = \Delta t_d$, or $\Delta t_s + 10$ ns $\leq \Delta t_d$.

Note that the I/O conflict time must be kept within 20 ns, even when using the I/O modulation function.

6.3.8 I/O conflict

If it is not possible to match the bidirectional pins' input and output values, the I/O conflict must not exceed 20 ns. The reference for judging I/O conflict is shown below.

Simulation Result	Expected Value	
	Input	Mode Undefined
Output 1	0, X	0, X
Output 0	1, X	1, X
Output X	0, 1, X	0, 1, X, Z

6.3.9 Testing multifunction I/O circuits

(1) Oscillators

Oscillators cannot be actually oscillated and tested with a simulator and LSI tester. Input a dummy signal to the input pin of the oscillator.

Use the inverted signal of the input signal as the expected value of the output of the oscillator.

The oscillator input signal is equivalent to the clock signal. Because a stable test cannot be performed due to conflict if this input signal and external data or set/reset input signals are changed at the same timing, be sure to stagger the timing.

Because the test pattern is not modeled in an oscillating state, the external timing of data or reset signals related to the clock in an oscillating state (oscillator input signals) is not tested.

(2) Open-drain output

The expected output value in the case of output disable must be high impedance (Z).

6.4 Notes on Creating DC Test Patterns

Restrictions for DC test patterns are basically same as those for function test patterns. The test pattern is not only used to test the functions but also used to test DC characteristics during shipment inspection. Therefore, the following points must be noted in creating a test pattern.

<1>   If possible, prepare a dedicated test pattern set for the DC test pattern.

<2>   The length of the DC test pattern should be more than 150 patterns. If the length of the pattern exceeds 32,000, perform the DC test between 1st and 32000th pattern.

<3>   If possible, make input pins change at least two times (except for oscillation stop control pin).

<4>   Output pins must output a high level and a low level at least once each.

<5>   The output pin of a three-state output buffer must output a high-impedance state (off state).

<6>   When a bidirectional buffer is used, make sure that the input state and output state are switched at least once.

<7>   The test cycle must be sufficiently longer than the delay time (operating time) of the circuit. The basic cycle is 200 ns. Be sure to set the output determination time (strobe time) towards the end of the cycle (this is so the output is determined after the circuit has entered the stable state).

<8>   If an RZ (Return to Zero) signal is input to an input pin, make sure that the RZ signal is not output as is. The output value of the output pin that outputs the RZ signal is always either one of two values at output determination time, and the other value cannot be tested.

<9>   Bus fighting and bus floating for the internal bus is prohibited.

<10> Initialize the circuit until 50th pattern.

<11> The IDDq test is performed in the DC measurement pattern. The measurement pattern is selected automatically. If possible, operate the internal circuit to improve coverage.

<12> Be sure to set to oscillation mode when an oscillator block is mounted.

<13> In the test pattern in oscillation mode, input the same pattern as normal clock pattern for the input pin (XT1) and expected value of output pin (XT2) should be its inverse.

The RZ signal has changes of "$0 \rightarrow 1 \rightarrow 0$" and "$1 \rightarrow 0 \rightarrow 1$" in one test pattern (1 test rate). By contrast, the NRZ (No Return to Zero) signal has only one change in one test pattern (1 test rate).

6.5 Test Pattern for On-Chip RAM

NEC Electronics supplies a test pattern for RAM, and the user does not have to consider RAM tests. However, the following limitations are applied if NEC Electronics supplies the test pattern for RAM. (For details, see **7.4 Memory**).

(1) Additional RAM pins (TIN, TEB, and TOUT) are needed in order to test the RAM.
(2) If there are multiple RAMs or connections between RAM and logic circuits, the connection to each RAM must be tested by the user test patterns.
(3) Be sure to set the TEB pin to user mode (high) for each of the user test patterns.

Figure 6-4. Test Pattern Example

DC test pattern · Function test pattern · High-speed function test pattern

Initialization pattern

Initialization pattern

Initialization pattern

RAM test circuit connection verification pattern
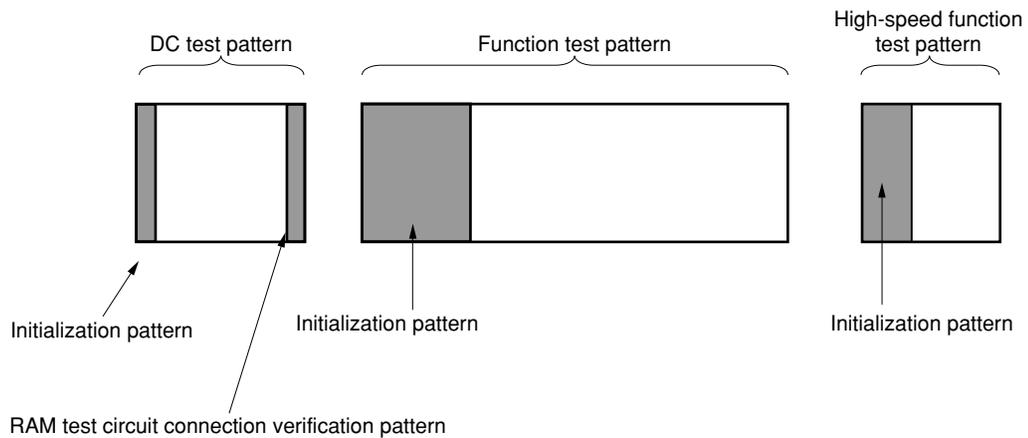
6.6 High-Speed Function Test (Real-Time Test)

Checking the designed circuit through simulation at the actual operating frequency is a very effective technique for checking the actual operation of the LSI. In this way, problems concerning the timing of the circuit during actual operation that may have been overlooked by the designer can be found.

During the shipment inspection of the product, the actual operating conditions cannot be always simulated because the performance of the LSI tester may be limited. The high-speed function test, however, can simulate conditions very close to the actual operating conditions.

This section describes the following limits of the high-speed function test. Create a test pattern observing these limits.

6.6.1 Limitation of the test pattern length

The length per test pattern must consist of 32,000 patterns MAX.

6.6.2 Test cycle (test rate)

The test rate is referred to as the cycle of one test pattern.

Currently, the test cycle limitation at NEC Electronics for a general high-speed function test is as follows:

Test cycle: 50 ns MIN.

6.6.3 Output determination time (strobe time)

The output determination time (strobe time) indicates the time required to verify the output value of the product against the expected value on the test pattern. Currently, up to two strobe times can be assigned per test pattern. However, only one strobe time can be assigned per pin. If three or more strobe times or several strobe times per pin must be established, each one must have its own test pattern.

Setting strobe time within 15 ns the beginning of the basic timing or with 10 ns before the end of the timing is prohibited.

Figure 6-5. Strobe Time

$$15 \text{ ns} \leq \text{strobe time} \leq T - 10 \text{ ns}$$
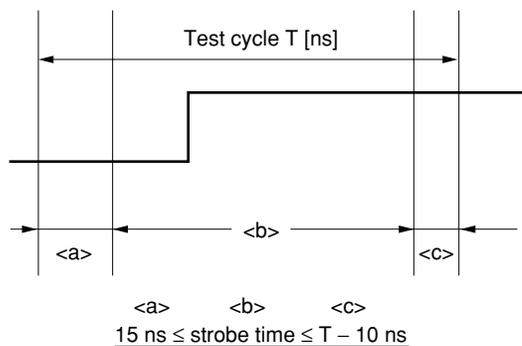
Caution   Open-drain, GTL, and HSTL buffers are not real-time test targets.

6.6.4 Notes on high-speed function testing

To conduct the high-speed function test, execute MIN/MAX simulations under the following conditions. The results of both the simulations must match.

Confirm these simulations before and after placement and routing.

Note that I/O modulation cannot be used.

> Ask NEC Electronics for the delay data (path delay file) after placement and routing.
> At this time, the load capacitance data file (DIF FILE) for the output pins used for simulation is necessary.
> Submit this file to NEC Electronics.
> For the format of the DIF file, see **APPENDIX C ALBATROSS AND DIF FILE FORMATS**.

The purpose of these simulations is to detect the possibility of occurrence of problems when inspection is performed with an LSI tester. Therefore, conditions different from the actual operating conditions must sometimes be set.

Specify settings of the time condition for input signals, the output determination time (strobe time), and the test cycle (test rate) for each phase in "High-speed function test guidelines".

    <1> MAX. simulation conditions

        Test cycle (T):   User-specified value

        Load capacitance (C_L):   Bidirectional pin: 125 pF, MAX. value of load capacitance with LSI tester

                                       Output pin: 90 pF

        Strobe time: Set to specified value –5 ns with skew of strobe time assumed to be –5 ns

    <2> MIN. simulation conditions

        Test cycle (T):   User-specified value

        Load capacitance (C_L):   50 pF, MIN. value of load capacitance with LSI tester

        Strobe time: Set to specified value +5 ns with skew of strobe time assumed to be +5 ns

During real-time simulation, the simulation result may not converge in one pattern and the output may change at the next pattern, as shown in Figure 6-6.

If the simulation result is different between the MAX simulation and MIN simulation, take the following measures:

- Change the expected output value of the test pattern, which differs between the two test patterns, to "X" (Don't care).
  Synthesize the test patterns (see **Figure 6-6**).
- Alternatively, include only the timing actually requiring inspection as the system, as the expected values.

Figure 6-6. Real-Time Simulation Results
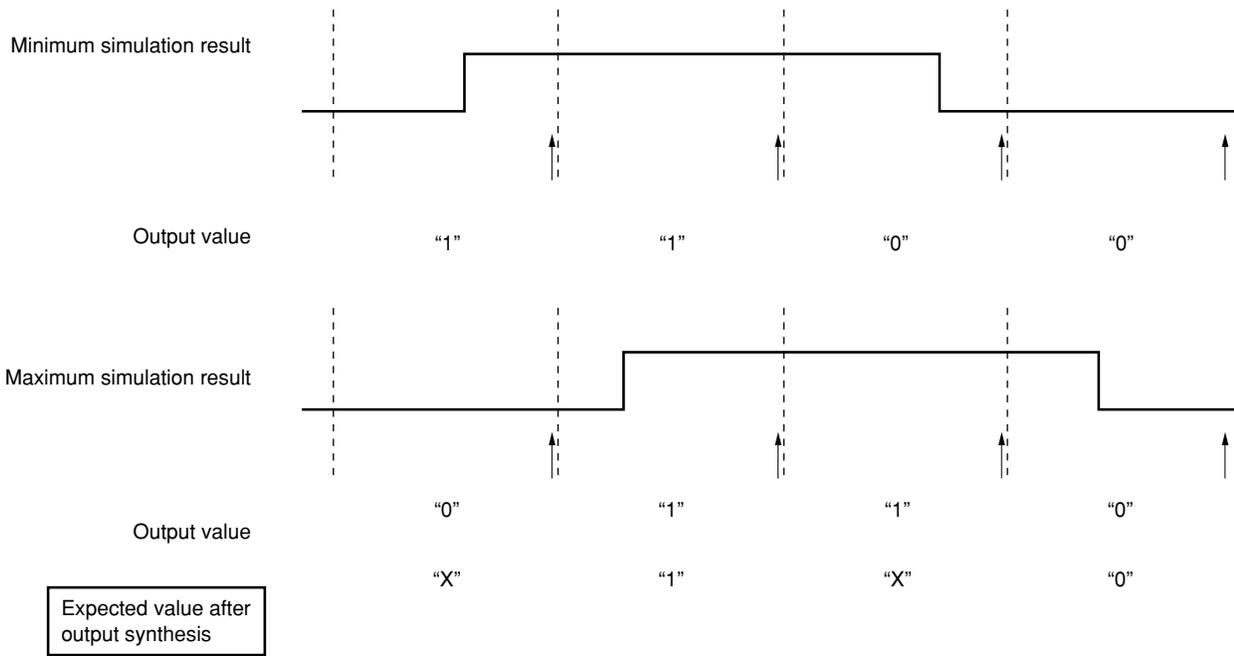
6.7 Testability (Fault Coverage)

6.7.1 Consideration of testability (fault coverage)

Fault simulation is a way to verify the testability (fault coverage) when an ASIC is developed. In other words, it diagnoses the validity of a test pattern created to test the functions of logic circuits and detects the faults that are not detected by that test pattern.

During the ASIC manufacturing process, various faults may arise. These faults are broadly classified into dynamic faults and static faults.

Dynamic faults create long delay paths, spikes, and timing violations. Such faults are caused by the operating environment or design errors.

Static faults are represented by physical damage to the chip such as routing shorts and opens. In most of the cases, the production process is responsible for these faults. Logic simulation verifies the functions and timing of a created circuit. However, it does not verify the test efficiency of a test pattern for detecting static faults in the chip actually produced. Fault simulation defines static faults in the circuit and verifies whether faults have been accurately detected by the input test pattern from the output pins of the ASIC developed.

The purpose of fault simulation is to inspect how efficiently test patterns can detect a fault at the boundary of the function blocks of the created circuit. The test efficiency of these test patterns is called testability (fault coverage) and is expressed as a percentage to indicate how well the test patterns can detect the faults in the circuit.

$$\text{Testability (fault coverage)} = \frac{\text{Number of faults detectable by given test input pattern}}{\text{Total number of faults in circuit tested}} \times 100 \ (\%)$$

If the testability (fault coverage) is low, the LSI may not be tested well and defective products may be shipped.

NEC Electronics recommends that the fault coverage, as far as possible, be made at least 90% in order to raise the quality of the product.

To improve testability (fault coverage), it is recommended to provide a test circuit at the circuit design stage and to employ the scan path test method.

6.7.2 Principle of fault simulation

Fault simulation generally operates by the same algorithm as the logic simulation that tests the logical functions. In the execution of fault simulation, however, the faults can be set in the circuit. Figure 6-7 shows examples of fault simulation.

Figure 6-7. Concept of Fault Simulation (1/2)

(a) Circuit example

(b) Test patterns
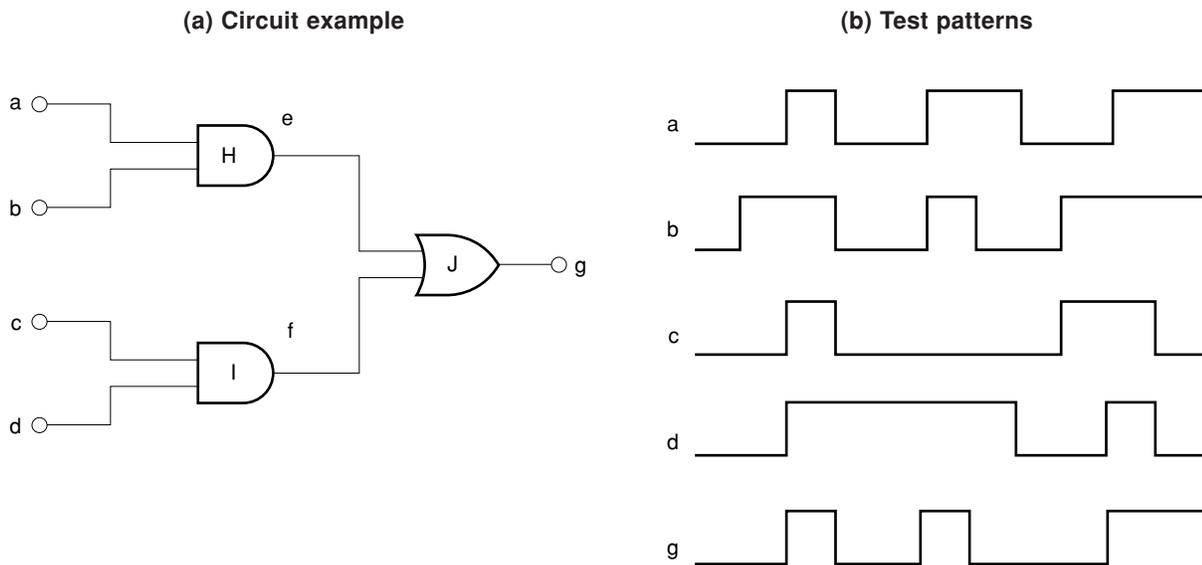
It is assumed that this circuit has a fault and that the output of the 2-input AND gate H is always at the low level. If an input signal the same as Figure 6-7 (c) is input in this case, it can be seen that the result of output "g" will be different (see **Figure 6-7 (c)** and **(d)**). Accordingly, this fault can be detected by these test patterns.

(c) Observation of point e and point f

(d) Fault result of AND H
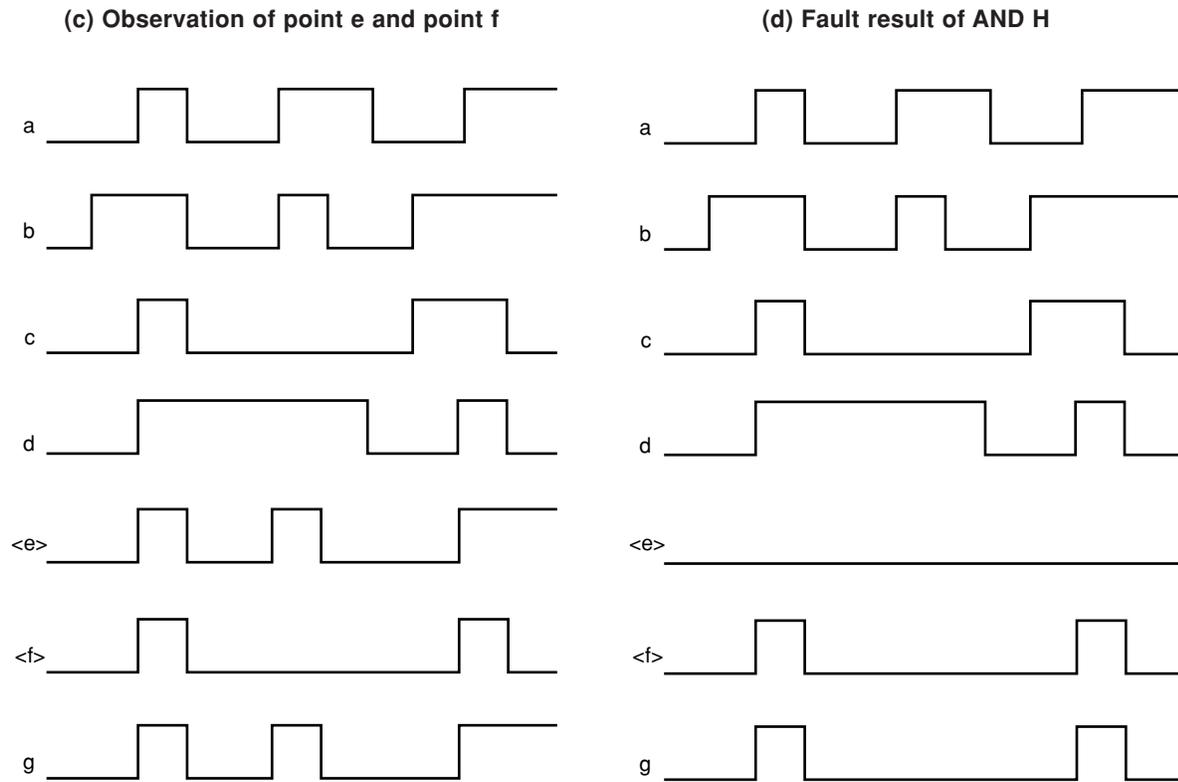
There may also be cases of a fault in which the output of the 2-input AND gate I is always at the low level.

As shown in Figure 6-7 (e), this input signal (test pattern) becomes the same as the test pattern in Figure 6-7 (c), which shows that they are ineffective in detecting this fault.

Figure 6-7. Concept of Fault Simulation (2/2)

(e) Fault result of AND I
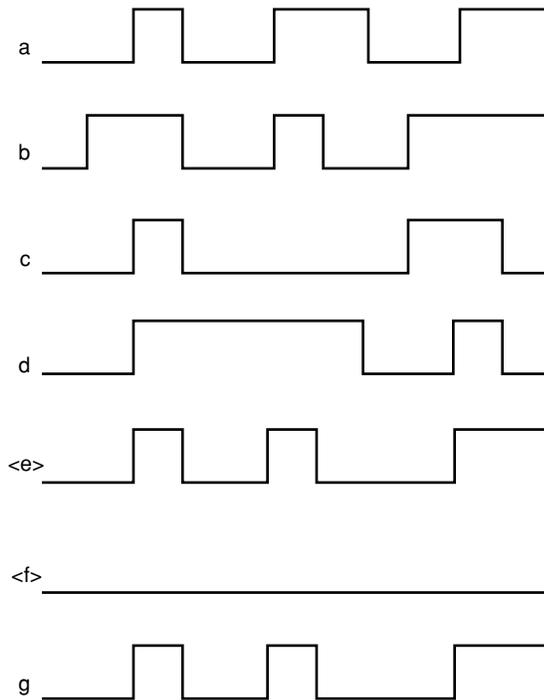
Fault simulation defines these types of faults one by one with respect to the internal circuit and checks whether the defined faults can be detected at the output pin by performing simulation.

The types of faults that can generally be defined by fault simulation are called single degenerate faults.

The following two types of single degenerate faults are defined in circuits:

 <1> Stuck-at-1: Fault where a given part is fixed at the high level ("1")

 <2> Stuck-at-0: Fault where a given part is fixed at the low level ("0")

6.8 Consideration of System Simulation

System simulation is a method for checking the functions of a gate array under development by simulating the operations of the gate array in an environment close to the actual operating environment, such as on a board or in equipment.

After checking the functions of the gate array in equipment, the test pattern of the gate array alone is extracted by monitoring the signals at the input/output pins of the gate array.

This test pattern can be used as a test pattern for LSI testing. However, be sure to confirm that there is no problem (that the points to be noted in creating the test pattern are satisfied) by executing a simulation of only the gate array.

Figure 6-8. Creating Test Patterns by System Simulation
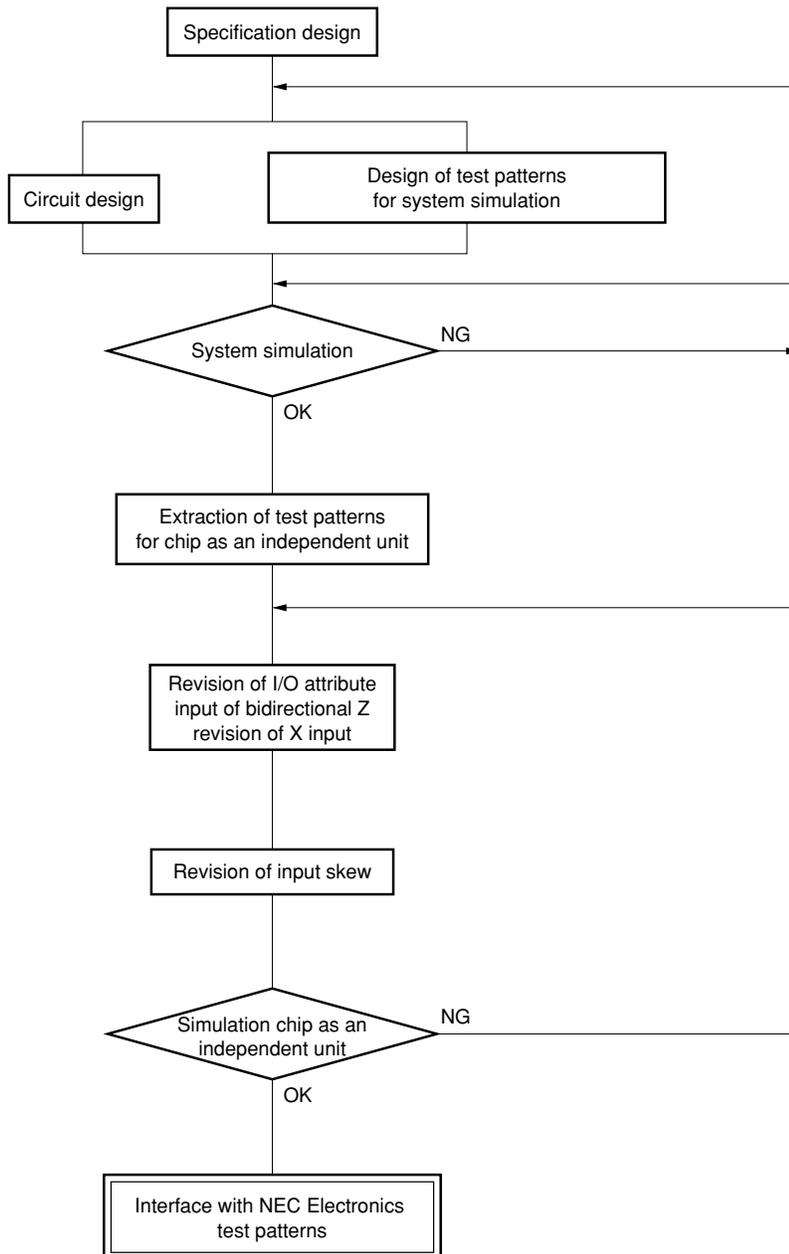
CHAPTER 7 MULTIFUNCTION BLOCKS

The CMOS-N5 Series offers the following multifunction blocks, in addition to the normal function blocks. This chapter explains the functions and usage of each multifunction block.

- Buffer with fail-safe function
- Buffer with on-chip pull-up/pull-down resistors
- Oscillator
- Memory block
- Megamacros

7.1 Buffer with Fail-Safe Function

Because input voltage higher than V_{DD} cannot be applied to a conventional gate array, no I/O voltage can be applied when the supply voltage of the gate array is turned off. A buffer with a fail-safe function can accept voltage even if the supply voltage to the gate array is off.

If a high-level signal is input to the normal input buffer while the power supply to the gate array is off, voltage is applied to the power line via a protection diode (see **Figure 7-1**). Also, if a high-level signal is input to N-ch open drain pins while the power supply to the gate array is off, voltage is applied to the power line via a protection diode. The buffer with a fail-safe function prevents voltage being applied to the power line when the supply voltage to the gate array is off, even if a high-level signal is input. It can therefore be used for hot insertion and removal as long as the specified static voltage condition is satisfied.

Figure 7-1. Equivalent Circuit Diagram for Buffer with Fail-Safe Function

(a) Conventional input buffer

(b) Input buffer with fail-safe function

(c) Conventional N-ch open-drain buffer

(d) N-ch open drain with fail-safe function
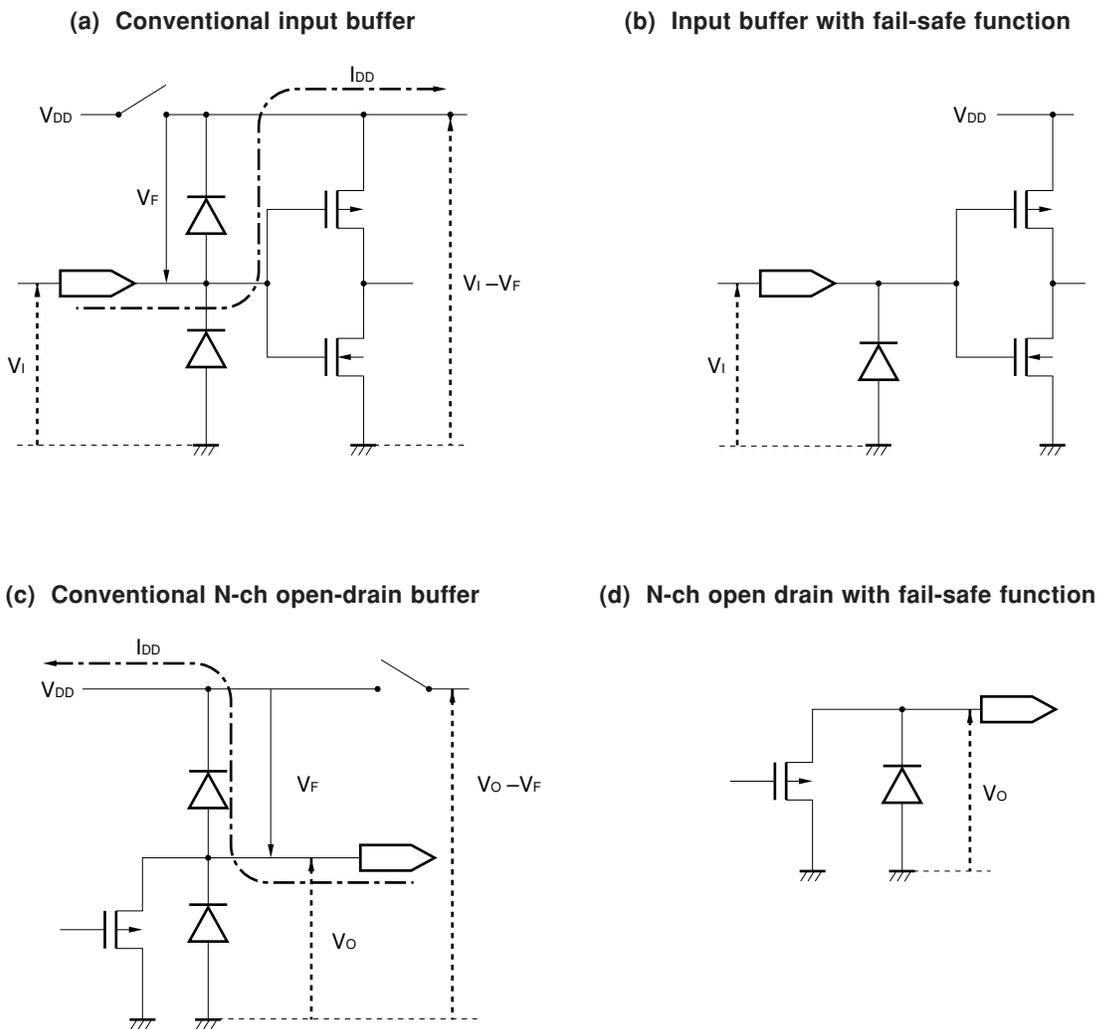
7.2 Input/Output/Bidirectional Buffers with On-Chip Pull-Up/Pull-Down Resistors

The CMOS-N5 Series has input buffers, Schmitt input buffers, 3-state output buffers, N-ch open-drain output buffers, bidirectional buffers, Schmitt input bidirectional buffers, and I/O blocks with on-chip pull-up/pull-down resistors. By using these, a more compact system can be created.

For the name of each block, contact NEC Electronics.

Pull-up resistor
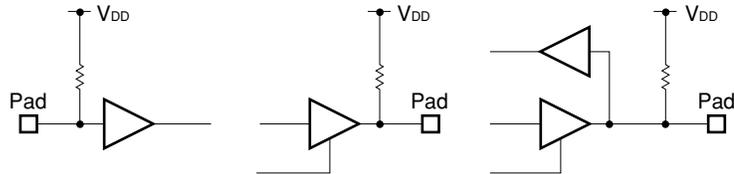
Pull-down resistor
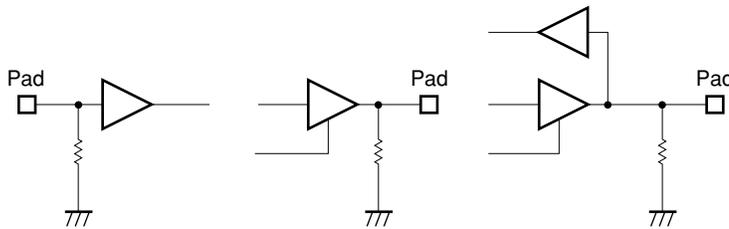
During simulation, undefined (X) or high-impedance (Z) values cannot be input to the input pins of the input buffers with on-chip pull-up/pull-down resistors and bidirectional buffers.

The expected output value must be set to high impedance (Z) or don't care (X) when the output pins of 3-state output buffers and bidirectional buffers with on-chip pull-up/pull-down resistors are not active.

7.3 Oscillator

7.3.1 Configuration of oscillator

Three types of dedicated oscillator blocks are provided for configuring an oscillator: one using external feedback resistors, one using internal feedback resistors, and one that includes an oscillation stop function. An oscillator can be configured using any of these blocks simply by connecting a resonator, capacitor, and limiting resistor to the external pins. Note that the maximum number of dedicated oscillator blocks that can be used is two (three or more blocks are not supportable). When two blocks are used, be sure to place the blocks at opposite polarity to prevent mutual interference, and design so that each circuit operates on a separate clock. If it is necessary to use more than one block, contact NEC Electronics.

In addition, do not use the clock generated by the oscillator on the both rising and falling edges.

The recommended oscillation frequency range and the combination of blocks for oscillator configuration are shown in Table 7-1.

For the configuration of an oscillator block whose placement is restricted, see the tables concerning pins that can be used for oscillators in **CMOS Gate Array, Embedded Array Package Design Manual (A16400E)**. When using an oscillator block that includes a stop function, be sure to control stopping the oscillator from an external source. Note that although there is no restriction on the placement of the stop control pin, it should be placed as close as possible to the oscillator block.

Table 7-1. Recommended Oscillation Frequency Range and Configuration

Feedback Resistor		Stop Function	Configuration		Frequency	Placement Restrictions
			Input	Output		
External	1 MΩ	No	OSI4	OSO9SW	MHz band	No
Internal		No	OSI1	OSO1SW	MHz band	Yes
		Yes	OSI2	OSO7SW		

Remark A new type (with "SW" at the block name end) and an old type (without "SW" at the block name end) of dedicated oscillator blocks are provided.

The following aspects of the old type have been improved in the new type of the dedicated oscillator block.
- Connection between oscillator circuit output and CTS is possible
- Improved compatibility with crystal resonators

Consult NEC Electronics when using an old type of the dedicated oscillator block.

Figure 7-2. Example of Oscillator Configuration
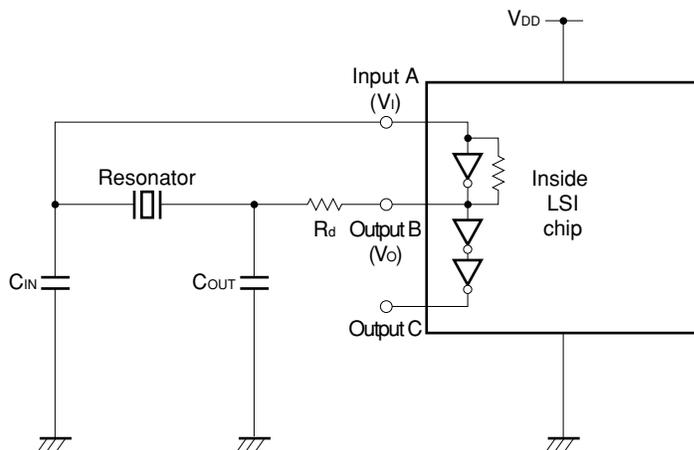
Remark Evaluation using an evaluation sample (ES or CS) is required to determine capacitors C_{IN} and C_{OUT}, limiting resistor R_d, and current consumption.

7.3.2 Description of oscillator

Describe as follows when using an oscillator.

Figure 7-3. Oscillator Configuration (1/2)

(a) OSI1 + OSO1SW
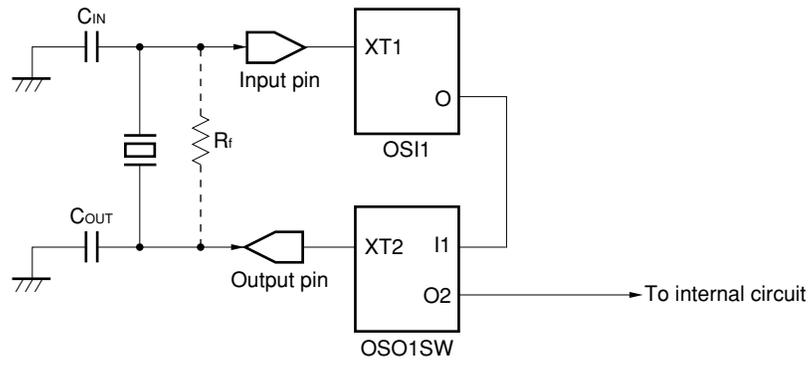
(b) OSI4 + OSO9SW
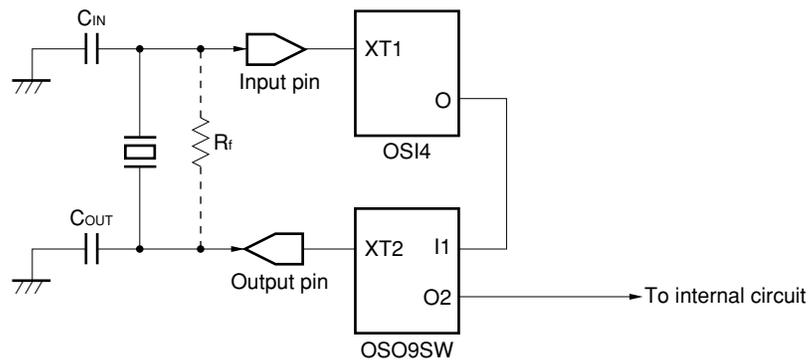
Remark When using OSO9SW, an external feedback resistor with a value of 1 MΩ, R_f, is required.

Figure 7-3. Oscillator Configuration (2/2)

(c) OSI2 + OSO7SW
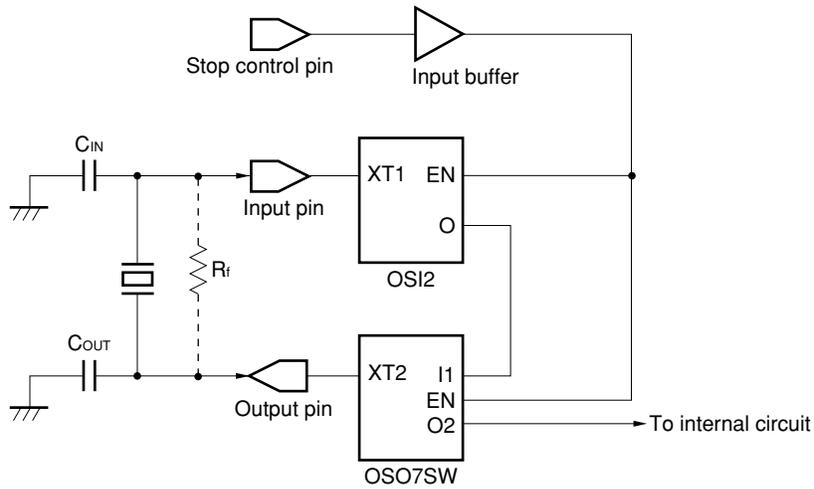
Caution **The input pin (XT1) must be set to high level when oscillation is stopped.**

Remark The output of O2 is low level when oscillation is stopped. The equivalent circuits and truth tables of OSI2 and OSO7SW are shown below.

OSI2 Equivalent Circuit

EN = H → S₁: close
EN = L → S₁: open
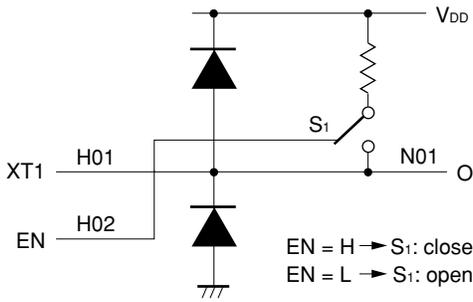
OSI2 Truth Table

XT1	EN	O	
0	0	0	
1	0	1	
1	1	1	
0	1	X	← Use prohibited

OSO7SW Equivalent Circuit
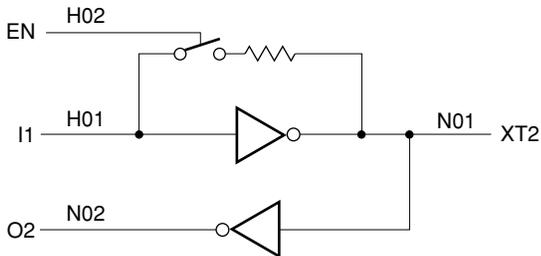
OSO7SW Truth Table

I1	EN	XT2	O2	
0	0	1	1	
1	0	0	0	
1	1	0	0	
0	1	X	X	← Use prohibited

Describe the test pattern of an oscillator as follows.

- Use the inverse of the pattern transmitted to the internal circuit as the input pattern of the input pin (XT1) of OSI1, OSI2, and OSI4.
- Use the same pattern that was transmitted to the internal circuit as the output pattern of the output pin (XT2) of OSO1SW, OSO7SW, and OSO9SW.
- Always input 0 to the stop control pin of OSO7SW in the DC test pattern.

The pattern transmitted to the internal circuit and the pattern output to the output pin (XT2) of OSO1SW, OSO7SW, and OSO9SW is the inverted input pattern.

7.3.3 Using oscillator (resonator) and CTS together

When using an oscillator (resonator) and CTS together, the CTS buffer must not be in an unstable state before oscillation starts, so implement a function that fixes the output value of the CTS buffer by inserting a gate circuit in front of the CTS buffer and connecting the reset pin of the F/F, etc., to that circuit.

Figure 7-4 shows an example of the recommended circuit configuration.

Figure 7-4. Example of Recommended Circuit Configuration
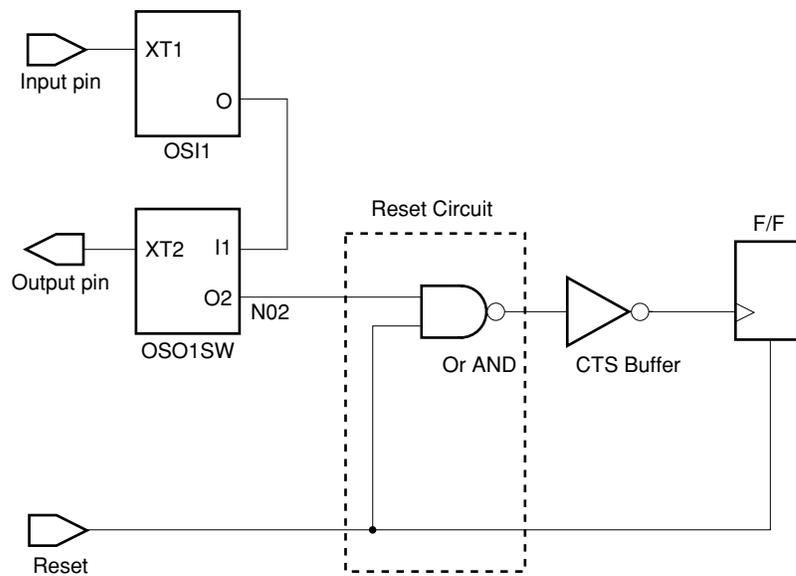
Remarks 1. The target oscillator blocks of this example of the recommended circuit configuration are OSO1SW, OSO7SW, and OSO9SW.
2. Add a CTS reset input circuit (circuit in the dotted lines) between the oscillator output and the CTS buffer and ensure that the CTS output value is fixed when a reset occurs.

7.3.4 Notes on configuring an oscillator

Because the CMOS-N5 gate array has an oscillation dedicated block, it can be used to configure an oscillator by connecting a resonator and external constants outside the package. Although an oscillator can be easily configured, certain differences from logic circuits must be noted because an oscillator is an analog circuit that operates at a high frequency. In order for the oscillator to operate stably, it is necessary to optimize the external constants (input capacitor, output capacitor, and limiting resistor). In addition, because the oscillator is an analog circuit, the following points must also be noted.

<1> Place V_{DD} and GND as follows around the oscillator pins (oscillator).

V_{DD}	GND	OSOxSW block pin	OSIx block pin	V_{DD}	GND

Remarks 1. Do not include the OSOxSW (oscillator) block pin as a target of the simultaneous operation review.
2. V_{DD} and GND surrounding the oscillator pins can be used in the simultaneous operation review.

<2> Place the pins that may cause malfunction due to noise such as clock pins and reset pins as far as possible from the oscillator pins.
<3> Output buffers are a source of noise, and so should be placed as far as possible from the oscillator pins (oscillator).
<4> The following points must be noted regarding the printed circuit board.
  • Place the input and output pins, and the resonator and external constants of the oscillator as close together as possible, and keep the length of the wiring between them as short as possible.
  • Keep the length of the wiring between the GND of the capacitors and of the gate array as short as possible. Use as thick a wiring line as possible.
  • Keep the leads of the resonator and capacitors as short as possible. Secure the resonator and capacitors onto the printed circuit board to minimize the effects of mechanical vibration.
  • Enclose the external constants in a GND pattern as far as possible.

Figure 7-5. Example of GND Pattern on Board
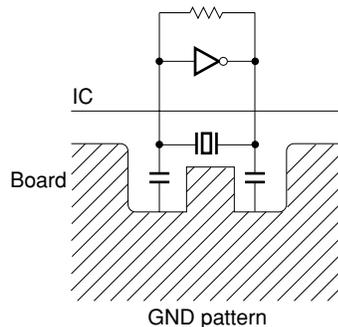
<5> To input the clock generated by the external oscillator from the input pins (OSI1, OSI2) of the oscillation block, connect it to the XIN (OSI1, OSI2) side and leave the XOUT (OSO1SW) side open. Since the oscillator is logically an inverter, a signal consisting of the inverted signal is input to the internal circuit.

The following points must be noted during evaluation to determine the external constants.
- It is recommended to attach an overtone circuit (LC). Figure 7-6 shows circuit examples.
- Evaluate the oscillator considering variations in the oscillation start time and voltage (etc.).
- Use the printed circuit board that is to be actually used (because the oscillation operation range may fluctuate due to the difference in the dielectric constant of the board).
- Check the external constants using a developed CMOS-N5 gate array (ES or CS) and the resonator to be actually used.

Figure 7-6. Example of Overtone Circuits
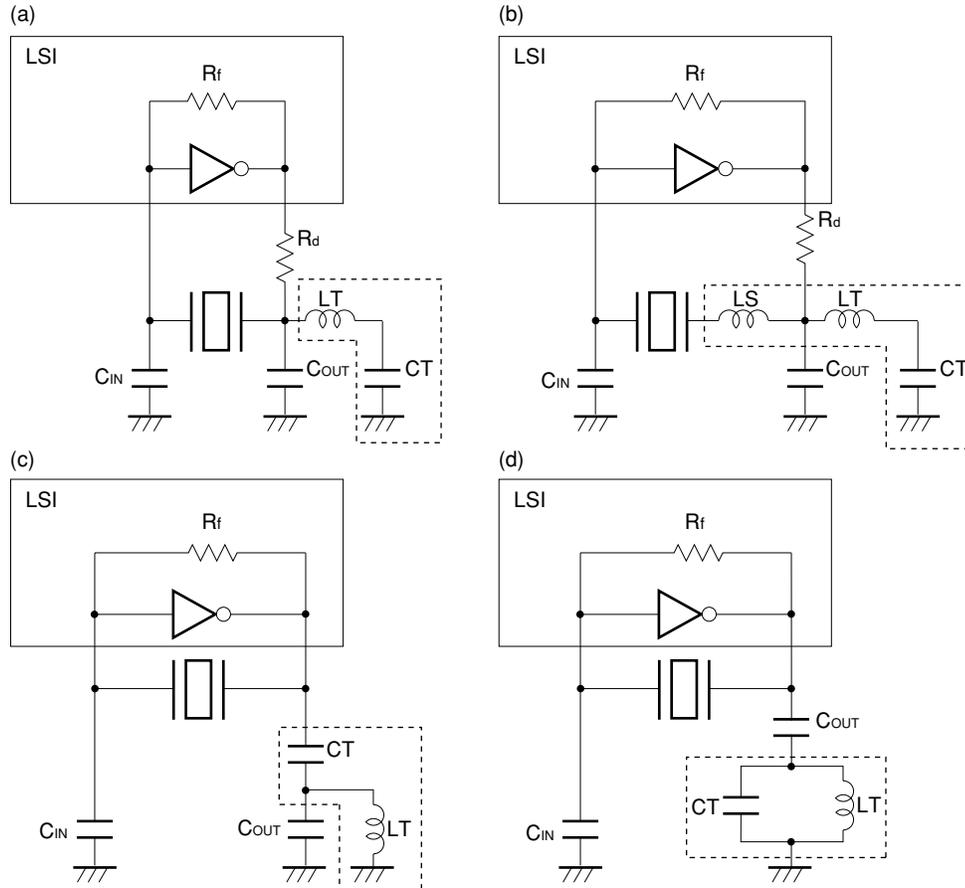
Remark The section within the broken lines is the overtone circuit.

7.3.5 Constants of external circuit

An evaluation of the matching with the resonator is required to generate a clock signal. Table 7-2 shows an example of the criteria for this evaluation. Determine the parameters to be measured through consultation with the resonator manufacturer.

Table 7-2. Example of Criteria

Items to Be Measured	Determination Criteria
<1> Oscillation frequency	Frequency must be within accuracy of resonator
<2> Oscillation start voltage (V_s)	2.0 V ≤ V_s ≤ 2.5 V
<3> Oscillation hold voltage (V_h)	V_h ≤ V_s
<4> Operation on power application	Check oscillation by repeatedly turning power on and off
<5> Current consumption	As low as possible
<6> Peak value of oscillated waveform	3.2 V ≤ V_{IH}, V_{OH} ≤ V_{DD} 0 V ≤ V_{IL}, V_{OL} ≤ 1.3 V
<7> Duty factor	50% ±10%

Note that oscillation is evaluated with an ES or CS model. However, because all the gate array, resonator, and external constants are subject to variations due to production and operating conditions, take these variations into consideration during evaluation.

When evaluating parameters <4> through <7> above, fluctuations in the power supply and temperature of the gate array must also be taken into consideration. Measure these parameters under the following MIN., TYP., and MAX. conditions.

[Example] When fluctuations in power supply and temperature are taken into consideration:

T_A = −40 to +85°C

V_{DD} = 5 V ±10%

Measure these parameters under the following MIN., TYP., and MAX. conditions.

	MIN.	TYP.	MAX.
T_A (°C)	−40	25	+85
V_{DD} (V)	5.5	5.0	4.5

Remark The values in this table indicate the conditions of the MIN., TYP., and MAX. values of the propagation delay time (t_{PD}) of the gate array, and do not refer to the MIN., TYP., and MAX. values of the oscillation frequency of the resonator.

Table 7-3 shows the resonators externally connected to OSO7SW (OSO1SW) or OSO9SW and the recommended external constants, and Figure 7-7 shows the circuit configuration. This data was evaluated in cooperation with each resonator manufacturer.

Caution **If the frequency exceeds 40 MHz when using a resonator, be sure to contact NEC Electronics beforehand.**

Table 7-3. List of Resonator Evaluations (1/2)

(a) Evaluation data of ceramic resonators made by Murata Manufacturing Co., Ltd.

Power Supply Voltage	Oscillator Block	Frequency (MHz)	Product Name	Capacitor	C_{IN} (pF)	C_{OUT} (pF)	limiting resistor R_d (Ω)	Circuit Configuration **Note**
3.0 V ± 0.3 V	OSO1SW	2	CSTCC2M00G56-R0	Internal	–	–	3.3 K	A
3.0 V ± 0.3 V	OSO7SW	4	CSTCR4M00G55-R0		–	–	1.5 K	
		8	CSTCE8M00G55-R0		–	–	680	
		16	CSTCE16M0V53-R0		–	–	330	
		20	CSTCE20M0V53-R0		–	–	220	
		32	CSTCG32M0V53-R0 (Small type)		–	–	150	
	OSO9SW	2	CSTCC2M00G56-R0		–	–	2.2 K	B
		4	CSTCR4M00G55-R0		–	–	1.0 K	
		8	CSTCE8M00G55-R0		–	–	330	
		16	CSTCE16M0V53-R0		–	–	150	
		20	CSTCE20M0V53-R0		–	–	100	
		32	CSTCG32M0V53-R0 (Small type)		–	–	100	
5.0 V ± 0.5 V	OSO1SW	2	CSTCC2M00G56-R0	Internal	–	–	3.3 K	A
	OSO7SW	4	CSTCR4M00G55-R0		–	–	1.5 K	
		8	CSTCE8M00G55-R0		–	–	680	
		16	CSTCE16M0V53-R0		–	–	330	
		20	CSTCE20M0V53-R0		–	–	220	
		32	CSTCW32M0X51-R0		–	–	22	
		32	CSTCG32M0V53-R0 (Small type)		–	–	150	
		40	CSTCW40M0X51-R0		–	–	22	
	OSO9SW	2	CSTCC2M00G56-R0		–	–	2.2 K	B
		4	CSTCR4M00G55-R0		–	–	1.0 K	
		8	CSTCE8M00G55-R0		–	–	330	
		16	CSTCE16M0V53-R0		–	–	150	
		20	CSTCE20M0V53-R0		–	–	100	
		32	CSTCW32M0X51-R0		–	–	22	
		32	CSTCG32M0V53-R0 (Small type)		–	–	100	
		40	CSTCW40M0X51-R0		–	–	22	

Note   The figures in this column correspond to the figures on **Figure 7-7 Oscillator Configuration Diagram**.

Remark   External feedback resistor of OSO9SW: 1 MΩ

Table 7-3. List of Resonator Evaluations (2/2)

(b) Evaluation data of crystal resonators made by Daishinku Corporation

Power Supply Voltage	Oscillator Block	Frequency (MHz)	Product Name	Capacitor	C_{IN} (pF)	C_{OUT} (pF)	limiting resistor R_d (Ω)	Circuit Configuration **Note**
3.3 V ± 0.3 5.0 V ± 0.5	OSO1SW	12	DSX321G	External	8	8	4.7 K	C
	OSO7SW				8	8	4.7 K	
	OSO9SW				8	8	4.7 K	D
	OSO1SW	26	DSX321G		5	5	1.0 K	C
	OSO7SW				5	5	1.0 K	
	OSO9SW				5	5	1.0 K	D
	OSO1SW	32	DSX321G		3	3	1.0 K	C
	OSO7SW				3	3	1.0 K	
	OSO9SW				3	3	1.0 K	D

Notes The figures in this column correspond to the figures on **Figure 7-7 Oscillator Configuration Diagram**.

Remark   External feedback resistor of OSO9SW: 1 MΩ

The circuit configuration is shown in Figure 7-7. In addition, it is recommended to reduce the capacitance of the system board (reduce the influence on C1 (C_{IN}) and C2 (C_{OUT}) as much as possible.

Figure 7-7. Oscillator Configuration Diagram
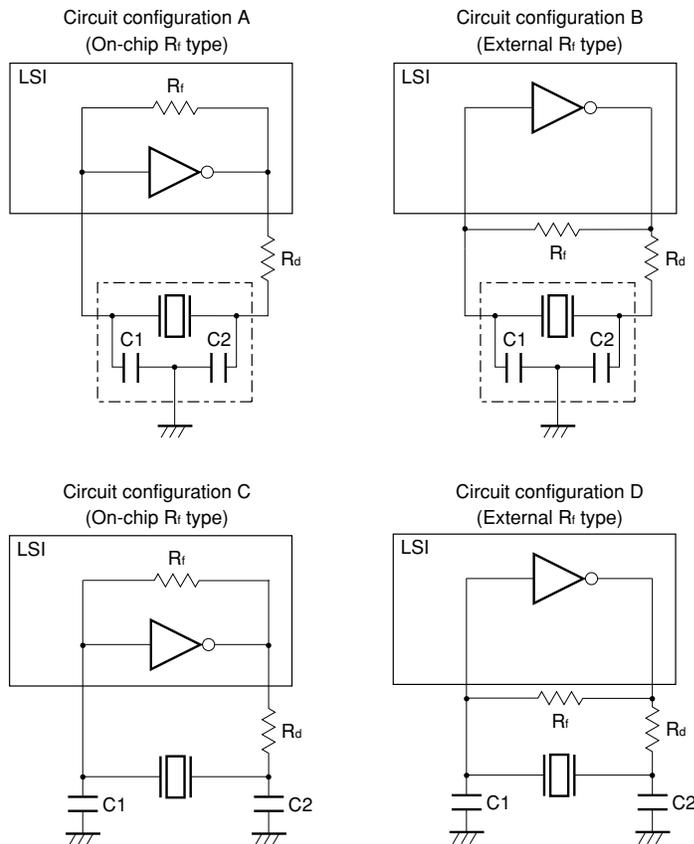
Remark R_f: Feedback resistor

7.4 Memory

The CMOS-N5 Series can be used to place memory blocks. This section explains the types of memory blocks and the points to be noted in using the memory blocks.

7.4.1 Types of memory blocks

The types of memory blocks available in the CMOS-N5 Series are listed below.

- Single-port RAM
- Dual-port RAM

Lists of each memory block are provided in Table 7-4. These memory blocks can also be mixed together.

Table 7-4. Memory Blocks

(a) Single-port RAM

Number of bits \ Number of words	16	32	64	128	256	512	1K	2K
4	RB47	RB49	RB4B	RB4D	RB4F	RB4H	RB4M	RB4S
8	RB87	RB89	RB8B	RB8D	RB8F	RB8H	RB8M	
10			RBAB	RBAD	RBAF	RBAH		
16	RBC7	RBC9	RBCB	RBCD	RBCF	RBCH	RBCM	
20			RBEB	RBED	RBEF	RBEH		
32	RBH7	RBH9	RBHB	RBHD	RBHF	RBHH		
40			RBKB	RBKD	RBKF	RBKH		

(b) Dual-port RAM

Number of bits \ Number of words	16	32	64	128	256	512
4	R947	R949	R94B	R94D	R94F	R94H
8	R987	R989	R98B	R98D	R98F	
10			R9AB	R9AD		
16	R9C7	R9C9	R9CB	R9CD	R9CF	
20			R9EB	R9ED		
32	R9H7	R9H9	R9HB			
40			R9KB			

7.4.2 RAM blocks

As shown in Figures 7-8 and 7-9, the high-density RAMs of the CMOS-N5 Series have a bit/word architecture based on basic macros (hard macros). The BIST (Built-In Self Test) circuit and on-chip selector are configured by soft macros. This architecture eases restrictions on placement and routing, and reduces complexity when multiple RAMs are incorporated.

The memory test is a test-dedicated macro, called BIST, that is incorporated in a soft macro. Three test pins eliminate the trouble of directly testing the I/O of all the pins.

When using an NEC Electronics RAM, be sure to use an NEC Electronics standard test circuit (BIST).

Figure 7-8. Single-Port RAM Circuit Configuration
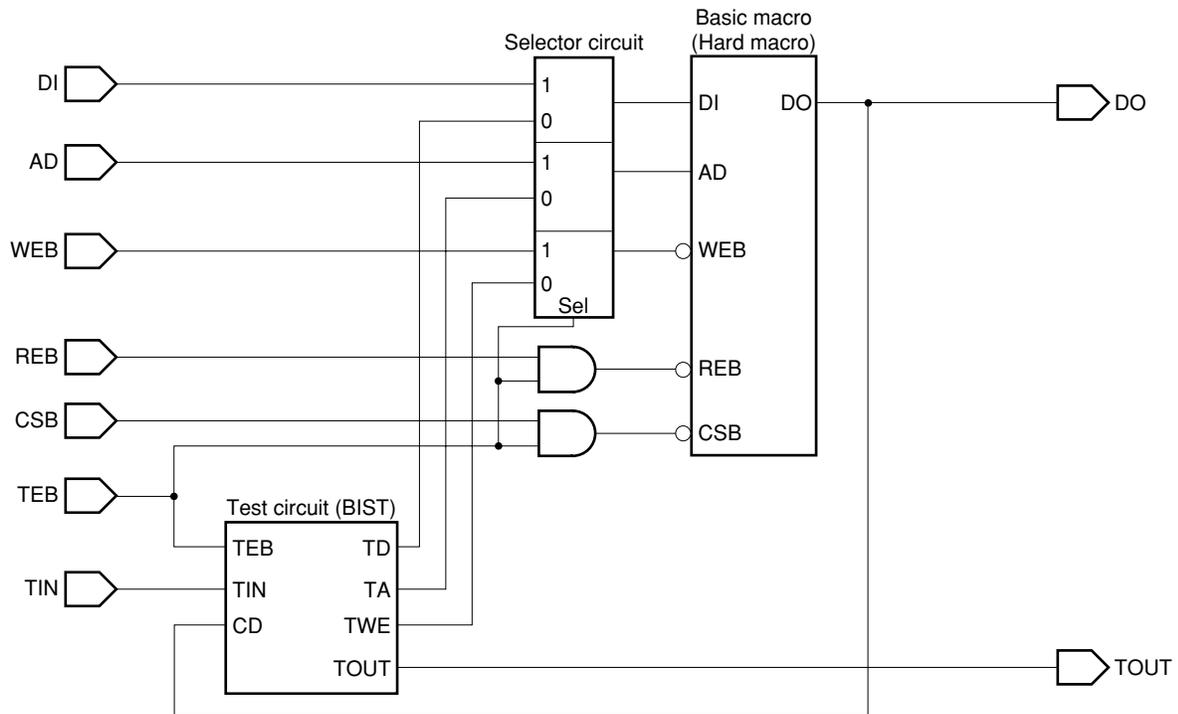
Figure 7-9. Dual-Port RAM Circuit Configuration
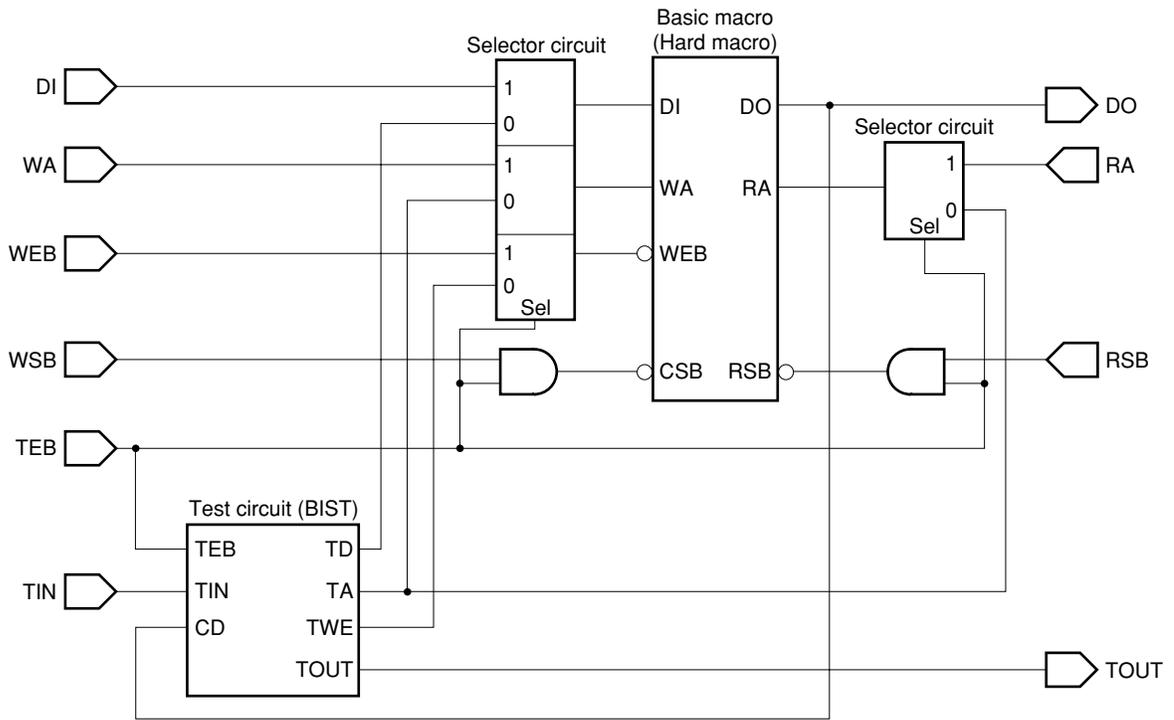
7.5 Writing Memory Blocks

When writing memory blocks as circuit diagrams or connection data, bear in mind the following points.

7.5.1 Selecting memory blocks

The RAM blocks of the CMOS-N5 Series are configured as soft macros. Therefore, RAM blocks with any bit/word configuration can be placed by combining the basic memory cells. However, the blocks that are used frequently are registered in advance as simulation models (see **CMOS-N5 Series Memory Block Library (A14683E)**). Select the block with the bit/word size closest to your needs from these models.

If a memory block with the desired size does not exist because the number of bits is exceeded, connect blocks of the same word size with different bit size in parallel.

Conversely, if the number of words is exceeded, divide the addresses by creating a chip select signal with a decoder, in the same manner as an ordinary memory circuit.

When using a memory with an unmatched number of bits and words, use soft macros in the way described above. For the circuit configuration and test circuit (BIST) configuration, consult NEC Electronics.

7.5.2 Using memory blocks

Memory blocks, as with other function blocks, have specifications for fan-in (F/I) and fan-out (F/O); see the **CMOS-N5 Series Memory Block Library (A14683E)**. The blocks must be connected without exceeding restrictions such as the limit on the number of fan-outs.

The RAM block cannot be used when the power supply voltage specification is 3.0 V or 3.3 V.

7.6 Memory Test

7.6.1 RAM test

Because the RAM block of the CMOS-N5 Series employs BIST, the limits on the number of test patterns is relaxed, so that the user can easily check the memory.

BIST consists of signal generators for test signals including test address, test data, and test enable, as well as an expected value generator, and a comparator, as shown in Figure 7-10. The user simply needs to connect the three pins, TIN, TEB, and TOUT, to external pins to test a RAM. When placing two or more RAM blocks, the test inputs (TIN and TEB) can be shared with the respective pins of the other RAM blocks. The test output (TOUT), however, cannot be shared. Connect the test output to different external pins. Figure 7-11 shows a connection example.

To test RAM, basically, data is applied from an external input pin to a test input pin (TIN or TEB), and a test output (TOUT) extracted from an external pin. If the signal is inverted or a clock is necessary because an inverter or flip-flop is used, the basic test pattern cannot be used. The final state of the user's test pattern must be in a state in which the test can be conducted (a state in which TIN, TOUT, and TEB can transfer the RAM test signal from external pins). The RAM test pattern is prepared by NEC Electronics.

Figure 7-10. Test Circuit (BIST) Block Diagram
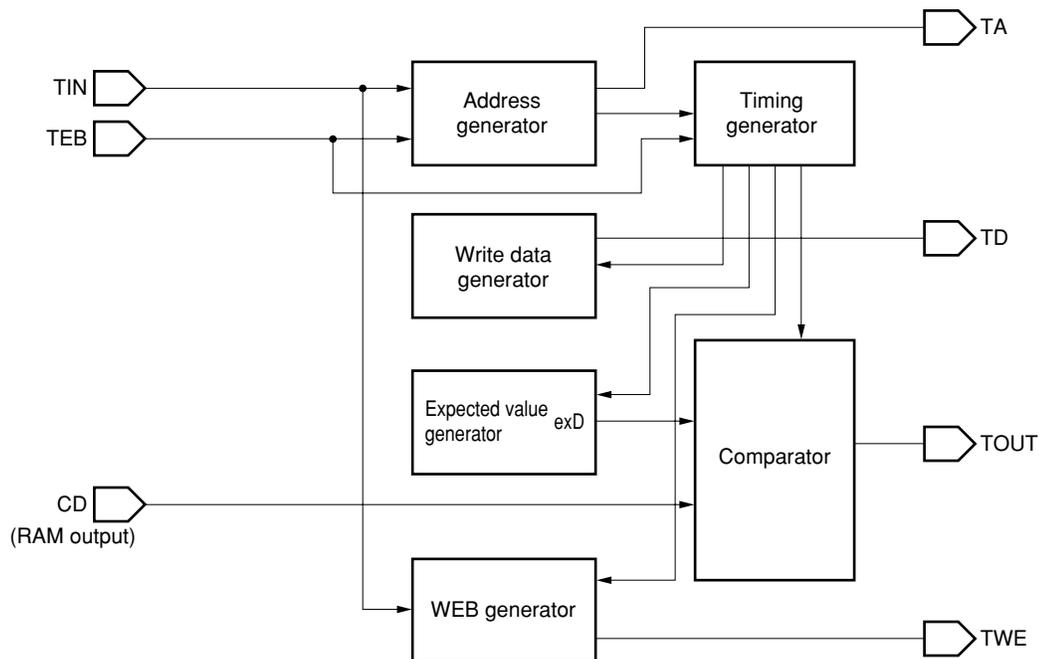
Figure 7-11. RAM Test Circuits (1/2)

(a) Connection example for placing one RAM block
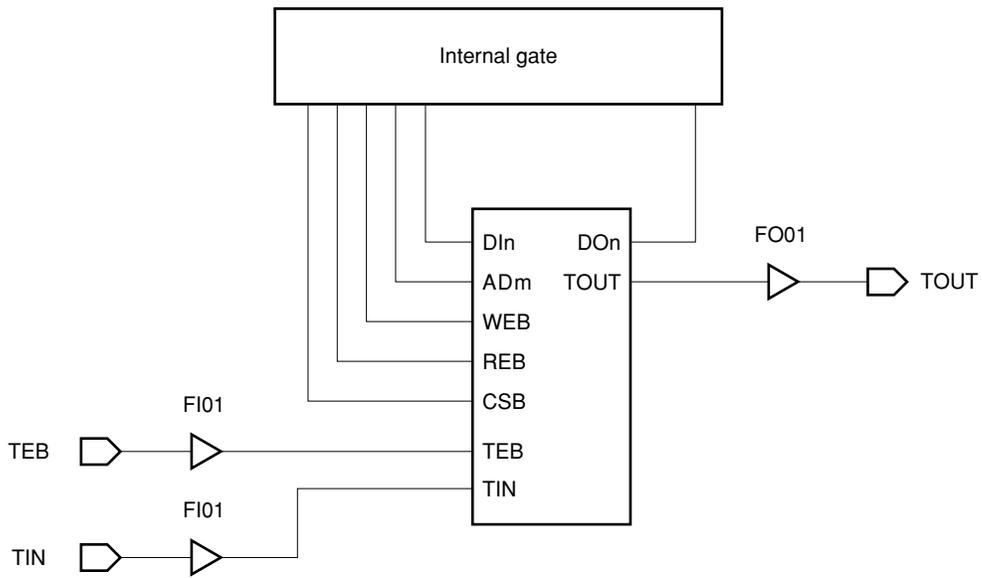
Figure 7-11. RAM Test Circuits (2/2)

(b) Connection example for placing multiple RAM blocks
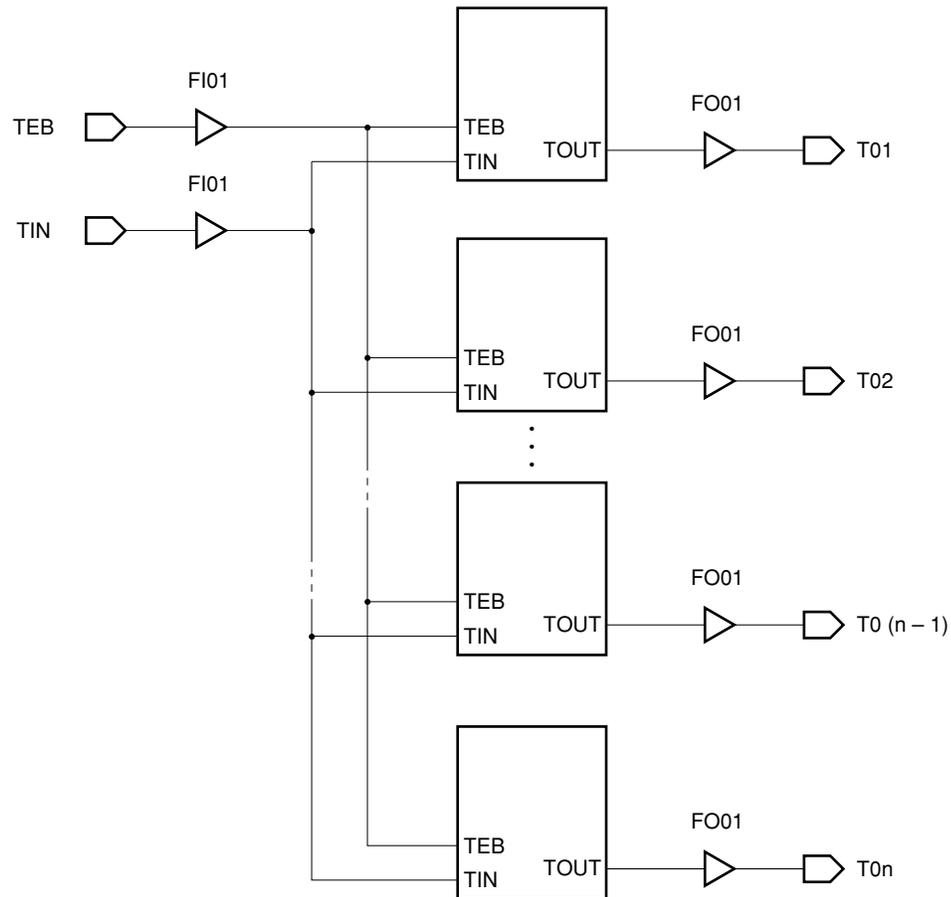
(1) Be sure to use <u>one</u> TEB input and TIN input. Connect each input to the respective RAM. Even if the capacitance of the RAM block differs, be sure to use one TEB input and TIN input commonly as shown in the figure.

(2) The TOUT pins must be made independent and must be output to external pins.

7.6.2 Assigning test I/O pins (TIN, TEB, and TOUT)

(1) When there are unused pins

If there are unused pins, excluding power supply pins and NC pins, they can be used for testing.

(2) When there are no unused pins

Pins used for logic can also be used as test pins. The points noted below must be considered when making pins alternate-function. Note that the TEB pin is a dedicated pin, therefore it cannot be used for other functions.

<1> Making the TIN pin alternate-function

The TIN pin can be used as a normal input pin and a normal output pin. To use as a normal output pin, the TEB signal must be made an enable signal and the pin must be made bidirectional. The pin then can be used as an output pin during normal usage and as an input pin during testing. Also, in this case, make the end of the user's test patten low level. Figure 7-12 shows a connection example.

<2> Making the TOUT pin alternate-function

The TOUT pin can be used as a normal input pin and a normal output pin. To use as a normal input pin, the TEB signal must be made an enable signal and the pin must be made bidirectional. The pin then can be used as an input pin during normal usage and as an output pin during testing. To use as a normal output pin, it can be used in combination with an internal selector circuit, and the pin can be switched by the TEB signal. Figure 7-13 shows a connection example.

Caution   Pins used for the GTL interface buffer, N-ch open-drain buffer, and CMOS 5 V tolerant buffer cannot be made alternate-function pins.

- **Handling pins on the board**

Handle each pin using one of the following procedures.

<1> TEB pin[Note 1]:   • Use a pull-up buffer
                         • Pull up externally
                         • Externally connect to V_{DD}
<2> TIN pin[Note 2]:   • Use a pull-up buffer
                         • Use a pull-down buffer
                         • Externally connect to V_{DD}
                         • Externally connect to GND

Notes 1. Handle in the direction that is not the test mode.
      2. When not alternatively used as a normal pin

Figure 7-12. Making TIN Pin Alternate Function

(a) Alternate-function use with normal input pin

(b) Alternate-function use with normal output pin (bidirectional pin)
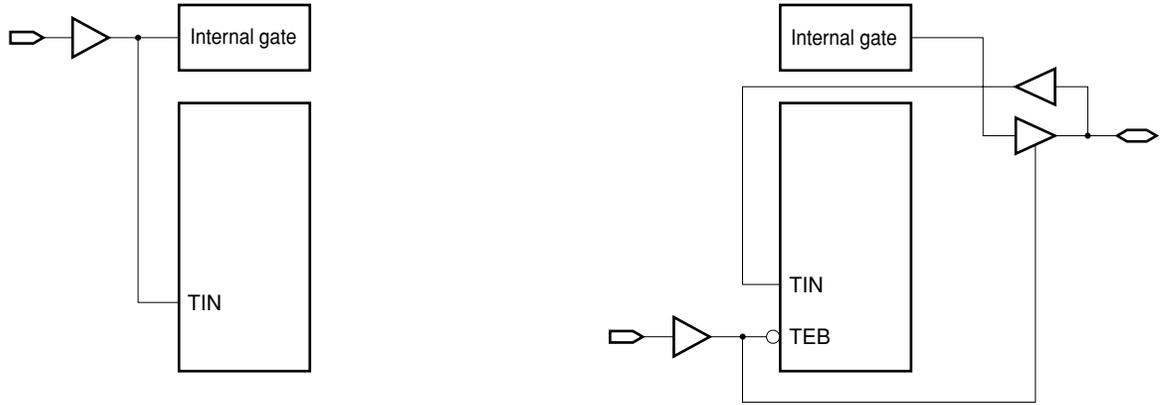
Figure 7-13. Making TOUT Pin Alternate Function

(a) Alternate-function use with normal input pin (bidirectional pin)

(b) Alternate-function use with normal output pin
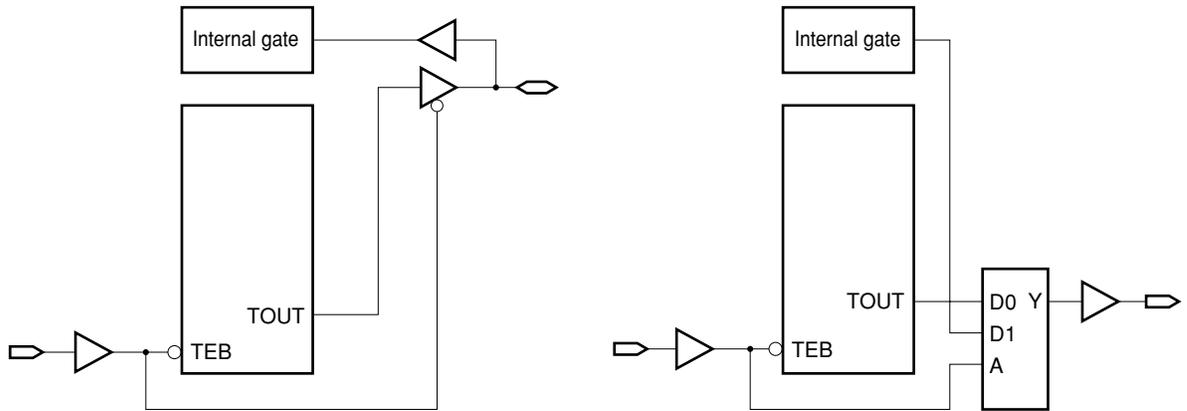
7.6.3 Checking connection of RAM test circuit

To check whether or not the BIST circuit is properly connected, carry out checking by RAMCHK flow on OPENCAD generating and adding the connection confirmation patterns (nine patterns) as shown in Figure 7-14 to the end of the user-provided test pattern (Test pattern for DC check: if the DC pattern is independent, then it is this pattern) by using OPENCAD RAMCHK. Be sure to perform RAMCHK before submitting the test pattern to NEC Electronics. In addition, set the status in which input and output for the pin signals required to the BIST test (TEB, TIN, and TOUTx) can be executed at the end of the test pattern (Test pattern for DC check: if the DC pattern is independent, then it is this pattern.) When using the TIN pin alternatively as a normal output pin, set the end of the user-provided test pattern to low level.

The RAM-BIST test pattern is provided by NEC Electronics and thus the user does not need to generate it.

Figure 7-14. Example of Test Patterns
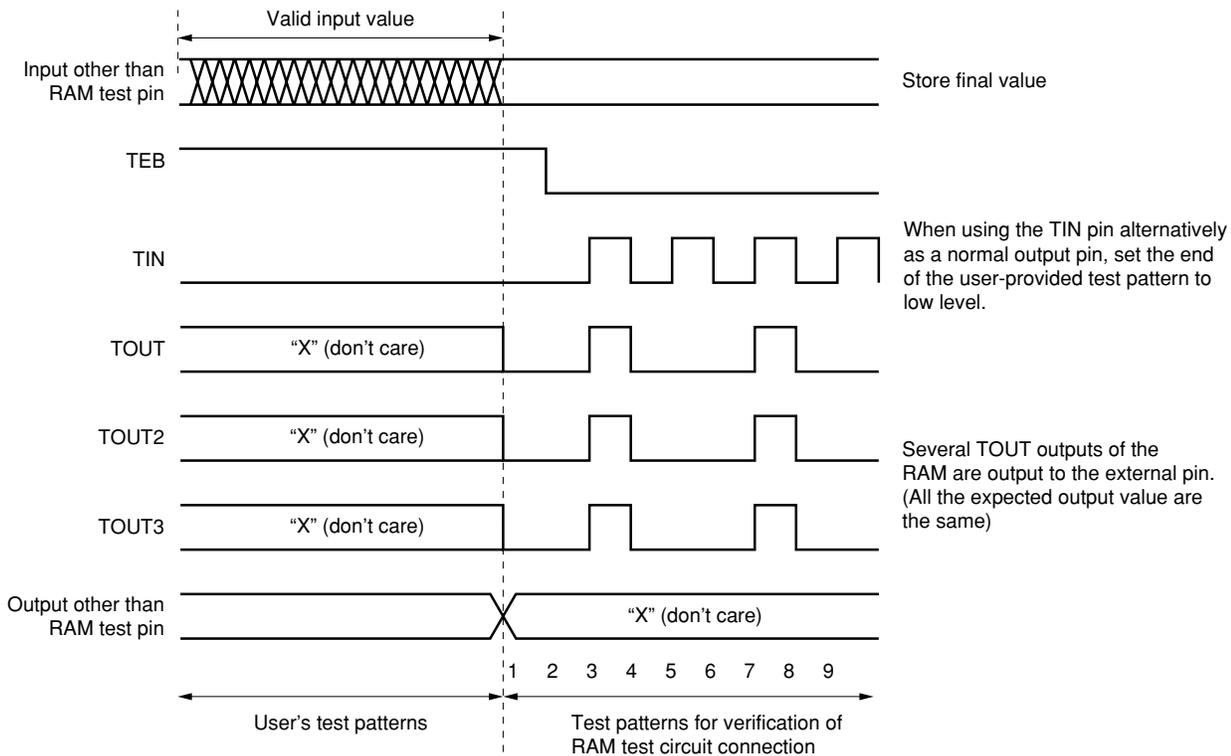
(1) Input other than RAM test pin: Input 9 patterns in such a way that the final value of the user test pattern is preserved.

(2) TEB: First input a high level for 1 pattern and then input a low level for 8 patterns.

(3) TIN: First input a low level for 1 pattern and then input 8 patterns of repetitive 01 signals.

(4) TOUT: Set the expected output value to 001000100. When multiple RAM is placed, several TOUT outputs of the RAM must be output to the external pins (the RAM test is executed completely in parallel).

(5) Output other than RAM test pin: Set the expected output value to "X" (don't care).

Remark The connection check pattern of BIST is automatically generated by RAMCHK and thus it is not necessary to add it to the user's patterns in advance.

In addition, simultaneous checking can be carried out by connecting TIN and TEB in common in the gate array type RAM and cell-based IC type RAM.

7.7 Scan Path Test Block

It is extremely difficult to generate a test pattern that checks the operation of an LSI efficiently with a circuit frequently using flip-flops and with a deep logical depth. Scan path testing can change the connections of all the internal flip-flops of an LSI like shift registers. Therefore, the circuit can be tested efficiently by easily initializing all the flip-flops of a circuit with a deep logical depth and reading all the flip-flop states in a certain state.

For details, see **NEC SYSTEM LSI DESIGN Design For Test User's Manual**.

Figure 7-15. Theory of Scan Path Test Method
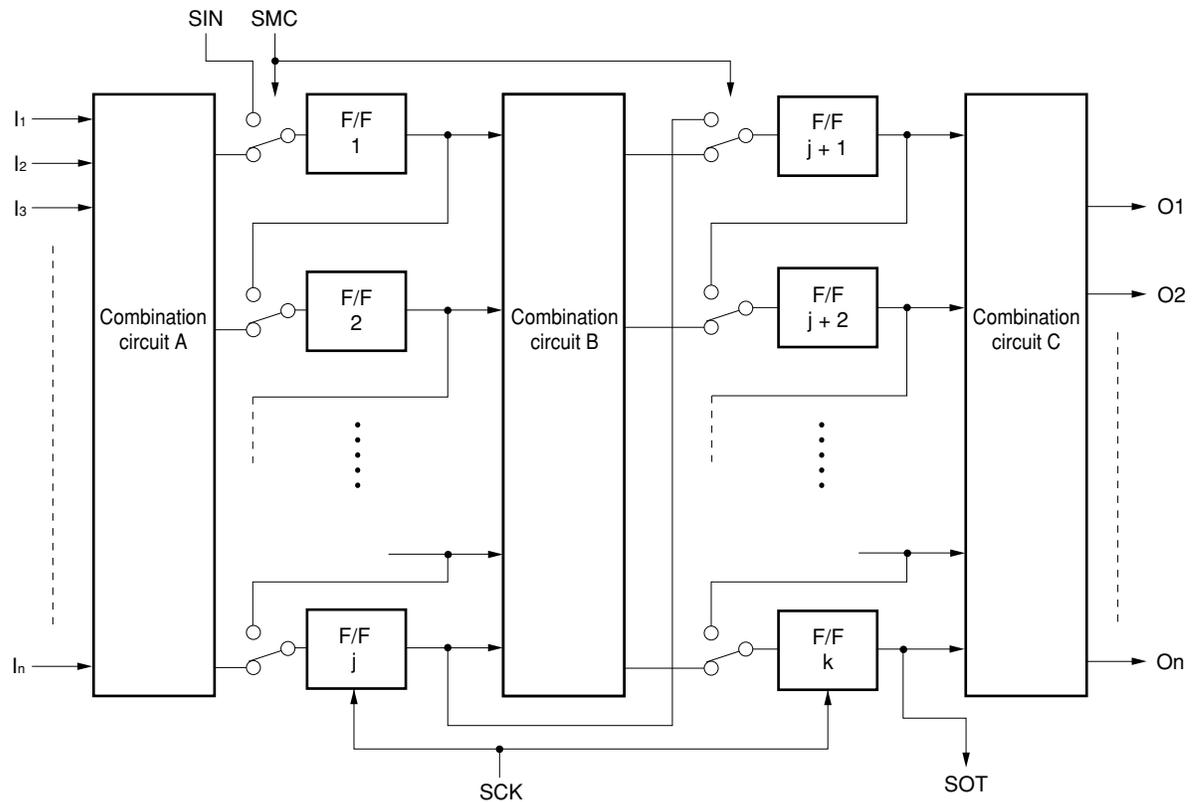
Remark I_n: Input signal when testing a combination circuit, or normal input

On: Diagnostic output when testing a combination circuit, or normal output

SIN: Input signal when testing a sequential circuit

SMC: Mode switching signal

SCK: Test clock

SOT: Diagnostic output when testing a sequential circuit

APPENDIX A POWER CONSUMPTION (PRELIMINARY)

An accurate calculation of the power consumption of internal circuits requires a very large amount of data, such as the capacitance, the number of synchronously operating blocks, and the operating frequency of each block. Consequently, the calculation becomes too complicated to be performed. On the basis of assumptions concerning such items as circuit operation and configuration, NEC Electronics provides reference values for power consumption. It must be noted that these values may be larger or smaller than the actual values, depending on factors such as the user's actual circuit and its configuration.

This chapter provides a power consumption calculation method that divides the power consumption of the internal circuit into combination circuits, latches, flip-flops. This calculation should be used to review circuit power consumption. However, if the results are to be used to calculate the life-span of a battery, an extra margin should be provided.

Internal cell power consumption

$$\Sigma\ P_{DCELL} = \Sigma\ P_{DGate} + \Sigma\ P_{DLatch} + \Sigma\ P_{DF/F} + \Sigma\ P_{DT}$$

(1) Combination circuits

$$P_{DGate} = 6.73 \times f \times Cell\ (\mu w)$$

f: Data operating frequency

Cell[Note]: Number of cells that operate at f

Note "Cell" is not the number of blocks.

(2) Latches

$$P_{DLatch} = (P_{D(Gate = ON)} \times N + P_{D(Gate = OFF)} \times (1 - N)) \times f \times Cell\ (\mu W)$$

$P_{D(Gate = ON)}$: 3.43 (μW/Cell/MHz)

N: Gate ON rate $= \dfrac{T_{(Gate = ON)}}{T_{(Gate = ON)} + T_{(Gate = OFF)}}$

$P_{D(Gate = OFF)}$: 0.23 (μW/Cell/MHz)

f: Data operating frequency

Cell[Note]:   Number of cells that operate at f

Note "Cell" is not the number of blocks.

(3) D-F/F, JK-F/F, shift registers, and counters

$$P_{DF/F} = \frac{2 \times P_{D(OUTPUT)} + P_{D(CLK)} \times (N - 2)}{N} \times f \times Cell \ (\mu W)$$

$P_{D(OUTPUT)}$: 1.19 (μW/Cell/MHz)

$P_{D(CLK)}$:   0.68 (μW/Cell/MHz)

N: $\dfrac{T_{(DATA)}}{T_{(CLK)}}$

$T_{(DATA)}$:   Data cycle

$T_{(CLK)}$:   Clock cycle

f: Clock operating frequency

Cell**Note**:   Number of cells that operate at f

Example The following indicates the case when the clock has a cycle speed double that of 1 data cycle.
N = 1/0.5 = 2

Note   "Cell" is not the number of blocks.

(4) T-F/F

$$P_{DT} = 3.8 \times f \times Cell \ (\mu W)$$

f: Clock operating frequency

Cell**Note**: Number of cells that operate at f

Note   "Cell" is not the number of blocks.

(5) Load dependency of power consumption (preliminary)

The power consumption depends to a great extent on the load capacitance, as expressed by

$$P_D = CV^2f$$

Figure A-1. Load Dependency of Power Consumption

Under study

The unit power consumption when F/O = 2 is an extremely small 3 μW/MHz. Because power consumption has a significant effect on reliability, a realistic value must be used.

The value covers a distribution of about 70% of load values, based on statistical data accumulated at NEC Electronics, such as wiring length and pin pairs.

Load =   (F/I equivalent)
Example
  F/O :   + L :

(Under study)

APPENDIX B PROPAGATION DELAY TIME

The delay time of each block varies significantly with the input signal waveform as shown in Figure B-1. With the CMOS-N5 Series whose delay time is as short as several 100 ps at each block, the influence of the input waveform is not negligible.

Figure B-1. Delay Time Increase Due to Input Waveform

t_r/t_f (MIN) < t_r/t_f (TYP) < t_r/t_f (MAX)
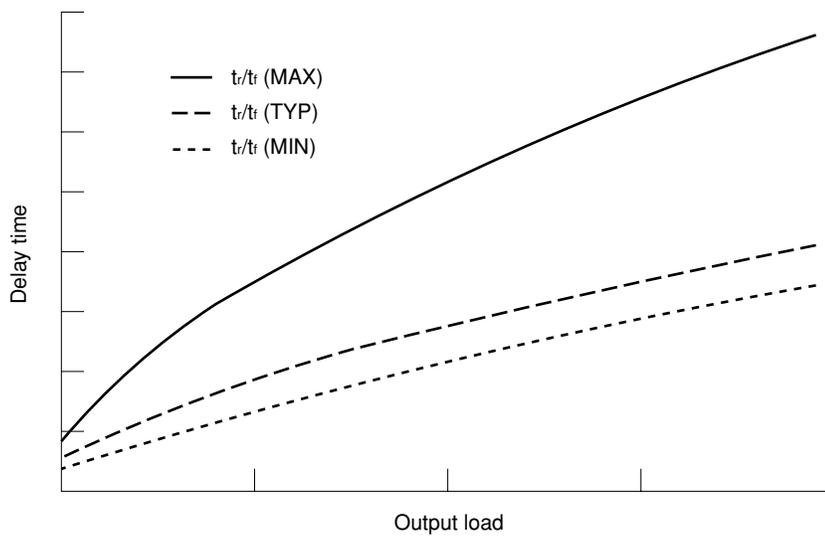
Consequently, the simulator considers the input waveform of each block so that a highly accurate delay simulation is executed. However, discrepancies in results due to the input waveform cannot be listed in the block library[Note]. For this reason, the accuracy of the propagation delay time calculations listed in the block library[Note] are valid only under certain limited conditions. The propagation delay times of critical paths, in which the load is likely to be light, are calculated accurately in the CMOS-N5 Series.

Note that Figure B-1 is indicating a tendency only. Verify the actual value by performing simulation.

Note   CMOS-N5 Series (5.0 V) Block Library (A13872E) and CMOS-N5 Series (3.3 V) Block Library (A15895E)

C.1 ALBATROSS File Format (Circuit Name.alb)

(1) File format

The ALBATROSS file format has the following restrictions:

- Free format
- Parameters must be separated by blank space or a colon (:).
- Each statement must be terminated with a semicolon (;).
- Items within quotes (" ") can be repeated.
- Maximum of 80 columns per line (when the last character is not a semicolon, the line must continue on the next line)
- Identifiers, pin names, and units (NS fixed) must be specified in uppercase letters
- Pin names consist of a maximum of 64 characters
- The description of the timing data (MODULATION + CLOCK) is based on the limitations shown in **6.6 High-Speed Function Test (Real-Time Test)**.

(2) File configuration

The ALBATROSS file consists of the following seven parameters.

*ALBATROSS	...	File header
*TIMING	...	Header
PERIOD	...	Pattern period
MODULATION	...	Input skew
CLOCK	...	Clock pin
*END_OF_TIMING	...	End record
*END	...	File end

(3) Details of file

The details of each parameter are as follows:

(a) File header

Syntax: *ALBATROSS circuit;

Function: Pattern header

1: circuit (character string) circuit name

(b) Header

Syntax: *TIMING

Function: Header

(c) Pattern period

Syntax: PERIOD period_t time_unit;

Function: Period value of pattern

1: period_t   Pattern cycle

2: time_unit   Cycle unit

(d) Input skew

Syntax: MODULATION modulation_t time_unit: "pin";

Function: Value of skew added to input pin

1: modulation_t   Value of input skew

2: time_unit   Unit of value of skew

3: pin   Pin name

(e) Clock

Syntax: CLOCK TYPE = type: "ch_time time_unit": pin;

Function: Definition of clock pin and clock waveform

- TYPE = type

  P: Positive clock

  N: Negative clock

- ch_time   Waveform time
- time_unit   Unit of change time
- pin   Pin name

(f) End

Syntax: *END_OF_TIMING;

Function: End

(g) File end

Syntax: *END

Function: File end

(4) Example

*ALBATROSS CF191

*TIMING;

PERIOD 200 NS;

MODULATION 20 NS: IN1 IN2 IN3;

CLOCK TYPE = P: 50NS 150NS: CLK;

*END_OF_TIMING;

*END

C.2 DIF File Format (Circuit Name.dif)

For details, see **NEC SYSTEM LSI DESIGN OPENCAD OPC_VSHELL User's Manual (A16306E)**.

(1) File format
The DIF file format has the following restrictions:

- Free format
- The delimiter is a blank space.
- Maximum of 512 characters per line
- The first column of a comment line begins with "-".

(2) File configuration
The DIF file consists of the following three parameters:
DIF   .... Header
/DESIGN .... Design block
/END   .... End

(3) Details of file
The details of each parameter are as follows:

(a) Header
Syntax: DIF
Function: Header

(b) Design block
Syntax: /PIA
Function: All external pins (V_{DD}, GND, etc.)

(c) Condition block
Syntax: /PIN
Function: Overall design (such as value of pin capacitance
               added to output pin)

(d) End card
Syntax: /END
Function: Termination of DIF file

(4) Example

*DIF opc_pinbe (1.11) 2002.12.12 (12:39:32)

/DESIGN 65880999

TECHNOLOGY = CMOSN5;

CONDITION = cmos_5.0V;

MASTER = 65880;

PACKAGE = LQFP;

PINS = 144;

LAYER = 3L;

 /CONDITION 1

   /PIN

     ADO

         DIR = INPUT

      ;

      DATA1

         DIR = IO

      ;

      PC1

         DIR = OUTPUT

       ;

    /END PIN

 /END CONDITION

/PIA

 /EPIN PAD

     ADO

         PAD =   77 # dut_ID 22 pin_type IN

         BLOCK = XINB;

     DATA1

         PAD =   24 # dut_ID 179 pin_type IO

         BLOCK = XWN2;

     PCR1

         PAD =   125 # dut_ID 68 pin_type OUT

         BLOCK = XB0D;

  /END EPIN

   /POWER PAD

         GND PAD = 13 191;

         VDD PAD = 14;

    /END POWER

 /END PIA

 /END DESIGN

 *END

APPENDIX D DRAWING CIRCUIT DIAGRAMS AND TIMING CHARTS

D.1 Drawing Circuit Diagrams

   Today circuits are designed using an engineering workstation (EWS). The circuit diagram drawn by the user is converted to NEC format on the EWS or through the interface service offered by NEC Electronics.

   When the user draws a circuit diagram, the following points should be kept in mind to ensure smooth interfacing with NEC Electronics.

D.1.1 Logic symbols

   As a general rule, use the logic symbols that are in the block library**Note**. However, when there are differences between the EWS library and the block library**Note**, follow the format of the EWS library.

   Note   CMOS-N5 Series (5.0 V) Block Library (A13872E) and **CMOS-N5 Series (3.3 V) Block Library (A15895E)**

D.1.2 Block names (function names)

   Input buffers and other blocks have different designations, but may have logic symbols that are virtually the same. In particular, the various input/output buffer interface levels cannot be determined from simulation results. Because of this, the block name should be entered so that it is easily understood.

   In addition, since block names are displayed in advance in EWS libraries, entries do not have to be made when using the EWS.

D.1.3 Pin names (I/O pin name of block)

   Block I/O pins are named in the order "H01, H02,.../N01, N02,...." If a block has more than one I/O pin, the pin names must be used whenever possible.

   Pin names are usually displayed in EWS libraries. If a pin name is displayed, it does not have to be entered. For more information on displaying pin names, follow the instructions in the interface manual for the EWS.

D.1.4 Gate names (specific name of each block)

   Enter the respective characteristic gate names for block names entered in a circuit diagram. A gate name must consist of no more than 255 alphanumeric characters. To avoid duplication of gate names and pin names, make the names unique.

   When an EWS is used, there are special cases where the naming rules are a function of the system being employed. For details, follow the instructions in the interface manual for the EWS.

D.1.5 I/O pin names

A pin name of up to 64 alphanumeric characters must be assigned to each I/O pin of the LSI device. Each pin name must be unique and must not duplicate a gate name.

When an EWS is used, there are special cases where the naming rules are a function of the system being employed. For details, follow the instructions in the interface manual for the EWS.

Figure D-1. Circuit Diagram Example
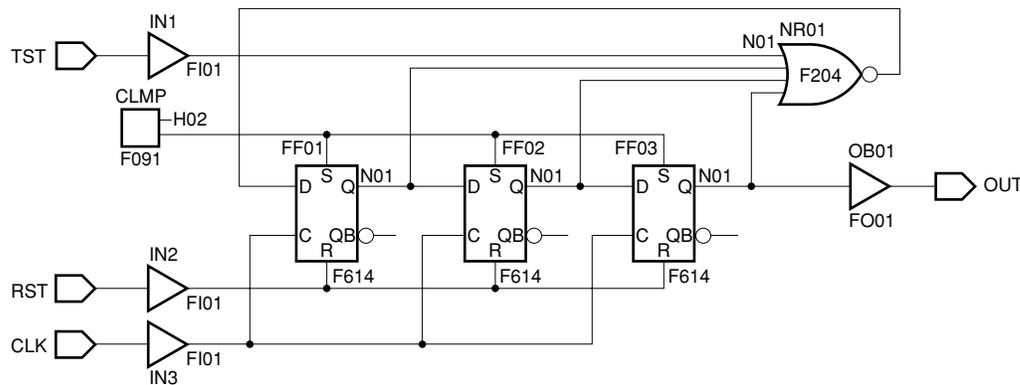
(1) Input pin names

The pin name of an input pin must consist of 1 to 64 alphanumeric characters.

In addition, undefined and high impedance states cannot be input to an input pin because this causes the measurement conditions to change during testing with the LSI tester, making measurement impossible. Undefined and high impedance states also cannot be input to the input pins of input buffers and bidirectional buffers with on-chip pull-up/pull-down resistors.

If undefined or high impedance states are input as a test pattern, an error will result when executing simulation.

(2) Bidirectional pin names

If the input and output of a bidirectional buffer are implemented from one pin, this must be named by using a bidirectional pin. The pin name must consist of 1 to 64 alphanumeric characters.

Figure D-2. Bidirectional Pin Names
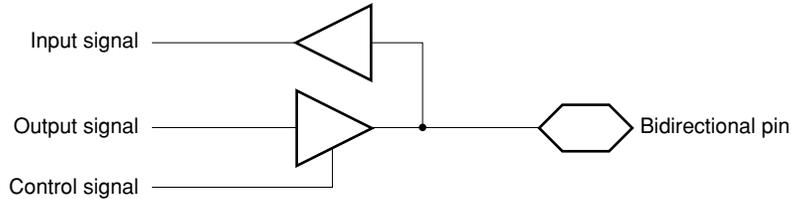
When a bidirectional pin test pattern is generated, care must be taken with regard to the following points:

<1> For switching from the output mode to the input mode, set the input and output signals to the same level.
<2> Do not set the control signal to the undefined state (if the state of the control signal becomes undefined, an undefined state is propagated to the input signal, generating an error in simulation).

During switching from the input mode to the output mode, an undefined state is propagated to the input signal due to the delay time of the control signal, generating an error in simulation. For such switching, it is important to configure the circuit so that an undefined state is not propagated to the input signal (see **6.3.6 Notes on switching I/O mode of bidirectional pin**).

Figure D-3. Bidirectional Pin Test Pattern Generation
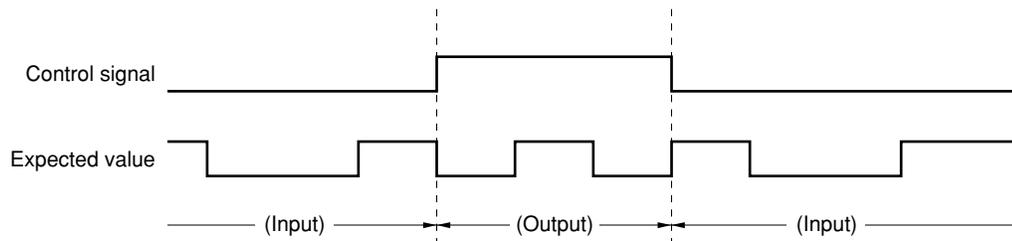
(3) 3-state output pin description

A 3-state output pin must be named as shown in the example in Figure D-4. The pin name must consist of 1 to 64 alphanumeric characters.

Figure D-4. 3-State Output Pin Names
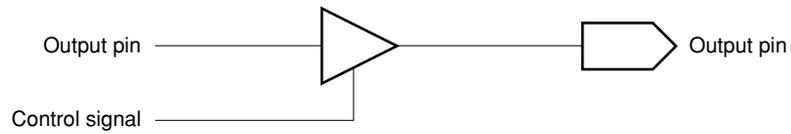
Figure D-5. 3-State Output Pin Test Pattern Generation
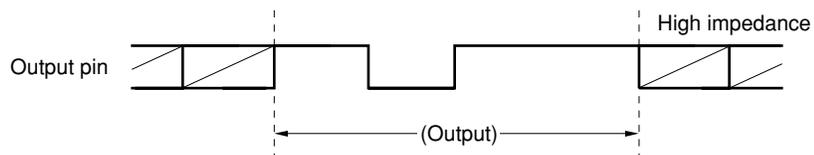
D.2 Handling Macros

The logic of a large-scale circuit is often designed using hierarchical techniques to enable block design in a system and to diversify the man-hours needed for design.

In the hierarchical design technique, functional units used in common are defined as macros (user macros). Each LSI chip is designed by connecting several macros to enable a specified function. In particular, a large-scale circuit is usually divided into several blocks, each of which is a hierarchical block and combined to configure the entire circuit.

When designing hierarchical circuits, note the following guidelines (see **Figure D-6**).

<1> Each hierarchical block should perform a single logical operation.

<2> Make the design in a way that the total structure and the signal flow can be understood at the top level hierarchy (the top level hierarchy should be drawn on a single page).

<3> Whenever possible, design circuits that comprise a closed loop so that the loop fits within the macro.

<4> Input pins and clamps (if needed) must be on the same page.

<5> Note should be taken of the clock line flow. Ensure that delay differentials between pages do not exceed basic rules.

<6> Each macro (bottom hierarchy) must have a single function.

<7> A page should not contain signal lines only (pass-through only).

<8> External I/O buffers can be specified only at the top level hierarchy. Avoid connecting I/O pins directly to an external device from a lower macro other than that at the top level hierarchy.

<9> A macro should not contain input, output, and bidirectional buffers.

Figure D-6. Handling Macros

(a) Good example
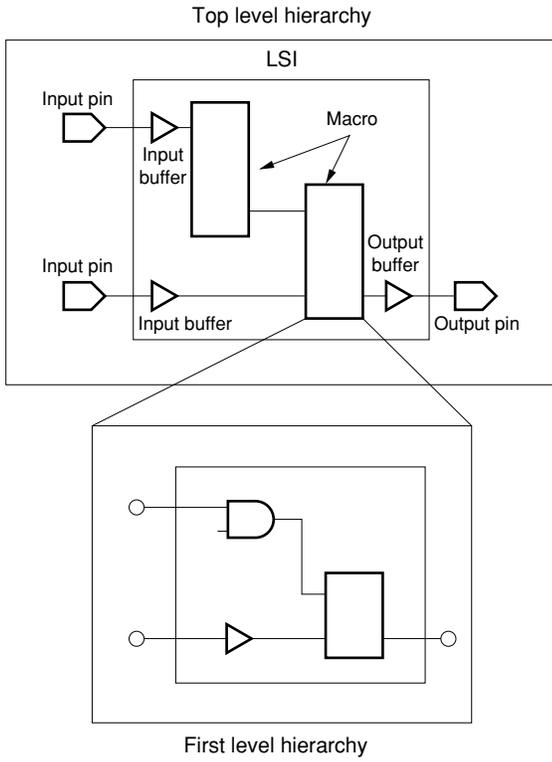
(b) Bad example
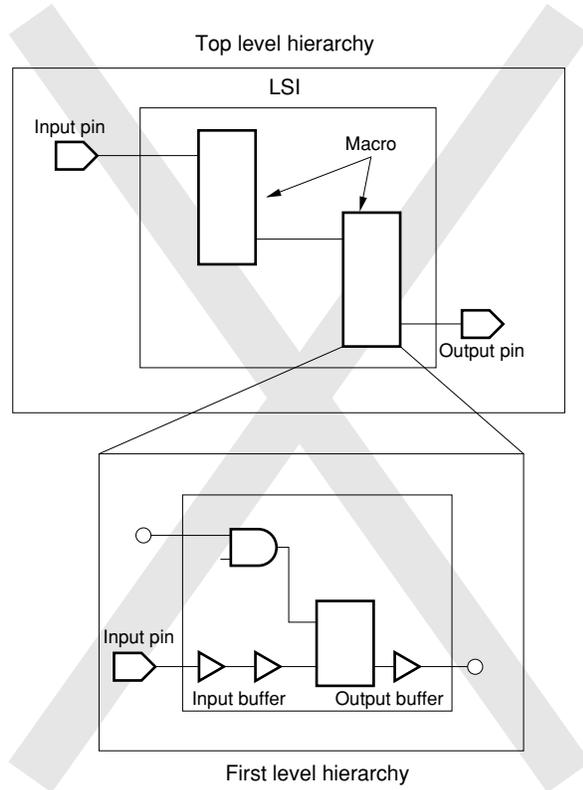
D.3 Preparing Timing Charts

If the user provides NEC Electronics with a timing chart for generating the test patterns, or even if the user generates the test patterns, the timing charts must be drawn using the guidelines explained in this section.

(1) Entry method
The pin names of all I/O pins must be written in the vertical column. For each pattern, apply 1 or 0 level for inputs and the expected values for outputs. Continuous sequential numbers, starting with 1, must be assigned to the test patterns.
Figure D-7 shows an example of filling out the timing chart.

Figure D-7. Timing Chart Entry
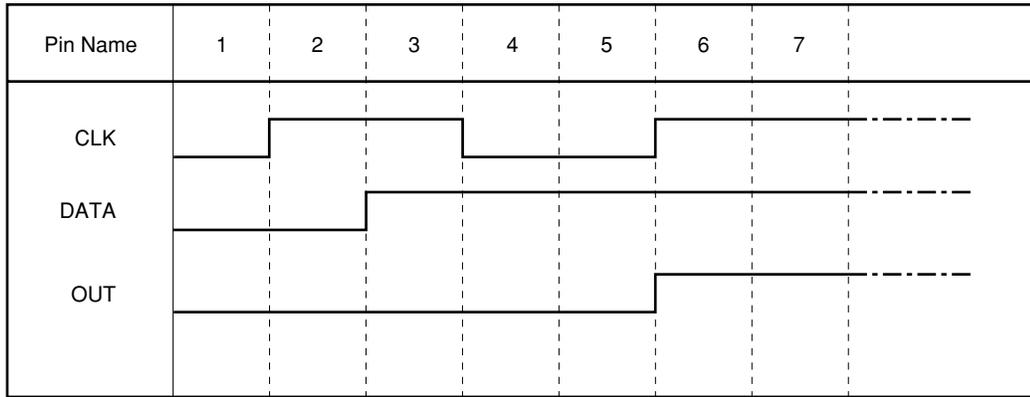
(2) Timing discrepancies
Because the output in actual circuits changes after the input pattern is applied, there is a timing delay between the input and output, as shown in Figure D-8 (a). However, the delay time between the input and output can be ignored when test patterns are generated, as shown in Figure D-8 (b). The patterns must be generated so that the entire circuit operates at the same timing.

Figure D-8. Timing Chart Example

(a) Actual circuit

(b) Timing chart entry
(Test pattern entry)
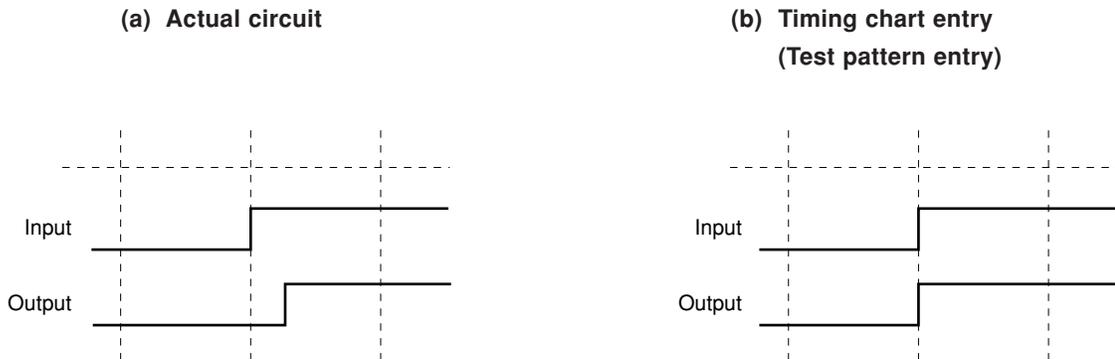
(3) Handling of "X" (undefined or don't care)

Depending on the configuration of the circuit, the value of an output pin may not be determined in the first few patterns. In that case, specify "X" (undefined) as the expected value of the output pin. When specifying "don't care" in cases where, due to the operation of the circuit it cannot be determined whether the value will become "1" or "0", only specify "X" as the expected output value during the corresponding period. In this case, the expected value will not be collated.

However, do not specify "X" for the input pin. If "X" is inadvertently specified for the input pin, an error will occur during simulation. If the input level of a certain period can be either high level or low level, specify either "1" or "0".

(4) Handling of "Z" (high impedance)

The output pins of a 3-state output buffer or a bidirectional buffer may become high impedance "Z" in some cases. In these cases, specify "Z" as the expected output value.

However, do not specify "Z" for the input pin. If "Z" is inadvertently specified for the input pin, an error will occur during simulation.

(5) Repeated pattern

When the same waveform is repeatedly input, such as in clock input, it can be efficiently input as a repeated pattern.

(6) Specifying critical path

In terms of system design, signal paths in which speed (the delay time between input and output) is especially important and paths in which the propagation delay time between input and output must be within a certain period, can be specified so that they satisfy the required performance, if clarified at the time of design.

If this is the case, specify the corresponding paths as critical paths. Critical paths include the following three types:

- Maximum delay time (t_{PD}) as an absolute value (MAX.)
- Minimum delay time (t_{PD}) as an absolute value (MIN.)
- Relative variable range between the paths

Specification of a critical path can be effective only for the delay time between input and output. A maximum of six paths can be specified as critical paths.

Entry example

	Mode No.	Assigned Pin	Output Load (pF)	Pattern No.	Delay Time (ns)		Determination
					MIN.	MAX.	
1	1	IN1 → OUT2	15	131	13	50	○
2							
3							
4							
5							
6							

Some blocks cannot be used, depending on the power supply voltage.

√: Can be used

Blank: Cannot be used

E.1 Interface Block

E.1.1 CMOS Level

Function	Block	5.0 V	3.3 V	Description	Cells (I/O)
Input Buffer	FI01	√	√	—	3 (1)
	FID1	√	√	50kΩ Pull-down	3 (1)
	FIU1	√	√	5kΩ Pull-up	3 (1)
	FIW1	√	√	5kΩ Pull-up	3 (1)
	FIS1W	√	√	Schmitt	6 (1)
	FDS1W	√	√	Schmitt 50kΩ Pull-down	6 (1)
	FUS1W	√	√	Schmitt 50kΩ Pull-up	6 (1)
	FWS1W	√	√	Schmitt 50kΩ Pull-up	6 (1)
Input Buffer with Failsafe	FIA1	√	√	—	3 (1)
	FDA1	√	√	50kΩ Pull-down	3 (1)
	FIE1W	√	√	Schmitt	6 (1)
	FDE1W	√	√	Schmitt 50kΩ Pull-down	6 (1)
Input Buffer with EN(AND)	FN11	√	√	—	6 (1)
	FN21	√	√	50kΩ Pull-down	6 (1)
Input Buffer with EN(OR)	FN13	√	√	—	4 (1)
	FN23	√	√	50kΩ Pull-down	4 (1)
Output Buffer	FO09	√	√	3mA	4 (1)
	FO04	√	√	6mA	4 (1)
	FO01	√	√	9mA	4 (1)
	FO02	√	√	12mA	12 (1)
	FO03	√	√	18mA	12 (1)
	FO06	√	√	24mA	12 (1)
Low-noise Output Buffer	FE09	√	√	3mA	5 (1)
	FE04	√	√	6mA	5 (1)
	FE01	√	√	9mA	5 (1)
	FE02	√	√	12mA	5 (1)
	FE03	√	√	18mA	5 (1)
	FE06	√	√	24mA	5 (1)

Function	Block	5.0 V	3.3 V	Description	Cells (I/O)
3-State Buffer	B00T	√	√	3mA	7 (1)
	B0DT	√	√	3mA 50kΩ Pull-down	7 (1)
	B0UT	√	√	3mA 50kΩ Pull-up	7 (1)
	B0WT	√	√	3mA 5kΩ Pull-up	7 (1)
	B00E	√	√	6mA	7 (1)
	B0DE	√	√	6mA 50kΩ Pull-down	7 (1)
	B0UE	√	√	6mA 50kΩ Pull-up	7 (1)
	B0WE	√	√	6mA 5kΩ Pull-up	7 (1)
	B008	√	√	9mA	7 (1)
	B0D8	√	√	9mA 50kΩ Pull-down	7 (1)
	B0U8	√	√	9mA 50kΩ Pull-up	7 (1)
	B0W8	√	√	9mA 5kΩ Pull-up	7 (1)
	B007	√	√	12mA	17 (1)
	B0D7	√	√	12mA 50kΩ Pull-down	17 (1)
	B0U7	√	√	12mA 50kΩ Pull-up	17 (1)
	B0W7	√	√	12mA 5kΩ Pull-up	17 (1)
	B009	√	√	18mA	17 (1)
	B0D9	√	√	18mA 50kΩ Pull-down	17 (1)
	B0U9	√	√	18mA 50kΩ Pull-up	17 (1)
	B0W9	√	√	18mA 5kΩ Pull-up	17 (1)
	B00H	√	√	24mA	17 (1)
	B0DH	√	√	24mA 50kΩ Pull-down	17 (1)
	B0UH	√	√	24mA 50kΩ Pull-up	17 (1)
	B0WH	√	√	24mA 5kΩ Pull-up	17 (1)

Function	Block	5.0 V	3.3 V	Description	Cells (I/O)
Low-noise 3-State Buffer	BE0T	√	√	3mA	7 (1)
	BEDT	√	√	3mA 50kΩ Pull-down	7 (1)
	BEUT	√	√	3mA 50kΩ Pull-up	7 (1)
	BEWT	√	√	3mA 5kΩ Pull-up	7 (1)
	BE0E	√	√	6mA	7 (1)
	BEDE	√	√	6mA 50kΩ Pull-down	7 (1)
	BEUE	√	√	6mA 50kΩ Pull-up	7 (1)
	BEWE	√	√	6mA 5kΩ Pull-up	7 (1)
	BE08	√	√	9mA	7 (1)
	BED8	√	√	9mA 50kΩ Pull-down	7 (1)
	BEU8	√	√	9mA 50kΩ Pull-up	7 (1)
	BEW8	√	√	9mA 5kΩ Pull-up	7 (1)
	BE07	√	√	12mA	7 (1)
	BED7	√	√	12mA 50kΩ Pull-down	7 (1)
	BEU7	√	√	12mA 50kΩ Pull-up	7 (1)
	BEW7	√	√	12mA 5kΩ Pull-up	7 (1)
	BE09	√	√	18mA	7 (1)
	BED9	√	√	18mA 50kΩ Pull-down	7 (1)
	BEU9	√	√	18mA 50kΩ Pull-up	7 (1)
	BEW9	√	√	18mA 5kΩ Pull-up	7 (1)
	BE0H	√	√	24mA	7 (1)
	BEDH	√	√	24mA 50kΩ Pull-down	7 (1)
	BEUH	√	√	24mA 50kΩ Pull-up	7 (1)
	BEWH	√	√	24mA 5kΩ Pull-up	7 (1)
N-ch Open drain Buffer	EXT1	√	√	9mA	4 (1)
	EXT3	√	√	9mA 50kΩ Pull-up	4 (1)
	EXW3	√	√	9mA 5kΩ Pull-up	4 (1)
	EXT9	√	√	12mA	4 (1)
	EXTB	√	√	12mA 50kΩ Pull-up	4 (1)
	EXWB	√	√	12mA 5kΩ Pull-up	4 (1)
	EXT5	√	√	18mA	4 (1)
	EXT7	√	√	18mA 50kΩ Pull-up	4 (1)
	EXW7	√	√	18mA 5kΩ Pull-up	4 (1)
	EXTD	√	√	24mA	4 (1)
	EXTF	√	√	24mA 50kΩ Pull-up	4 (1)
	EXWF	√	√	24mA 5kΩ Pull-up	4 (1)
N-ch Open drain Buffer with Failsafe	EXO1	√	√	9mA	4 (1)
	EXO9	√	√	12mA	4 (1)
	EXO5	√	√	18mA	4 (1)
	EXOD	√	√	24mA	4 (1)

Function	Block	5.0 V	3.3 V	Description	Cells (I/O)
N-ch Open drain I/O Buffer with Failsafe	EBA1	√	√	9mA	7 (1)
	EBA9	√	√	12mA	7 (1)
	EBA5	√	√	18mA	7 (1)
	EBAD	√	√	24mA	7 (1)
N-ch Open drain Schmitt I/O Buffer with Failsafe	EBE1W	√	√	9mA	10 (1)
	EBE9W	√	√	12mA	10 (1)
	EBE5W	√	√	18mA	10 (1)
	EBEDW	√	√	24mA	10 (1)
I/O Buffer	B00U	√	√	3mA	10 (1)
	B0DU	√	√	3mA 50kΩ Pull-down	10 (1)
	B0UU	√	√	3mA 50kΩ Pull-up	10 (1)
	B0WU	√	√	3mA 5kΩ Pull-up	10 (1)
	B00C	√	√	6mA	10 (1)
	B0DC	√	√	6mA 50kΩ Pull-down	10 (1)
	B0UC	√	√	6mA 50kΩ Pull-up	10 (1)
	B0WC	√	√	6mA 5kΩ Pull-up	10 (1)
	B003	√	√	9mA	10 (1)
	B0D3	√	√	9mA 50kΩ Pull-down	10 (1)
	B0U3	√	√	9mA 50kΩ Pull-up	10 (1)
	B0W3	√	√	9mA 5kΩ Pull-up	10 (1)
	B001	√	√	12mA	20 (1)
	B0D1	√	√	12mA 50kΩ Pull-down	20 (1)
	B0U1	√	√	12mA 50kΩ Pull-up	20 (1)
	B0W1	√	√	12mA 5kΩ Pull-up	20 (1)
	B005	√	√	18mA	20 (1)
	B0D5	√	√	18mA 50kΩ Pull-down	20 (1)
	B0U5	√	√	18mA 50kΩ Pull-up	20 (1)
	B0W5	√	√	18mA 5kΩ Pull-up	20 (1)
	B00F	√	√	24mA	20 (1)
	B0DF	√	√	24mA 50kΩ Pull-down	20 (1)
	B0UF	√	√	24mA 50kΩ Pull-up	20 (1)
	B0WF	√	√	24mA 5kΩ Pull-up	20 (1)

Function	Block	5.0 V	3.3 V	Description	Cells (I/O)
Low-noise I/O Buffer	BE0U	√	√	3mA	10 (1)
	BEDU	√	√	3mA 50kΩ Pull-down	10 (1)
	BEUU	√	√	3mA 50kΩ Pull-up	10 (1)
	BEWU	√	√	3mA 5kΩ Pull-up	10 (1)
	BE0C	√	√	6mA	10 (1)
	BEDC	√	√	6mA 50kΩ Pull-down	10 (1)
	BEUC	√	√	6mA 50kΩ Pull-up	10 (1)
	BEWC	√	√	6mA 5kΩ Pull-up	10 (1)
	BE03	√	√	9mA	10 (1)
	BED3	√	√	9mA 50kΩ Pull-down	10 (1)
	BEU3	√	√	9mA 50kΩ Pull-up	10 (1)
	BEW3	√	√	9mA 5kΩ Pull-up	10 (1)
	BE01	√	√	12mA	10 (1)
	BED1	√	√	12mA 50kΩ Pull-down	10 (1)
	BEU1	√	√	12mA 50kΩ Pull-up	10 (1)
	BEW1	√	√	12mA 5kΩ Pull-up	10 (1)
	BE05	√	√	18mA	10 (1)
	BED5	√	√	18mA 50kΩ Pull-down	10 (1)
	BEU5	√	√	18mA 50kΩ Pull-up	10 (1)
	BEW5	√	√	18mA 5kΩ Pull-up	10 (1)
	BE0F	√	√	24mA	10 (1)
	BEDF	√	√	24mA 50kΩ Pull-down	10 (1)
	BEUF	√	√	24mA 50kΩ Pull-up	10 (1)
	BEWF	√	√	24mA 5kΩ Pull-up	10 (1)

Function	Block	5.0 V	3.3 V	Description	Cells (I/O)
Schmitt I/O Buffer	BSIUW	√	√	3mA	13 (1)
	BSDUW	√	√	3mA 50kΩ Pull-down	13 (1)
	BSUUW	√	√	3mA 50kΩ Pull-up	13 (1)
	BSWUW	√	√	3mA 5kΩ Pull-up	13 (1)
	BSICW	√	√	6mA	13 (1)
	BSDCW	√	√	6mA 50kΩ Pull-down	13 (1)
	BSUCW	√	√	6mA 50kΩ Pull-up	13 (1)
	BSWCW	√	√	6mA 5kΩ Pull-up	13 (1)
	BSI3W	√	√	9mA	13 (1)
	BSD3W	√	√	9mA 50kΩ Pull-down	13 (1)
	BSU3W	√	√	9mA 50kΩ Pull-up	13 (1)
	BSW3W	√	√	9mA 5kΩ Pull-up	13 (1)
	BSI1W	√	√	12mA	23 (1)
	BSD1W	√	√	12mA 50kΩ Pull-down	23 (1)
	BSU1W	√	√	12mA 50kΩ Pull-up	23 (1)
	BSW1W	√	√	12mA 5kΩ Pull-up	23 (1)
	BSI5W	√	√	18mA	23 (1)
	BSD5W	√	√	18mA 50kΩ Pull-down	23 (1)
	BSU5W	√	√	18mA 50kΩ Pull-up	23 (1)
	BSW5W	√	√	18mA 5kΩ Pull-up	23 (1)
	BSIFW	√	√	24mA	23 (1)
	BSDFW	√	√	24mA 50kΩ Pull-down	23 (1)
	BSUFW	√	√	24mA 50kΩ Pull-up	23 (1)
	BSWFW	√	√	24mA 5kΩ Pull-up	23 (1)

Function	Block	5.0 V	3.3 V	Description	Cells (I/O)
Low-noise Schmitt I/O Buffer	BFIUW	√	√	3mA	13 (1)
	BFDUW	√	√	3mA 50kΩ Pull-down	13 (1)
	BFUUW	√	√	3mA 50kΩ Pull-up	13 (1)
	BFWUW	√	√	3mA 5kΩ Pull-up	13 (1)
	BFICW	√	√	6mA	13 (1)
	BFDCW	√	√	6mA 50kΩ Pull-down	13 (1)
	BFUCW	√	√	6mA 50kΩ Pull-up	13 (1)
	BFWCW	√	√	6mA 5kΩ Pull-up	13 (1)
	BFI3W	√	√	9mA	13 (1)
	BFD3W	√	√	9mA 50kΩ Pull-down	13 (1)
	BFU3W	√	√	9mA 50kΩ Pull-up	13 (1)
	BFW3W	√	√	9mA 5kΩ Pull-up	13 (1)
	BFI1W	√	√	12mA	13 (1)
	BFD1W	√	√	12mA 50kΩ Pull-down	13 (1)
	BFU1W	√	√	12mA 50kΩ Pull-up	13 (1)
	BFW1W	√	√	12mA 5kΩ Pull-up	13 (1)
	BFI5W	√	√	18mA	13 (1)
	BFD5W	√	√	18mA 50kΩ Pull-down	13 (1)
	BFU5W	√	√	18mA 50kΩ Pull-up	13 (1)
	BFW5W	√	√	18mA 5kΩ Pull-up	13 (1)
	BFIFW	√	√	24mA	13 (1)
	BFDFW	√	√	24mA 50kΩ Pull-down	13 (1)
	BFUFW	√	√	24mA 50kΩ Pull-up	13 (1)
	BFWFW	√	√	24mA 5kΩ Pull-up	13 (1)
I/O Buffer with EN(AND)	BN2U	√	√	3mA	13 (1)
	BN4U	√	√	3mA 50kΩ Pull-down	13 (1)
	BN2C	√	√	6mA	13 (1)
	BN4C	√	√	6mA 50kΩ Pull-down	13 (1)
	BN23	√	√	9mA	13 (1)
	BN43	√	√	9mA 50kΩ Pull-down	13 (1)
	BN21	√	√	12mA	23 (1)
	BN41	√	√	12mA 50kΩ Pull-down	23 (1)
	BN25	√	√	18mA	23 (1)
	BN45	√	√	18mA 50kΩ Pull-down	23 (1)
	BN2F	√	√	24mA	23 (1)
	BN4F	√	√	24mA 50kΩ Pull-down	23 (1)

Function	Block	5.0 V	3.3 V	Description	Cells (I/O)
I/O Buffer with EN(OR)	BN3U	√	√	3mA	11 (1)
	BN5U	√	√	3mA 50kΩ Pull-down	11 (1)
	BN3C	√	√	6mA	11 (1)
	BN5C	√	√	6mA 50kΩ Pull-down	11 (1)
	BN33	√	√	9mA	11 (1)
	BN53	√	√	9mA 50kΩ Pull-down	11 (1)
	BN31	√	√	12mA	21 (1)
	BN51	√	√	12mA 50kΩ Pull-down	21 (1)
	BN35	√	√	18mA	21 (1)
	BN55	√	√	18mA 50kΩ Pull-down	21 (1)
	BN3F	√	√	24mA	21 (1)
	BN5F	√	√	24mA 50kΩ Pull-down	21 (1)

E.1.2 TTL Level

Function	Block	5.0 V	3.3 V	Description	Cells (I/O)
Input Buffer	FI02	√	√	—	3 (1)
	FID2	√	√	50kΩ Pull-down	3 (1)
	FIU2	√	√	50kΩ Pull-up	3 (1)
	FIW2	√	√	5kΩ Pull-up	3 (1)
	FIS2W	√	√	Schmitt	6 (1)
	FDS2W	√	√	Schmitt 50kΩ Pull-down	6 (1)
	FUS2W	√	√	Schmitt 50kΩ Pull-up	6 (1)
	FWS2W	√	√	Schmitt 5kΩ Pull-up	6 (1)
Input Buffer with Failsafe	FIA2	√	√	—	3 (1)
	FDA2	√	√	50kΩ Pull-down	3 (1)
	FIE2W	√	√	Schmitt	6 (1)
	FDE2W	√	√	Schmitt 50kΩ Pull-down	6 (1)
Input Buffer with EN(AND)	FN12	√	√	—	7 (1)
	FN22	√	√	50kΩ Pull-down	7 (1)
Input Buffer with EN(OR)	FN14	√	√	—	4 (1)
	FN24	√	√	50kΩ Pull-down	4 (1)

Caution   The TTL-level Schmitt buffer cannot be used when the power supply voltage specification is 3.0 V.

Function	Block	5.0 V	3.3 V	Description	Cells (I/O)
N-ch Open drain I/O Buffer with Failsafe	EBA2	√	√	9mA	7 (1)
	EBAA	√	√	12mA	7 (1)
	EBA6	√	√	18mA	7 (1)
	EBAE	√	√	24mA	7 (1)
N-ch Open drain Schmitt I/O Buffer with Failsafe	EBE2W	√	√	9mA	10 (1)
	EBEAW	√	√	12mA	10 (1)
	EBE6W	√	√	18mA	10 (1)
	EBEEW	√	√	24mA	10 (1)
I/O Buffer	B00V	√	√	3mA	10 (1)
	B0DV	√	√	3mA 50kΩ Pull-down	10 (1)
	B0UV	√	√	3mA 50kΩ Pull-up	10 (1)
	B0WV	√	√	3mA 5kΩ Pull-up	10 (1)
	B00D	√	√	6mA	10 (1)
	B0DD	√	√	6mA 50kΩ Pull-down	10 (1)
	B0UD	√	√	6mA 50kΩ Pull-up	10 (1)
	B0WD	√	√	6mA 5kΩ Pull-up	10 (1)
	B004	√	√	9mA	10 (1)
	B0D4	√	√	9mA 50kΩ Pull-down	10 (1)
	B0U4	√	√	9mA 50kΩ Pull-up	10 (1)
	B0W4	√	√	9mA 5kΩ Pull-up	10 (1)
	B002	√	√	12mA	20 (1)
	B0D2	√	√	12mA 50kΩ Pull-down	20 (1)
	B0U2	√	√	12mA 50kΩ Pull-up	20 (1)
	B0W2	√	√	12mA 5kΩ Pull-up	20 (1)
	B006	√	√	18mA	20 (1)
	B0D6	√	√	18mA 50kΩ Pull-down	20 (1)
	B0U6	√	√	18mA 50kΩ Pull-up	20 (1)
	B0W6	√	√	18mA 5kΩ Pull-up	20 (1)
	B00G	√	√	24mA	20 (1)
	B0DG	√	√	24mA 50kΩ Pull-down	20 (1)
	B0UG	√	√	24mA 50kΩ Pull-up	20 (1)
	B0WG	√	√	24mA 5kΩ Pull-up	20 (1)

Caution   The TTL-level Schmitt buffer cannot be used when the power supply voltage specification is 3.0 V.

Function	Block	5.0 V	3.3 V	Description	Cells (I/O)
Low-noise I/O Buffer	BE0V	√	√	3mA	10 (1)
	BEDV	√	√	3mA 50kΩ Pull-down	10 (1)
	BEUV	√	√	3mA 50kΩ Pull-up	10 (1)
	BEWV	√	√	3mA 5kΩ Pull-up	10 (1)
	BE0D	√	√	6mA	10 (1)
	BEDD	√	√	6mA 50kΩ Pull-down	10 (1)
	BEUD	√	√	6mA 50kΩ Pull-up	10 (1)
	BEWD	√	√	6mA 5kΩ Pull-up	10 (1)
	BE04	√	√	9mA	10 (1)
	BED4	√	√	9mA 50kΩ Pull-down	10 (1)
	BEU4	√	√	9mA 50kΩ Pull-up	10 (1)
	BEW4	√	√	9mA 5kΩ Pull-up	10 (1)
	BE02	√	√	12mA	10 (1)
	BED2	√	√	12mA 50kΩ Pull-down	10 (1)
	BEU2	√	√	12mA 50kΩ Pull-up	10 (1)
	BEW2	√	√	12mA 5kΩ Pull-up	10 (1)
	BE06	√	√	18mA	10 (1)
	BED6	√	√	18mA 50kΩ Pull-down	10 (1)
	BEU6	√	√	18mA 50kΩ Pull-up	10 (1)
	BEW6	√	√	18mA 5kΩ Pull-up	10 (1)
	BE0G	√	√	24mA	10 (1)
	BEDG	√	√	24mA 50kΩ Pull-down	10 (1)
	BEUG	√	√	24mA 50kΩ Pull-up	10 (1)
	BEWG	√	√	24mA 5kΩ Pull-up	10 (1)

Caution   The TTL-level Schmitt buffer cannot be used when the power supply voltage specification is 3.0 V.

Function	Block	5.0 V	3.3 V	Description	Cells (I/O)
Schmitt I/O Buffer	BSIVW	√	√	3mA	13 (1)
	BSDVW	√	√	3mA 50kΩ Pull-down	13 (1)
	BSUVW	√	√	3mA 50kΩ Pull-up	13 (1)
	BSWVW	√	√	3mA 5kΩ Pull-up	13 (1)
	BSIDW	√	√	6mA	13 (1)
	BSDDW	√	√	6mA 50kΩ Pull-down	13 (1)
	BSUDW	√	√	6mA 50kΩ Pull-up	13 (1)
	BSWDW	√	√	6mA 5kΩ Pull-up	13 (1)
	BSI4W	√	√	9mA	13 (1)
	BSD4W	√	√	9mA 50kΩ Pull-down	13 (1)
	BSU4W	√	√	9mA 50kΩ Pull-up	13 (1)
	BSW4W	√	√	9mA 5kΩ Pull-up	13 (1)
	BSI2W	√	√	12mA	23 (1)
	BSD2W	√	√	12mA 50kΩ Pull-down	23 (1)
	BSU2W	√	√	12mA 50kΩ Pull-up	23 (1)
	BSW2W	√	√	12mA 5kΩ Pull-up	23 (1)
	BSI6W	√	√	18mA	23 (1)
	BSD6W	√	√	18mA 50kΩ Pull-down	23 (1)
	BSU6W	√	√	18mA 50kΩ Pull-up	23 (1)
	BSW6W	√	√	18mA 5kΩ Pull-up	23 (1)
	BSIGW	√	√	24mA	23 (1)
	BSDGW	√	√	24mA 50kΩ Pull-down	23 (1)
	BSUGW	√	√	24mA 50kΩ Pull-up	23 (1)
	BSWGW	√	√	24mA 5kΩ Pull-up	23 (1)

Caution   The TTL-level Schmitt buffer cannot be used when the power supply voltage specification is 3.0 V.

Function	Block	5.0 V	3.3 V	Description	Cells (I/O)
Low-noise Schmitt I/O Buffer	BFIVW	√	√	3mA	13 (1)
	BFDVW	√	√	3mA 50kΩ Pull-down	13 (1)
	BFUVW	√	√	3mA 50kΩ Pull-up	13 (1)
	BFWVW	√	√	3mA 5kΩ Pull-up	13 (1)
	BFIDW	√	√	6mA	13 (1)
	BFDDW	√	√	6mA 50kΩ Pull-down	13 (1)
	BFUDW	√	√	6mA 50kΩ Pull-up	13 (1)
	BFWDW	√	√	6mA 5kΩ Pull-up	13 (1)
	BFI4W	√	√	9mA	13 (1)
	BFD4W	√	√	9mA 50kΩ Pull-down	13 (1)
	BFU4W	√	√	9mA 50kΩ Pull-up	13 (1)
	BFW4W	√	√	9mA 5kΩ Pull-up	13 (1)
	BFI2W	√	√	12mA	13 (1)
	BFD2W	√	√	12mA 50kΩ Pull-down	13 (1)
	BFU2W	√	√	12mA 50kΩ Pull-up	13 (1)
	BFW2W	√	√	12mA 5kΩ Pull-up	13 (1)
	BFI6W	√	√	18mA	13 (1)
	BFD6W	√	√	18mA 50kΩ Pull-down	13 (1)
	BFU6W	√	√	18mA 50kΩ Pull-up	13 (1)
	BFW6W	√	√	18mA 5kΩ Pull-up	13 (1)
	BFIGW	√	√	24mA	13 (1)
	BFDGW	√	√	24mA 50kΩ Pull-down	13 (1)
	BFUGW	√	√	24mA 50kΩ Pull-up	13 (1)
	BFWGW	√	√	24mA 5kΩ Pull-up	13 (1)
I/O Buffer with EN(AND)	BN2V	√	√	3mA	14 (1)
	BN4V	√	√	3mA 50kΩ Pull-down	14 (1)
	BN2D	√	√	6mA	14 (1)
	BN4D	√	√	6mA 50kΩ Pull-down	14 (1)
	BN24	√	√	9mA	14 (1)
	BN44	√	√	9mA 50kΩ Pull-down	14 (1)
	BN22	√	√	12mA	24 (1)
	BN42	√	√	12mA 50kΩ Pull-down	24 (1)
	BN26	√	√	18mA	24 (1)
	BN46	√	√	18mA 50kΩ Pull-down	24 (1)
	BN2G	√	√	24mA	24 (1)
	BN4G	√	√	24mA 50kΩ Pull-down	24 (1)

Caution   The TTL-level Schmitt buffer cannot be used when the power supply voltage specification is 3.0 V.

Function	Block	5.0 V	3.3 V	Description	Cells (I/O)
I/O Buffer with EN(OR)	BN3V	√	√	3mA	11 (1)
	BN5V	√	√	3mA 50kΩ Pull-down	11 (1)
	BN3D	√	√	6mA	11 (1)
	BN5D	√	√	6mA 50kΩ Pull-down	11 (1)
	BN34	√	√	9mA	11 (1)
	BN54	√	√	9mA 50kΩ Pull-down	11 (1)
	BN32	√	√	12mA	21 (1)
	BN52	√	√	12mA 50kΩ Pull-down	21 (1)
	BN36	√	√	18mA	21 (1)
	BN56	√	√	18mA 50kΩ Pull-down	21 (1)
	BN3G	√	√	24mA	21 (1)
	BN5G	√	√	24mA 50kΩ Pull-down	21 (1)

Caution   The TTL-level Schmitt buffer cannot be used when the power supply voltage specification is 3.0 V.

E.1.3 Oscillator

Function	Block	5.0 V	3.3 V	Description	Cells (I/O)
Oscillator Input Buffer	OSI1	√	√	—	0 (1)
Oscillator Input Buffer for Enable	OSI2	√	√	—	0 (1)
Oscillator Input Buffer for OSO9	OSI4	√	√	—	0 (1)
Oscillator Output Buffer (Internal Feedback Resistor)	OSO1SW	√	√	—	0 (1)
Oscillator Output Buffer (for Enable Type)	OSO7SW	√	√	—	0 (1)
Oscillator Output Buffer (External Feedback Resistor)	OSO9SW	√	√	—	0 (1)
Oscillator Output Buffer (Internal Feedback Resistor)	OSO1	√	√	—	0 (1)
Oscillator Output Buffer (for Enable Type)	OSO7	√	√	—	0 (1)
Oscillator Output Buffer (External Feedback Resistor)	OSO9	√	√	—	0 (1)

E.2 Function Block

E.2.1 Level Generator

Function	Block	5.0 V	3.3 V	Description	Cells (I/O)
H,L Level Generator	F091	√	√	—	1 (—)

E.2.2 Inverter, Buffer, CTS Driver, Delay Gate

Function	Block	5.0 V	3.3 V	Description	Cells (I/O)
Inverter	L101	√	√	Single Out, Low Power	1 (—)
	F101	√	√	Single Out	1 (—)
	F102	√	√	Single Out, x2-drive	2 (—)
	F143	√	√	Single Out, x3-drive	3 (—)
	F144	√	√	Single Out, x4-drive	4 (—)
	F145	√	√	Single Out, x5-drive	5 (—)
	F146	√	√	Single Out, x6-drive	6 (—)
	F148	√	√	Single Out, x8-drive	12 (—)
Buffer	L111	√	√	Single Out, Low Power	1 (—)
	F111	√	√	Single Out	2 (—)
	F112	√	√	Single Out, x2-drive	3 (—)
	F153	√	√	Single Out, x3-drive	4 (—)
	F154	√	√	Single Out, x4-drive	5 (—)
	F158	√	√	Single Out, x8-drive	11 (—)
CTS Driver (Inverter Type)	FC42	√	√	Single type	132 (—)
	FC82	√	√	Single type, x2-drive	396 (—)
	FC44	√	√	Double type	340 (—)
	FC84	√	√	Double type, x2-drive	1020 (—)
Delay Gate	F131	√	√	—	6 (—)
	F132	√	√	—	10 (—)

E.2.3 OR(NOR)

Function	Block	5.0 V	3.3 V	Description	Cells (I/O)
2-Input NOR	L202	√	√	Low Power	1 (—)
	F202	√	√	—	2 (—)
	F222	√	√	x2-drive	4 (—)
	F282	√	√	x4-drive	6 (—)
3-Input NOR	L203	√		Low Power	2 (—)
	F203	√	√	—	3 (—)
	F223	√	√	x2-drive	6 (—)
4-Input NOR	L204	√		Low Power	2 (—)
	F204	√	√	—	4 (—)
5-Input NOR	L205	√	√	Low Power	4 (—)
	F205	√	√	—	5 (—)
	F225	√	√	x2-drive	6 (—)
6-Input NOR	F206	√	√	—	5 (—)
	F226	√	√	x2-drive	6 (—)
8-Input NOR	L208	√	√	Low Power	7 (—)
	F208	√	√	—	7 (—)
	F228	√	√	x2-drive	8 (—)
2-Input OR	L212	√	√	Low Power	2 (—)
	F212	√	√	—	2 (—)
	F232	√	√	x2-drive	3 (—)
	F252	√	√	x4-drive	6 (—)
3-Input OR	L213	√	√	Low Power	2 (—)
	F213	√	√	—	3 (—)
	F233	√	√	x2-drive	4 (—)
4-Input OR	L214	√	√	Low Power	3 (—)
	F214	√	√	—	3 (—)
	F234	√	√	x2-drive	4 (—)
5-Input OR	L215	√	√	Low Power	4 (—)
	F215	√	√	—	5 (—)
	F235	√	√	x2-drive	7 (—)
6-Input OR	L216	√	√	Low Power	4 (—)
	F216	√	√	—	5 (—)
	F236	√	√	x2-drive	7 (—)
8-Input OR	L218	√	√	Low Power	6 (—)
	F218	√	√	—	8 (—)
	F238	√	√	x2-drive	9 (—)

E.2.4 AND(NAND)

Function	Block	5.0 V	3.3 V	Description	Cells (I/O)
2-Input NAND	L302	√	√	Low Power	1 (—)
	F302	√	√	—	2 (—)
	F322	√	√	x2-drive	4 (—)
	F382	√	√	x4-drive	6 (—)
3-Input NAND	L303	√	√	Low Power	2 (—)
	F303	√	√	—	3 (—)
	F323	√	√	x2-drive	6 (—)
4-Input NAND	L304	√	√	Low Power	2 (—)
	F304	√	√	—	4 (—)
	F324	√	√	x2-drive	8 (—)
5-Input NAND	F305	√	√	—	5 (—)
	F325	√	√	x2-drive	6 (—)
6-Input NAND	F306	√	√	—	5 (—)
	F326	√	√	x2-drive	6 (—)
8-Input NAND	F308	√	√	—	6 (—)
	F328	√	√	x2-drive	7 (—)
2-Input AND	L312	√	√	Low Power	2 (—)
	F312	√	√	—	2 (—)
	F332	√	√	x2-drive	3 (—)
	F352	√	√	x4-drive	6 (—)
3-Input AND	L313	√	√	Low Power	2 (—)
	F313	√	√	—	3 (—)
	F333	√	√	x2-drive	4 (—)
4-Input AND	L314	√	√	Low Power	3 (—)
	F314	√	√	—	3 (—)
	F334	√	√	x2-drive	4 (—)
5-Input AND	L315	√	√	Low Power	4 (—)
	F315	√	√	—	5 (—)
	F335	√	√	x2-drive	7 (—)
6-Input AND	L316	√	√	Low Power	4 (—)
	F316	√	√	—	5 (—)
	F336	√	√	x2-drive	7 (—)
8-Input AND	L318	√	√	Low Power	5 (—)
	F318	√	√	—	6 (—)
	F338	√	√	x2-drive	8 (—)

E.2.5 AND-NOR

Function	Block	5.0 V	3.3 V	Description	Cells (I/O)
1-2-Input AND-NOR	L421	√	√	Low Power	2 (—)
	F421	√	√	—	3 (—)
1-1-2-Input AND-NOR	L422	√		Low Power	2 (—)
	F422	√	√	—	4 (—)
1-3-Input AND-NOR	L423	√	√	Low Power	2 (—)
	F423	√	√	—	4 (—)
2-2-Input AND-NOR	L424	√	√	Low Power	2 (—)
	F424	√	√	—	4 (—)
2-2-2-Input AND-NOR	L425	√		Low Power	3 (—)
	F425	√		—	6 (—)
2-3-Input AND-NOR	L427	√		Low Power	3 (—)
	F427	√	√	—	5 (—)
1-2-2-Input AND-NOR	L428	√		Low Power	3 (—)
	F428	√	√	—	5 (—)
2-2-2-2-Input AND-NOR	L429	√	√	Low Power	6 (—)
	F429	√	√	—	6 (—)
1-4-Input AND-NOR	L440	√		Low Power	3 (—)
	F440	√	√	—	5 (—)
1-5-Input AND-NOR	L441	√	√	Low Power	5 (—)
	F441	√	√	—	7 (—)
4-4-4-Input AND-NOR	L444	√	√	Low Power	8 (—)
	F444	√	√	—	8 (—)
1-1-1-2-Input AND-NOR	L446	√	√	Low Power	4 (—)
	F446	√	√	—	5 (—)
1-1-1-3-Input AND-NOR	L447	√	√	Low Power	5 (—)
	F447	√	√	—	5 (—)
1-1-2-2-Input AND-NOR	L448	√	√	Low Power	5 (—)
	F448	√	√	—	5 (—)
3-3-3-3-Input AND-NOR	F449	√	√	—	8 (—)
3-3-3-Input AND-NOR	L460	√	√	Low Power	6 (—)
	F460	√	√	—	7 (—)
1-2-3-Input AND-NOR	F462	√		—	6 (—)
1-1-3-Input AND-NOR	L463	√		Low Power	3 (—)
	F463	√		—	5 (—)
1-1-4-Input AND-NOR	L464	√	√	Low Power	5 (—)
	F464	√	√	—	5 (—)
1-1-1-1-2-Input AND-NOR	F465	√	√	—	5 (—)
4-4-4-4-Input AND-NOR	F466	√	√	—	10 (—)

E.2.6 OR-NAND

Function	Block	5.0 V	3.3 V	Description	Cells (I/O)
1-4-Input OR-NAND	L430	√	√	Low Power	4 (—)
	F430	√	√	—	5 (—)
1-2-Input OR-NAND	L431	√	√	Low Power	2 (—)
	F431	√	√	—	3 (—)
1-1-2-Input OR-NAND	L432	√	√	Low Power	2 (—)
	F432	√	√	—	4 (—)
1-3-Input OR-NAND	L433	√		Low Power	2 (—)
	F433	√	√	—	4 (—)
2-2-Input OR-NAND	L434	√		Low Power	2 (—)
	F434	√	√	—	4 (—)
2-3-Input OR-NAND	F435	√		—	5 (—)
3-3-Input OR-NAND	L436	√		Low Power	3 (—)
	F436	√		—	6 (—)
1-2-2-Input OR-NAND	F437	√		—	5 (—)
2-2-2-Input OR-NAND	F438	√		—	6 (—)
1-5-Input OR-NAND	L439	√	√	Low Power	5 (—)
	F439	√	√	—	6 (—)
2-4-Input OR-NAND	L450	√	√	Low Power	5 (—)
	F450	√	√	—	6 (—)
4-4-Input OR-NAND	L451	√	√	Low Power	7 (—)
	F451	√	√	—	8 (—)
1-1-3-Input OR-NAND	L452	√	√	Low Power	4 (—)
	F452	√	√	—	5 (—)
1-1-4-Input OR-NAND	L453	√	√	Low Power	5 (—)
	F453	√	√	—	6 (—)
4-4-4-Input OR-NAND	F457	√	√	—	10 (—)
1-1-1-2-Input OR-NAND	L458	√		Low Power	3 (—)
	F458	√	√	—	5 (—)
1-1-1-3-Input OR-NAND	L459	√	√	Low Power	5 (—)
	F459	√	√	—	5 (—)
1-1-1-1-2-Input OR-NAND	F490	√	√	—	5 (—)
1-2-3-Input OR-NAND	L491	√	√	Low Power	5 (—)
	F491	√	√	—	5 (—)
3-3-3-Input OR-NAND	L493	√	√	Low Power	6 (—)
	F493	√	√	—	7 (—)
1-1-2-2-Input OR-NAND	F495	√		—	6 (—)
3-3-3-3-Input OR-NAND	F496	√	√	—	8 (—)
4-4-4-4-Input OR-NAND	F498	√	√	—	14 (—)

E.2.7 Exclusive OR, Exclusive NOR

Function	Block	5.0 V	3.3 V	Description	Cells (I/O)
2-Input Exclusive OR	L511	√	√	Low Power	3 (—)
	F511	√	√	—	4 (—)
3-Input Exclusive OR	L516	√	√	Low Power	6 (—)
	F516	√	√	—	7 (—)
2-Input Exclusive NOR	L512	√	√	Low Power	3 (—)
	F512	√	√	—	4 (—)
3-Input Exclusive NOR	L517	√	√	Low Power	7 (—)
	F517	√	√	—	7 (—)

E.2.8 Adder, 3-State Buffer, Decoder, Multiplexer, Generator

Function	Block	5.0 V	3.3 V	Description	Cells (I/O)
1-Bit Full Adder	F521	√	√	—	9 (—)
4-Bit Full Adder	F523	√	√	—	32 (—)
4-Bit Look Ahead Carry Generator	F526	√	√	—	34 (—)
4-Bit Carry Look Ahead Adder	F527	√	√	—	69 (—)
3-State Buffer	L531	√	√	with EN, Low Power	4 (—)
	F531	√	√	with EN	5 (—)
	F533	√	√	with EN, x2-drive	7 (—)
	F53F	√	√	with EN, x4-drive	11 (—)
	L532	√	√	with ENB, Low Power	4 (—)
	F532	√	√	with ENB	5 (—)
	F534	√	√	with ENB, x2-drive	7 (—)
	F53G	√	√	with ENB, x4-drive	11 (—)
	F541	√	√	Inverter with EN	6 (—)
	F543	√	√	Inverter with EN, x2-drive	8 (—)
	F54F	√	√	Inverter with EN, x4-drive	12 (—)
	F542	√	√	Inverter with ENB	6 (—)
	F544	√	√	Inverter with ENB, x2-drive	8 (—)
	F54G	√	√	Inverter with ENB, x4-drive	12 (—)
2 to 4 Decoder	L560	√	√	Positive Out, Low Power	6 (—)
	F560	√	√	Positive Out	10 (—)
	L561	√	√	Negative Out, Low Power	6 (—)
	F561	√	√	Negative Out	10 (—)
2 to 1 Multiplexer (Positive Out)	L565	√	√	Low Power	3 (—)
	F565	√	√	—	4 (—)
	L571	√	√	with ENB, Low Power	4 (—)
	F571	√	√	with ENB	6 (—)
4 to 1 Multiplexer (Positive Out)	F564	√	√	—	8 (—)
	F570	√	√	with ENB	10 (—)
8 to 1 Multiplexer (Positive Out)	F563	√	√	—	18 (—)
	F569	√	√	with ENB	18 (—)
Quad 2 to 1 Multiplexer (Negative Out)	L572	√	√	with ENB, Low Power	15 (—)
	F572	√	√	with ENB	17 (—)
8-Bit Odd Parity Generator	F581	√	√	—	19 (—)
8-Bit Even Parity Generator	F582	√	√	—	19 (—)

E.2.9 RS-Latch, RS-F/F

Function	Block	5.0 V	3.3 V	Description	Cells (I/O)
RS-Latch	F595	√	√	—	5 (—)
RS-F/F with R,S	F596	√	√	—	11 (—)

E.2.10 D-Latch

Function	Block	5.0 V	3.3 V	Description	Cells (I/O)
D-Latch	F601	√	√	—	6 (—)
	L601	√	√	Q Out, Low Power	4 (—)
	F601NQ	√	√	Q Out	5 (—)
	F601NB	√	√	QB Out	5 (—)
D-Latch, High Speed	F6R1	√	√	—	6 (—)
D-Latch with R	F602	√	√	—	6 (—)
	L602	√	√	Q Out, Low Power	5 (—)
	F602NQ	√	√	Q Out	6 (—)
	F602NB	√	√	QB Out	5 (—)
D-Latch with R, High Speed	F6R2	√	√	—	7 (—)
D-Latch with RB	F603	√	√	—	7 (—)
	L603	√	√	Q Out, Low Power	5 (—)
	F603NQ	√	√	Q Out	5 (—)
	F603NB	√	√	QB Out	6 (—)
D-Latch with RB, High Speed	F6R5	√	√	—	6 (—)
D-Latch with SB	F60K	√	√	—	7 (—)
	F60KNQ	√	√	Q Out	6 (—)
	F60KNB	√	√	QB Out	5 (—)
D-Latch with RB,SB	F60J	√	√	—	7 (—)
	F60JNQ	√	√	Q Out	6 (—)
	F60JNB	√	√	QB Out	6 (—)
D-Latch (GB)	F604	√	√	—	6 (—)
	L604	√	√	Q Out, Low Power	4 (—)
	F604NQ	√	√	Q Out	5 (—)
	F604NB	√	√	QB Out	5 (—)
D-Latch (GB), High Speed	F6R8	√	√	—	6 (—)
D-Latch (GB) with RB	F605	√	√	—	7 (—)
	L605	√	√	Q Out, Low Power	5 (—)
	F605NQ	√	√	Q Out	5 (—)
	F605NB	√	√	QB Out	6 (—)
D-Latch (GB) with RB, High Speed	F6R9	√	√	—	6 (—)

E.2.11 D-F/F

Function	Block	5.0 V	3.3 V	Description	Cells (I/O)
D-F/F	F641	√	√	—	8 (—)
	L641	√	√	Q Out, Low Power	6 (—)
	F641NQ	√	√	Q Out	7 (—)
	F641NB	√	√	QB Out	7 (—)
D-F/F with R	F642	√	√	—	9 (—)
	F642NQ	√	√	Q Out	8 (—)
	F642NB	√	√	QB Out	8 (—)
D-F/F with S	F643	√	√	—	9 (—)
	F643NQ	√	√	Q Out	8 (—)
	F643NB	√	√	QB Out	8 (—)
D-F/F with R,S	F644	√	√	—	10 (—)
	L644	√	√	Q Out, Low Power	8 (—)
	F644NQ	√	√	Q Out	9 (—)
	F644NB	√	√	QB Out	9 (—)
D-F/F with RB	F615	√	√	—	9 (—)
	L645	√	√	Q Out, Low Power	7 (—)
	F615NQ	√	√	Q Out	8 (—)
	F615NB	√	√	QB Out	8 (—)
D-F/F with SB	F616	√	√	—	9 (—)
	F616NQ	√	√	Q Out	8 (—)
	F616NB	√	√	QB Out	8 (—)
D-F/F with RB,SB	F647	√	√	—	10 (—)
	L647	√	√	Q Out, Low Power	8 (—)
	F647NQ	√	√	Q Out	9 (—)
	F647NB	√	√	QB Out	9 (—)
D-F/F (CB)	F661	√	√	—	8 (—)
	L661	√	√	Q Out, Low Power	6 (—)
	F661NQ	√	√	Q Out	7 (—)
	F661NB	√	√	QB Out	7 (—)
D-F/F (CB) with RB	F665	√	√	—	9 (—)
	F665NQ	√	√	Q Out	8 (—)
	F665NB	√	√	QB Out	8 (—)
D-F/F (CB) with SB	F666	√	√	—	9 (—)
	F666NQ	√	√	Q Out	8 (—)
	F666NB	√	√	QB Out	8 (—)
D-F/F (CB) with RB,SB	F667	√	√	—	10 (—)
	L667	√	√	Q Out, Low Power	8 (—)
	F667NQ	√	√	Q Out	9 (—)
	F667NB	√	√	QB Out	9 (—)
D-F/F with 2 to 1 Selector	F641S	√	√	—	10 (—)
	F641SQ	√	√	Q Out	9 (—)
	F641SB	√	√	QB Out	9 (—)

Function	Block	5.0 V	3.3 V	Description	Cells (I/O)
D-F/F with R,2 to 1 Selector	F642S	√	√	—	11 (—)
	F642SQ	√	√	Q Out	10 (—)
	F642SB	√	√	QB Out	10 (—)
D-F/F with S,2 to 1 Selector	F643S	√	√	—	11 (—)
	F643SQ	√	√	Q Out	10 (—)
	F643SB	√	√	QB Out	10 (—)
D-F/F with R,S,2 to 1 Selector	F644S	√	√	—	12 (—)
	F644SQ	√	√	Q Out	11 (—)
	F644SB	√	√	QB Out	11 (—)
D-F/F with RB,2 to 1 Selector	F615S	√	√	—	11 (—)
	F615SQ	√	√	Q Out	10 (—)
	F615SB	√	√	QB Out	10 (—)
D-F/F with SB,2 to 1 Selector	F616S	√	√	—	11 (—)
	F616SQ	√	√	Q Out	10 (—)
	F616SB	√	√	QB Out	10 (—)
D-F/F with RB,SB,2 to 1 Selector	F647S	√	√	—	12 (—)
	F647SQ	√	√	Q Out	11 (—)
	F647SB	√	√	QB Out	11 (—)
D-F/F (CB) with 2 to 1 Selector	F661S	√	√	—	10 (—)
	F661SQ	√	√	Q Out	9 (—)
	F661SB	√	√	QB Out	9 (—)
D-F/F (CB) with RB,2 to 1 Selector	F665S	√	√	—	11 (—)
	F665SQ	√	√	Q Out	10 (—)
	F665SB	√	√	QB Out	10 (—)
D-F/F (CB) with SB,2 to 1 Selector	F666S	√	√	—	11 (—)
	F666SQ	√	√	Q Out	10 (—)
	F666SB	√	√	QB Out	10 (—)
D-F/F (CB) with RB,SB,2 to 1 Selector	F667S	√	√	—	12 (—)
	F667SQ	√	√	Q Out	11 (—)
	F667SB	√	√	QB Out	11 (—)
D-F/F with Hold	F641H	√	√	—	10 (—)
	F641HQ	√	√	Q Out	9 (—)
	F641HB	√	√	QB Out	9 (—)
D-F/F with RB,Hold	F615H	√	√	—	11 (—)
	F615HQ	√	√	Q Out	10 (—)
	F615HB	√	√	QB Out	10 (—)
D-F/F with SB,Hold	F616H	√	√	—	11 (—)
	F616HQ	√	√	Q Out	10 (—)
	F616HB	√	√	QB Out	10 (—)
D-F/F with RB,SB,Hold	F647H	√	√	—	12 (—)
	F647HQ	√	√	Q Out	11 (—)
	F647HB	√	√	QB Out	11 (—)
D-F/F (CB) with 2 to 1 Selector(2 CTRL),RB	F673	√	√	—	11 (—)
D-F/F (CB) with Hold,2 to 1 Selector(2 CTRL),RB	F674	√	√	—	12 (—)

E.2.12 T-F/F, JK-F/F

Function	Block	5.0 V	3.3 V	Description	Cells (I/O)
T-F/F with R,S	F744	√	√	—	9 (—)
	L744	√	√	Q Out, Low Power	7 (—)
	F744NQ	√	√	Q Out	8 (—)
T-F/F with RB	F745	√	√	—	8 (—)
	F745NQ	√	√	Q Out	7 (—)
T-F/F with RB,SB	F747	√	√	—	9 (—)
	L747	√	√	Q Out, Low Power	7 (—)
	F747NQ	√	√	Q Out	8 (—)
T-F/F with Data-Hold R,S	F791	√	√	—	12 (—)
T-F/F (TB) with RB	F765	√	√	—	8 (—)
	F765NQ	√	√	Q Out	7 (—)
T-F/F (TB) with RB,SB	F767	√	√	—	9 (—)
	L767	√	√	Q Out, Low Power	7 (—)
	F767NQ	√	√	Q Out	8 (—)
T-F/F (TB) with Data-Hold RB,SB	F792	√	√	—	12 (—)
JK-F/F	F771	√	√	—	10 (—)
	F771NQ	√	√	Q Out	9 (—)
	F771NB	√	√	QB Out	9 (—)
JK-F/F, High Speed	F7D1	√	√	—	10 (—)
JK-F/F with R,S	F774	√	√	—	12 (—)
	F774NQ	√	√	Q Out	11 (—)
	F774NB	√	√	QB Out	11 (—)
JK-F/F with RB	F775	√	√	—	11 (—)
	F775NQ	√	√	Q Out	10 (—)
	F775NB	√	√	QB Out	10 (—)
JK-F/F with SB	F776	√	√	—	11 (—)
	F776NQ	√	√	Q Out	10 (—)
	F776NB	√	√	QB Out	10 (—)
JK-F/F with RB,SB	F777	√	√	—	12 (—)
	F777NQ	√	√	Q Out	11 (—)
	F777NB	√	√	QB Out	11 (—)
JK-F/F (CB)	F781	√	√	—	10 (—)
	F781NQ	√	√	Q Out	9 (—)
	F781NB	√	√	QB Out	9 (—)
JK-F/F (CB), High Speed	F7E1	√	√	—	10 (—)
JK-F/F (CB) with RB,SB	F787	√	√	—	12 (—)
	F787NQ	√	√	Q Out	11 (—)
	F787NB	√	√	QB Out	11 (—)

E.3 Scan Path Block

E.3.1 Standard Type

Function	Block	5.0 V	3.3 V	Description	Cells (I/O)
Scan D-F/F with R,S,2 to 1 Selector	S000	√	√	—	12 (—)
Scan D-F/F with 2 to 1 Selector	S002	√	√	—	10 (—)
Scan D-F/F with 2 to 1 Selector, High Speed	S003	√	√	—	11 (—)
Scan D-F/F with R,S,Hold,2 to 1 Selector	S050	√	√	—	16 (—)
Scan D-F/F with Hold,2 to 1 Selector	S052	√	√	—	14 (—)
Scan JK-F/F with R,S,D-F/F Function	S100	√	√	—	14 (—)
Scan JK-F/F with D-F/F Function	S102	√	√	—	12 (—)
Scan JK-F/F with R,S,Hold,D-F/F Function	S150	√	√	—	18 (—)
Scan JK-F/F with Hold,D-F/F Function	S152	√	√	—	16 (—)
Scan D-Latch with R,D-F/F Function	S201	√	√	—	13 (—)
Scan D-Latch with D-F/F Function	S202	√	√	—	12 (—)
Scan D-Latch with D-F/F Function, High Speed	S204	√	√	—	12 (—)
Scan D-Latch with R,Special Function,R	S301	√	√	—	8 (—)
Scan D-Latch with Special Function	S302	√	√	—	7 (—)
Scan D-Latch with Special Function, High Speed	S303	√	√	—	7 (—)

E.3.2 NEC Scan

Function	Block	5.0 V	3.3 V	Description	Cells (I/O)
NEC Scan D-Latch	SE601	√	√	—	13 (—)
NEC Scan D-Latch with R	SE602	√	√	—	14 (—)
NEC Scan D-Latch with RB	SE603	√	√	—	14 (—)
NEC Scan D-Latch(GB)	SE604	√	√	—	13 (—)
NEC Scan D-Latch(GB) with RB	SE605	√	√	—	14 (—)
NEC Scan D-F/F	SE611	√	√	—	11 (—)
NEC Scan D-F/F with R,S	SE614	√	√	—	13 (—)
NEC Scan D-F/F with RB	SE615	√	√	—	12 (—)
NEC Scan D-F/F with SB	SE616	√	√	—	12 (—)
NEC Scan D-F/F with RB,SB	SE617	√	√	—	13 (—)
NEC Scan D-F/F (CB)	SE631	√	√	—	11 (—)
NEC Scan D-F/F (CB) with RB,SB	SE637	√	√	—	13 (—)

E.3.3 Scan Controller

Function	Block	5.0 V	3.3 V	Description	Cells (I/O)
Clock Distributor	SCD1	√	√	—	8 (—)
Clock Distributor with Test (Positive Clock)	SCDC	√	√	—	2 (—)
Clock Distributor with Test (Negative Clock)	SCDD	√	√	—	2 (—)
I/F Control (AMC) with EN	SFEH	√	√	—	3 (—)
I/F Control (AMC) with ENB	SFEL	√	√	—	2 (—)
I/F Control (SMC) with EN	SOEH	√	√	—	3 (—)
I/F Control (SMC) with ENB	SOEL	√	√	—	2 (—)
Megamacro Skip	SMS1	√	√	—	4 (—)
Set/Reset Control	SRH1	√	√	—	2 (—)
Set-B/Reset-B Control	SRL1	√	√	—	2 (—)
Loop Cut	SRPD	√	√	—	12 (—)
Clock Generator	SCKG	√	√	—	16 (—)
Common Input	SCI1	√	√	—	2 (—)
Common Output	SCO1	√	√	—	4 (—)
GND	SGND	√	√	—	2 (—)

E.4 Boundary Scan Block

E.4.1 TAP Macro

Function	Block	5.0 V	3.3 V	Description	Cells (I/O)
BScan TAP Macro	SBCJ	√	√	—	262 (—)
BScan TAP Macro with NEC Scan	SBCL	√	√	—	315 (—)

E.4.2 Level Generator

Function	Block	5.0 V	3.3 V	Description	Cells (I/O)
BScan Level Generator (CLANP)	SBZ1	√	√	—	1 (—)

E.4.3 Data Register

Function	Block	5.0 V	3.3 V	Description	Cells (I/O)
BScan Data Register for Input	SVRNI2	√	√	—	12 (—)
BScan Data Register for Output	SVRN22	√	√	—	24 (—)
BScan Data Register for 3-state	SVRN32	√	√	—	50 (—)
BScan Data Register for Bid	SVRNB2	√	√	—	57 (—)

E.4.4 D-latch, Selector, Shift Register

Function	Block	5.0 V	3.3 V	Description	Cells (I/O)
BScan D-Latch with SB Q Out, Low Power	L606	√	√	—	5 (—)
BScan Selector	SBD1	√	√	—	4 (—)
BScan Shift Register	SBR1	√	√	—	8 (—)
BScan Data Selector for Output	SVSNA2	√	√	—	7 (—)
BScan Data Selector for Bid	SVSNB2	√	√	—	7 (—)
BScan Data Enable Selector for 3-state	SVSNC2	√	√	—	9 (—)
BScan Data Enable Selector for Bid	SVSNE2	√	√	—	9 (—)

E.4.5 Soft Macro

Function	Block	5.0 V	3.3 V	Description	Cells (I/O)
BScan TAP Controller	SBCK	√	√	—	392 (—)
BScan Instruction Register (Internal Circuit)	SBM4	√	√	—	46 (—)
BScan Instruction Register	SBM5	√	√	—	140 (—)
BScan Instruction Decoder	SBM6	√	√	—	24 (—)
BScan Instruction Decoder with NEC Scan	SBMC	√	√	—	37 (—)
BScan Bypass Register	SBS3	√	√	—	26 (—)

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