NEC

Customer Notification

QB-78K0FX2™

In-Circuit Emulator

Operating Precautions

Target Devices
78K0/Fx2 Series

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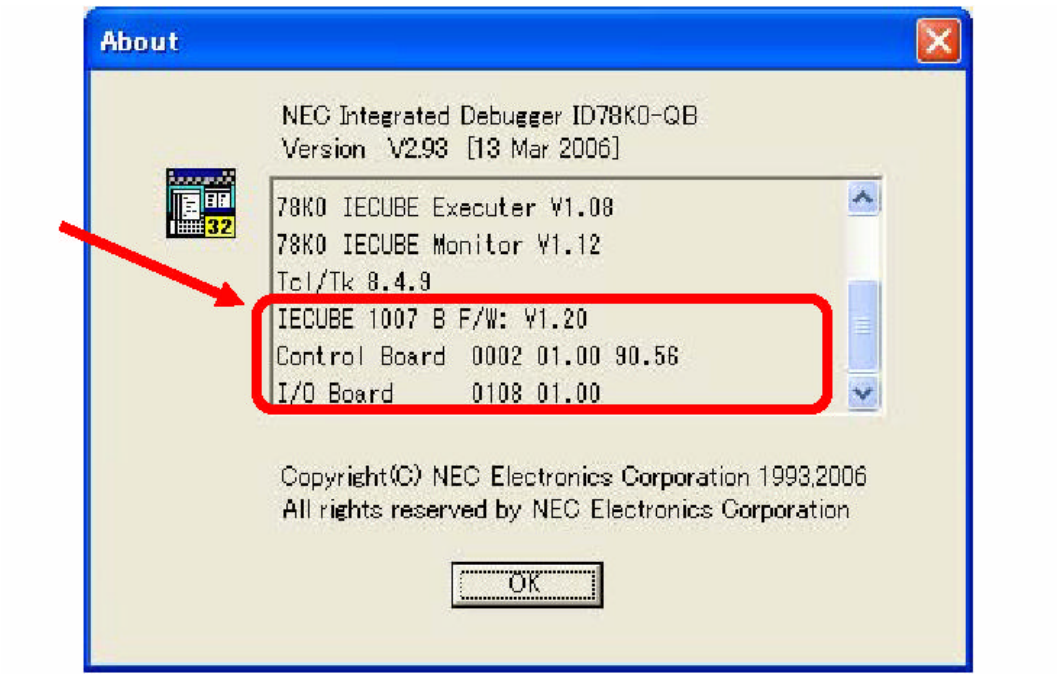
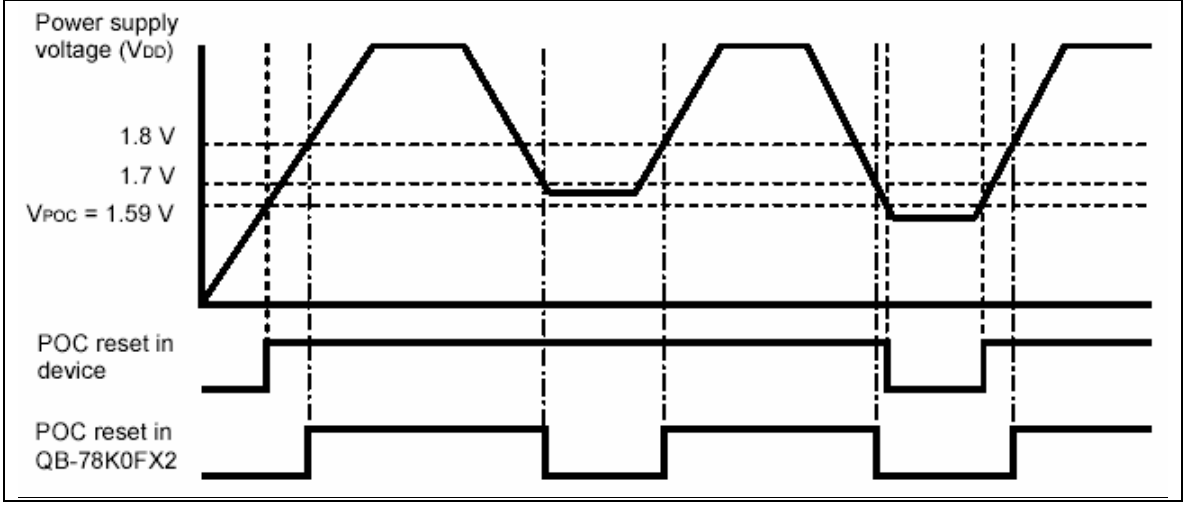
2	Internal ROM area (Technical Limitation)		✗	✓	
3	Caution on target system voltage during break (Direction of Use)		✗	✗	
4	General cautions on product handling (Direction of Use)		✗	✗	

✓ : Not applicable
✗ : applicable

Note:
1. The “control code” is the second digit from the left in the 10-digit serial number in the warranty supplied with the product you purchased (if it has not been upgraded). If the product has been upgraded, a label indicating the new version is attached to the product and the x in V-UP LEVEL x on this label indicates the control code.
2. The control code can be checked by selecting [About] from the [Help] menu when the ID78K0-QB is running. “X” in version information “IECUBE **** X F/W: V*.**” is the control code.



(B) Description of Operating Precautions

No. 1	Power-On-Clear / Low Voltage Indication (Specification Change)
	Details The Power-On-Clear detection voltage differs between the In-Circuit-Emulator QB-78K0FX2-ZZZ-EE and the 78K0/Fx2 Series devices
	78K0/Fx2 Series devices: An internal reset signal is generated, during power up of the application. The reset state is released when the power supply voltage (V_{DD}) exceeds the detection voltage (V_{POC} = 1.59V ± 0.15V). The power supply voltage (V_{DD}) and the detection voltage (V_{POC} = 1.59V ± 0.15V) are compared, an internal reset signal is generated when V_{DD} drops lower than V_{POC} ($V_{DD} < V_{POC}$), and the reset state is released, when V_{DD} becomes V_{POC} or higher ($V_{DD} = V_{POC}$)
	QB-78K0FX2-ZZZ-EE: An internal reset signal is generated, during power up of the application. The reset state is released when the power supply voltage (V_{DD}) exceeds the detection voltage 1.80V. An internal reset signal is generated when V_{DD} drops lower than 1.70V (V_{DD} < 1.70V), and the reset state is released, when V_{DD} becomes 1.80V or higher (V_{DD} = 1.80V)
	

No. 2	Internal ROM area (Technical Limitation)
	Details Data in the internal ROM area may be overwritten, if the Source window or Assemble window is open during program execution. As a result, an unexpected fail-safe break (such as Write Protect Break or Non Map Break) may occur.

No. 3	Caution on target system voltage during break (Direction of Use)
	Details Do not decrease the target system voltage during a break. If a reset by LVI or POC occurs during a break, the debugger operation may become illegal or a communication error may occur.

No. 4	General cautions on product handling (Direction of Use)

Details

a. Circumstances not covered by product guarantee

- If the product was disassembled, altered, or repaired by the customer
- If it was dropped, broken, or given another strong shock
- Use at overvoltage, use outside guaranteed temperature range, storing outside guaranteed temperature range
- If power was turned on while the AC adapter, interface cable, or target system connection was in an unsatisfactory state
- If the AC adapter cable, interface cable, emulation probe, or the like was bent or pulled excessively
- If an AC adapter other than the one supplied with the product is used
- If the product got wet
- If the product and target system were connected while a potential difference existed between the GND of the product and the GND of the target system
- If a connector or cable was removed while the power was being supplied to the product
- If an excessive load was placed on a connector or socket

b. Safety precautions

- If used for a long time, the product may become hot (50°C to 60°C). Be careful of low temperature burns and other dangers due to the product becoming hot.
- Be careful of electrical shock. There is a danger of electrical shock if the product is used as described above in **a. Circumstances not covered by product guarantee.**

No. 5	AFCAN Sleep Mode Wakeup (Specification Change)

1. Description

When the AFCAN macro is set into SLEEP mode, it can be waken up by CAN bus activity.
This waking up is asynchronous to the operation of the macro and the CPU. By configuration setting, a WAKEUP interrupt can be generated by the AFCAN macro on the wakeup event.
While the interrupt is generated asynchronously, the AFCAN macro may need another dominant edge on the CAN bus, or software clearing of the SLEEP mode, in order to restart its synchronous operation.
During the time, after the interrupt already has been indicated, and before the CAN macro has restarted its synchronous operation, the registers of the AFCAN macro will not operate, because the AFCAN macro still remains in SLEEP mode. This time we will refer to as “wakeup dead time” in the following context.
To resolve from the wakeup dead time, software and/or hardware measures are required.

2. Exclusions

This Operating Precaution is **only applicable** to applications, which are fulfilling at least one of the following three conditions:

- SLEEP Mode of AFCAN is used **and** the possibility to wake up AFCAN by CAN-Bus events is given (see remark 1 below).
- During SLEEP mode of the AFCAN macro, a CAN-Bus wakeup condition occurs, while the AFCAN macro is supplied with clock (see remark 2 below) **and**
  - after waking up from SLEEP mode of the AFCAN macro, the application software does not wait until the SLEEP mode is released by polling the CnCTRL (PSMODE) register, before continuing operation with the AFCAN macro (see remark 3 below) and
  - the CPU can reach instructions, where AFCAN registers are accessed while the AFCAN macro is still in SLEEP mode, due to the missing waiting condition.
- During SLEEP mode of the AFCAN macro, a CAN-Bus wakeup condition occurs, while the AFCAN macro is supplied with clock (see remark 2 below) **and**
  1. after waking up from SLEEP mode of the AFCAN macro, the CAN Bus Transceiver generates a **long-lasting or permanent dominant level** to the CRXD input of the AFCAN macro, instead of the propagated CAN-Bus level.

Remarks:

1. If the CAN-Bus Transceiver does not propagate the CAN-Bus signal, while the AFCAN macro is in SLEEP mode, and also does not forward a wakeup signal to CRXD, **this Operating Precaution is not applicable**.
2. The clock supply to the AFCAN macro can be stopped, depending on the features of the device, and the system design of the application. If the clock supply to the AFCAN macro is stopped, while a wakeup condition occurs, **this Operating Precaution is not applicable.**
3. The maximum waiting time for this loop can be up to 10 bits of the CAN-Bus Baudrate. Waiting while retrying to clear CnINTS (Bit 5) can be used alternatively.

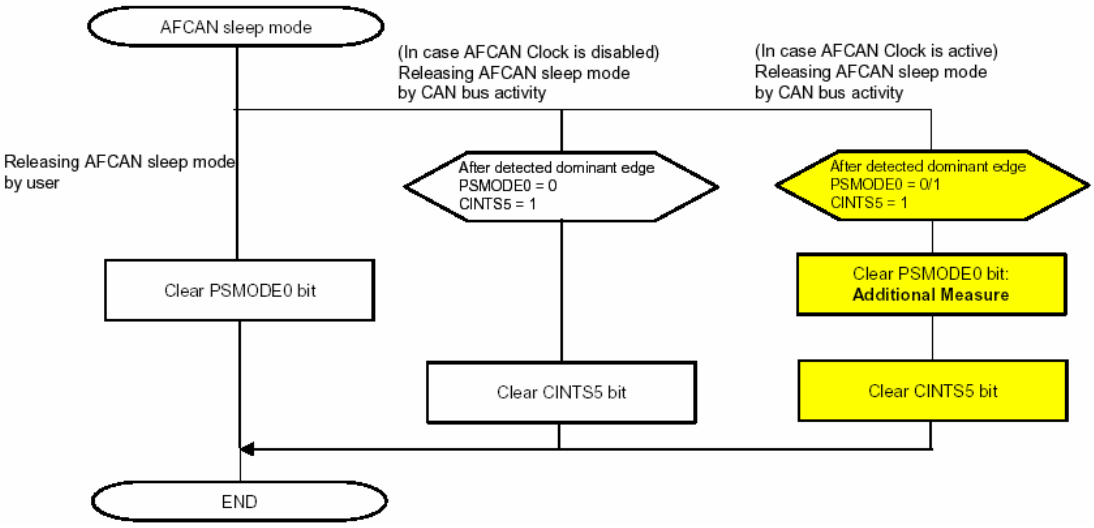
All other applications are not affected by this Operating Precaution.

3. Application Dependency

3.1 Overview

The following flowchart illustrates, how and whether additional measures have to be taken in software, to avoid the wakeup dead time.

Figure: Additional Measures in case AFCAN clock is active when waking up



3.2 Not affected Applications

3.2.1 Applications not using SLEEP mode

If SLEEP mode is not used, **this Operating Precaution is not applicable.**

3.2.2 Applications waking up from SLEEP mode by User Request only

If there is no condition, when SLEEP mode can be left by CAN-Bus activity, but only on User Request (by clearing the PSMODE flag by software), **this Operating Precaution is not applicable**.

3.2.3 Applications using a CPU Power Save Mode

If the clock to the AFCAN macro is disabled, while it is waken up from SLEEP mode, **this Operating Precaution is not applicable**.
This means, if the user selects a power save mode of the target device, which switches off the clock of the AFCAN macro, immediately after it had been set into SLEEP mode, like the CPU STOP mode, the precaution needs not to be considered.
This is associated with the software improvement hints below.

3.3 Affected Applications

3.3.1 Applications not waiting until SLEEP mode is left

If bus transceivers are used in conjunction with AFCAN, which will propagate the CAN bus signal to AFCAN permanently (not switched off or not in power saving modes), or, if bus transceivers are used in conjunction with AFCAN, which will propagate the unmodified CAN-Bus signal when waking up from a power save mode, the wakeup dead time lasts from the first recessive-to-dominant edge of the CAN-Bus signal, which generates the wake-up, until the next recessive-to-dominant edge of the CAN-Bus signal.
The worst case (maximum length) of the wakeup dead time, is given by the CAN bus speed and the rule of the CAN bus about the frequency of recessive-to-dominant edges. Given by the stuffing rule, at least every 10 bits, a recessive-to-dominant edge must occur.
If during the wakeup dead time, the CPU waits until the SLEEP mode is indicated to be cleared (either by polling the PSMODE flag, or by retrying to clear CnINTS[5]), **this Operating Precaution is not applicable**. In this case, the improvement hint according to 4.2.2 is followed implicitly. If during the wakeup dead time, the CPU does not perform any access to the AFCAN macro in any case, **this Operating Precaution is not applicable**.

3.3.2 Applications using Bus Transceivers generating long-lasting dominant CAN-Bus Signals

If bus transceivers are used in conjunction with AFCAN, which *generate a permanent or long-lasting dominant level* when waking up from a power save mode, the Operating Precaution must be considered in any case.
In this case, the wakeup dead time lasts from the first recessive-to-dominant edge of the CAN bus signal, which generates the wake-up, until the next recessive-to-dominant edge of the CAN bus signal, depending on the behaviour of the CAN bus transceiver.
If no further dominant edge on the CAN bus occurs (in case of some CAN transceivers, which only provide one single edge on waking up), the time until SLEEP mode is left may become endless. Therefore, the waking up procedure of AFCAN regarding software, must be adjusted according to 4.1.1.

4. Software Improvement Hints

4.1 Recommended WAKEUP Handling by Software

4.1.1 Clearing the SLEEP Mode by Software

Within the WAKEUP interrupt routine, before accessing any other register or area of AFCAN, the SLEEP mode can be canceled by software, followed by a clearance of the WAKEUP interrupt flag.
Doing so, the AFCAN macro will start its synchronous operation right after these accesses. In the following C-code example, replace the objects in “<>” brackets by the hardware locations within your implementation. Use the appropriate access types, as described in the User’s Manual.

```
WAKEUP INTERRUPT VECTOR -->
                                <CnCTRL_PSMODE> = 0;        /* Clear SLEEP Mode */
                                <CnINTS_CINTS5> = 1;/* Clear INTS5 */
                                ...
                                /* following other parts of interrupt routine */
                                ...
```

Remark: Clearing INTS5 is required to get another WAKEUP interrupt anyway, by specification.

4.2 Other WAKEUP Handling Hints

4.2.1 Switching off the Clock Supply to AFCAN, while in SLEEP Mode

If the clock supply to the AFCAN macro is stopped, while it is in SLEEP mode, the synchronization of the WAKEUP works without any restriction. To achieve this, the documentation of clock controlling unit of the target device should be consulted. Usually this is performed by setting the STOP mode of the CPU of the target device.
However, the user has to consider, that there must not be any WAKEUP condition (dominant level on the CAN-Bus), while the software is executing between setting SLEEP mode and stopping the AFCAN clock.

4.2.2 Using a Waiting Loop within the WAKEUP interrupt routine

Within the WAKEUP interrupt routine, create a waiting loop, which tests the capability of clearing the WAKEUP interrupt flag within AFCAN, by checking the actual power save mode.
In the following C-code example, replace the objects in "<>" brackets by the hardware locations within your implementation. Use the appropriate access types, as described in the User's Manual.

```
do
{
        AFCAN_SleepStatus = <CnCTRL_PSMODE>
        if( AFCAN_SleepStatus != 0 )
        {
                /* macro is still in SLEEP mode (waiting for latency time) */
                <CnINTS_CINTS5> = 1;/* repeated trying to clear CINTS5 */
        }
} while( AFCAN_SleepStatus != 0 );
```

This improvement hint **cannot be applied**, if a CAN-Bus-Transceiver is attached to AFCAN, which generates a permanent or long-lasting dominant level to the FCRXDn receive input pin, if a wakeup condition occurs. Missing another dominant edge on the bus, the synchronisation will not happen, and the loop could run endlessly.

4.2.3 Using INIT Mode instead of SLEEP Mode

In this case, the waking up by CAN-bus activity must be performed via another free external interrupt. The CAN receive signal must be distributed on the FCRXDn pin, and to another external interrupt pin in parallel.
Using this external interrupt, the AFCAN macro can be restored into the previous operation mode. This implementation will not use the SLEEP mode of AFCAN at all, and use the INIT mode instead.

(C) Valid Specification

Item	Date published	Document No.	Document Title
1	July 15th, 2005 or later	U17669EJ1V0UM00 or later	User's Manual

(D) Revision History

Item	Date published	Document No.	Comment
1	September 5th, 2005	TPS-LE-OP-0TQBFX2 (U18093EE1V0IF00)	1st Release
2	August 24th, 2006	U18093EE2V0IF00	1st Update Item 1 revised Item2 added
3	September 8th, 2006	U18093EE2V0IF00	2nd Update Item 5 added