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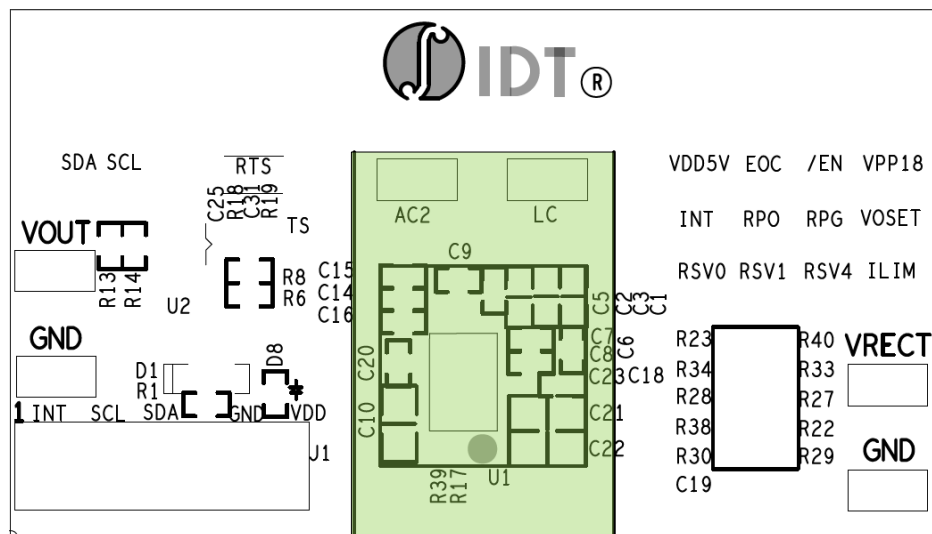
# 1. Introduction

The P9225-R Wireless Power Receiver (Rx) is a highly integrated solution for 5W applications. The reference layout has been optimized to minimize the printed circuit board (PCB) area (9mm × 9mm), and it can be easily copied and pasted into a design for a compact system, such as mobile phone applications.

In the layout, there are high current AC signals. It is critical that the current path is handled well in the printed circuit board (PCB) design to achieve optimum performance in electromagnetic compatibility (EMC) tests. The thermal management is also very important to the P9225-R performance, and the PCB layout should be optimized and balanced between proper design of the layout area and heat dissipation.

In the reference layout, the V-cut slots are designed on the bottom layer so that the area of the PCB with the core function circuits (green shaded area in Figure 1) can be easily detached and built into prototype products. Contact IDT for further technical information.

**Figure 1. P9225-R Reference Layout**



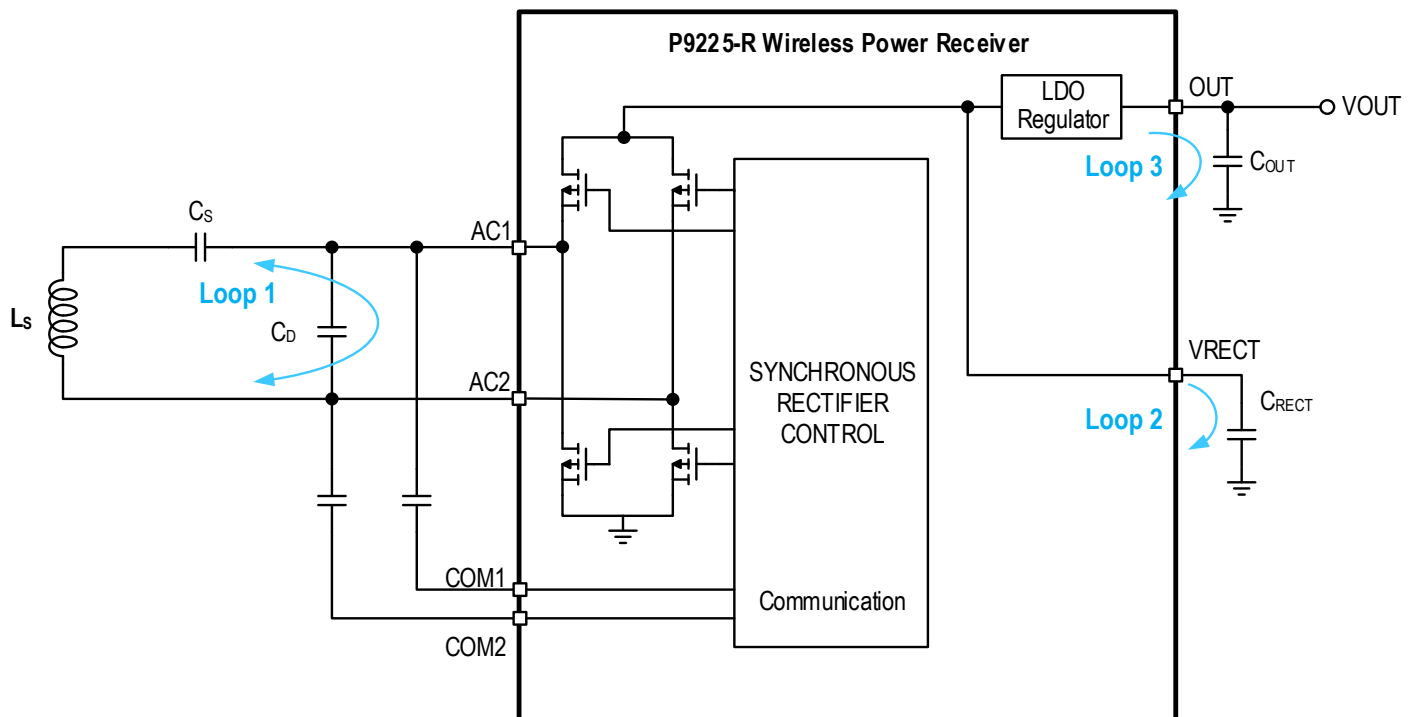
## 1.1 Key Points for Optimal Layout

- Route the power connections wide and keep them on the same side of the PCB as the P9225-R ( $\geq 70$  mils) for the LC, AC1, AC2, OUT, VRECT, and GND nets.
- Use the bottom layer of the board as a solid ground plane, and also place additional ground plane on the second layer.
- Connect all 8 GND pins to the ground plane(s) using via-in-pads. Add a thermal pad for the J-row GND pins.
- Avoid unnecessary layer transitions of the AC power connections (LC node and the VRECT, AC1, AC2, and GND pins).
- Place the P9225-R as close as possible to the center of the board. Avoid placing it along the PCB edge.
- Connect as much copper as possible to every pin of the P9225-R, including pins that do not carry high current.
- Place components in the following order: resonance capacitors, VRECT pin capacitors, BST pin capacitors, OUT pin capacitors, VDD18 pin capacitors, and VDD5V pin capacitors.
- Follow the placement and routing suggestions outlined in the remainder of this document for the specific types of circuits. Refer to the schematics in section 5 for the location of components.

## 2. Power Circuits

Figure 2 shows the main circuits and components involved in power circuits. The main power current flows from the Rx coil to the AC1 pin via the  $C_S$  capacitors and returns to other end of the Rx coil from the AC2 pin. Loop 1 identified in Figure 2 is the AC current, and the polarity changes in every driving cycle. In Loop 2, high frequency harmonic current in the LC tank returns to GND via  $C_{RECT}$ . In Loop 3,  $C_{OUT}$  buffers the output of the LDO on the OUT pin. Details of the layout guidelines for each of the current loops will be covered in subsequent sections.

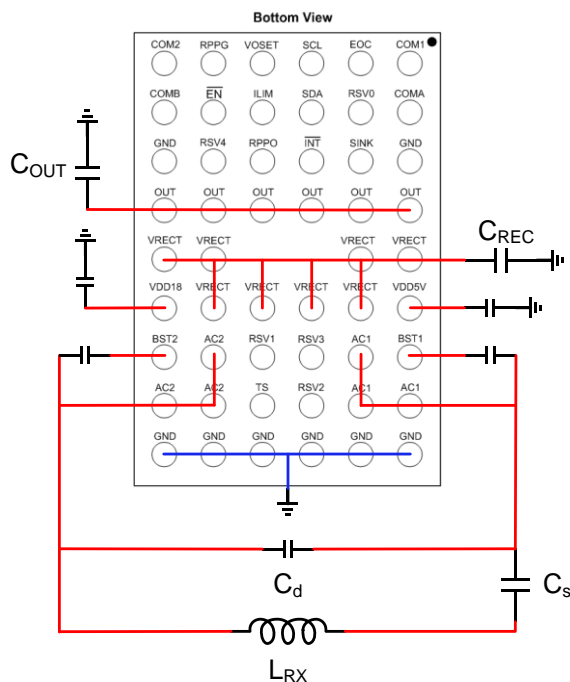
**Figure 2. P9225-R Power Block Diagram**



When the PCB dimensions have been determined based on mechanical constraints, the connection points for the receiver coil  $L_S$  should be determined. Next, the P9225-R should be placed in the center of the allocated PCB area. The orientation of the chip should be determined based on the route connections to key components. The key components should be placed in the following order of priority: resonance capacitors ( $C_S$ ), rectifier capacitors ( $C_{RECT}$ ), output capacitor ( $C_{OUT}$ ), and VDD5V and VDD18 capacitors.

**Figure 3. Recommended Orientation for the P9225-R Layout**

Note: Not all necessary connections are shown in Figure 3. Trace widths are not to scale. All GND pins should be connected to GND.

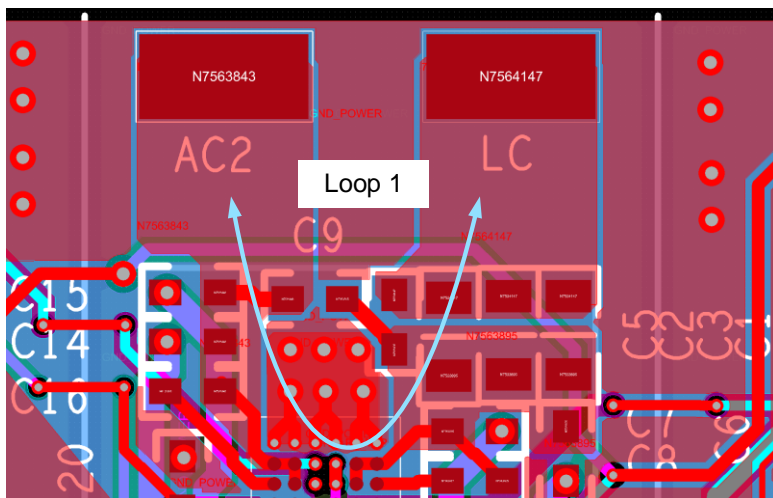


## 2.1 LC Tank

The LC tank circuit consists of the receiver coil ( $L_S$ ) and the  $C_S$  resonant capacitance ( $C_1$ ,  $C_2$ ,  $C_3$ , and  $C_5$ ) as illustrated in Figure 4 and Figure 10. The current runs through Loop 1 as indicated in the Figure 4, and it contains high frequency harmonics. The loop area must be minimized to reduce radiated emission noise.

Recommendation: Route the loop on the top layer and place components compactly. Along the current loop, copper width should be maximized if space allows. Using a large copper plane on the  $C_S$  capacitors and AC2 net will help to reduce copper loss caused by large currents, and it also helps to spread the heat away from  $C_S$  capacitors and the P9225-R.

**Figure 4. P9225-R Reference Layout (LC Tank)**

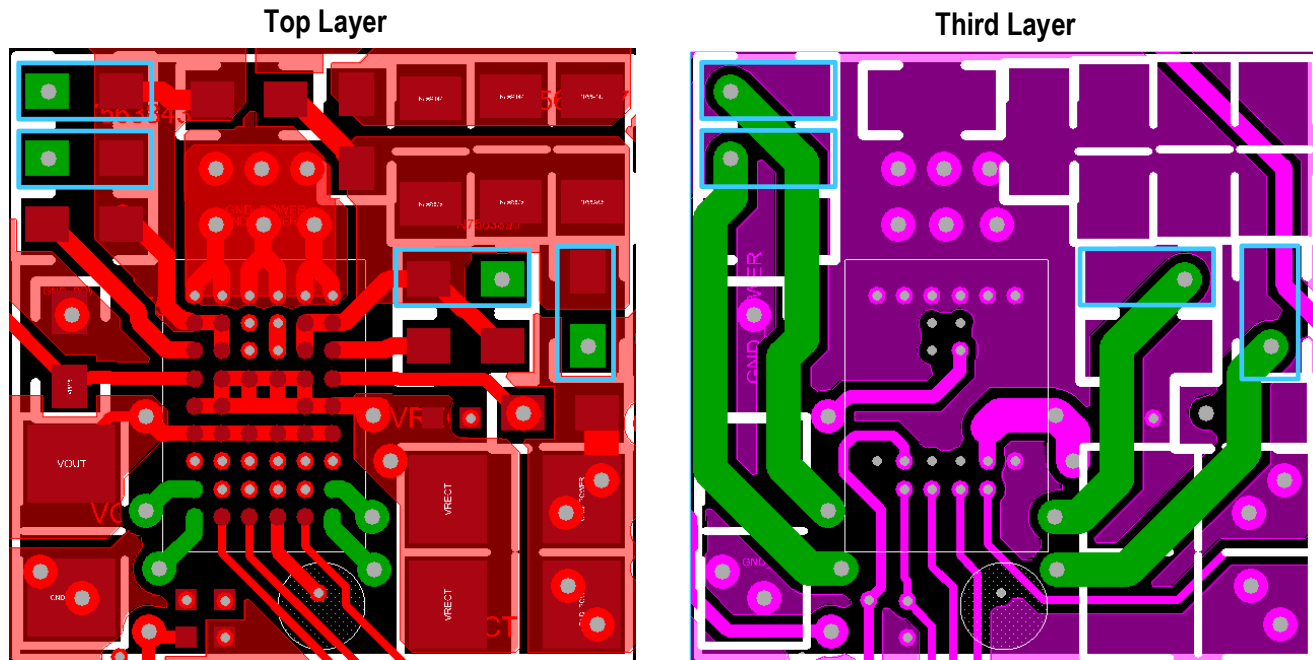


## 2.2 Communication Capacitors

Communication capacitors C6, C14 (for WPC), C7, and C15 (for PMA) should be placed on the top layer in order to have a direct connection to the AC1 or AC2 net without using vias as indicated in Figure 5 by the blue rectangles. The traces for the terminals on the other side of the capacitors must be routed via the third layer to connect to the respective pins on the P9225-R, and the trace width should be at least 20mil.

When communication is on-going, these capacitors function as a load to the system; therefore it is necessary to keep the trace wide enough to handle the current. To minimize the layout area, there are vias on the solder pad of the capacitors. The vias must be plugged at the bottom layer to avoid poor soldering caused by paste leakage.

**Figure 5. COMx Capacitors Layout**



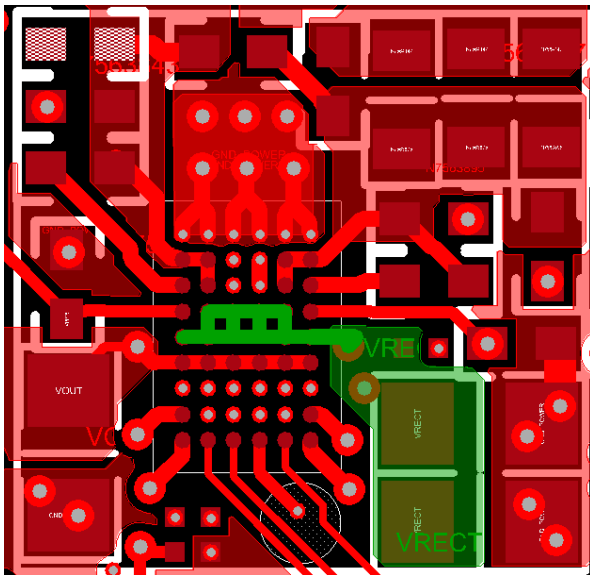
## 2.3 VRECT Capacitors

High frequency harmonic currents in the LC tank are rectified and filtered by the capacitors on the VRECT pin. High frequency radiated emission noise could be induced if the loop is not minimized.

Recommendation: Place the VRECT capacitors (C23, C22, and C21) on the same layer as the P9225-R and place them as close as possible as illustrated by the green-shaded area in Figure 6.

The trace width should also be maximized. C23 (100nF) should be placed closer to the VRECT pin because it filters higher frequencies. To minimize the layout area, C21 and C22 have a low-profile 0805 package. If the space allowed or cost is a concern, C21 and C22 could be replaced by three 10 $\mu$ F capacitors with a 0603 package and the same voltage rating. Vias should be plugged on the bottom layer due to the via-on-pads design. At least two GND vias (10mil) should be placed to have a good connection to a solid GND plane on the bottom layer.

**Figure 6. VRECT Capacitor Layout – Top Layer**



## 2.4 OUT Pin Capacitor

Output capacitor should be placed close to the P9225-R OUT pin as well. Using long traces between the OUT pin and the output capacitor would introduce inductance, which could degrade the stability of the output LDO. The width of the trace between the OUT pin and capacitor should be maximized. At least two GND vias (10mil) should be placed to have a good connection to GND plane. To minimize the layout area, the output capacitor has a low-profile 0805 package. It could be replaced by two 10 $\mu$ F capacitors with a 0603 package and the same voltage rating if space allowed or cost is concern. The VOUT trace to the system load should be maximized to prevent copper losses and a rise in temperature on the board.

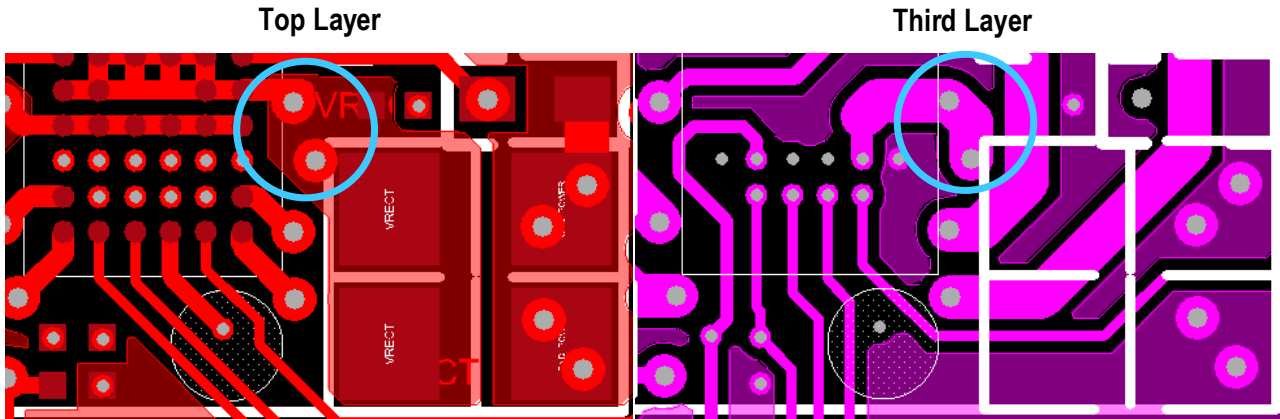
## 2.5 VDD5V and VDD18 Capacitors

The capacitors on VDD5V (C18) and VDD18 (C20) are used to stabilize the P9225-R's internal 5V and 1.8V supplies respectively. On each pin, a single 1 $\mu$ F capacitor is sufficient since the load on each rail is quite small. Each capacitor should be placed close to the respective P9225-R pin. An 8mil trace is wide enough to handle the current.

## 2.6 SINK Trace

The SINK pin is directly connected to VRECT net. There will be current flow if there is an over-voltage condition on the VRECT net. A trace that is at least 12mil should be used on the third layer to connect the VRECT net and SINK pin, and two 10mil vias should be placed.

**Figure 7. SINK Net Layout**



## 2.7 Programming Resistors

The programming resistors on the VOSET, ILIM, RPPO, RPPG, EOC, and INT pins are in a less sensitive circuit, and they can be placed away from the P9225 if the layout is crowded. The 0201 package is sufficient for these resistors.

Recommendation: Place C19 (100nF) close to the VPP18 net that is used to pull up programming resistors.

## 2.8 EEPROM Circuits and Programming Interface

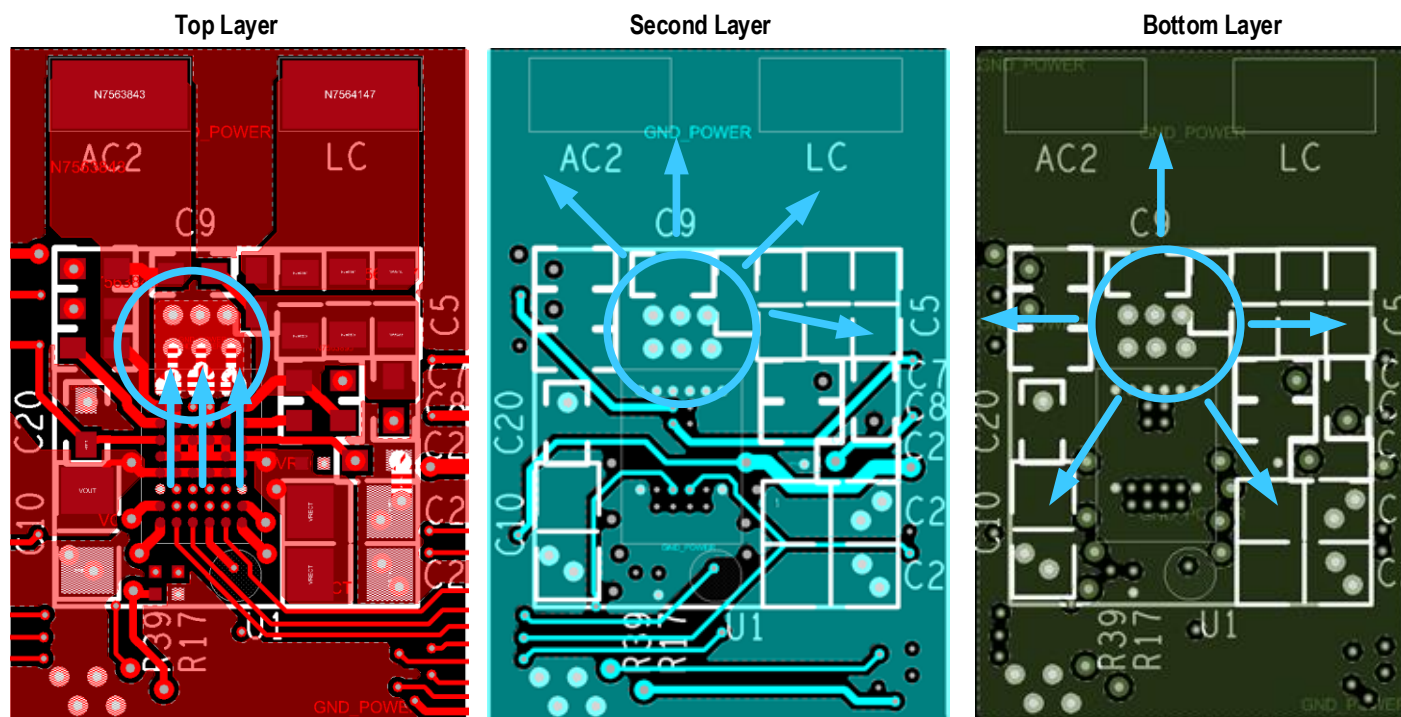
Recommendation for the product development phase: Add the EEPROM circuit on the board if space allows. It is helpful for quick firmware updates. The programming interface should have test points implemented for the PS (external power supply), I2C SDA, I2C SCL, and GND net, and the test points should be grouped together in a location with easy access to the programming dongle.

## 2.9 Thermal Management

On the top layer, a GND plane should be placed with a strong connection to the P9225-R GND pins to improve the heat dissipation. At least six 10mil vias should be placed on the top layer thermal pad to transition heat to other layers. If space allows, place more vias and a larger thermal pad on the top layer.

The second layer is directly under the P9225-R, and more GND copper in this layer could also help to dissipate the heat from the P9225-R. The bottom layer should be solid GND plane, as it is the most effective layer to directly exchange heat with the ambient environment. In addition to the PCB assembly, the Rx receiver coil is another heat source. When designing the system mechanical structure, it is necessary to avoid placing the Rx coil close to the top of the PCB assembly because even without physical contact, both the PCBA and coil will heat each other due to heat radiation. The NTC sensor (RTS) can be placed close to the P9225-R, which is the only heat source on the board.

**Figure 8. P9225-R Layout Heat Flow**





### 3. PCB Footprint Design

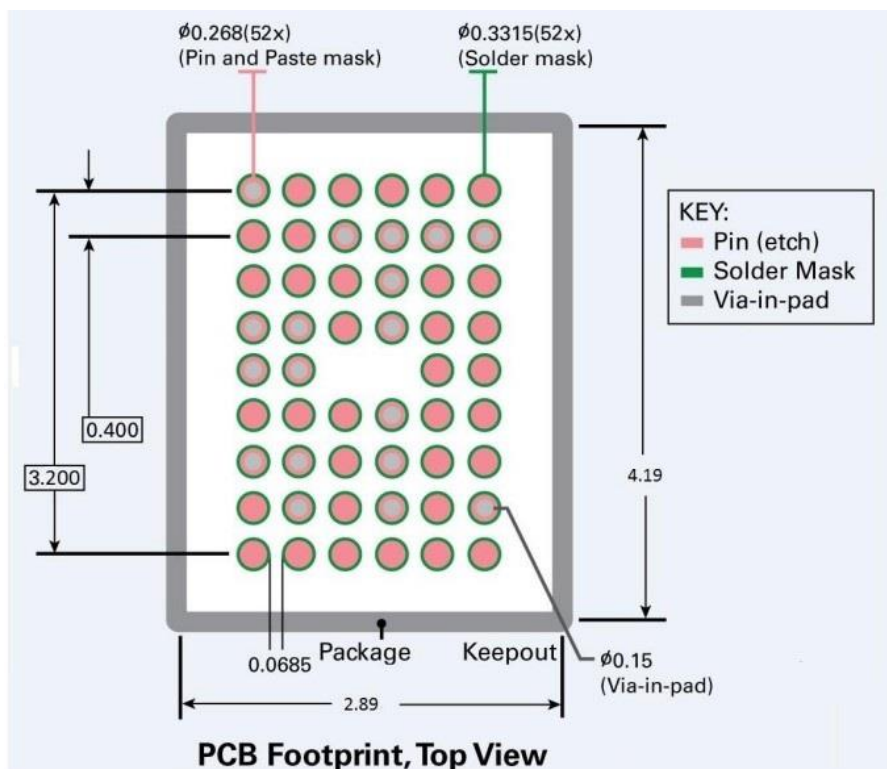
The P9225-R package is a fine-pitch WLCSP package. Improper footprint design can lead to solder shorts or open circuits. Poor PCB footprint design can also cause the performance to be degraded by limiting the robustness and diameter of the pin-to-board connections. In order to minimize the risk of such events, it is recommended that the PCB pin pads and via-in-pads be designed using the following guidance.

Non-solder mask defined pins are recommended, and solder paste should be applied with stencil openings of 0.127mm to 0.268mm (recommendation: 0.19mm typical) based on stencil thickness and the solder paste selected. The pin diameter should be set to 0.268mm, the solder mask should be 0.3315mm, and via-in-pads should be 0.127mm diameter holes.

The current version of the WLCSP package outline drawing and land pattern are accessible via this link:

[www.idt.com/document/psc/ahg52-package-outline-2640-x-3940mm-body-04mm-pitch-dsbga](http://www.idt.com/document/psc/ahg52-package-outline-2640-x-3940mm-body-04mm-pitch-dsbga)

**Figure 9. P9225-R Recommended PCB Footprint Dimensions in mm**



## 4. Audible Noise Suppression

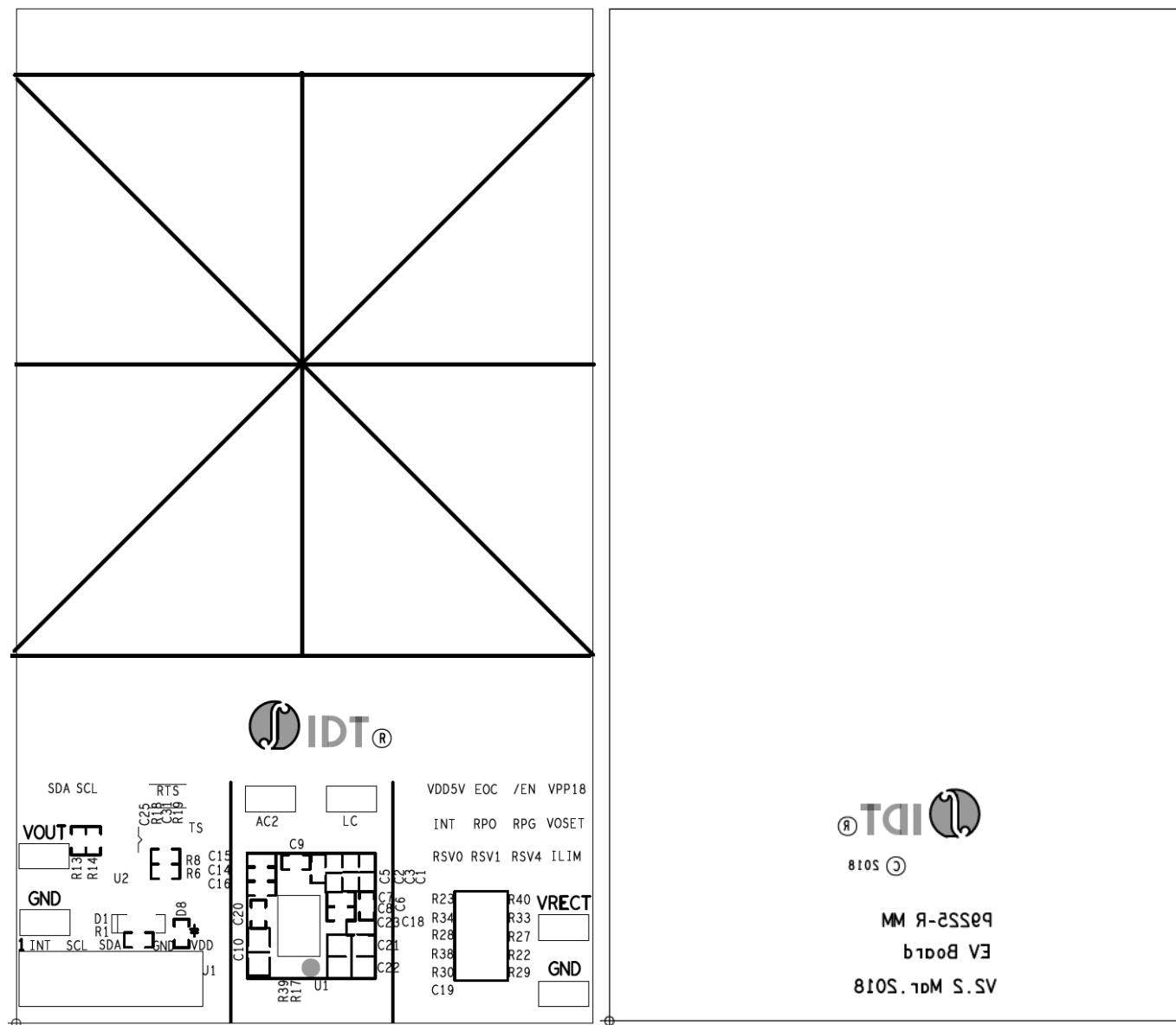
Wireless power receiver solutions have been observed to produce audible noise. If sound is detected, there are several steps that can be taken to reduce or eliminate the noise. Some of the sources of the audible noise have been identified to be the rectifier capacitors, the Rx coil ferrite, and communication capacitors. Typically, the rectifier capacitors are the most significant source of audible noise. This is due to the WPC communication signals being generated in the audible frequency range and the use of small-form factor ceramic capacitors. The noise occurs due to the piezoelectric effect of ceramic capacitors. The capacitors constrict and expand while providing the communication pulses, and this noise is amplified as it flexes the PCB. The primary solution to this issue is to use low-acoustic noise capacitors. Alternatively, higher voltage rated components can have superior piezoelectric properties that can reduce the audible noise. Placing the capacitors on both sides of the PCB (directly above and below each other) counters the piezoelectric forces applied to the PCB (it cancels the force by each capacitor). Another method is to add slots through the PCB on both outer sides of the capacitors or directly under each capacitor. One additional approach is to place additional lower capacitance value components in parallel to reduce the mechanical force of the piezoelectric effect per component. For any additional questions, contact IDT technical support (see last page for contact information).

### Figure 10. P9225-R Schematic

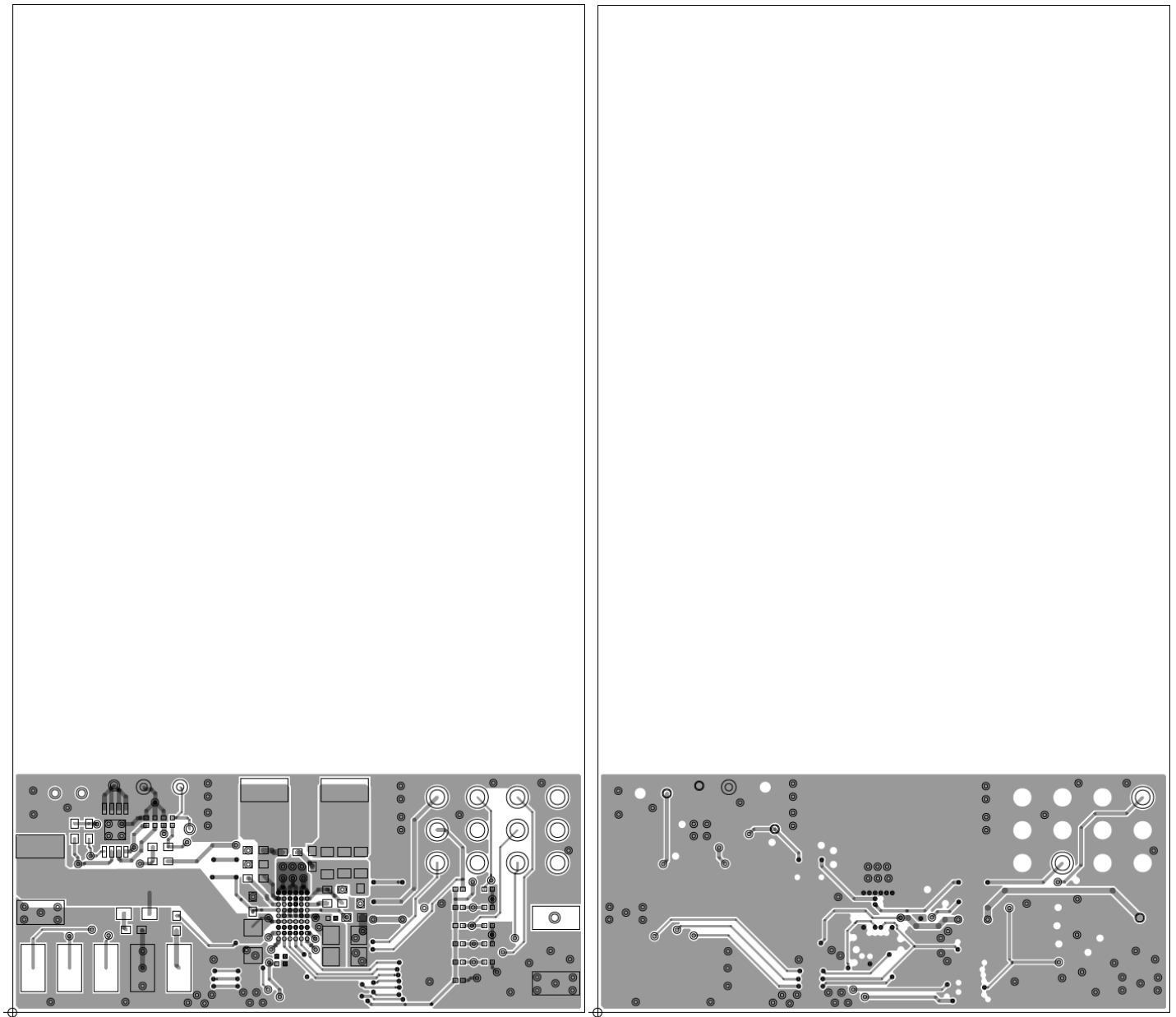


## 6. Board Layout

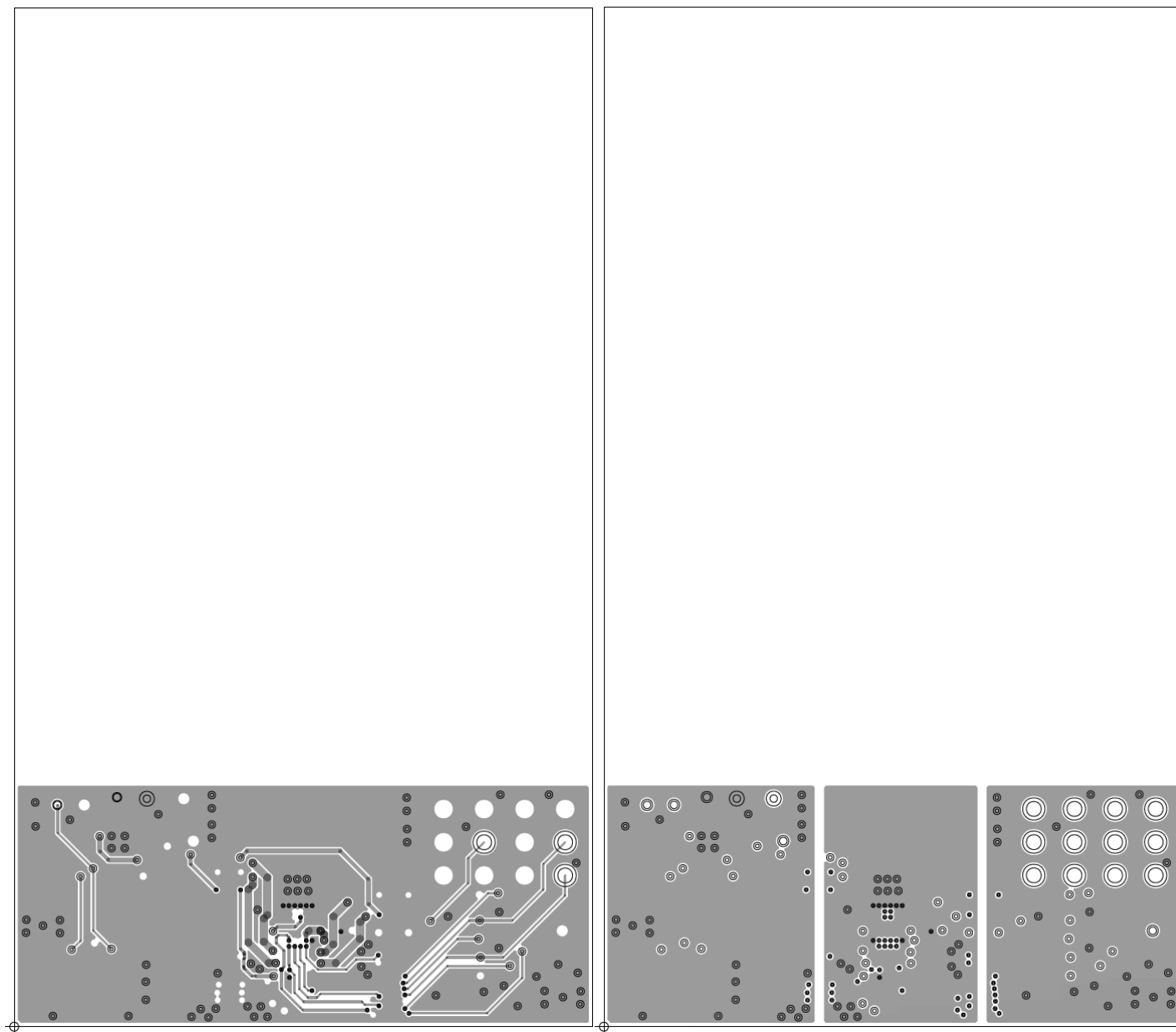
**Figure 11. P9225-R Top Silkscreen (left) and Bottom Silkscreen (right)**



**Figure 12. P9225-R Top Layer (left) and Second Layer (right)**



**Figure 13. P9225-R Third Layer (left) and Bottom Layer (right)**



## 7. Revision History

| Revision Date | Description of Change |
|---------------|-----------------------|
| May 5, 2018   | Initial release.      |

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