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April 1st, 2010
Renesas Electronics Corporation

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RENESAS

Customer Notification

IE-789234-NS-EM1™

Emulation Board

Operating Precautions

Target Devices

78K0S/KY1+ Series
78K0S/KA1+ Series
78K0S/KB1+ Series

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Table of Contents

(A) Table of Operating Precautions 4

(B) Description of Operating Precautions 5

(C) Valid Specification 10

(D) Revision History 11

IE-789234-NS-EM1

(A) Table of Operating Precautions

No.	Outline	Control Code[Note]	IE-789234-NS-EM1 A	B	C	
1	Restriction on oscillation stabilization time (Technical Limitation)		✗	✗	✗	
2	Target device not supported (Technical Limitation)		✗	✓	✓	
3	General cautions (Technical Limitation)		✗	✗	✗	
4	AD Converter (Technical Limitation)		✗	✗	✓	
5	P121/X1 pin function (Technical Limitation)		✗	✗	✓	
6	Hang up after stop execution (Technical Limitation)		✗	✗	✓	

✓ : Not applicable
✗ : Applicable
- : Specification is not supported

Note: The control code is the **second letter** from the left of the 10 digit serial number (version that have not been upgraded).
For upgraded versions, an upgrade label is affixed to the product. The version-up level on this sticker corresponds to the actual control code (i.e. the X in the V-UP LEVEL X indicates the control code X).

(B) Description of Operating Precautions

No. 1 Restriction on oscillation stabilization time
(Technical Limitation)

Details

When the IE-789234-NS-EM1 is used in combination with the IE-78K0S-NS, the emulator may not be activated depending on the combination of the oscillation stabilization time and frequency of the clock supplied to X1 set by the option byte, as shown below.

This restriction does not apply when using the IE-789234-NS-EM1 in combination with the IE-78K0S-NS-A.

Option Byte Setting		Oscillation Stabilization Time	Frequency of clock supplied to X1	Result
SW3-7	SW3-6			
DEFOSTS1	DEFOSTS0			
0	0	2^{10}/fx	500KHz to 10MHz	OK
0	1	2^{12}/fx	500KHz to 10MHz	
1	0	2^{15}/fx	500KHz to 10MHz	May not be activated when the frequency is lower than 1MHz
1	1	2^{17}/fx	500KHz to 10MHz	

Workaround

- Supply a 1 MHz or higher clock to X1 when the oscillation stabilization time is set to 2^{15}/fx (DEFOSTS1: 1 and DEFOSTS0: 0)
- Supply a 2 MHz or higher clock to X1 when the oscillation stabilization time is set to 2^{17}/fx (DEFOSTS1: 1 and DEFOSTS0: 1)

No. 2 Target device not supported
(Technical Limitation)

Details

The IE-789234-NS-EM1 does not support the devices shown below.

- 78K0S/KY1+: uPD 78F9210, 78F9211, 78F9212
- 78K0S/KB1+: uPD 78F9232, 78F9234

It only supports 78K0S/KA1+: uPD 78F9221, 78F9222

No. 3a General cautions
Option byte
(Technical Limitation)

Details

Since the IE-789234-NS-EM1 sets the option byte using SW3, the value set to address 80H is not reflected in the debugger.

No. 3b	General caution Port registers (Technical Limitation)
	Details Some bits of the port registers that are fixed to 0 can be overwritten by program. However, writing is not possible on the SFR window.

No. 3c	General cautions AD converter (Technical Limitation)
	Details AD conversion can be started without waiting for 1us or longer even if bit 0 (ADCE) of the AD conversion mode register (ADM) is set to 1.

No. 3d	General cautions Reset flag register (RESF) (Technical Limitation)
	Details Bit 4 (WDTRF) and bit 0 (LVIRF) of the reset control flag register (RSEF) cannot be initialized by the reset button of the debugger or reset button (SW2) of the IE-78K0S-NS and IE-78K0S-NS-A. Input a reset from the target side, re-apply power to the emulator or press SW4 on the IE-789234-NS-EM1 to clear the reset control flag register (RESF).

No. 3e	General cautions Self programming (Technical Limitation)
	Details The IE-789234-NS-EM1 does not support the self programming function of the flash memory.

No. 3f	General cautions HALT mode (Technical Limitation)
	Details When HALT mode is released by an interrupt, the program is restored two or three clocks earlier than the target device.

No. 3g	General cautions Low-voltage detection level (Technical Limitation)
	Details An error of several mV occurs in the IE-789234-NS-EM1 compared to the target device.

No. 3h	General cautions AD converter characteristics (Technical Limitation)
	Details The characteristics of the AD converter of the IE-789234-NS-EM1 differ from those of the target device because a probe is connected between the IE-789234-NS-EM1 and the target system.

No. 3i	General cautions 8-bit timer H1 (Technical Limitation)
	Details When the low speed ring osc. is selected as the 8-bit timer count clock, the timer does not stop while the program is stopped even if “Break” is selected for “Peripheral Break” in the configuration dialog box of the debugger.

No. 3j	General cautions RESET pin (Technical Limitation)
	Details Since the RESET pin alternately functions as P34, it is connected to a protective resistor (pull-down) inside the emulator. Consequently, the RESET pin is always low level. Normally a reset does not occur because “Mask: RESET” is set in the configuration dialog box. But if the “Mask: RESET” setting is canceld, a reset is always applied, which causes the debugger to hang up. When inputting an external reset from the RESET pin, first pull the reset pin up and cancel the “Mask:RESET” setting in the configuration box.

No. 4	AD Converter (Technical Limitation)
	Details The A/D function may not operate if any of the following operations is performed while the use environment temperature is low. • Changing the settings of analog input channel specification register (ADS) during A/D conversion • Changing the settings of A/D converter mode register (ADM) during A/D conversion *Workaround* Stop the A/D converter operation (ADCS = 0) then change the settings of ADS or ADM.

No. 5	P121/X1 pin function (Technical Limitation)

Details
When the P121/X1 pin is used as an external clock input pin, the P121/X1 pin does not function as the I/O port. However, it functions as an output port if bit 1 of port mode register 12 (PM12) is set to select output mode.

Workaround
When using the P121/X1 pin as an external clock input pin, do not set bit 1 of PM12 to select output mode.

No. 6 Hang up after stop execution
(Technical Limitation)

Details
Regarding the standby release conditions after a STOP instruction is executed, if an arbitrary interrupt mask flag is cleared to 0 while an interrupt enable flag is 0 (by executing the DI instruction), an interrupt is generated (interrupt request flag = 1), then the STOP instruction is executed, the standby state is not released and the debugger hangs up. Moreover, the standby state is not released even if a standby release signal is generated due to another interrupt request, and the debugger hangs up.

Example 1 A standby release signal is generated due to INTP0 immediately before executing a STOP instruction while interrupts are disabled

```
• DI          ; Disables interrupts
• SET1 PIF0   ; Sets INTP0 interrupt request flag
• CLR1 PMK0   ; Clears masking of INTP0 interrupt
• SET1 P2.0   ; Sets port 20 to “1”
• STOP        ; Enters STOP mode
• CLR1 P2.0   ; Clears port 20 to “0” (not executed)
```

The same situation occurs when a standby release signal is generated while interrupts are enabled and an instruction that holds interrupt requests pending is executed immediately before a STOP instruction.

Example 2 A standby release signal is generated due to INTP0 immediately before executing a STOP instruction while interrupts are enabled

```
• EI          ; Enables interrupts
• SET1 P2.0   ; Sets port 20 to “1”
• SET1 PIF0   ; Sets interrupt request flag
• CLR1 PMK0   ; Executes an instruction that holds interrupt requests pending
              ; immediately before executing a STOP instruction
• STOP        ; Enters STOP mode
• CLR1 P2.0   ; Clears port 20 to “0” (not executed)
```

Remark Instructions that hold interrupt requests pending
- Instructions that perform writing to the interrupt request flag register (IF0 or IF1)
- Instructions that perform writing to the interrupt mask flag register (MK0 or MK1)

Workaround
Be sure to set the interrupt enable flag to 1 (EI instruction) before executing a STOP instruction. Moreover, do not execute an instruction that holds interrupt requests pending immediately before executing the STOP instruction.

Example Execute an EI instruction immediately before executing the STOP instruction

```
DI              ; Disables interrupts
SET1 PIF0       ; Sets INTP0 interrupt request flag
CLR1 PMK0       ; Clears masking of INTP0 interrupt
SET1 P2.0       ; Sets port 20 to “1”
EI              ; Enables interrupts
STOP            ; Enters STOP mode
CLR1 P2.0       ; Clears port 20 to “0” (executed)
```

Remark In the case that an interrupt occurs immediately before a STOP instruction, the interrupt request flag is cleared before executing the STOP instruction. To release the STOP mode, therefore, another interrupt must be generated.

(C) Valid Specification

Item	Date published	Document No.	Document Title
1	June 2005 or later	U17381EJ	User's Manual IE-789234-NS-EM1

(D) Revision History

Item	Date published	Document No.	Comment
1	April 6th , 2004	TPS-LE-OP-T9234-A	1st release
2	January 11th, 2005	TPS-LE-OP-T9234-B	Addition of control code “B” and caution “3j”
3	June 27th, 2005	TPS-LE-OP-T9234-C	Addition of control code “C”