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ISL6731AEVAL2Z and ISL6731BEVAL2Z: High Performance Boost CCM PFC Front End for Server Power Applications

Introduction

This application note describes the design and implementation of a 390V, 750W, Continuous Conduction Mode (CCM) Boost PFC converter using either ISL6731A or ISL6731B. The converter exhibits high power factor, low THD and high conversion efficiency. The ISL6731A, ISL6731B are voltage mode power factor correction (PFC) controllers designed to drive cost-effective high performance converters to meet the tight input line harmonic requirements. The IC can be ISL6731A (124kHz) or ISL6731B (64kHz).

Application

PFC front end for server, data center, telecom, industrial and infrastructure power applications.

Key Features

- Universal input: 90V~265VAC
- Adaptive control to achieve extremely low THD and high PF without DSP.
- Compact implementation

References

- "ISL6731A, ISL6731B" datasheet

Design Specifications

- Input Voltage, V_{IN}: 90V - 265VAC
- Output Voltage, V_O: 390VDC
- Output Current, I_O: 1.92A (750W)
- Switching Frequency: ISL6731A (124kHz) or ISL6731B (64kHz)
- Efficiency: Full Load, 93% @ 115V; 97% @ 230V
- PF: Full Load, 0.99
- THD: Full Load, 2%
- Board Dimension: 121×96×38 mm^3(L×W×H)

Test Setup

- See the test set-up in Figure 9 on page 7
- A 12VDC FAN is needed to cool the heat-sink during the test, especially at full load with low line 90~140VAC input!

Ordering Information

PART NUMBER	DESCRIPTION
ISL6731AEVAL2Z	750W Boost CCM PFC, 124KHz
ISL6731BEVAL2Z	750W Boost CCM PFC, 64kHz

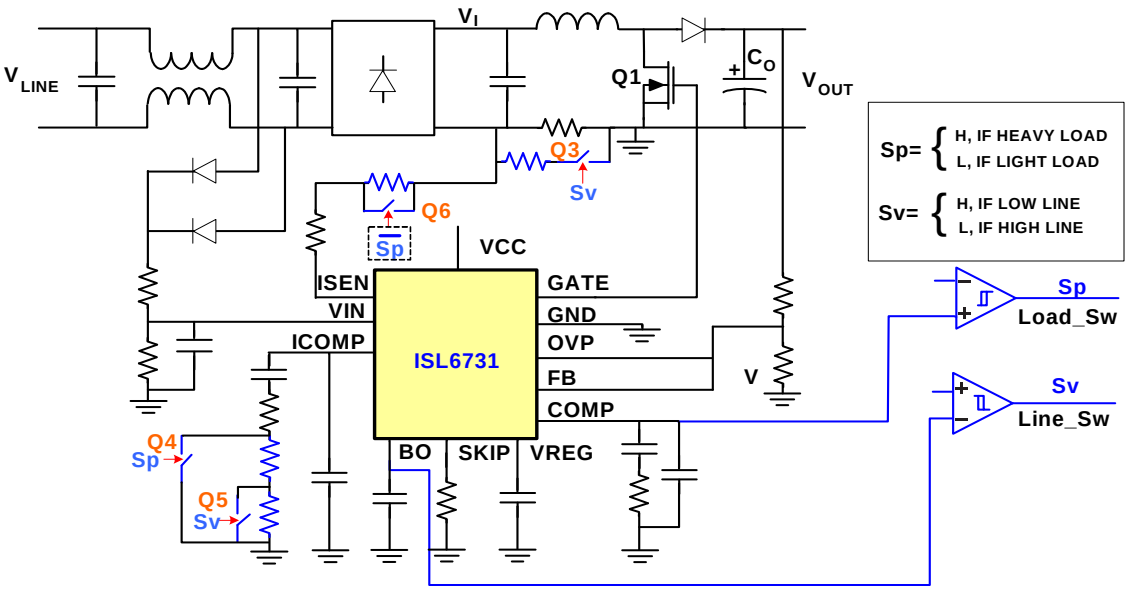


FIGURE 1. SIMPLIFIED SCHEMATIC

Component Selection Guidelines

A 750W, universal input, PFC converter design is provided for demonstration. The design method is for a continuous current mode power factor correction boost converter with the ISL6731B. The switching frequency is 64kHz.

Table 1 shows the design parameters.

TABLE 1. CONVERTER DESIGN PARAMETERS

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
V_{LINE}		90	115/230	265	VAC
F_{LINE}		47		63	Hz
P_{OMAX}	Maximum Output Power			750	W
T_{HOLD}	Hold Up Time		20		ms
Efficiency	V_{LINE} = 115VAC	92			%

BOOST INDUCTOR SELECTION

First, calculate the maximum input RMS current, I_{INMAX}.

$$I_{INMAX} = \frac{P_{OMAX}}{\eta \bullet V_{RMSmin}} \quad \text{(EQ. 1)}$$

Where η is the converter efficiency at V_{RMSmin}. PF is the power factor at V_{RMSmin}.

$$I_{INMAX} = \frac{750W}{0.92 \bullet 90V} = 9.06A \quad \text{(EQ. 2)}$$

Assuming the current is sinusoidal and the peak-to-peak ripple at line is 40%.

The boost inductor, L_{BST}, is given by the following equation:

$$L_{BST} \geq \frac{\sqrt{2}V_{RMSmin}}{0.4 \bullet F_{sw} \bullet \sqrt{2} \bullet I_{INMAX}} \bullet \left(1 - \frac{\sqrt{2} \bullet V_{RMSmin}}{V_{OUT}}\right) \quad \text{(EQ. 3)}$$

$$L_{BST} \geq \frac{90V}{0.4 \bullet 64kHz \bullet 9.06A} \bullet \left(1 - \frac{\sqrt{2} \bullet 90V}{390V}\right) = 261\mu H \quad \text{(EQ. 4)}$$

An 850µH inductor was selected. The peak current of the inductor is the sum of the average peak inductor current and half of the peak-to-peak ripple current. Select and design the boost inductor as given by Equation 3. The ISL6731A and ISL6731B provide a peak current limit function that can prevent the boost inductor saturation. Assuming 25% margin is given to the OCP threshold, select and design the boost inductor with saturation current given by Equation 5 with 25% margin.

$$I_{LPeak} = \sqrt{2} \bullet I_{INMAX} + \frac{1}{2} \bullet \Delta_I \quad \text{(EQ. 5)}$$

$$_{.}Peak = \sqrt{2} \bullet 9.06A + \frac{(3.152A)}{2} = 14.4A \quad \text{(EQ. 6)}$$

INPUT RECTIFIER

The maximum average input current is calculated:

$$I_{INAVE(max)} = \frac{2 \bullet \sqrt{2} \bullet I_{INMAX}}{\pi} \quad \text{(EQ. 7)}$$

$$I_{INAVE(max)} = \frac{2 \bullet \sqrt{2} \bullet 9.06A}{\pi} = 8.2A \quad \text{(EQ. 8)}$$

Select the bridge diode using Equation 9 and sufficient reverse breakdown voltage. Assuming the forward voltage, $V_{F,BR}$, is 1.1V across each rectifier diode. The power loss of the rectifier bridge can be calculated:

$$P_{BR} = 2 \bullet V_{F,BR} \bullet I_{INAVE(MAX)} \quad \text{(EQ. 9)}$$

$$P_{BR} = 2 \bullet 1.1V \bullet 8.2A = 17.9W \quad \text{(EQ. 10)}$$

INPUT CAPACITOR SELECTION

Refer to the “Recommended Filtering Capacitor” table, in the ISL6731A, ISL6731B datasheet for the recommended input filter capacitor value.

$$C_{F1} = 750W \bullet \frac{0.22}{100} = 1.65\mu F \quad \text{(EQ. 11)}$$

The definition of C_{F1} is on the block diagram in the ISL6731A, ISL6731B datasheet.

This is the recommended capacitor used after the diode bridge. For better power factor, less capacitance can be used. To lower the input filter inductor size, more capacitance can be used.

One 0.68µF capacitor is used for C_{F1}.

BOOST DIODE SELECTION

The boost diode loss is determined by the diode forward voltage drop, V_F and the output average current. The maximum output current is:

$$I_{OUT(max)} = \frac{P_{OMAX}}{V_{OUT}} \quad \text{(EQ. 12)}$$

$$I_{OUT(max)} = \frac{750W}{390V} = 1.923A \quad \text{(EQ. 13)}$$

The forward power loss on the diode is:

$$P_{FD} = I_{OUT(max)} \bullet V_F \quad \text{(EQ. 14)}$$

$$P_{FD} = 1.923A \bullet 1.3V = 2.5W \quad \text{(EQ. 15)}$$

The IDH05S60C part is selected.

The reverse recovery loss on the diode can be calculated. The Q_{RR} is found from the diode datasheet. Q_{RR} = 12nC.

The reverse recover loss on the diode can be estimated:

$$P_{RRD} = \frac{1}{4} \bullet Q_{RR} \bullet V_{OUT} \bullet F_{sw} \quad \text{(EQ. 16)}$$

$$P_{RRD} = \frac{1}{4} \bullet 12nC \bullet 390V \bullet 64kHz = 0.075W \quad \text{(EQ. 17)}$$

The total power loss on the diode is:

$$P_D = P_{FD} + P_{RRD} = (2.5 + 0.075)W = 2.575W \quad \text{(EQ. 18)}$$

MOSFET POWER DISSIPATION

The power dissipation on the MOSFET is from two different types of losses; the conduction loss and the switching loss.

For the MOSFET, the worst case is at minimum line input voltage.

First, the drain to source RMS current is calculated:

$$I_{DS(max)} = I_{INMAX}\sqrt{1-\frac{8\sqrt{2}}{3\pi}\bullet\frac{V_{RMSmin}}{V_{OUT}}} \quad \text{(EQ. 19)}$$

$$I_{DS(max)} = 9.06A\sqrt{1-\frac{8\sqrt{2}}{3\pi}\bullet\frac{90V}{390V}} = 7.7A \quad \text{(EQ. 20)}$$

The MOSFET, SPP20N60C3 is selected.

$$P_{COND} = I_{DS(max)}^2 \bullet R_{DS(on)} \quad \text{(EQ. 21)}$$

$$P_{COND} = 7.7A^2 \bullet 0.188\Omega = 11.12W \quad \text{(EQ. 22)}$$

The switching loss of the MOSFET consists of three parts: the turn-on loss, the turn-off loss and the C_{OSS} loss.

From the MOSFET datasheet, the typical switching losses curves are provided.

E_{ON} = 0.022mJ, E_{OFF} = 0.029mJ.

The switching loss due to transition is calculated:

$$P_{SW} = (E_{ON} + E_{OFF}) \bullet F_{sw} \quad \text{(EQ. 23)}$$

$$P_{SW} = (0.022mJ + 0.029mJ) \bullet 64kHz = 3.26W \quad \text{(EQ. 24)}$$

The loss caused by C_{OSS} can be estimated as:

$$P_{OSS} = \frac{2}{3}C_{OSS} \bullet V_{OUT}^2 \bullet F_{sw} \quad \text{(EQ. 25)}$$

From the datasheet, the C_{OSS} is 61pF at 390V.

$$P_{OSS} = \frac{2}{3}61pF \bullet 390V^2 \bullet 64kHz = 0.394W \quad \text{(EQ. 26)}$$

THE TOTAL LOSS ON THE MOSFET

$$P_{COND} + P_{SW} + P_{OSS} = 11.12W + 3.26W + 0.394W = 14.78W \quad \text{(EQ. 27)}$$

OUTPUT CAPACITOR SELECTION

The output capacitor, C_O, is required to hold the output above 300V during one line cycle. For capacitors with 10% tolerance, the tolerance should be taken into consideration. Thus, the output capacitance should be greater than:

$$C_O \geq \frac{2 \cdot T_{HOLD} \cdot P_{OMAX}}{V_{OUT}^2 - V_{HOLD}^2} \cdot \frac{1}{1-0.1} \quad \text{(EQ. 28)}$$

$$C_O \geq \frac{2 \cdot 20ms \cdot 750W}{(390)^2 - (300V)^2} \cdot 1.25 = 537\mu F \quad \text{(EQ. 29)}$$

Calculate the ripple RMS current through the capacitor:

$$I_{CORMS(max)} = I_{OUT(max)}\sqrt{\frac{8\sqrt{2}}{3\pi}\bullet\frac{V_{OUT}}{V_{RMSmin}} - 1} \quad \text{(EQ. 30)}$$

$$I_{CORMS(max)} = 1.923A\sqrt{\frac{8\sqrt{2}}{3\pi}\bullet\frac{390V}{90V} - 1} = 3.942A \quad \text{(EQ. 31)}$$

Select the proper capacitor according to the hold time and ripple RMS current requirement. The actual capacitance is 2x270µF.

It is important to make sure the output peak-to-peak ripple is less than the minimum OVP threshold. The ESR of the capacitor at 2 times the line frequency is found in the capacitor datasheet. The ESR is 367mΩ.

$$V_{Opp} = I_{OUT(max)} \cdot \frac{\sqrt{(4\pi f_{line} \cdot C_O \cdot ESR)^2 + 1}}{(4\pi f_{line}) \cdot C_O \cdot 0.8} \quad \text{(EQ. 32)}$$

$$V_{Opp} = 1.923A \cdot \frac{\sqrt{(4\pi \cdot 60Hz \cdot 540\mu F \cdot 0.367\Omega)^2 + 1}}{(4\pi \cdot 60Hz) \cdot 540\mu F \cdot 0.8} = 5.97V \quad \text{(EQ. 33)}$$

The minimum OVP threshold is 103% of the nominal output value. The maximum output peak-to-peak ripple should be less than 6% of the nominal value, which is 23.4V_{P-P}.

CURRENT SENSING RESISTORS

Please refer to Equation 34 for calculation of the current sensing resistor R_{CS}.

$$R_{CS} \geq \frac{120mV \cdot 265V \cdot 0.92}{\sqrt{2} \cdot 750W} = 0.028\Omega \quad \text{(EQ. 34)}$$

While a large R_{CS} renders better current sensing accuracy, larger R_{CS} also incurs higher power dissipation. Select R_{CS} from available standard value resistors to determine the sense resistor.

$$R_{CS} = 0.044\Omega \quad \text{(EQ. 35)}$$

The maximum power dissipation on the R_{CS} occurs at low line and full load condition. The maximum power dissipation is calculated:

$$P_{RCSMAX} = I_{INMAX}^2 \bullet R_{CS} \quad \text{(EQ. 36)}$$

$$P_{RCSMAX} = 9.06A^2 \bullet 0.044\Omega = 3.61W \quad \text{(EQ. 37)}$$

The resistor R_{SEN} sets the overcurrent protection limit.

$$R_{SEN} \geq \frac{R_{CS} \bullet I_{LPeak} \bullet (1 + 0.25)}{2 \bullet 0.5|I_{OC}|} \quad \text{(EQ. 38)}$$

Where |x| stands for the ABS (x) function. I_{OC} is overcurrent threshold (in datasheet).

$$R_{SEN} \geq \frac{0.044\Omega \bullet 14.4A \bullet 1.25}{159\mu A} = 5.0k\Omega \quad \text{(EQ. 39)}$$

The selected R_{SEN} is 5.2kΩ.

CURRENT LOOP COMPENSATION

The input current shaping is achieved by comparing the sensed current signal to the sensed input voltage signal. The current error amplifier (Gmi), together with the current compensation network, adjusts the duty cycle so that the inductor current traces the sensed rectified voltage. Thus, unity power factor is achieved.

The compensation network consists of the Trans-Conductance error amplifier (Gmi) and the impedance network (Z_{ICOMP}). The goal of the compensation network is to provide a closed loop transfer function with the sufficient 0dB crossing frequency

(f_{0dB}) and adequate phase margin. Phase margin is the difference between the open loop phase at f_{0dB} and 180°. The following equations relate the compensation network's poles, zeros and gain to the components (R_{ic}, C_{ic} and C_{ip}) in Figure 2.

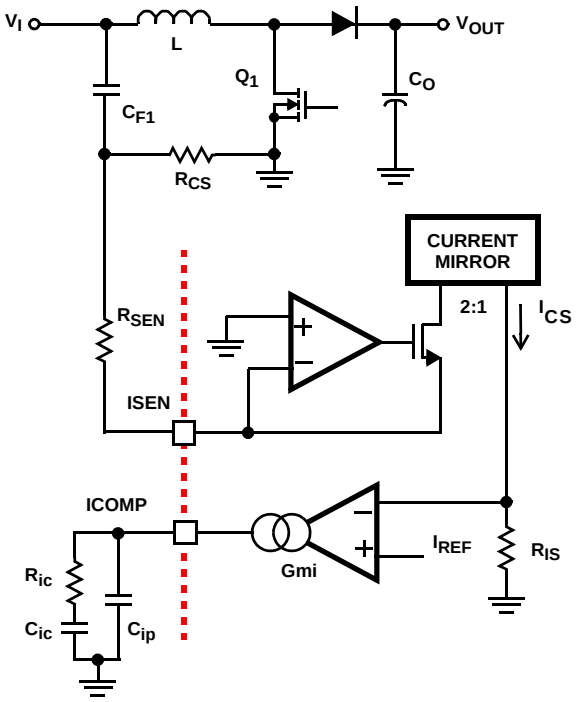


FIGURE 2. INDUCTOR CURRENT SENSING SCHEME

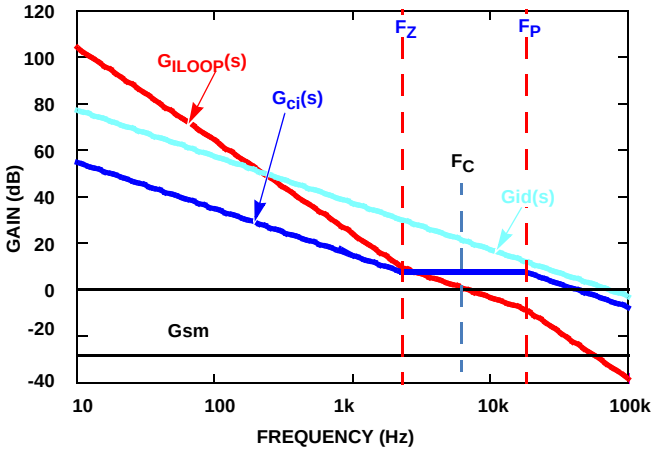


FIGURE 3. ASYMPTOTIC BODE PLOT OF CURRENT LOOP GAIN

$$F_Z = \frac{1}{2\pi \bullet R_{ic} \bullet C_{ic}} \quad \text{(EQ. 40)}$$

$$F_P = \frac{1}{2\pi \bullet R_{ic} \bullet \frac{C_{ip} \bullet C_{ic}}{C_{ip} + C_{ic}}} \quad \text{(EQ. 41)}$$

Use the following guidelines for locating the poles and zeros of the compensation network.

Near crossover frequency, the transfer function from duty cycle to inductor current is well approximated Equation 42:

$$G_{id}(s) = \frac{V_{OUT}}{L_{BST} \cdot s} \quad \text{(EQ. 42)}$$

The compensation gain uses external impedance networks as shown in Figure 2, $G_{ci}(s)$ is given by:

$$G_{ci}(s) = Gmi \frac{1}{(C_{ic} + C_{ip}) \cdot s} \bullet \frac{\frac{s}{2 \cdot \pi \cdot F_Z} + 1}{\frac{s}{2 \cdot \pi \cdot F_P} + 1} \quad \text{(EQ. 43)}$$

The current gain and modulation gain Gsm is:

$$Gsm = \frac{Rcs}{Rsen} \cdot \frac{Ris}{2} \frac{1}{Vm} \quad \text{(EQ. 44)}$$

where Vm is the amplitude of the PWM carrier. The open loop gain of the current loop is

$$G_{ILOOP}(s) = G_{id}(s) \bullet G_{sm} \bullet G_{ci}(s) \quad \text{(EQ. 45)}$$

It is recommended to set the crossover frequency from 1/10 to 1/6 of the switching frequency with phase margin of about 60°. A high frequency pole is set at 1/2 or less of the switching frequency for ripple filtering. In this example, we set the crossover, F_C at 1/9 of the switching frequency.

$$F_Z = \frac{F_C}{\tan\left(\operatorname{atan}\left(\frac{F_C}{F_P}\right) + \Phi_M\right)} \quad \text{(EQ. 46)}$$

Where $F_C = F_{sw}/9 = 7.1kHz$, Φ_M is the phase margin, which is 50°. $F_P = F_{sw}/4 = 16kHz$.

Thus, the current loop compensation zero is:

$$F_Z = \frac{(64kHz)/9}{\tan\left(\operatorname{atan}\left(\frac{4}{9}\right) + 50deg\right)} = 2.04kHz \quad \text{(EQ. 47)}$$

The total compensation capacitance is calculated:

$$C_{ip} + C_{ic} = \left(\left(\frac{V_{OUT}}{L_{BST} \cdot (2\pi f_c)^2} \cdot \frac{A_{IDC}}{V_m} \cdot \frac{R_{CS}}{R_{SEN}}\right) \cdot \sqrt{\frac{1 + (f_c/f_z)^2}{1 + (f_c/f_p)^2}}\right) \quad \text{(EQ. 48)}$$

$$C_{ip} + C_{ic} = 8.148nF \quad \text{(EQ. 49)}$$

$$C_{ip} = (C_{ip} + C_{iC}) \frac{f_z}{f_p} \quad \text{(EQ. 50)}$$

The value of the noise filtering capacitor is:

$$C_{ip} = 8.148nF \cdot \frac{2.04kHz}{16kHz} = 1.041nF \quad \text{(EQ. 51)}$$

The value of C_{ic} is:

$$C_{ic} = 8.148nF - 1.041nF = 7.1nF \quad \text{(EQ. 52)}$$

The value of R_{ic} is:

$$R_{ic} = \frac{1}{2\pi \cdot 2.04kHz \cdot 7.1nF} = 10.96k\Omega \quad \text{(EQ. 53)}$$

Select the R_C value from the standard value, we have:

R_{ic} = 10kΩ, C_{ic} = 6.8nF, C_{ip} = 1nF. Figure 4 shows the bode plot of current loop gain, where $f_s = F_{sw}$.

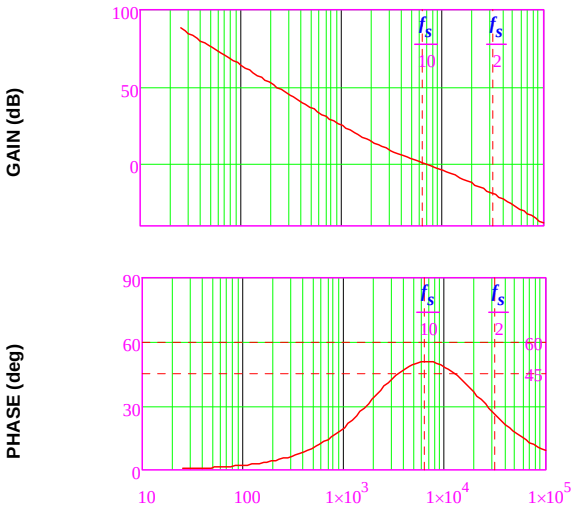


FIGURE 4. BODE PLOT OF THE ACTUAL CURRENT LOOP GAIN

INPUT VOLTAGE SETTING

First, set the BO resistor divider gain, K_{BO} according to Equation 54.

Assuming the converter starts at V_{LINE} = 80V_{RMS}, then the BO resistor divider gain, K_{BO} should be:

$$K_{BO} = \frac{0.5V}{80V - 2V} = 0.00641 \quad \text{(EQ. 54)}$$

In this design, two 200kΩ resistors in series are used for R_{IN2}. So, R_{IN1} is calculated:

$$R_{IN1} = \frac{0.00641}{1 - 0.00641} \cdot (440k\Omega) = 2.581k\Omega \quad \text{(EQ. 55)}$$

Using resistor from the standard value, R_{IN1} = 2.49kΩ, the actual K_{BO} is calculated:

$$K_{BO} = \frac{R_{IN1}}{R_{IN1} + R_{IN2}} = 0.00619 \quad \text{(EQ. 56)}$$

NEGATIVE INPUT CAPACITOR GENERATION

The ISL6731A and ISL6731B generate an equivalent negative capacitance at the input to cancel the input filter capacitance. Thus, more input capacitors can be used without reducing the power factor.

The input equivalent negative capacitance is a function of the current sensing gain, BO resistor divider gain and the compensation components.

$$C_{NEG} = \left(K_{BO} \cdot 0.8 - \frac{V_m}{V_{OUT}}\right)\frac{R_{SEN}}{R_{CS}A_{iDC}}(C_{ic} + C_{ip}) \quad \text{(EQ. 57)}$$

$$C_{NEG} = \left(0.00619 \cdot 0.8 - \frac{1.5}{390}\right)\frac{5.2k}{0.044 \cdot 1.9}(6.8nF + 1nF) = 0.54\mu F \quad \text{(EQ. 58)}$$

This equivalent negative capacitor cancels the input filter capacitor required for EMI filtering. Therefore, the displacement power factor significantly improves.

For example, refer to the block diagram on page 4 in the ISL6731A, ISL6731B datasheet C_{F2}+C_{F3} = 2µF, C_{F1} = 0.68µF, when V_{LINE} = 230VAC, f_{LINE} = 50Hz, P_O = 750W.

Assuming 95% efficiency under the above test condition, the resistive component of the line current, which is in phase to voltage:

$$I_a = \frac{P_o}{V_{LINE} \cdot 0.95} = 3.432A \quad \text{(EQ. 59)}$$

The reactive current through the input capacitors:

$$I_c = V_{LINE} \bullet (2\pi \cdot f_{LINE}) \bullet (C_{F1} + C_{F2} + C_{F3}) = 0.232A \quad \text{(EQ. 60)}$$

Thus, the displacement power factor is:

$$PF_{DIS} = \frac{I_a}{\sqrt{(I_a)^2 + (I_c)^2}} = 0.9977 \quad \text{(EQ. 61)}$$

The reactive current generated by the equivalent negative capacitor is:

$$I_{cneg} = V_{LINE} \bullet (2\pi \cdot f_{LINE}) \bullet (C_{NEG}) = 0.046A \quad \text{(EQ. 62)}$$

With the equivalent negative capacitor, the total reactive current reduces to:

$$I_c - I_{cneg} = 0.186A \quad \text{(EQ. 63)}$$

The displacement power factor increases to:

$$PF_{DIS} = \frac{I_a}{\sqrt{(I_a)^2 + (I_c - I_{cneg})^2}} = 0.9985 \quad \text{(EQ. 64)}$$

VOLTAGE LOOP COMPENSATION

The average boost diode forward current can be approximated by:

$$I_{D(ave)} = \frac{P_{in}}{V_{OUT}} \quad \text{(EQ. 65)}$$

Assuming the input current traces the input voltage perfectly. The input power is in proportion to (V_{COMP} - 1V).

$$I_{D(ave)} = \frac{R_{SEN}}{R_{CS} \cdot 0.5 \cdot R_{IS}} \bullet \frac{1}{V_{OUT}} \bullet \left(\frac{0.25}{((2\sqrt{2})/\pi)^2 \cdot K_{BO}}\right) \bullet \Delta_{COMP} \quad \text{(EQ. 66)}$$

Where Δ_{COMP} is the V_{COMP} - 1V. 1V is the offset voltage.

R_{IS} is the internal current scaling resistor. R_{IS} = 14.2kΩ.

$$I_{D(ave)} = (2.13)\frac{A}{V} \bullet \Delta_{COMP} \quad \text{(EQ. 67)}$$

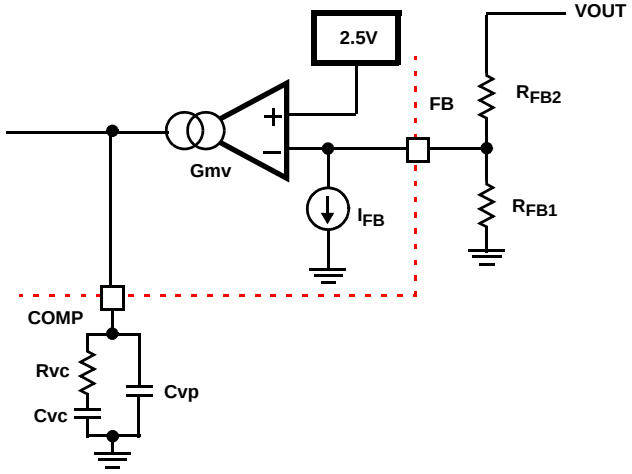


FIGURE 5. OUTPUT VOLTAGE SENSING AND COMPENSATION

Thus, the transfer function from $\overline{V}_{COMP}$ to $\overline{V}_{OUT}$ is:

$$G_{PS}(s) = \frac{V_{OUT}(s)}{\Delta_{COMP}} = \frac{1}{C_O \cdot s} \cdot \frac{I_{D(ave)}}{\Delta_{COMP}} \quad \text{(EQ. 68)}$$

$$G_{PS}(s) = \left(\frac{I_{D(ave)}}{C_O \cdot s} \cdot \frac{1}{\Delta_{COMP}}\right) = \frac{2.13}{C_O \cdot s} \quad \text{(EQ. 69)}$$

As shown in Figure 5, the voltage loop gain is:

$$G_{VLOOP}(s) = G_{PS}(s) \bullet G_{DIV} \bullet Gmv \bullet Z_{COMP}(s) \quad \text{(EQ. 70)}$$

The output feedback resistor divider gain, G_{DIV} is:

$$G_{DIV} = \frac{V_{REF}}{V_{OUT}} \quad \text{(EQ. 71)}$$

The compensation gain uses external impedance networks as shown in Figure 5, $Z_{COMP}(s)$ is given by:

$$Z_{COMP}(s) = \frac{1}{(C_{vc} + C_{vp}) \cdot s} \bullet \frac{R_{vc} \bullet C_{vc} \bullet s + 1}{\frac{R_{vc} \bullet C_{vc} \bullet C_{vp}}{C_{vc} + C_{vp}} \bullet s + 1} \quad \text{(EQ. 72)}$$

The targeted crossover frequency, F_{CV} is 10Hz. The high frequency pole, F_{PV} is required in order to reject the 2 time line frequency component. F_{PV} = 20Hz. The targeted phase margin is 50°.

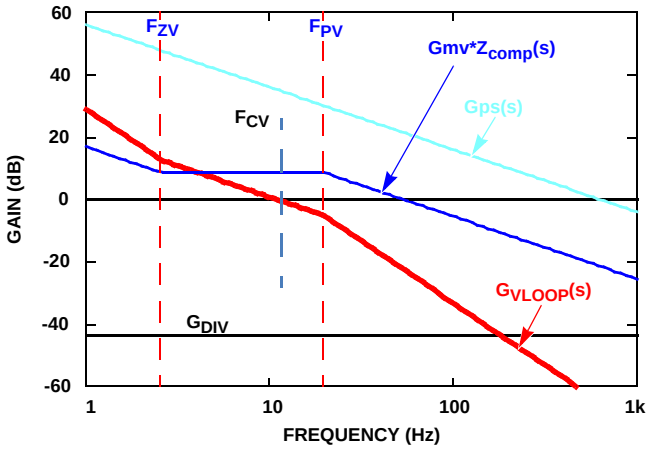


FIGURE 6. ASYMPTOTIC BODE PLOT OF VOLTAGE LOOP GAIN

The zero, F_{Zv} is calculated:

$$F_{Zv} = \frac{F_{CV}}{\tan(\Phi_m + \operatorname{atan}(F_{CV}/(F_{Pv})))} \quad \text{(EQ. 73)}$$

$$F_{Zv} = \frac{10Hz}{\tan(50deg + \operatorname{atan}((10Hz)/(20Hz)))} = 2.389Hz \quad \text{(EQ. 74)}$$

Then the total capacitance used for compensation is calculated:

$$C_{vc} + C_{vp} = \frac{|G_{PS}(i \bullet (2\pi F_{CV}))| \bullet G_{DIV} \bullet Gmv}{(2\pi F_{CV})} \bullet \sqrt{\frac{(F_{CV}/F_{ZV})^2 + 1}{(F_{CV}/F_{PV})^2 + 1}} \quad \text{(EQ. 75)}$$

Thus, the total compensation capacitance is:

$$C_{vc} + C_{vp} = 1233nF \quad \text{(EQ. 76)}$$

$$C_{vp} = 1233nF \bullet \frac{F_{ZV}}{F_{PV}} = 147nF \quad \text{(EQ. 77)}$$

$$C_{vc} = 1233nF - 147nF = 1086nF \quad \text{(EQ. 78)}$$

$$R_{vc} = \frac{1}{2 \cdot \pi \cdot F_{ZV} \cdot C_{VC}} = 61.3k\Omega \quad \text{(EQ. 79)}$$

Choose components from the standard values. We have C_{VP} = 150nF, C_{VC} = 1µF, R_{VC} = 62kΩ. The actual bode plot is shown in Figure 7.

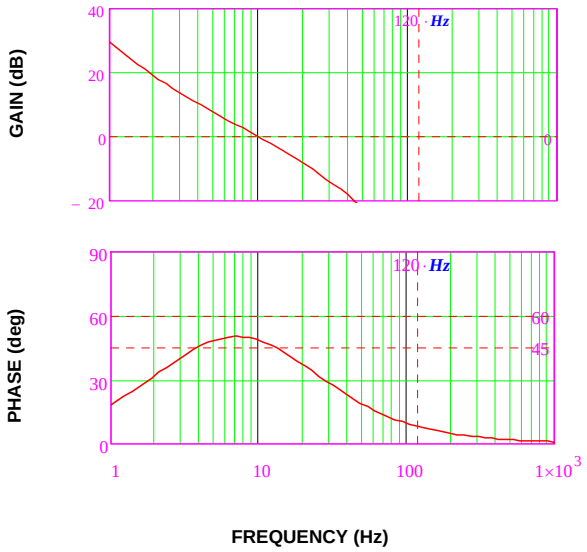


FIGURE 7. BODE PLOT OF THE ACTUAL VOLTAGE LOOP GAIN

ADAPTIVE CONTROL

ISL6730 and ISL6731 family have excellent power factor correction capability to achieve low THD and high PF with the above circuit optimization. To further improve THD at light and high line condition, Q3, Q4, Q5 and Q6 and two comparators are added to dynamically change current loop and current sense gain (refer to Figure 1). This simple analog implementation can achieve same level of THD and PF performance as DSP control.

The signal Sp controls Q6 (inverted) and Q4. Sp is controlled by load power level via the voltage level on COMP pin. Sp goes high at heavy load and low at light load.

At light load condition, COMP voltage is low. Sp goes low. Q4 turns off to increase Ric resistance to increase current loop gain and Q6 turns on to increase current sense gain. The increase of current loop and sense gain will push crossover frequency higher to improve THD.

The signal Sv controls Q3 and Q5. Sv is controlled by line voltage via the voltage level on BO pin. Sv goes high at low line and low at high line.

At high line condition, BO voltage is low. Sv goes low. Q5 turns off to increase Ric resistance to increase current loop gain and Q3 turns off to increase current sense gain. The increase of current loop and sense gain will push crossover frequency higher to improve THD.

At light load or high line condition, the boost inductor current is relatively small. The converter runs in discontinuous conduction mode. In this condition the CCM frequency domain model cannot be used for analysis. In DCM condition, the current loop will be inherently stable and thus can be pushed to run in a higher gain and crossover frequency configuration.

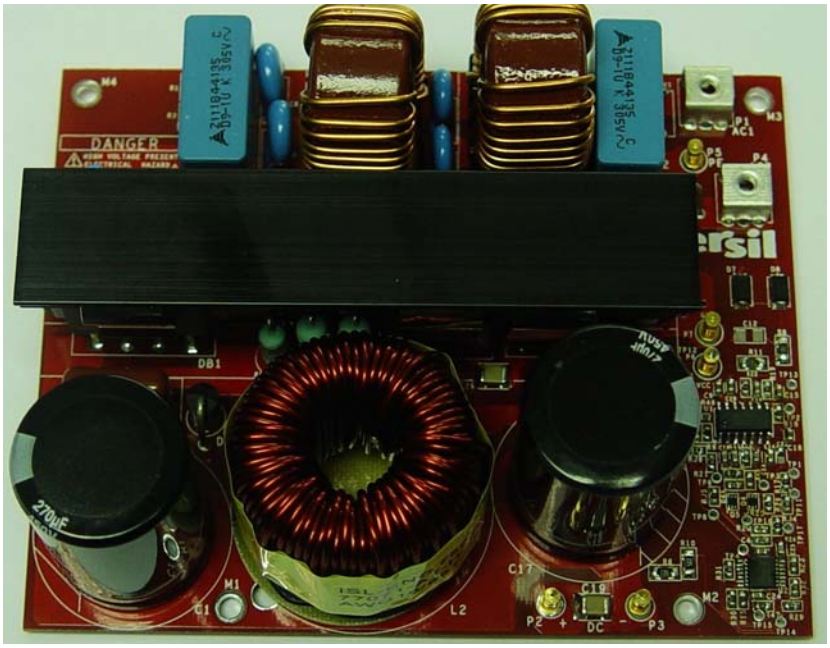


FIGURE 8. PHOTO OF THE EVALUATION BOARD

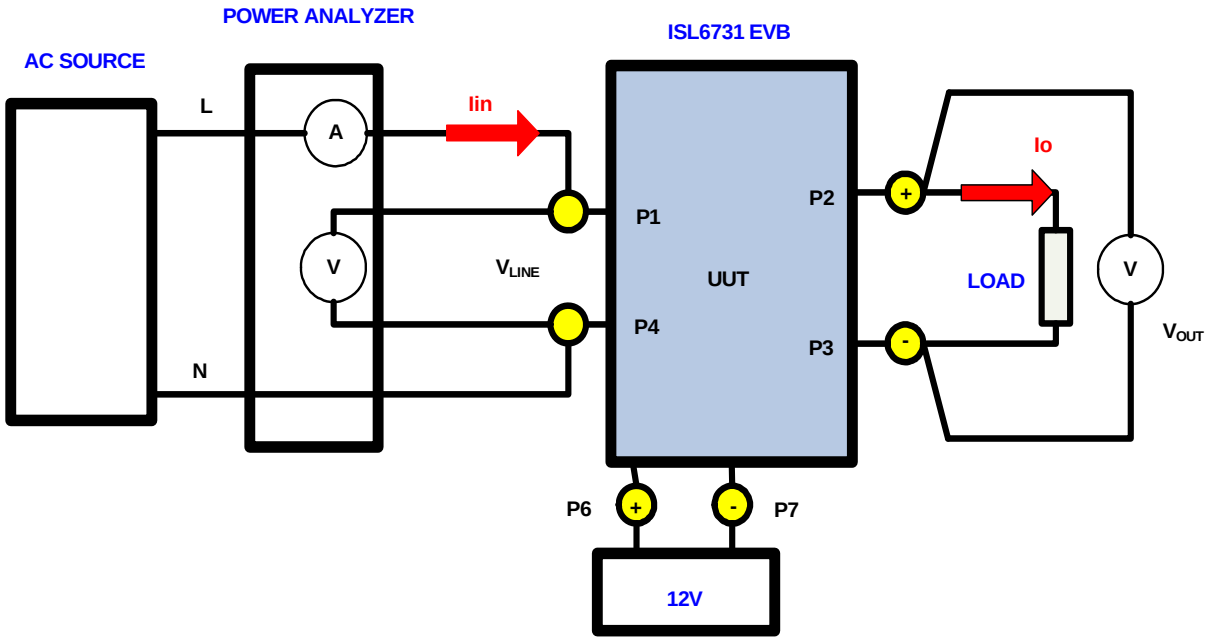
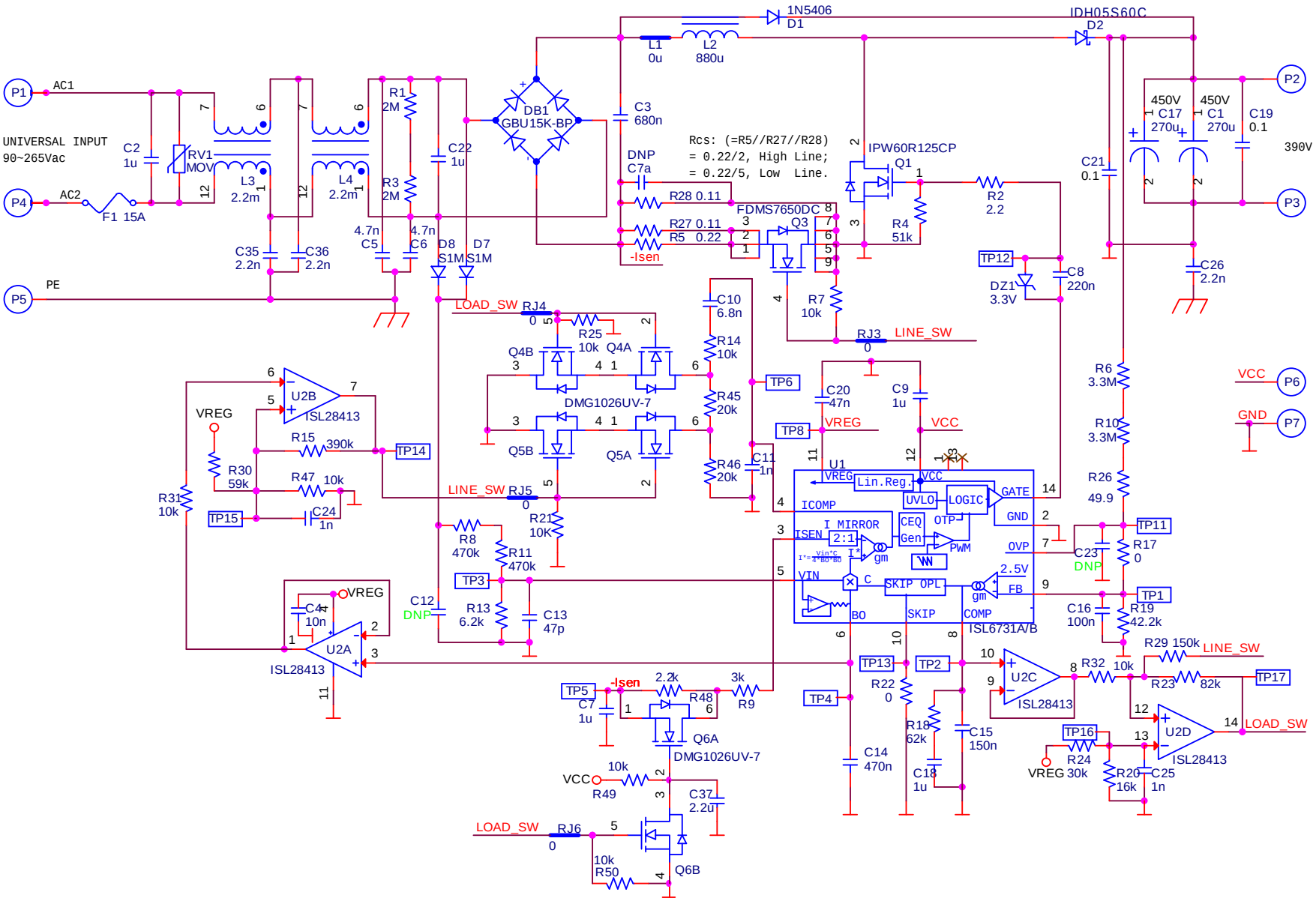


FIGURE 9. TEST SETUP

Schematic


UNIVERSAL INPUT
90~265Vac
AC1
AC2
PE
F1 15A
RV1 MOV
DB1 GBU15K-BP
1N5406 D1
IDH05S60C D2
L1 0u
L2 880u
L3 2.2m
L4 2.2m
C2 1u
C3 680n
C5 4.7n
C6 4.7n
C22 1u
C35 2.2n
C36 2.2n
R1 2M
R3 2M
D8 S1M
D7 S1M
DNP C7a
R28 0.11
R27 0.11
R5 0.22
-Isen
Rcs: (=R5//R27//R28)
= 0.22/2, High Line;
= 0.22/5, Low Line.
IPW60R125CP Q1
FDMS7650DC Q3
R2 2.2
R4 51k
R7 10k
C21 0.1
450V C17 270u
450V C1 270u
C19 0.1
390V
C26 2.2n
TP12
DZ1 3.3V
C8 220n
RJ3 LINE_SW
RJ4 LOAD_SW
R25 10k
Q4A
Q4B
DMG1026UV-7
Q5A
Q5B
C10 6.8n
R14 10k
R45 20k
R46 20k
C11 1n
TP6
TP8
C20 47n
C9 1u
VREG
VCC
U1
Lin.Reg.
UVLO
LOGIC
GATE
GND
OVP
OTP
PWM
ICOMP
I MIRROR 2:1
ISEN
VIN
SKIP OPL
SKIP
BO
COMP
2.5V
FB
ISL6731A/B
R6 3.3M
R10 3.3M
R26 49.9
R17 0
C23 DNP
TP11
TP1
C16 100n
R19 42.2k
R29 150k
LINE_SW
R32 10k
R23 82k
TP17
U2C
ISL28413
U2D
ISL28413
LOAD_SW
TP16
R24
VREG 30k
R20 16k
C25 1n
R22 0
R18 62k
C18 1u
C15 150n
C14 470n
TP13
TP2
TP4
TP5
C7 1u
2.2k
R48
3k
R9
Q6A
DMG1026UV-7
10k
R49
C37 2.2u
LOAD_SW
RJ6
10k
R50
Q6B
R21 10K
R8 470k
R11 470k
TP3
C12 DNP
R13 6.2k
C13 47p
C4 10n
U2A
ISL28413
R31 10k
R30 59k
R15 390k
R47 10k
C24 1n
TP15
TP14
U2B
ISL28413
VREG
P1
P2
P3
P4
P5
P6
P7
VCC
GND

Bill of Materials

QTY	REFERENCE DESIGNATOR	TYPE/PACKAGE	VALUE	VOL/TOL/MAT	MANUFACTURER	MANUFACTURER PART #
2	C1, C17	Cap; TH; Radial	270µ	450V; 20%; ELECT, Aluminum	Panasonic	EETUQ2W271DA
2	C2, C22	Cap; TH; Radial	1µ	X2; 20%; EMI, X2-class	EPCOS	
1	C3	Cap; TH; Radial	680n	450V; 20%; Metallized Polyester Film	Panasonic	ECW-F2W684J
1	C4	Cap; SM; 0603	10n	16V; 5%; NPO	TDK	
2	C5, C6	Cap; TH; Radial	4.7n	Y1; 20%; EMI, Y2-class	TDK	CS11-E2GA4722MYNS
2	C7, C9	Cap; SM; 0603	1µ	50V; 20%; X7R	TDK	
1	C8	Cap; SM; 0603	220n	25V; 20%; X7R	TDK	
1	C10	Cap; SM; 0603	6.8n	25V; 10%; X7R	TDK	
1	C11	Cap; SM; 0603	1n	25V; 10%; X7R	TDK	
1	C13	Cap; SM; 0603	47p	16V; 5%; NPO	TDK	
1	C14	Cap; SM; 0603	470n	16V; 10%; X7R	TDK	
1	C15	Cap; SM; 0603	150n	50V; 10%; X7R	TDK	
1	C16	Cap; SM; 0603	100n	50V; 10%; X7R	TDK	
1	C18	Cap; SM; 0603	1µ	16V; 10%; X7R	TDK	
2	C19, C21	Cap; SM; 1812	0.1	630V; 10%; -	Murata	GRM43DR72J104KW01L
1	C20	Cap; SM; 0603	47n	25V; 10%; X7R	TDK	
2	C24, C25	Cap; SM; 0603	1n	16V; 5%; NPO	TDK	
3	C26, C35, C36	Cap; TH; Radial	2.2n	Y1; 20%; EMI,Y2-class	TDK	CS11-E2GA222MYNS
1	C37	Cap; SM; 0603	2.2µ	50V; 20%; X7R	TDK	
1	DB1	Diode; TH; BRU806	GBU15K-BP	800V; 15A; Bridge Rectifier	Diodes Inc	
1	DZ1	Zener; SM; SOD323	3.3V	5%; Zener	NXP	BZX384-B3V3
1	D1	Diode; TH; DO-201AD	1N5406	800V; 3A; Standard Recovery	Micro Commercial Co	1N5406-TP
1	D2	Diode; TH; TO-220	IDH05S60C	600V; 4A; SiC Schottky	Cree	
2	D7, D8	Diode; SM; SMA	S1M	1kV; 1A; Standard Recovery	Diodes Inc	S1M-13-F
1	L2	Ind; TH; -	880µ	Core:Magmetics 0077071-A7 HT22; ; AWG16,85T.	-	Intersil Engineering
2	L3, L4	CMC; TH; -	2.2m	Common Mode Choke	Wurth	7448258022
1	Q1	MOSFET; TH; TO-247	IPW60R125CP	650V; ; N-Chan	Infineon	
1	Q3	MOSFET; TH; SO-8-EP	FDMS7650DC	650V; ; N-Chan	Fairchild	
3	Q4, Q5, Q6	MOSFET; SM;	DMG1026UV-7	60V; 400mA; N-Chan, Dual	Diode Inc	
1	RV1	Rv; TH; Radial	MOV	Varistors	Panasonic-ECG	ERZV14D391
2	R1, R3	Res; SM; 1206	2M	5%;		
1	R2	Res; SM; 0603	2.2	1%;		
1	R4	Res; SM; 0603	51k	1%;		
1	R5	Res; TH; Axial	0.22	1W; 5%; WW	Yageo	KNP100JR-73-0R22
2	R6, R10	Res; SM; 1206	3.3M	1%;		
9	R7, R14, R21, R25, R31, R32, R47, R49, R50	Res; SM; 0603	10k	1%;		

Bill of Materials (Continued)

QTY	REFERENCE DESIGNATOR	TYPE/PACKAGE	VALUE	VOL/TOL/MAT	MANUFACTURER	MANUFACTURER PART #
2	R8, R11	Res; SM; 1206	470k	1%;		
1	R9	Res; SM; 0603	3k	1%;		
1	R13	Res; SM; 0603	6.2k	1%;		
1	R15	Res; SM; 0603	390k	1%;		
1	R18	Res; SM; 0603	62k	1%;		
1	R19	Res; SM; 0603	42.2k	1%;		
1	R20	Res; SM; 0603	16k	1%;		
1	R23	Res; SM; 0603	82k	1%;		
1	R24	Res; SM; 0603	30k	1%;		
1	R26	Res; SM; 0603	49.9	1%;		
2	R27, R28	Res; TH; Axial	0.11	2W; 5%; WW	Yageo	FKN200JR-73-0R1
1	R29	Res; SM; 0603	150k	1%;		
1	R30	Res; SM; 0603	59k	1%;		
2	R45, R46	Res; SM; 0603	20k	1%;		
1	R48	Res; SM; 0603	2.2k	1%;		
1	U1	IC; SM; SOIC14	ISL6731A/B		Intersil	ISL6731AFBZ or ISL6731BFBZ
1	U2	IC; SM; MSOP14	ISL28413	Quad; 2M RRIO OpAmp	Intersil	ISL28413FVZ

PCB Layout

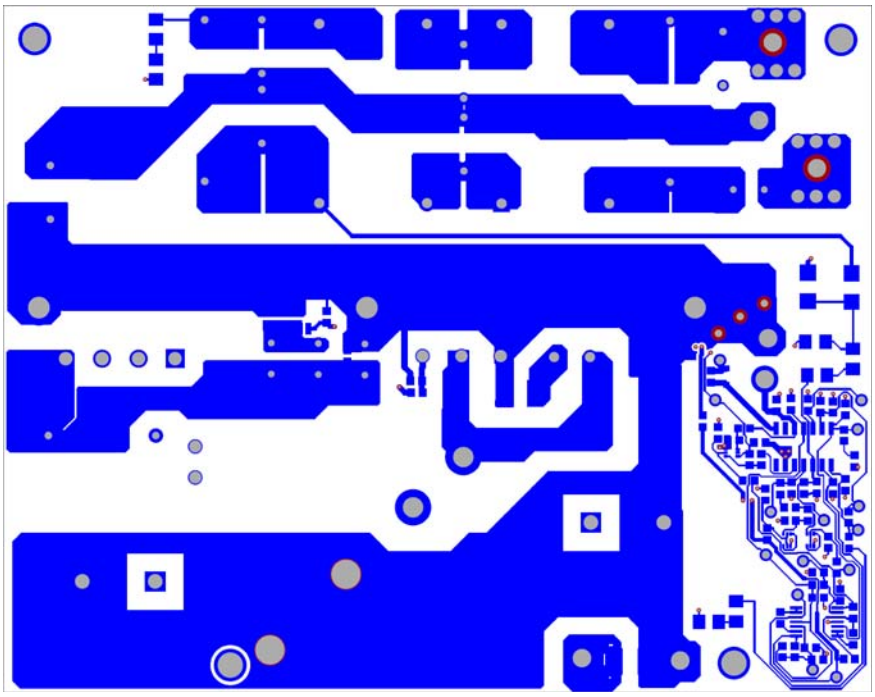


FIGURE 10. TOP LAYER

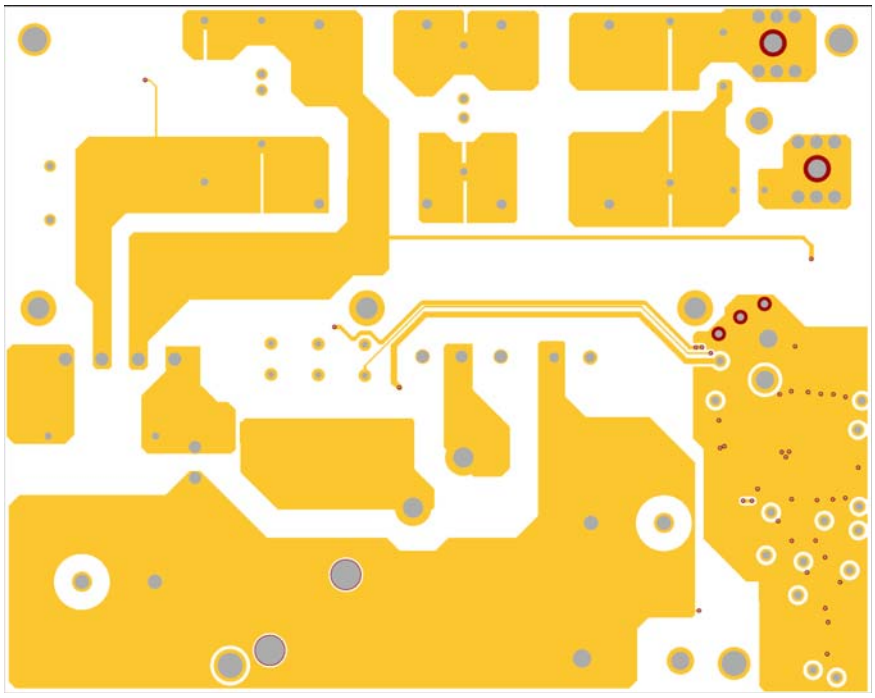


FIGURE 11. BOTTOM LAYER

Assembly Drawing

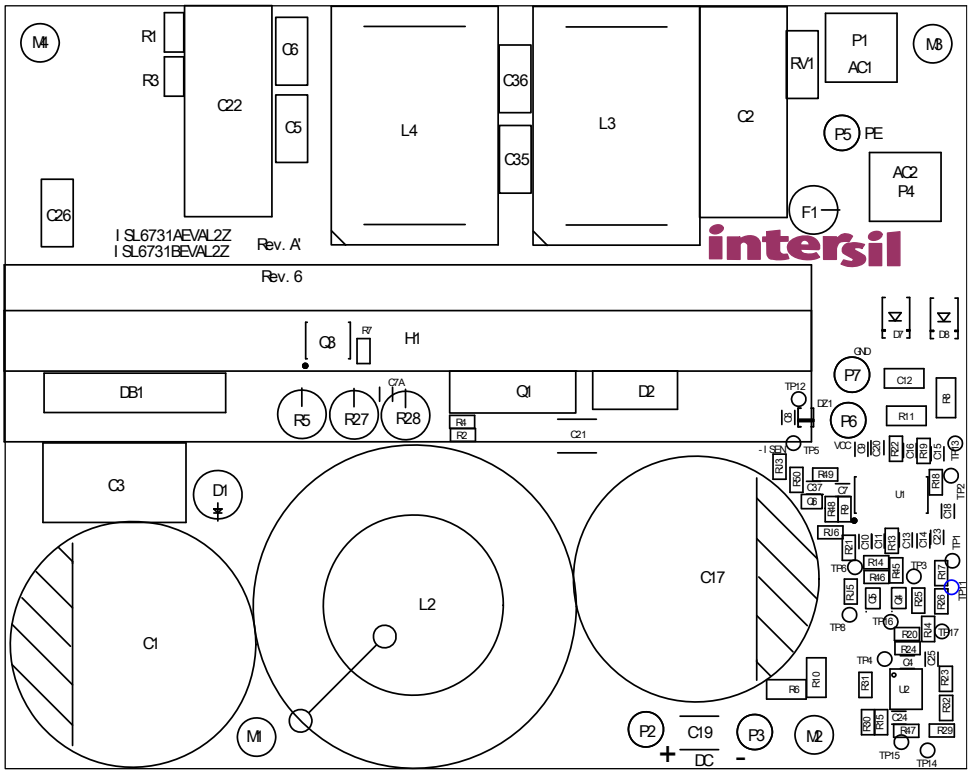


FIGURE 12. ASSEMBLY ON TOP

Performance Curves and Typical Waveforms

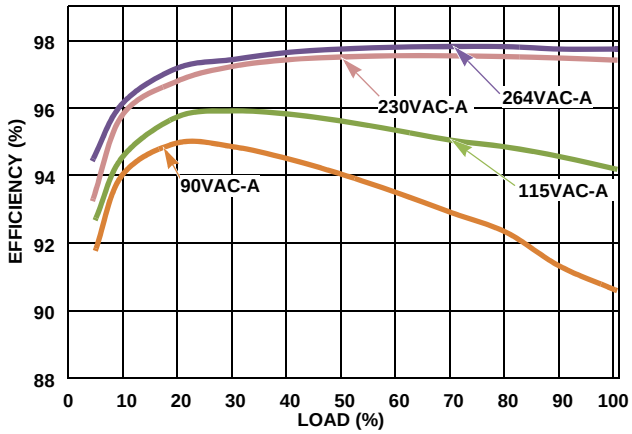


FIGURE 13. EFFICIENCY vs LOAD, ISL6731AEVAL2Z

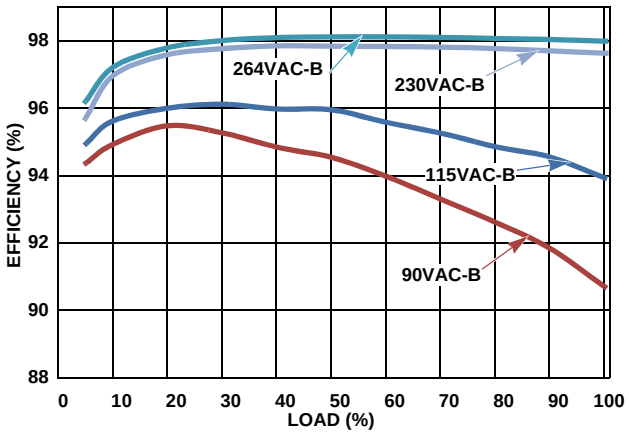


FIGURE 14. EFFICIENCY vs LOAD, ISL6731BEVAL2Z

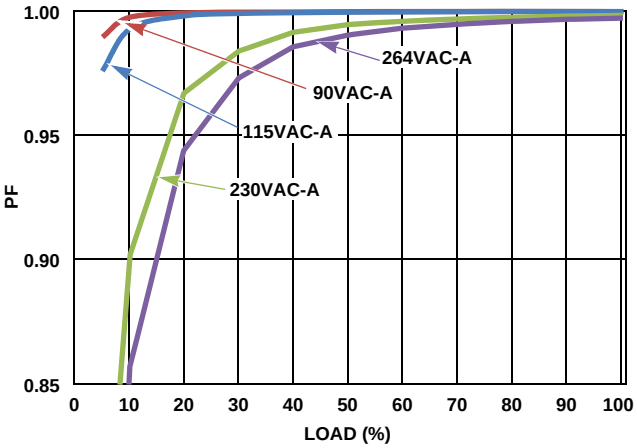


FIGURE 15. POWER FACTOR vs LOAD, ISL6731AEVAL2Z

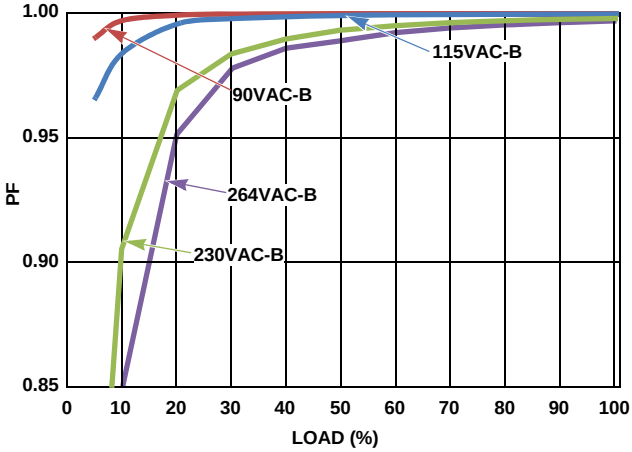


FIGURE 16. POWER FACTOR vs LOAD, ISL6731BEVAL2Z

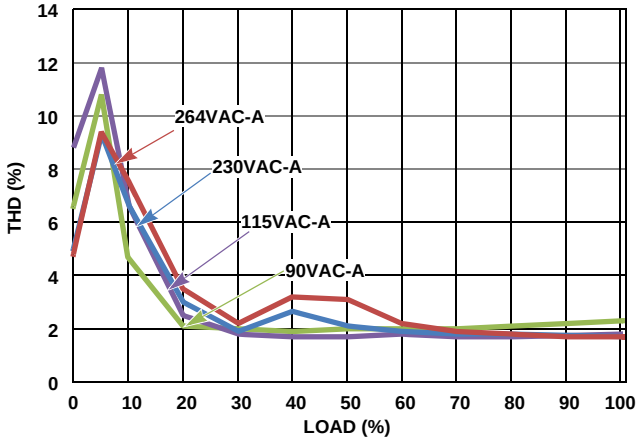


FIGURE 17. THD vs LOAD, ISL6731AEVAL2Z

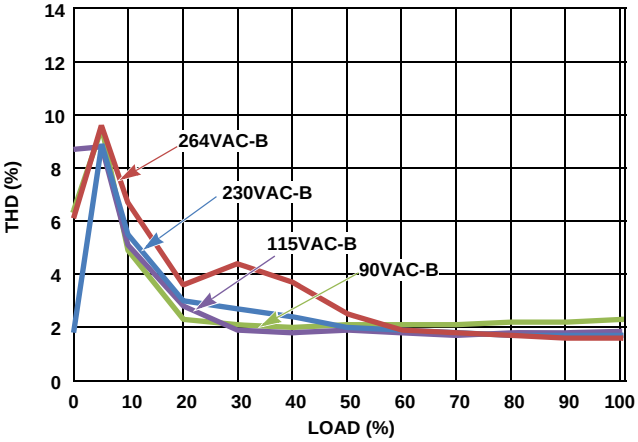


FIGURE 18. THD vs LOAD, ISL6731BEVAL2Z

Performance Curves and Typical Waveforms (Continued)

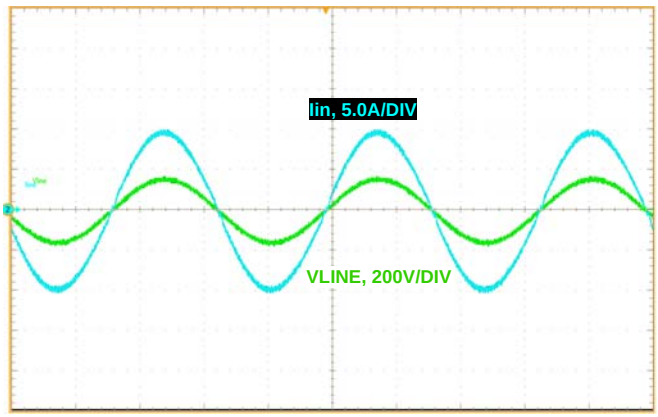


FIGURE 19. WAVEFORMS OF LINE CURRENT AND VOLTAGE (115V/FULL LOAD)

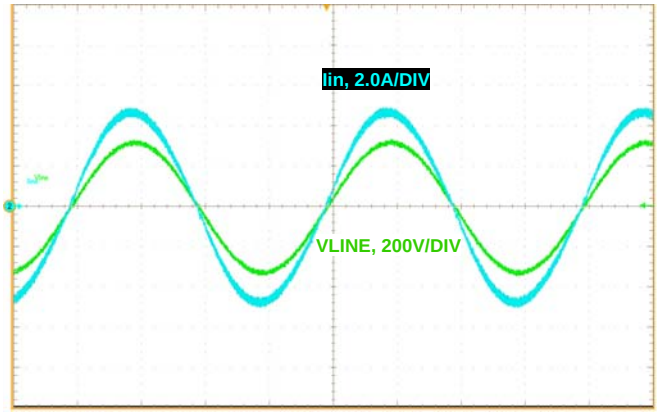


FIGURE 20. WAVEFORMS OF LINE CURRENT AND VOLTAGE (230V/FULL LOAD)

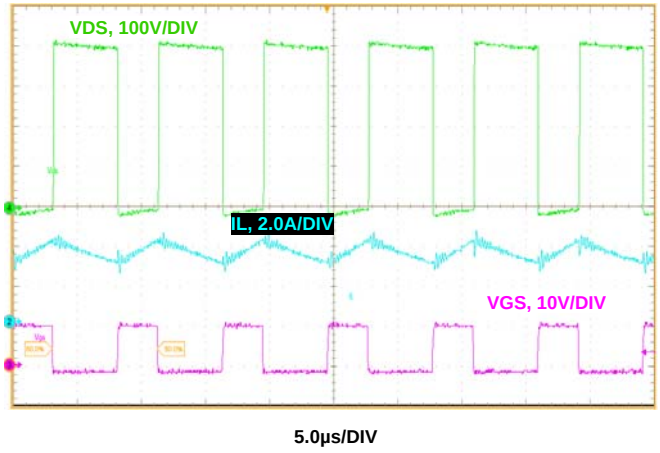


FIGURE 21. SWITCHING WAVEFORMS