FemtoClock®2 Debug Guide

This guide assists users through the process of debugging and bringing up evaluation boards for FemtoClock2 devices such as the RC32504A and the RC22504A. Troubleshooting steps are provided for common issues related to device communications, hardware setup, and performance.

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1. Unable to Connect to Renesas IC Toolbox

FemtoClock2 devices are configured using either I2C or SPI programmable interfaces through the SCL_SCLK and SDA_SDIO pins. The polarity of the OE_nCS pin determines the selection of the communication protocol. The default setup on the Renesas evaluation board uses I2C to communicate with the device through a USB-C interface. Through the Renesas IC Toolbox software, a connection can be established and the device can be setup to run user created configurations. The following looks at possible issues that may arise when trying to communicate with the device.

1. Ensure the latest Renesas IC Toolbox software and FemtoClock2 GUI are installed on the connected computer.
   - The versions of each are found by clicking on the help menu button at the top of the screen and going to the about selection.
   - The latest version of the Renesas IC Toolbox software and FemtoClock2 GUI can be located on the FemtoClock®2 Evaluation Kit page.
2. If using the evaluation board, ensure that the USB-C cable is securely connect to the evaluation board and the green LED near the connector is illuminated. The LED is an indicator if the device is receiving power from the USB connection. If the green LED is not on, then disconnect the USB cable from the EVB and reconnect it. Also, try another USB port on the computer.
3. Check to see if the jumpers are in the correct orientation for connection between the onboard serial device and the FemtoClock2 device. See the evaluation board user guide for more information regarding jumper orientations:
4. Ensure that the onboard serial device is detected by the computer connected through the device manager.
   - If the device is not detected by the device manager, then
     - disconnect the USB cable from the EVB and reconnect it.
     - try another USB port on the computer.
     - try another USB cable.
     - try a different PC.
     - in each case, wait a few seconds to allow Windows to recognize the new connection.

- If above actions do not show the device connected, it may be an issue with the evaluation board. Contact Renesas support for more help.

5. The VDDD domain is responsible for handling the device communication. Ensure that it is powered by either 1.8V or 3.3V.
6. If the device is configured for SPI access, then check the polarity of the OE_nCS pin. Ensure that the I2C pull-up resistors are not active.
7. If using I2C, then ensure the signals are pulled-up to VDDD.
8. Probe the SDA and SCL signals while attempting to connect. The device should both receive the communication signals and send an acknowledgement signal back to the serial device.

2. Outputs Not Toggling

The main reason outputs are unseen is that the APLL is not locked to a valid input reference. If that is not the issue, then it is important to double-check the configuration setup, power domains, and hardware setup.

1. If the APLL Is unlocked, the device will disable the outputs. Ensure there is a signal at either RefClk or OSCI and that it is correctly selected in the configuration.
2. Check the lock status of the APLL by probing the LOCK pin. See the Pin Descriptions table in the respective device datasheet for more information on the LOCK pin.
3. If using Renesas IC Toolbox, check to see if the output is enabled in the overview page under the output section.
4. Power cycle the device and check the outputs before loading a configuration. The device will default to the OTP configuration and begin outputting if there is a valid and locked APLL reference.
5. Ensure the device is powered correctly. If using the evaluation board, then double check the jumpers to see if the corresponding VDDO is powered by looking at the power enable jumper.
6. Probe the VDDO pin near the device to ensure that it has the correct voltage. This will verify that the power LDO is functioning correctly.
7. Check in the configuration if a GPIO is used as an OE (output enable). If so, then verify that the GPIO voltage level is correct for the enabled output.
8. Create a new configuration and program the output to a new frequency.
9. Ensure that the device measuring the output is rated for the frequency.
10. If the output is showing up on the measurement device but the power is low (< -10dBm), then check to see if both legs of the output are toggling.
    - If both are toggling, then ensure that the output type matches the programmed terminations.
    - Ensure that the measurement device is rated for the output signal type and amplitude.
    - If using a balun, then check the frequency rating on it and the possible power loss across it.
    - If all is correct, then double-check the cabling.

3. Outputs Frequencies are Incorrect

The FemtoClock2 device will track the frequency accuracy of its input clocks. If the device is running in synthesizer mode, then the output frequency will track the APLL reference frequency. If the device is setup for jitter attenuator mode, then the device will track the DPLL reference frequency.

1. Ensure the tracked reference is connected and toggling.

   Use the LOCK pin to detect a lock on either the APLL or DPLL.

2. Ensure the reference frequency is correct.

   For example, if the device is in synthesizer mode and the reference is set to 50MHz in the configuration, but is 49.152MHz on board, then the output will be offset.

3. Check to see if the measurement device is tracking the actual output frequency and not of a harmonic.

   The output power is a good indicator for this. Lower than -10dBm indicates a possible issue.

4. Use an accurate instrument (frequency counter or a phase noise system) to measure the frequency. Oscilloscopes are fine for coarse measurements, but they are not as accurate.

4. Phase Noise Does Not Match the Datasheet

The datasheet's phase noise plot was captured with a fractional jitter attenuator configuration outputting 156.25MHz.

1. Check the output power shown on the plot. Ensure that the power is high enough to get a valid reading from the phase noise analyzer.
   a. If the power is lower than -10dBm, then check to see if the output terminations in the device configuration match the chosen output type.
   b. Ensure that the phase noise analyzer input is rated for the output type being used and has the correct input terminations.
   c. Ensure that the selected frequency band of the phase noise system matches the signal under test. An incorrect band selection can create invalid measurements.
2. If the close-in noise is high, then compare the output to the input references of the device.
   a. Output phase noise can be affected by the input reference all the way up until the APLL bandwidth offset.
   b. If the input reference signal is noisy then the close-in noise of the output will be noisy as well.
   c. Check the signal integrity on the input reference. Poor signal integrity, such as a missing 50Ω termination, can cause close-in phase noise to increase.
3. If using Renesas IC Toolbox, then ensure that the TOP.APLL.APLL_FB_SDM_CNFG.apll_fb_sdm_cnfg bitset is unlocked in the configuration view.
   a. The APLL SDM order is optimized in the Renesas IC Toolbox software to give the best performance by being automatically set based on how the APLL is configured.
4. Contact Renesas support for device and hardware setup configurations used for respective device's phase noise plots.

5. Revision History

Revision	Date	Description
1.0	Apr 26, 2021	Initial release.

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