Errata

SLG46721

CE-GP-022

Abstract

This document contains the known errata for SLG46721 and the recommended workarounds.

1 Information

Table 1: Information Table

Package(s)	20-pin STQFN: 2 x 3 x 0.55 mm, 0.4 mm pitch

2 Errata Summary

Table 2: Errata Summary

Issue #	Issue Title
1	Long RC OSC Settling Time
2	LATCH Block nRESET Incorrect Operation
3	Glitches on ACMP Output
4	Delay Lock-up by a Short Pulse
5	Device Damage by High Input Voltage on External Vref PIN of ACMP
6	FILTER Cell does not Filter Out Glitches
7	Extra Short RC OSC Settling Time

3 Errata Details

3.1 Long RC OSC Settling Time

3.1.1 Effect

RC OSC, Counter, Delay

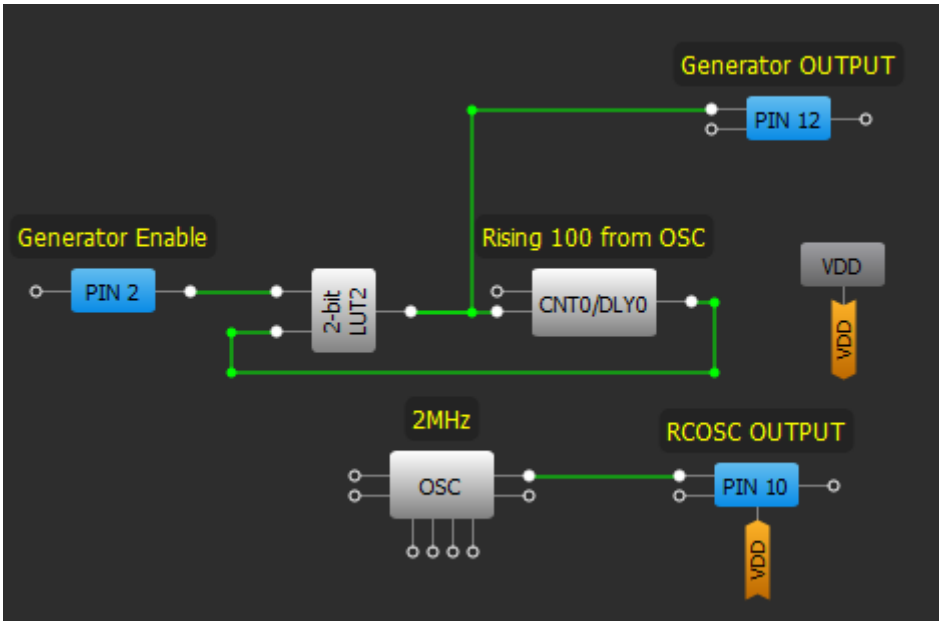
3.1.2 Conditions

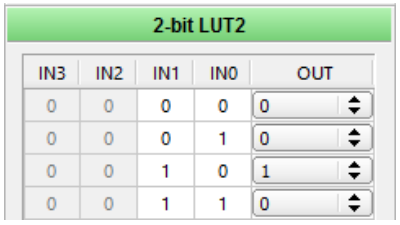
RC OSC configured as 2 MHz with Auto Power On.

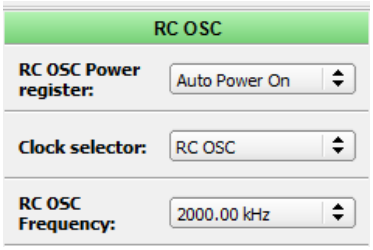
3.1.3 Technical Description

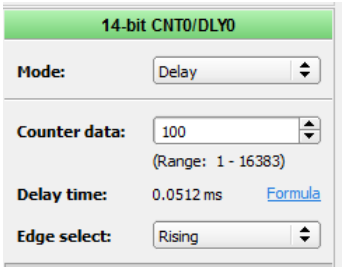
An example of such issue is in the following configuration:

The RC OSC has a longer settling time when configured as 2 MHz with Auto Power On in the designs that have very short RC OSC disable time.

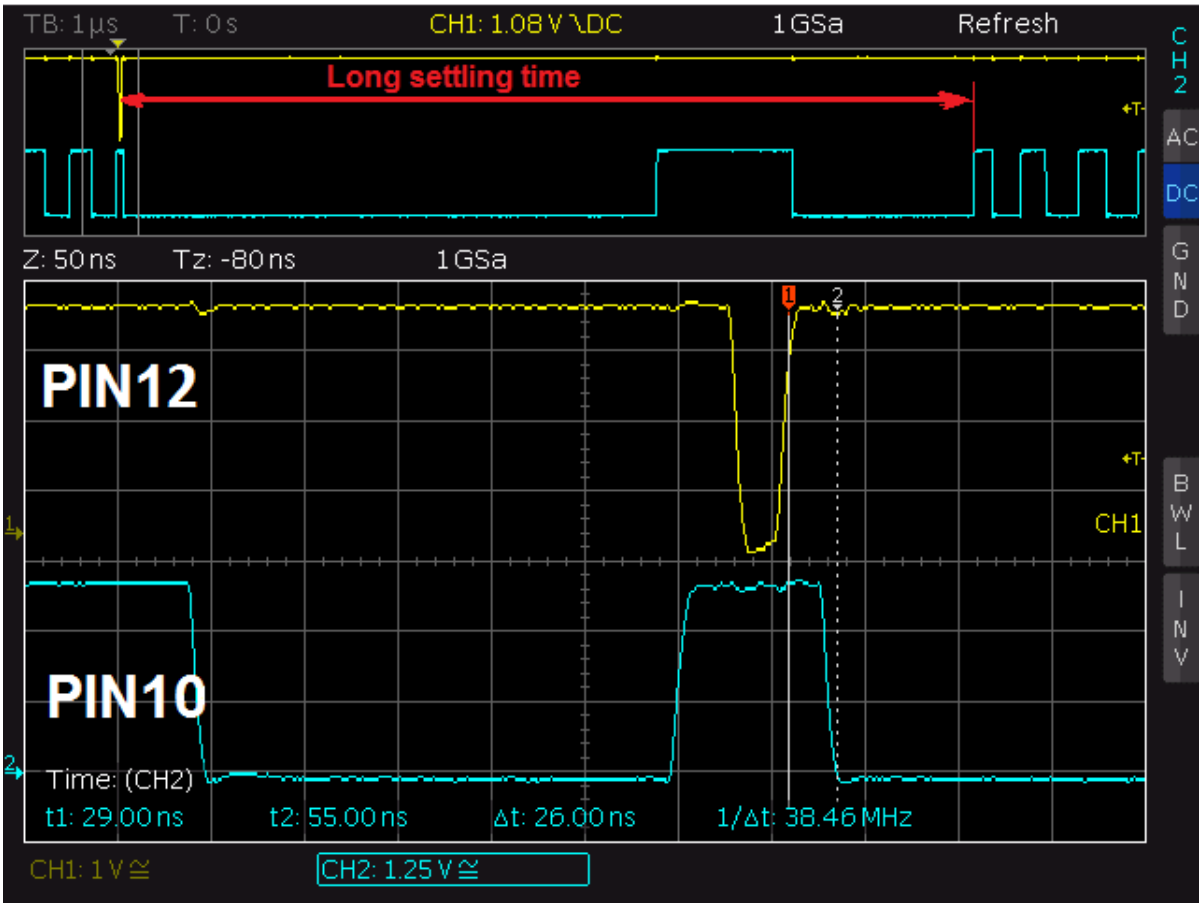








The configuration shown above generates a periodical signal with a frequency defined by the Delay cell and started by a HIGH signal on PIN2. The issue becomes apparent in a longer settling time when the scheme generates short pulses (Delay is configured as a rising edge delay only). See waveform below.

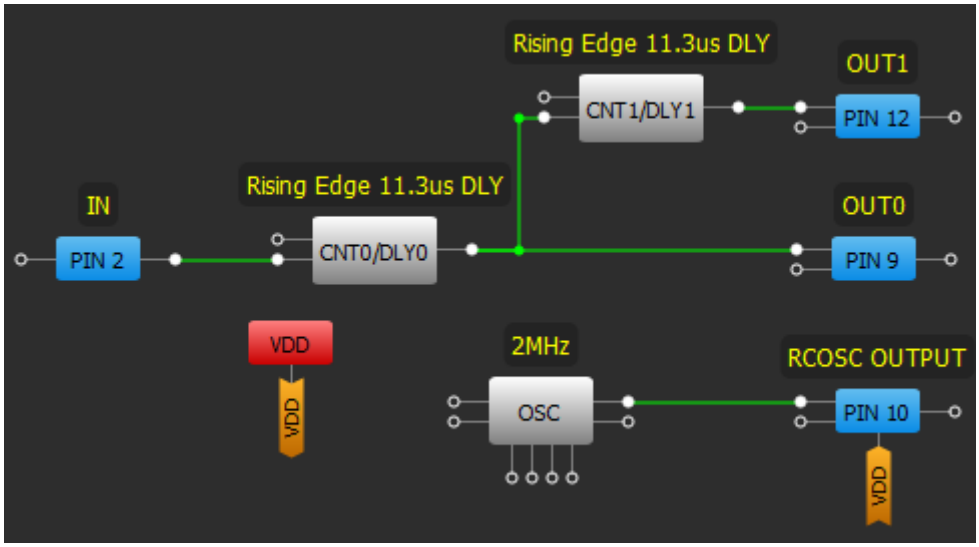


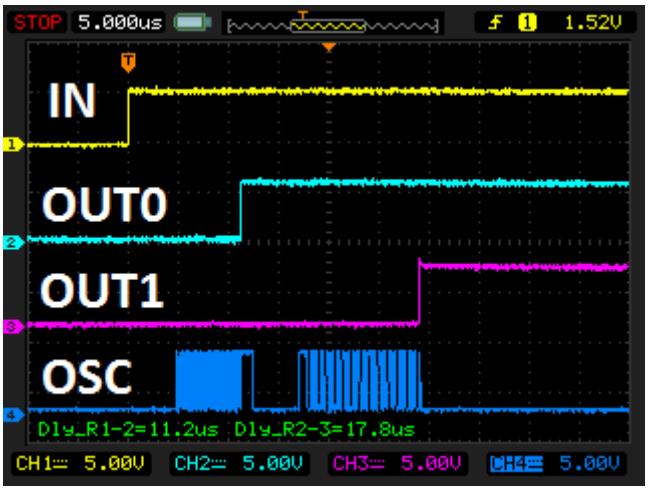
Channel 1 – 2-bit LUT0 output; Channel 2 – RC OSC output

Such behavior will lead to substantial error in period calculations if the delay time is relatively small.

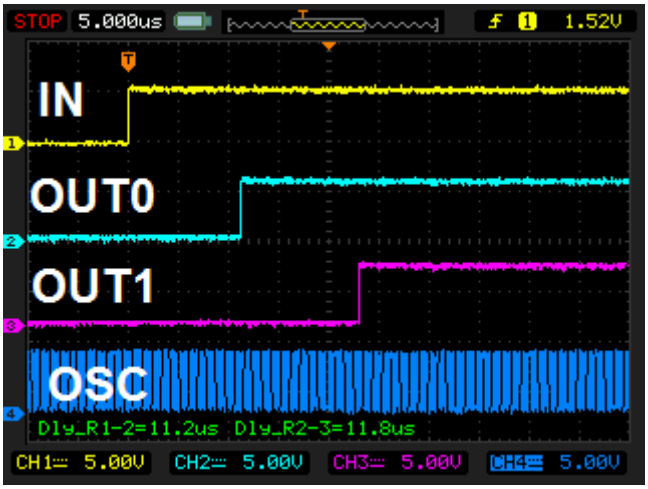
The same situation occurs while using two connected delays (all edge detect types except for a pair “Rising edge DLY – Falling edge DLY”).

In the following example, Delay0 and Delay1 are configured in the same way. However, Delay1 time is 17.8 us instead of expected 11.3 us (Delay0 time).



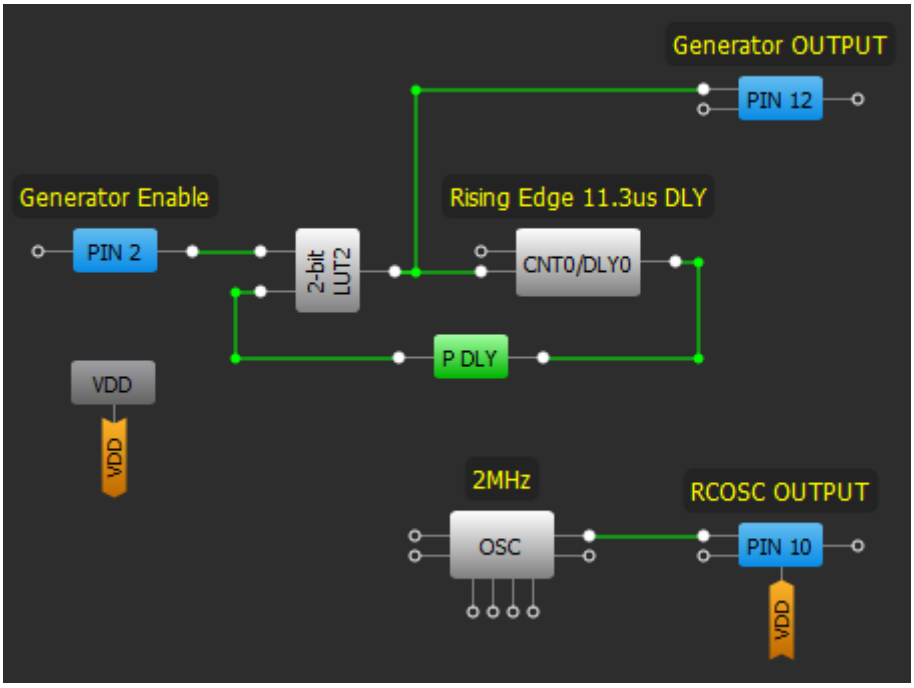


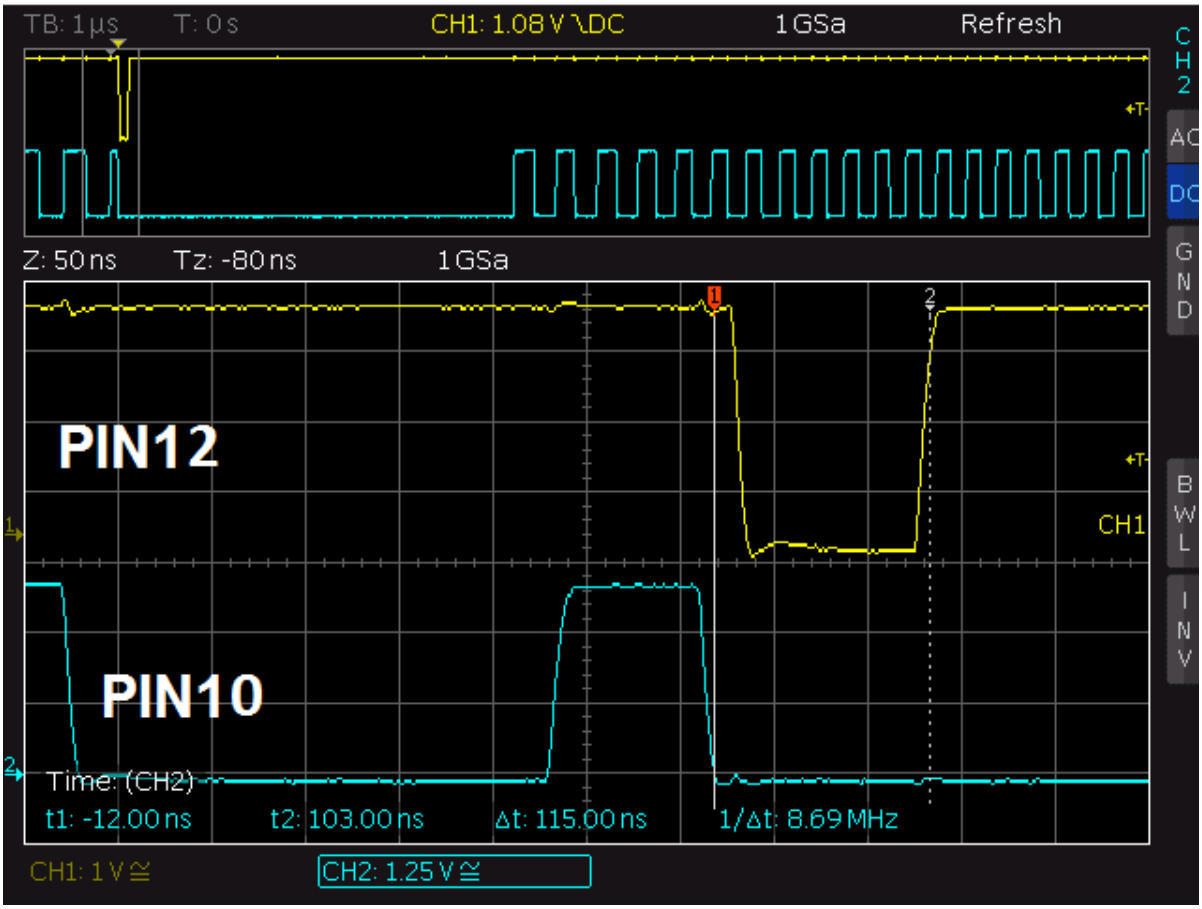
If there are some inner blocks which use RC OSC at the moment or RC OSC is forced power on when such error appears, RC OSC will be operational and delay value will be proper.



3.1.4 Workaround

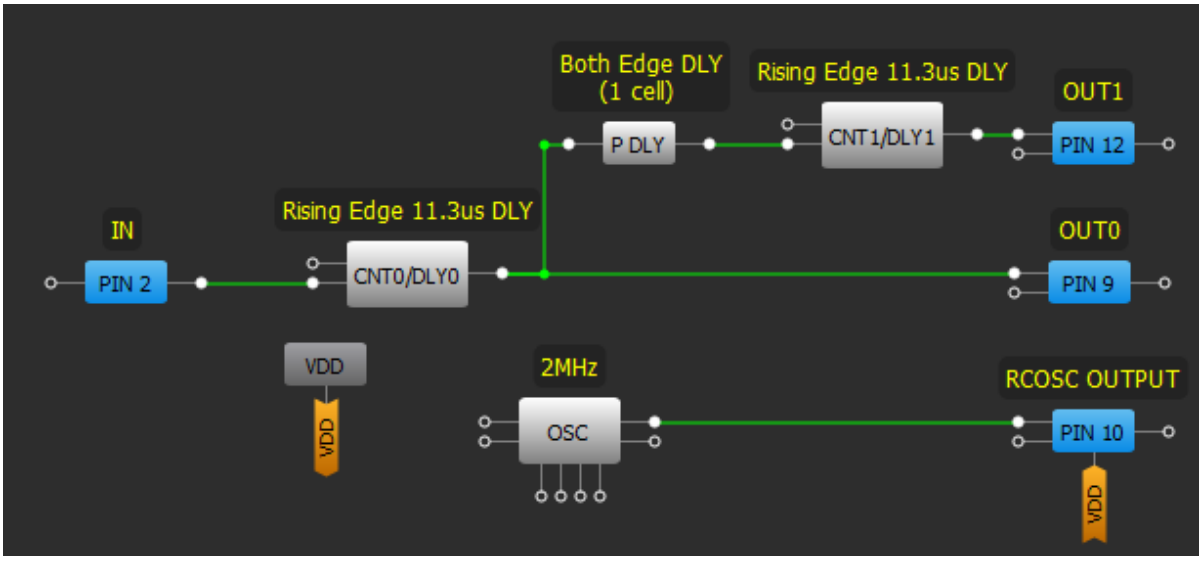
- In first case use block with longer propagation time.





Channel 1 – 2-bit LUT0 output; Channel 2 – RC OSC output

- using two delays in series (except for a pair “Rising edge DLY – Falling edge DLY”) use one Filter cell or P DLY between delay blocks. Using LUTs won`t help in this case.



- use the “Force power on” RC OSC power control option to make the RC OSC operate at all times.

3.2 LATCH Block nRESET Incorrect Operation

3.2.1 Effect

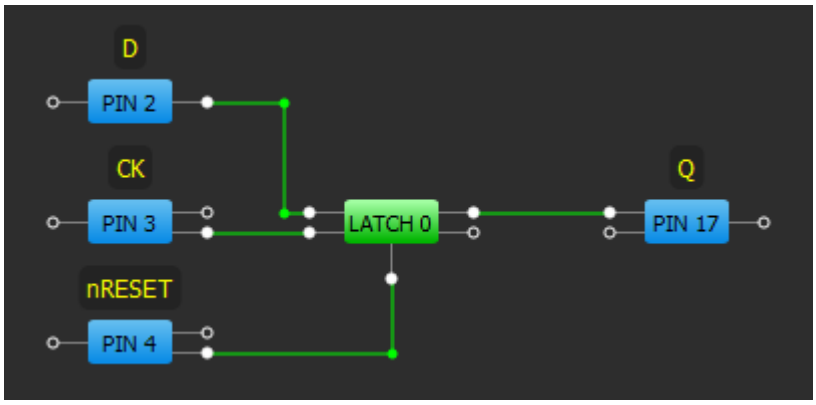
LATCH

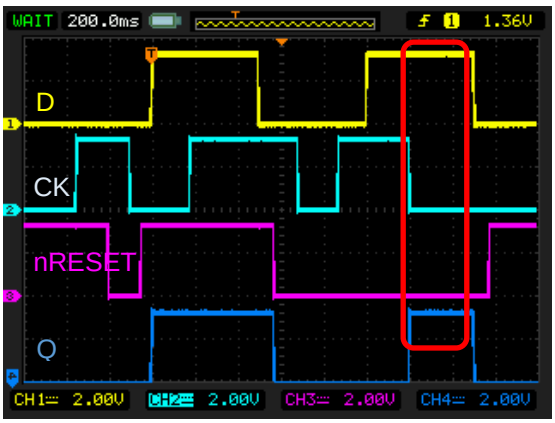
3.2.2 Conditions

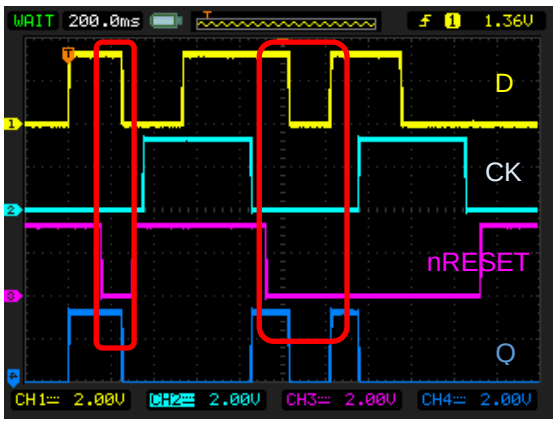
When nRESET input is set LOW.

3.2.3 Technical Description

The reset function in LATCH blocks does not operate correctly. This can be described as function failure when nRESET input is set LOW.



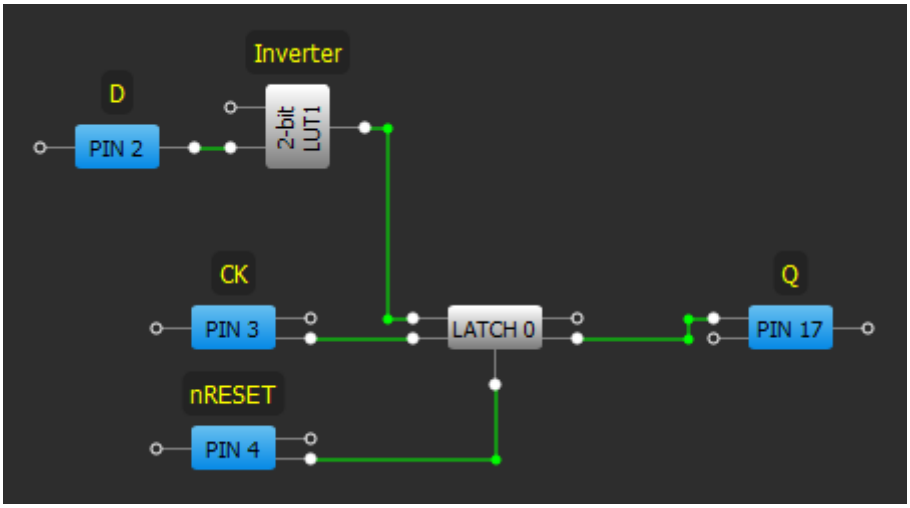


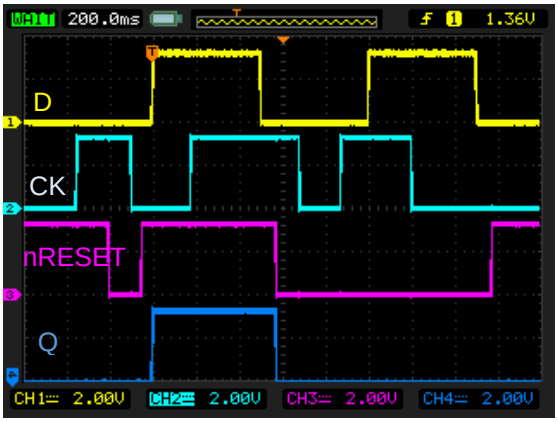


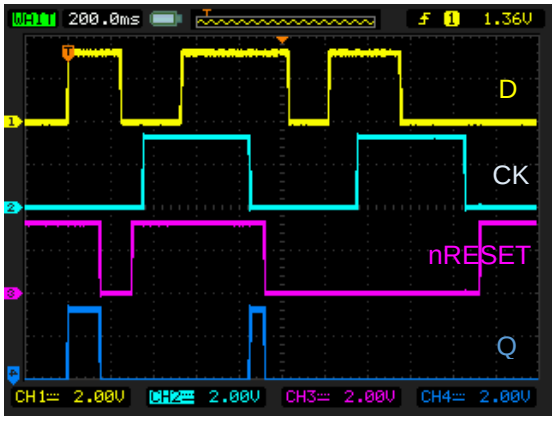
The scope shots shown above show the incorrect nRESET function operation marked with red rectangles. From these waveforms can be seen that the reset function operates only when the CK signal is HIGH, in all other cases it is inoperational.

3.2.4 Workaround

- Avoid using nRESET function in LATCH blocks in SLG46721/722 devices, if possible, use SLG46110/120 devices, where this function operates correctly.
- Use nSET configuration, initial state HIGH, add inverter on D input and use nQ (inverted) output of the LATCH block:







3.3 Glitches on ACMP Output

3.3.1 Effect

ACMP

3.3.2 Conditions

Conditions of glitches appearing are determined by IN- voltage, V_{DD} value and V_{DD} Ramp (see example in table below).

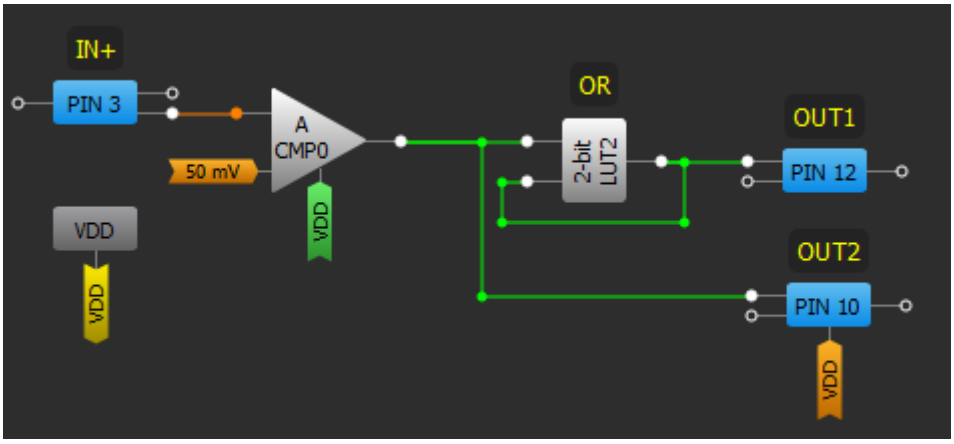
IN- Voltage, mV	V_{DD}, V	V_{DD} Ramp Time	Glitch presence
50	1.8	10 us	+
50	1.8	1 s	-
50	3.3	10 us	+
50	3.3	1 s	+
50	5.5	10 us	+
50	5.5	1 s	+
600	1.8	10 us	-
600	1.8	1 s	-
600	3.3	10 us	+
600	3.3	1 s	-
600	5.5	10 us	+
600	5.5	1 s	-
1200	1.8	10 us	-

1200	1.8	1 s	-
1200	3.3	10 us	-
1200	3.3	1 s	-
1200	5.5	10 us	+
1200	5.5	1 s	-

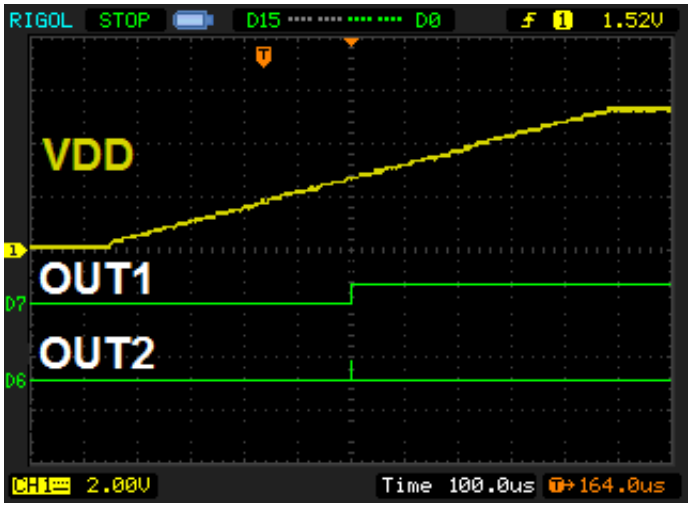
3.3.3 Technical Description

In some cases, ACMP may have short high-level glitches on its output (even if IN+ voltage is less than IN- voltage) after GreenPAK chip being powered up. Such cases may appear when using ACMP with Low Bandwidth mode enabled and Power Up is connected directly to the V_{DD}.

In order to detect such glitches, scheme with additional LUT was used. This LUT detects high level on ACMP output and stays high until chip powers down.

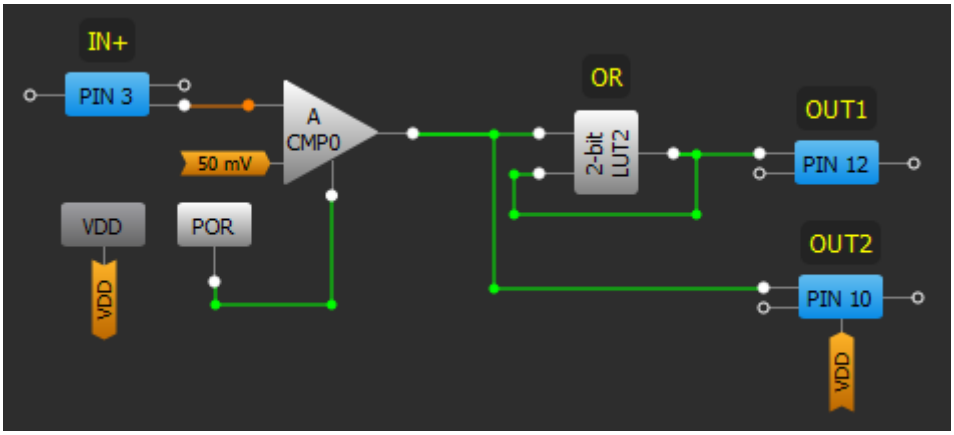


ACMP IN+ is connected to the Ground.



3.3.4 Workaround

Use POR block, connected to the ACMP's Power-Up pin. However, in this case ACMP will start working with low level output and will be able to go high only after POR goes high + ACMP power on time.



3.4 Delay Lock-up by a Short Pulse

3.4.1 Effect

Delay

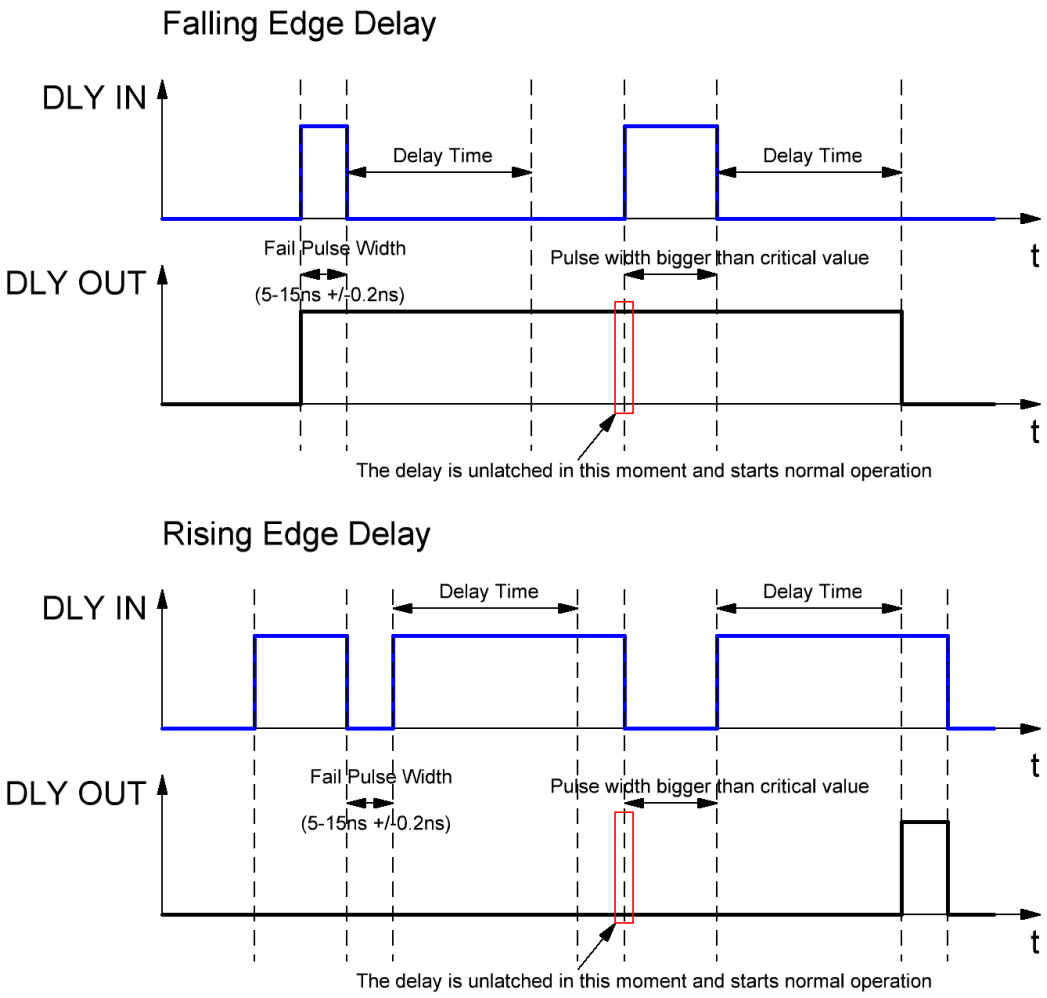
3.4.2 Conditions

When a short pulse appears on Delay input.

3.4.3 Technical Description

The delay output could be latched despite the input change when a short pulse is input. For example, if the delay cell is configured as a falling edge delay, the short pulse (see NOTE) appears on its input the delay cell output will switch from LOW to HIGH but may not switch from HIGH to LOW even after the delay time has passed.

NOTE: The pulse width varies from chip to chip and with different V_{DD} voltage. It is in range of 5-15 ns and in the window +/-0.2 ns, so it should be very precise for issue happen.



Also, note that both edge delays do not have such issue.

3.4.4 Workaround

Use P DLY/FILTER block configured as a both edge delay or FILTER.

3.5 Device Damage by High Input Voltage on External Vref PIN of ACMP

3.5.1 Effect

ACMPs

3.5.2 Conditions

Voltage higher than 2 V applied to IN- of ACMP as an external reference voltage.

3.5.3 Technical Description

The device may be damaged by the voltage higher than 2 V applied to IN- of ACMP as an external reference voltage.

3.5.4 Workaround

There is no workaround to this issue, avoid applying more than 2 V on IN- of ACMP used as external voltage reference.

3.6 FILTER Cell does not Filter Out Glitches

3.6.1 Effect

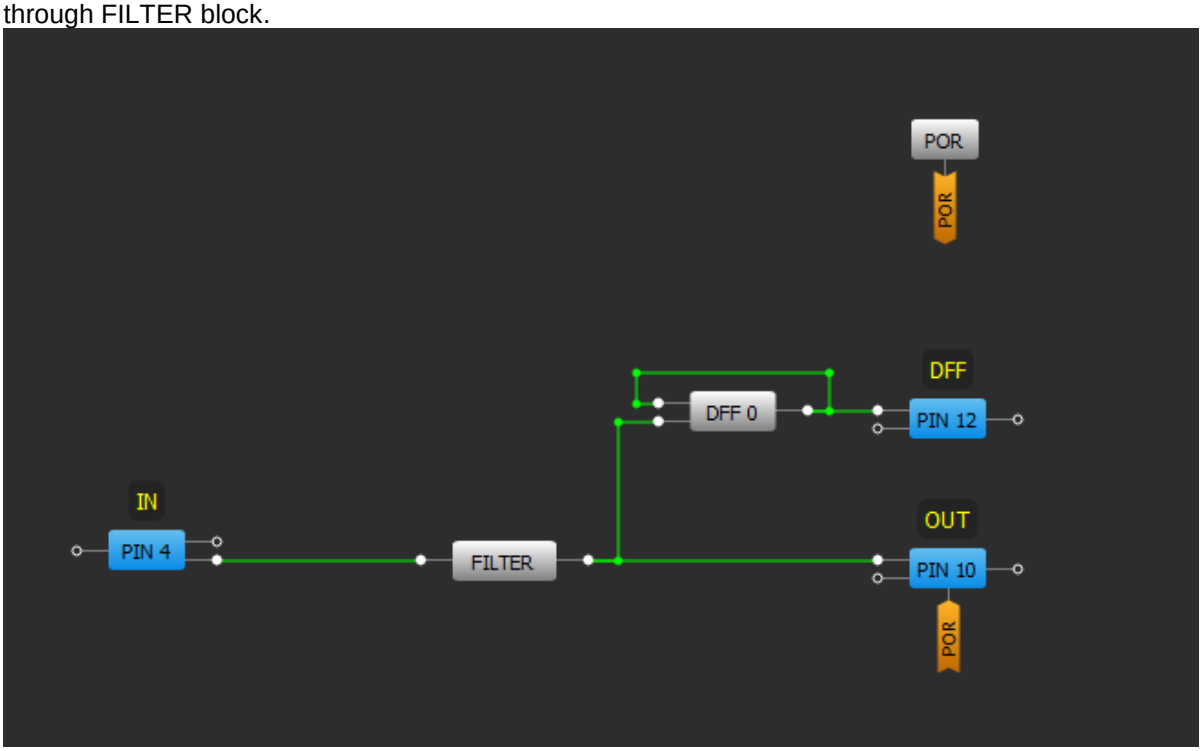
Filter

3.6.2 Conditions

If clock type high frequency input comes in.

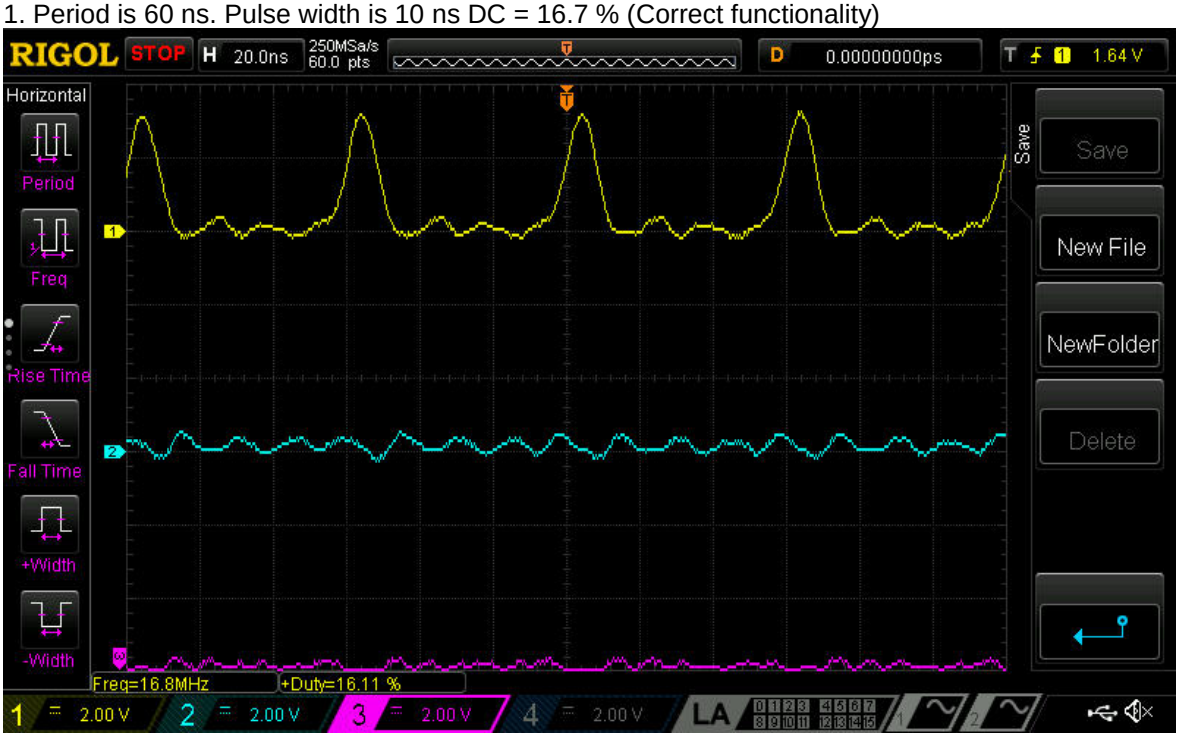
3.6.3 Technical Description

If clock type high frequency input comes in, the FILTER cell may not filter out it. There are several factors like input frequency, duty cycle and LOW duration in such signal that may lead to its passing through FILTER block.

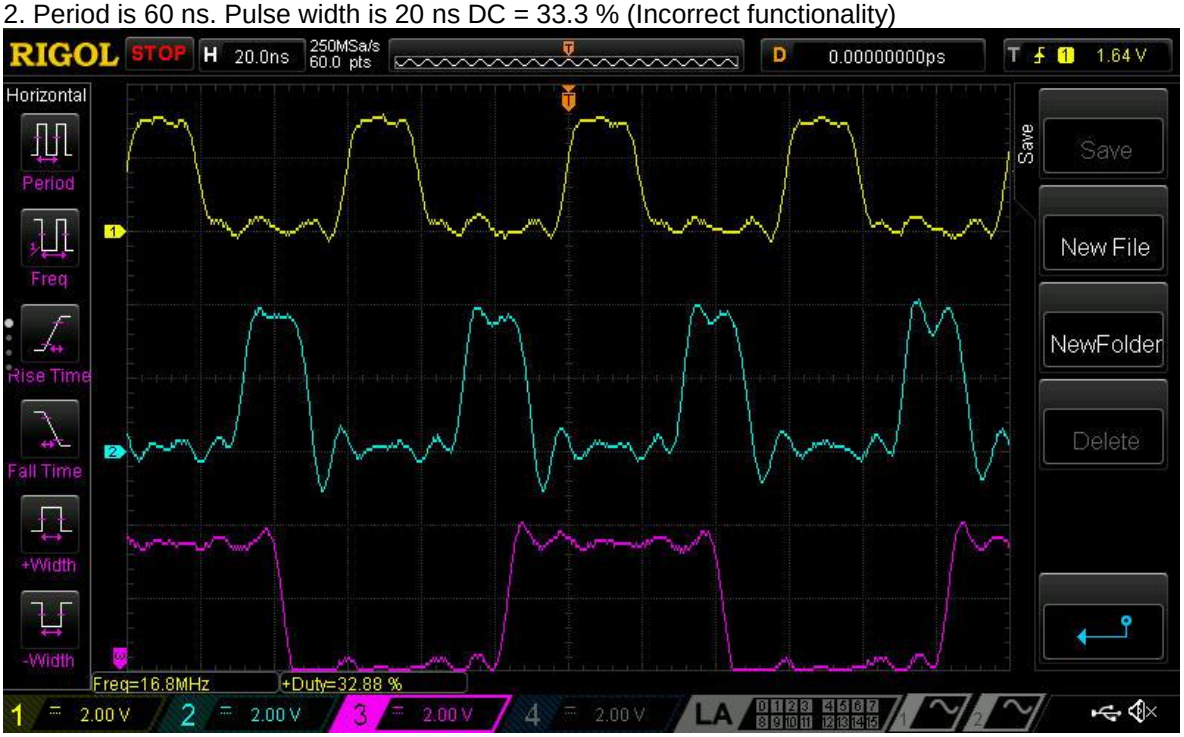


Channel 1 (yellow/top line) – PIN#4 (IN)
Channel 2 (light blue/2nd line) – PIN#10 (OUT)
Channel 3 (magenta /3rd line) – PIN#12 (DFF)

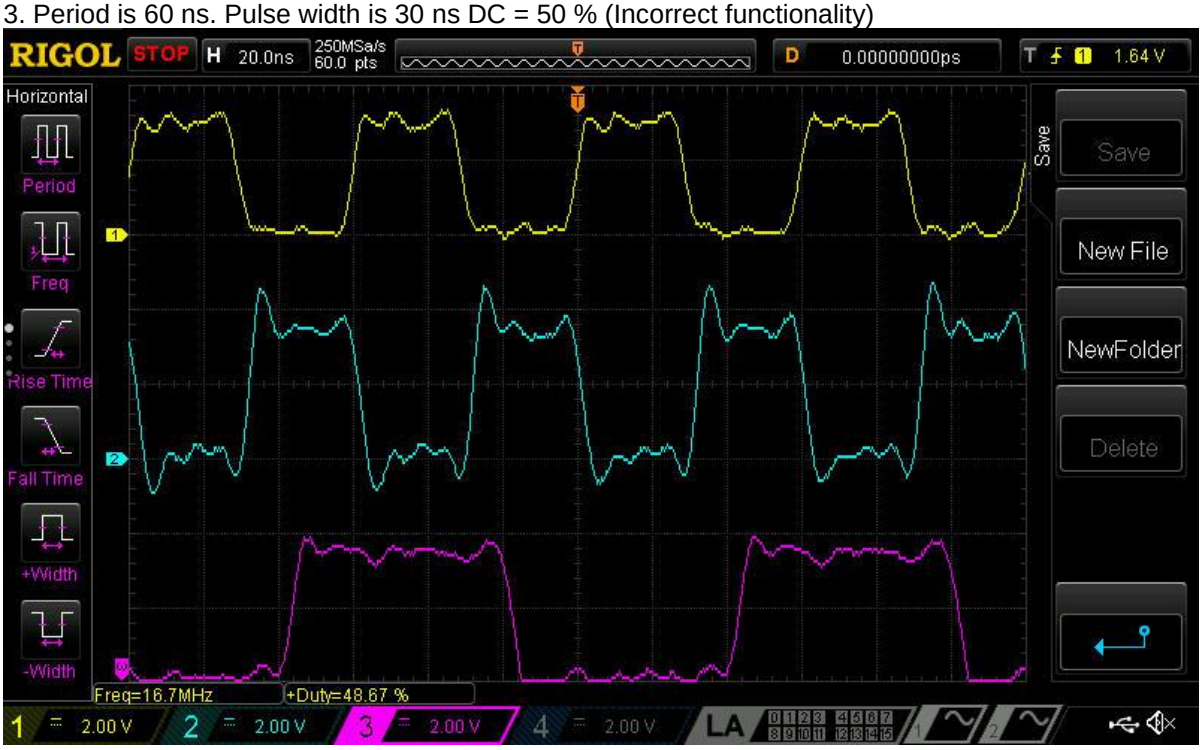
1. Period is 60 ns. Pulse width is 10 ns DC = 16.7 % (Correct functionality)



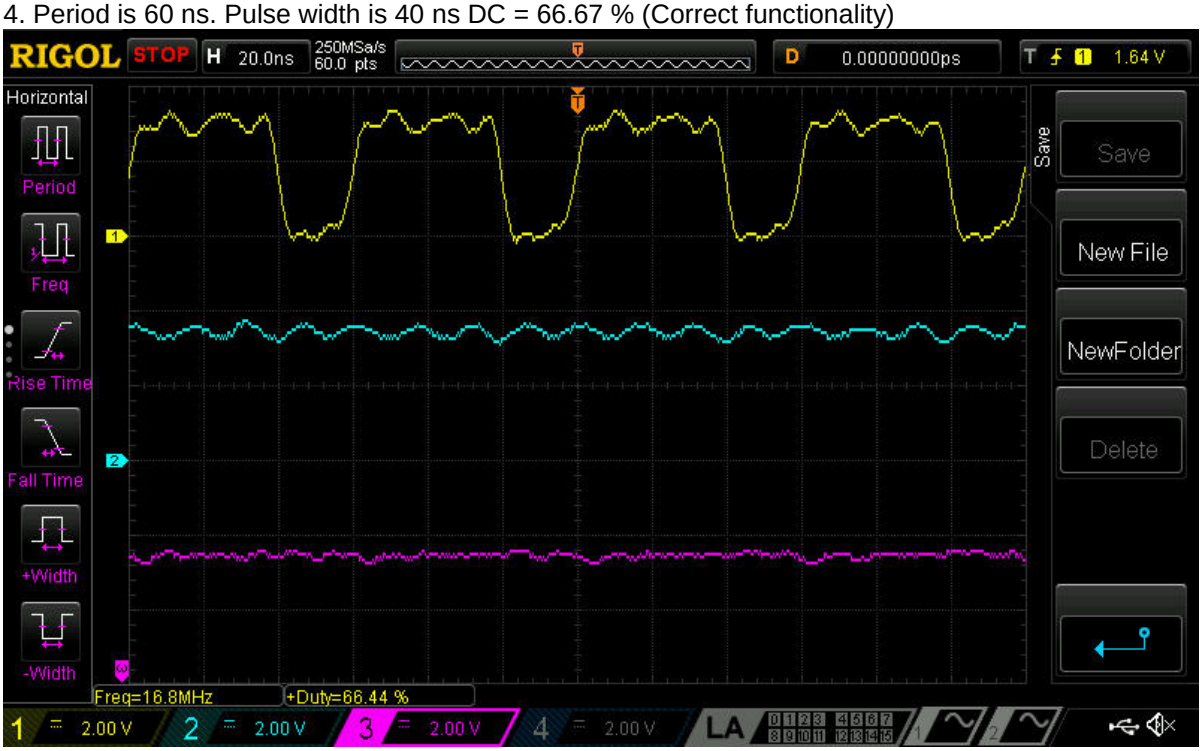
2. Period is 60 ns. Pulse width is 20 ns DC = 33.3 % (Incorrect functionality)



3. Period is 60 ns. Pulse width is 30 ns DC = 50 % (Incorrect functionality)



4. Period is 60 ns. Pulse width is 40 ns DC = 66.67 % (Correct functionality)



3.6.4 Workaround

Currently there is no workaround for this issue. Filter block is good at filtering short spontaneous glitches. It is intended to be used in series connection before the delay cell to avoid its latching (see issue #5).

3.7 Extra Short RC OSC Settling Time

3.7.1 Effect

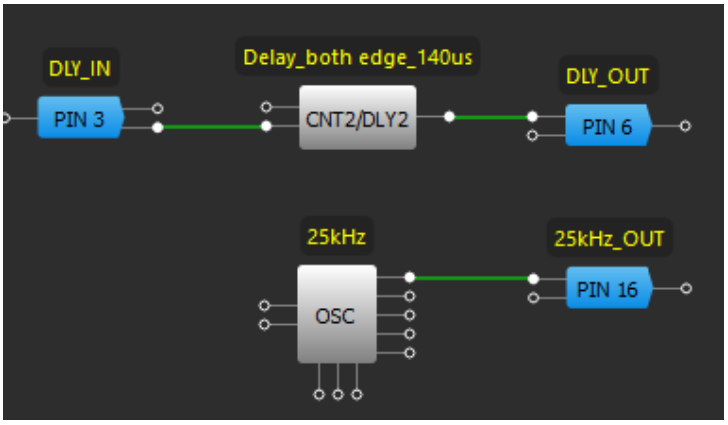
RC OSC, Counter, Delay

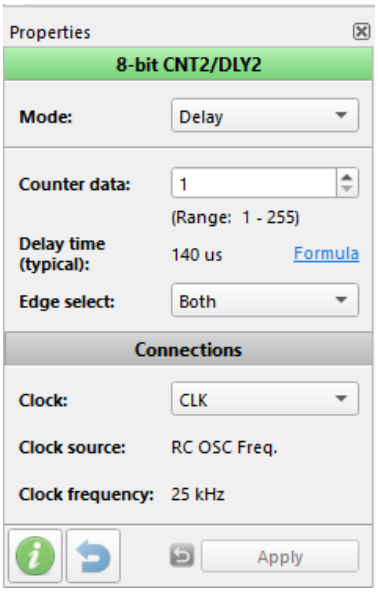
3.7.2 Conditions

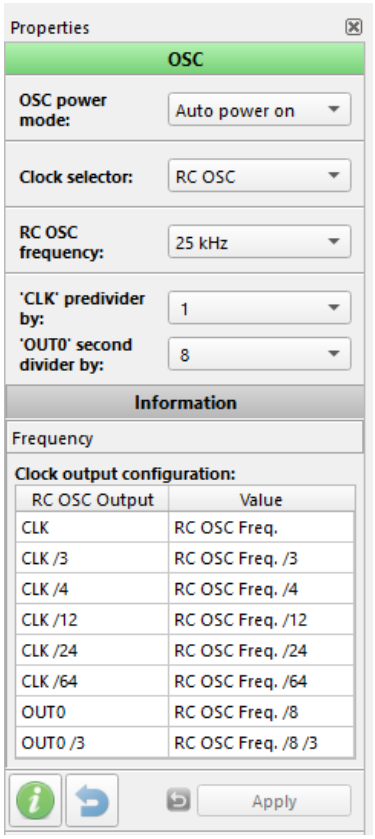
OSC configured as 25 kHz with Auto Power On.

3.7.3 Technical Description

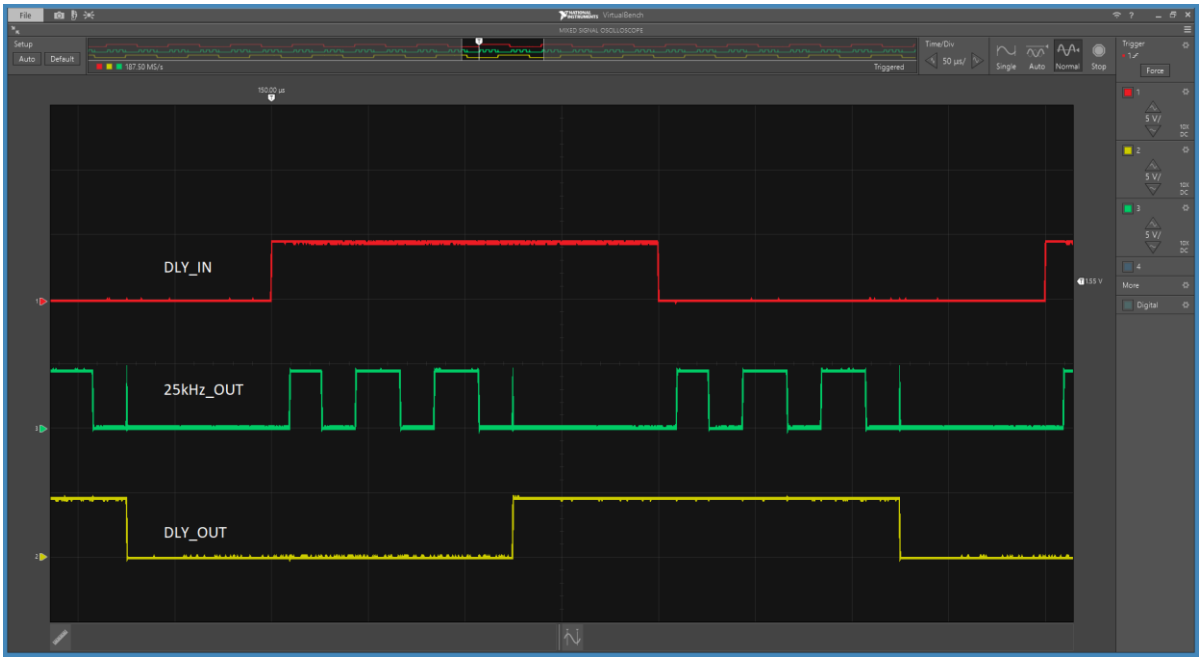
The first period of the RC OSC can be very short when OSC configured as 25 kHz with Auto Power On in the designs. This can occur when V_{DD} is above 4.0 V. Critical for CNT/DLY with a low counter data (less than 10) or if it is necessary to use the frequency of the OSC to clock external elements. An example of such issue is in the following configuration:



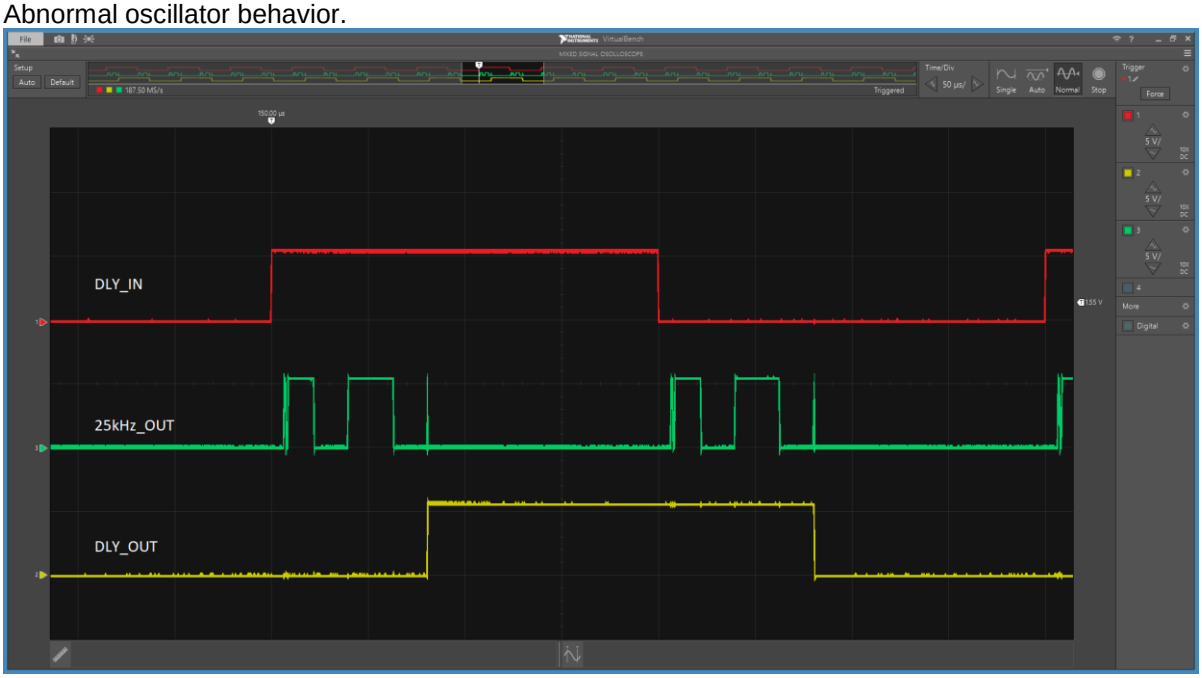




Normal oscillator behavior.



Abnormal oscillator behavior.



3.7.4 Workaround

- Avoid V_{DD} higher than 4 V
- Force ON OSC

Document Revision History

Revision	Date	Description
1.1	11-Mar-2022	Fixed typos Renesas rebranding
1.0	30-Dec-2021	Added issues #7 Updated according to Dialog's format

Status Definitions

Status	Definition
DRAFT	The content of this document is under review and subject to formal approval, which may result in modifications or additions.
APPROVED or unmarked	The content of this document has been approved for publication.

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