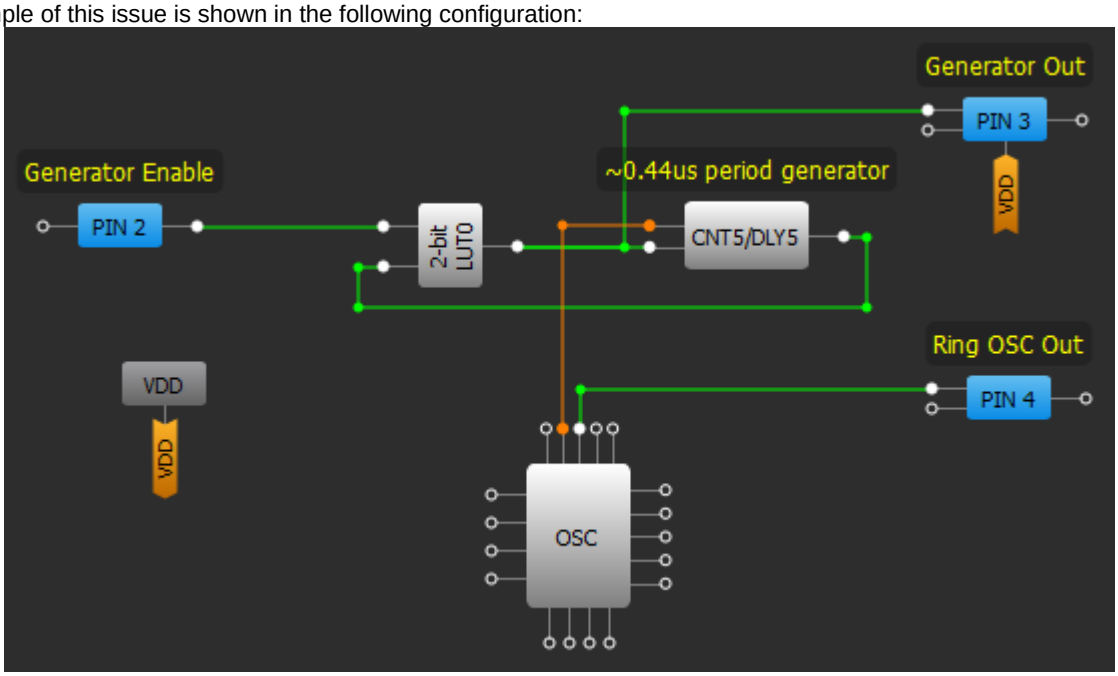
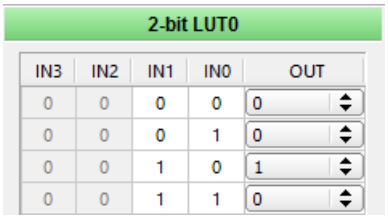
SLG46621

ISSUE 1: Long Settling Time for Ring OSC
Functional Blocks Affected: Ring OSC, Delay, Counter

Description:

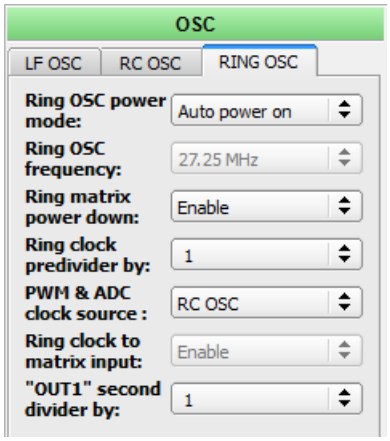
The Ring OSC has a longer settling time when configured as Auto Power On in the designs that have a very short Ring OSC disable time. An example of this issue is shown in the following configuration:





2-bit LUT0

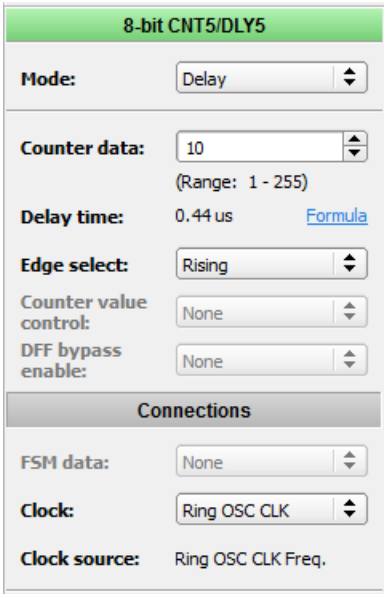
IN3	IN2	IN1	IN0	OUT
0	0	0	0	0
0	0	0	1	0
0	0	1	0	1
0	0	1	1	0



OSC

LF OSC | RC OSC | RING OSC

Ring OSC power mode:	Auto power on
Ring OSC frequency:	27.25 MHz
Ring matrix power down:	Enable
Ring clock predivider by:	1
PWM & ADC clock source :	RC OSC
Ring clock to matrix input:	Enable
"OUT1" second divider by:	1



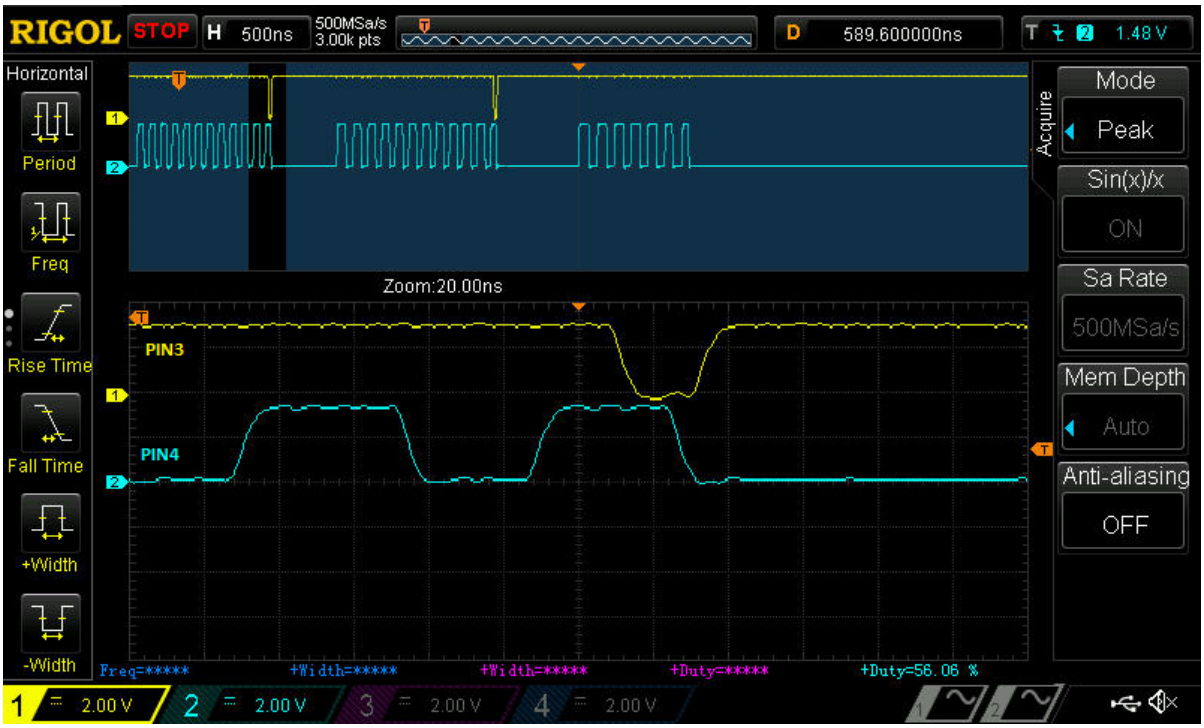
8-bit CNT5/DLY5

Mode:	Delay
Counter data:	10
	(Range: 1 - 255)
Delay time:	0.44 us Formula
Edge select:	Rising
Counter value control:	None
DFF bypass enable:	None

Connections

FSM data:	None
Clock:	Ring OSC CLK
Clock source:	Ring OSC CLK Freq.

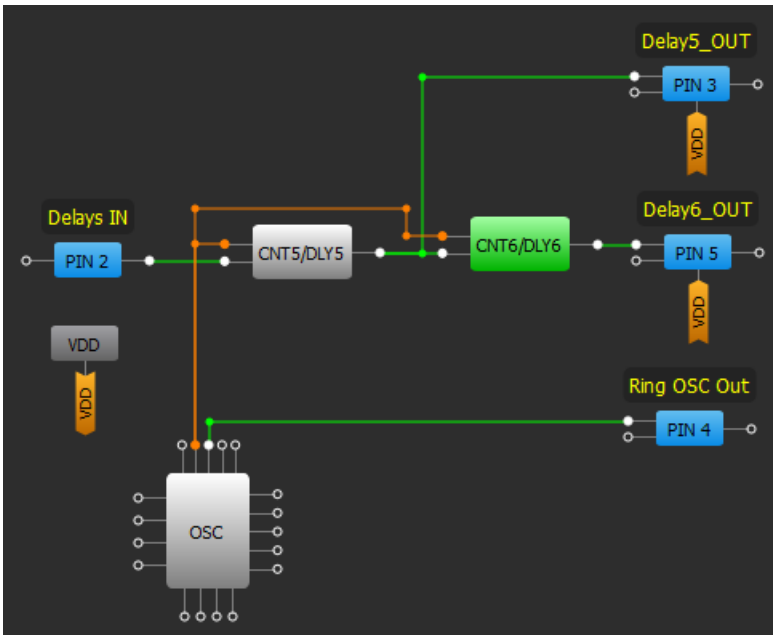
The configuration shown above generates a periodical signal with a frequency defined by the Delay cell and started by a high signal on PIN2. The issue becomes apparent in a longer settling time when the scheme generates short pulses (Delay is configured as a rising edge delay only). See waveform below.



Channel 1 – 2-bit LUT0 output; Channel 2 – Ring OSC output

Such behavior will lead to substantial error in period calculations if the delay time is relatively small.

A similar situation can occur when using two connected delays (all edge detect types except when pairing “Rising edge DLY – Falling edge DLY”).
In the following example, Delay5 and Delay6 are configured in the same way. However, Delay5 time is 11.4us instead of expected 0.4us (Delay5 time).



Workaround:

- Set Ring OSC power mode to “Force Power On”
- or, Set Turn on by register option in BG (Band Gap) block as “Enable”

ISSUE 2: PGA has an Offset when Loaded

Functional Blocks Affected: PGA, Vref

Description:

The PGA block has an offset when its output through the VREF is loaded. For reference, the table below shows the load vs PGA 4x gain.

Load, mA	Gain (ideal = 4x)
0	3.87
1	3.84
5	3.78
10	3.71
20	3.5
40	3
80	2.2
160	1.4

When the load current is higher than 10 mA the output offset is large and may influence the design operation significantly.

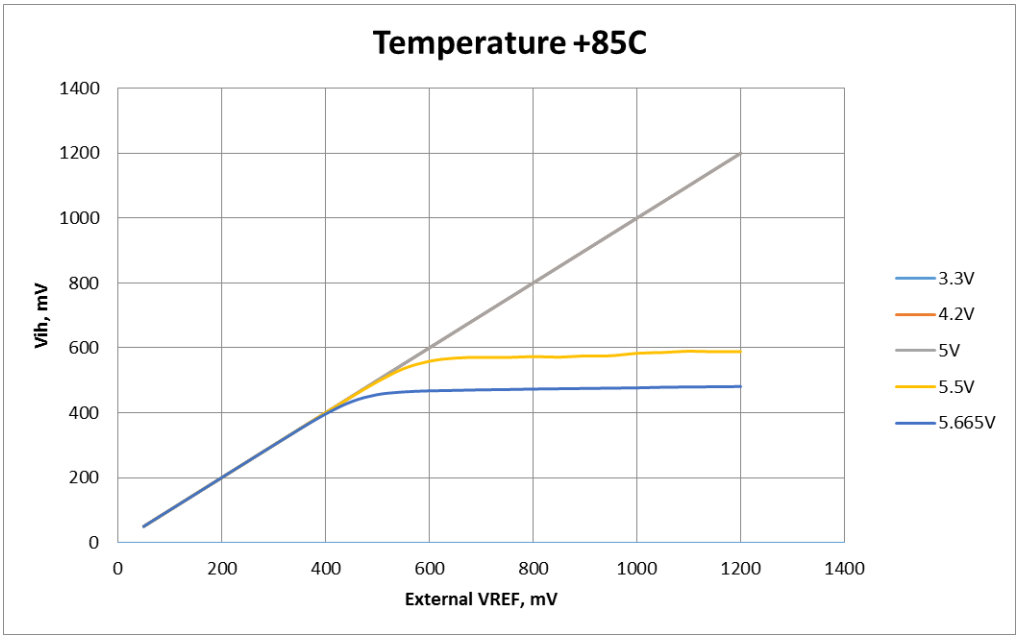
Workaround:

- Use an external buffer to support high load.

ISSUE 3: ACMP Output is Inaccurate when Using External Vref at High VDD and Temperature Functional Block Affected: ACMP

Description:

When using an external Vref source, the ACMP comparison may happen at the wrong threshold if the external Vref voltage is higher than a particular value (please see figure below) at high VDD values (> 5V) and high temperature.



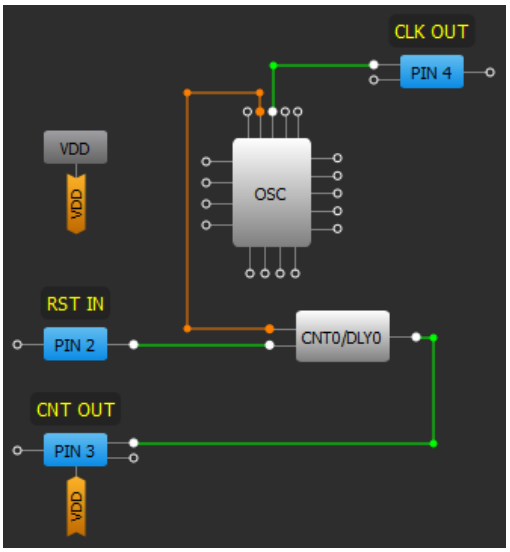
Workaround:

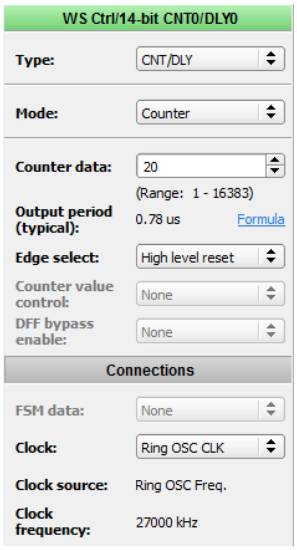
- Avoid using ACMPs in such conditions.

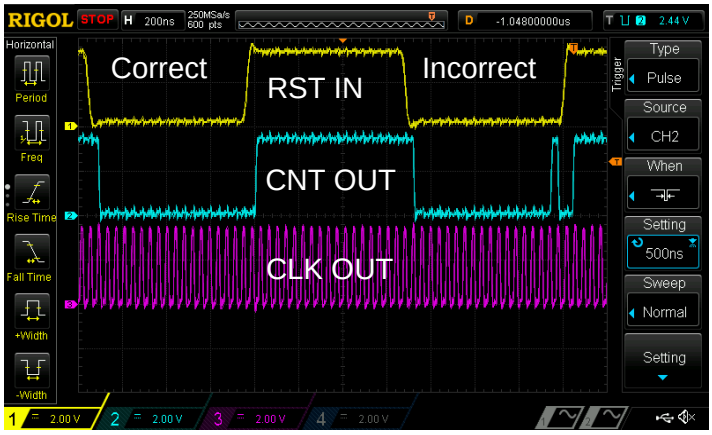
ISSUE 4: Incorrect Counter Operation after the Reset Functional Block Affected: Counter

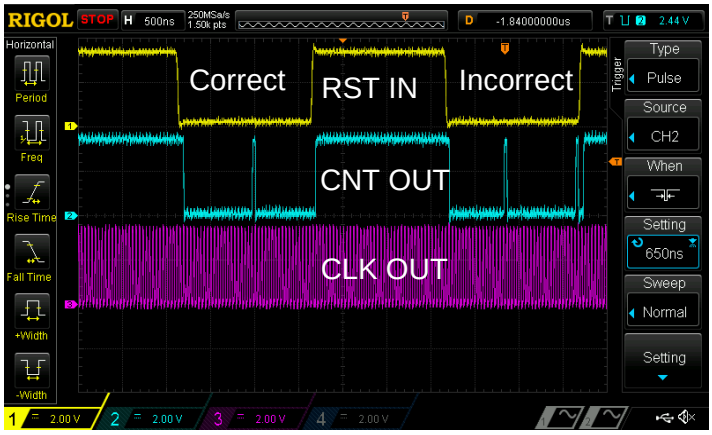
Description:

If the Counter Reset occurs at a time very close to a rising edge of the clock signal during clock signal generation (for example OSC operation), there is a possibility that the Counter Data of the Counter is reset incorrectly and the counter end signal (HIGH pulse) may appear faster than expected. This phenomena appears more frequently the higher the clock frequency is.



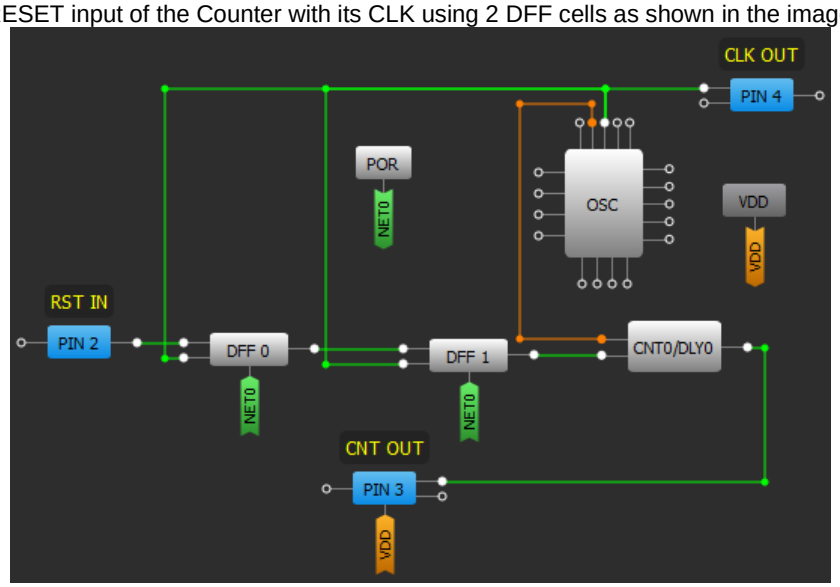






Workaround:

- Synchronize the RESET input of the Counter with its CLK using 2 DFF cells as shown in the image below.

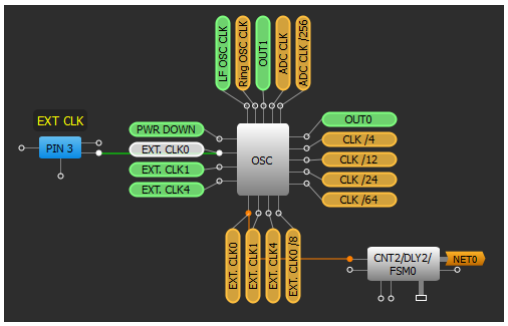


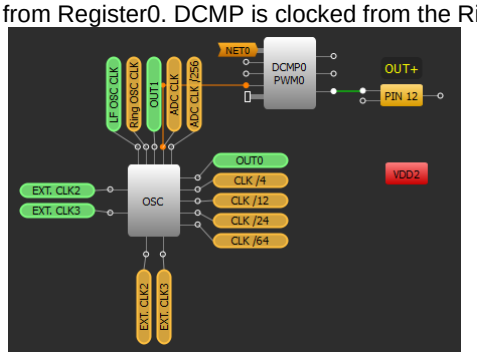
ISSUE 5: DCMP OUT+ Output Glitch
Functional Block Affected: DCMPs

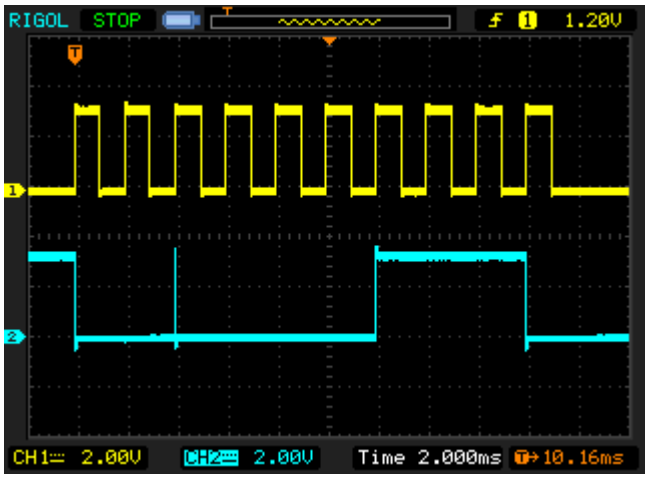
Description:

DCMP's OUT+ output may have a glitch when the input data is changed. This issue appears more frequently the higher DCMP clock is.

For example, DCMP IN+ sources from FSM0 and IN- from Register0. DCMP is clocked from the Ring OSC.

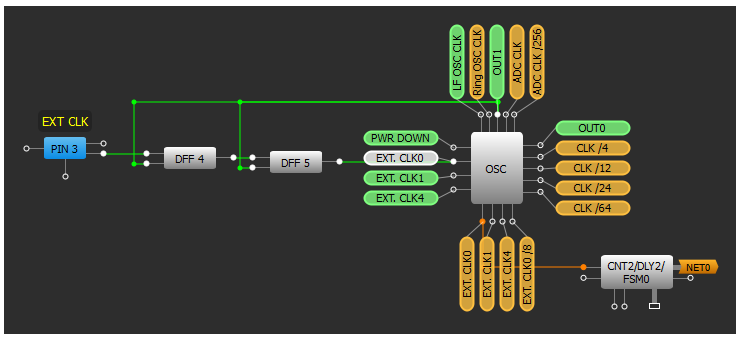


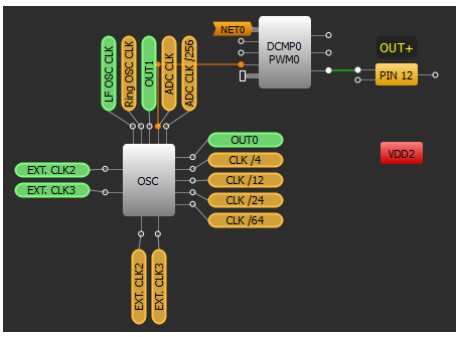




Workaround:

- Synchronize the data source clock with the DCMP clock source using 2 DFF cells as shown in the images below.





ISSUE 6: ACMP IN- Leakage Current when Powered Down
Functional Block Affected: ACMPs

Description:

There is a leakage current from the EXT Vref pin when ACMP uses EXT Vref and the ACMP is powered down.

Workaround:

- Currently there is no workaround. The only alternative is to turn off the IN- external Vref source.

ISSUE 7: Oscillator Frequency Drift due to Aging
Functional Blocks Affected: all that use internal oscillator

Description:

Oscillator has frequency drift due to aging.

Workaround:

- Currently there is no workaround. Please take this into account while creating the design.

ISSUE 8: ACMP Output Glitch due to Ring OSC Operation
Functional Blocks Affected: W/S Control, ACMP

Description:

The output of the ACMP incorrectly goes low even when IN+ is greater than IN- if the RING OSC is active when the WS signal rises

Channel 1 – ACMP out
Channel 2 – WS_OUT

Workaround:

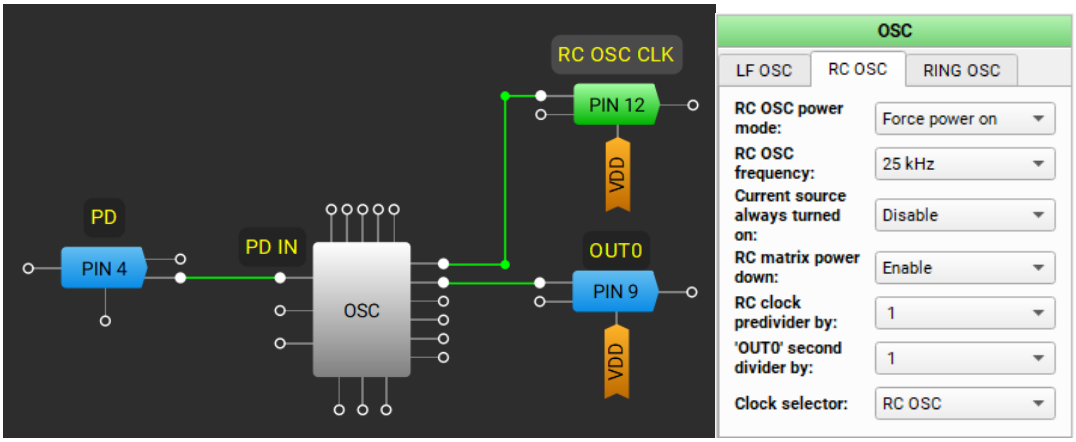
Avoid using the RING OSC with the WS Controller, or add a filtering block on the ACMP output to filter out the glitch.

ISSUE 9: OSC Long Start-Up Time

Functional Block Affected: OSCs

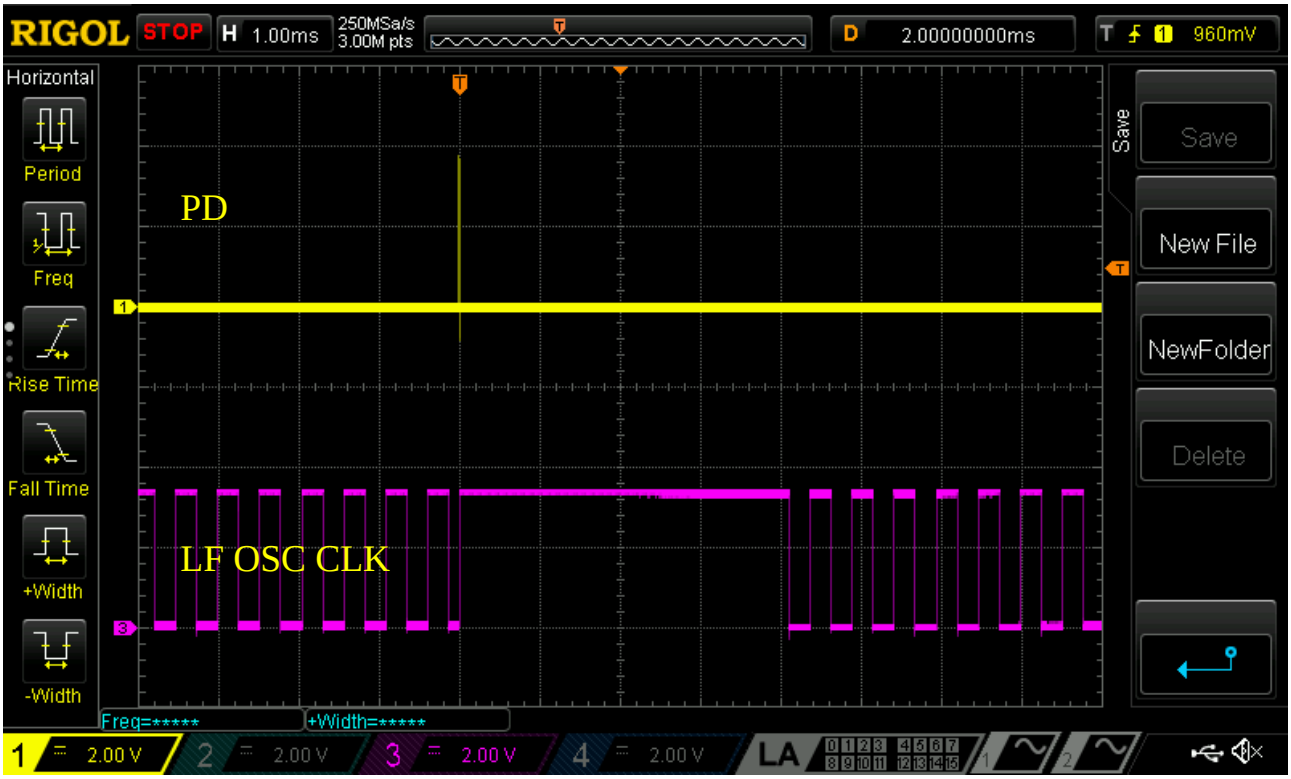
Description:

If a pulse with a duration of less than ~40 ns is applied to the PWR DOWN input of an oscillator, the oscillator outputs remain stuck for milliseconds.

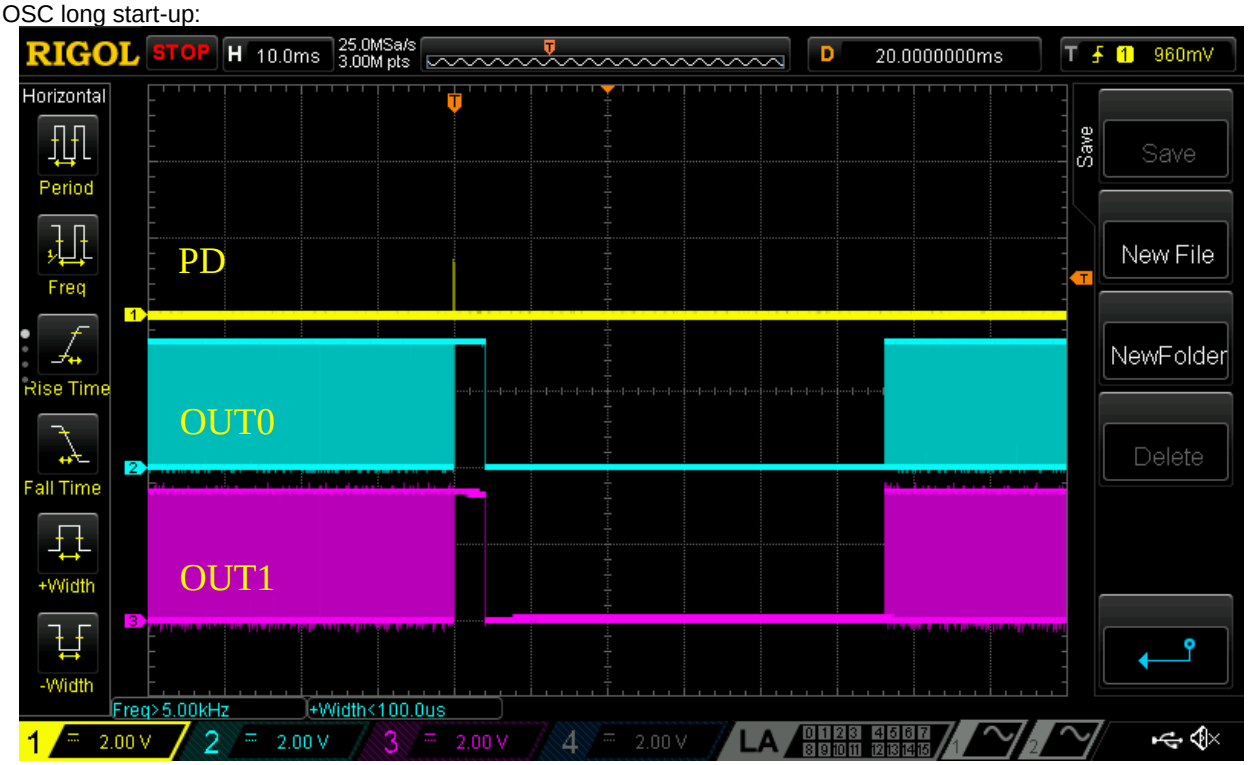


The issue is observed for all available oscillators.

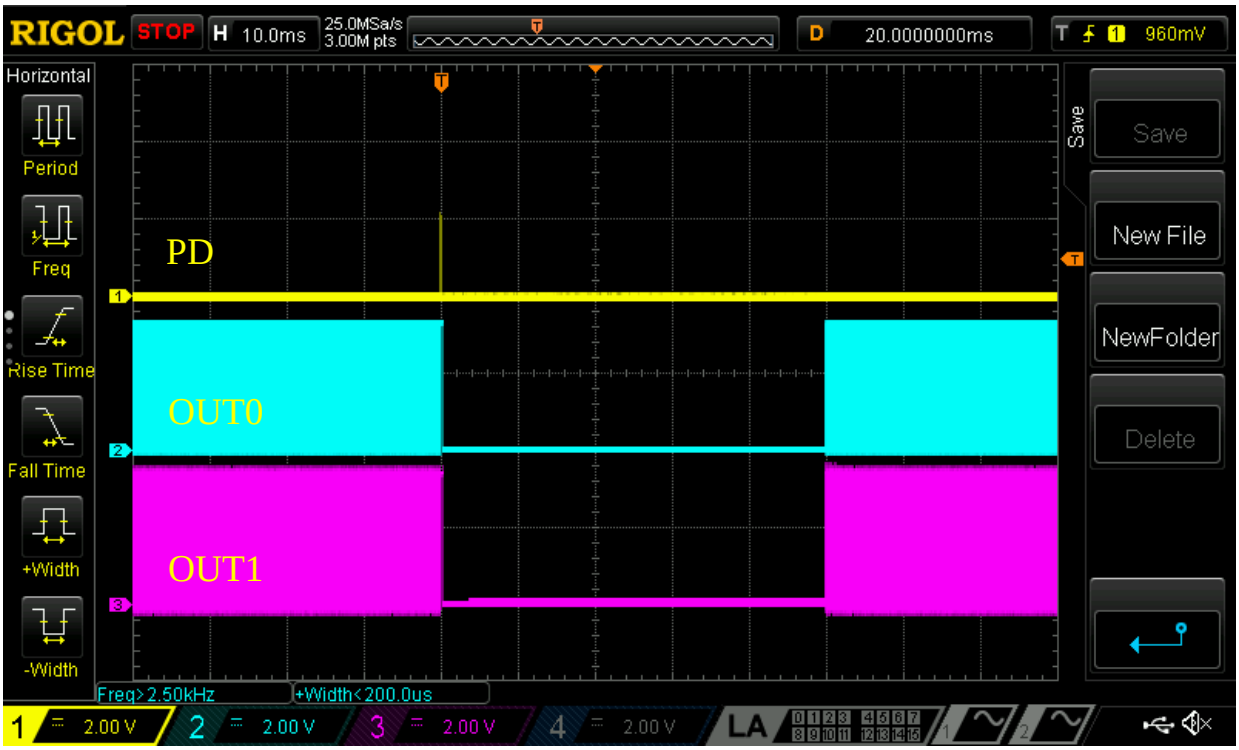
1.9 kHz OSC long start-up:



25 kHz OSC long start-up:



2 MHz OSC long start-up:



Workaround

Avoid applying glitches to the PWR DOWN input of an OSC.

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RoHS Compliance

Renesas Electronics Corporation's suppliers certify that its products are in compliance with the requirements of Directive 2011/65/EU of the European Parliament on the restriction of the use of certain hazardous substances in electrical and electronic equipment. RoHS certificates from our suppliers are available on request.