IDT82V3285 Device Errata

Notes

Supplemental Information

This errata supplements the datasheet. It provides information regarding MFRSYNC_2K of the master and slave devices synchronization to each other in pulse mode.

Description

In master-slave configurations where both MFRSYNC_2K and FRSYNC_8K must be synchronized, the slave EX_SYNC1 must be connected to the master MFRSYNC_2K. If MFRSYNC_2K is placed in pulsed mode, then the master MFRSYNC_2K pulse and slave MFRSYNC_2K will not synchronize to each other after the slave is reset or after the slave is reset and the slave registers are reloaded.

Work-Around: The IDT82V3285 master MFRSYNC_2K must be in clock mode [or Register 74h bit 0 = '0'] in order for the slave MFRSYNC_2K to sync to the master MFRSYNC_2K. The FRSYNC_8K will synchronize in both clock mode and pulse mode.

This known discrepancy is fixed in the new silicon IDT82V3285A revision.