

MOS INTEGRATED CIRCUIT

V850E/PHO3

V850E/PHO3

32-Bit Single-Chip Microcontroller

DESCRIPTION

The V850E/PHO3 single-chip microcontroller devices make the performance gains attainable with 32-bit RISC-based controllers available for embedded control applications. The V850E/PHO3 devices provide an excellent combination of general purpose peripheral functions like serial communication interfaces, timers/counters, measurement and control functions, with dedicated motor control timers and full CAN network support. The integrated FlexRay™ interface implements the FlexRay™ network protocol. Thus equipped, the V850E/PHO3 product is ideally suited for automotive control and electric power steering (EPS) applications. It is also an excellent choice for other applications where a combination of sophisticated peripheral functions and CAN network support is required.

FEATURE

- 32-bit RISC CPU with Harvard Architecture
- Internal flash memory: 992 KB
- Internal RAM: 60 KB
- Data Flash: 32 KB
- Operating Clocks
 - CPU Frequency: 80 / 128MHz with PLL factor 5 / 8
 - MainOsc: operates on 16MHz crystal
 - PLL ratio: factor 5
 - FlexRay™: 80MHz
- I/O lines: 143 + 5 input only
- Timers
 - 10 ch 16-bit general purpose timer/counter
 - 2 ch 16-bit timer/counter with Motor Control
 - 2 ch 16-bit general purpose timer/counter with PWM function
- A/D Converter: 2 x 10 channels
 - 10 bit resolution
- FlexRay Interface: 1 (2 channels) (protocol specification v2.1)
- CAN Interface: 2 channel (AFCAN)
- Serial Interfaces: 7 channels
 - clocked serial: 2 channels (CSIB)
 - clocked serial: 2 channels (CSIE)
 - UARTC: 3 channels
- DMA: 8 channels
- Random Number Generator
- Aux. Frequency Output
- Clock Monitor
- Power Save Mode: HALT
- On Chip Debug: N-Wire and Non Break Debug interface
- Power supply: 3.3V +/- 0.3V and 1.5V +/- 10% (refer to related chapter)
- Temperature range:
 - Package: -40°C to +125°C
 - Bare Die: -40°C to +150°C
- Package: 357 pin FPBGA, 0.8 mm ball-pitch (20 × 20 mm)

ORDERING INFORMATION

Product Name	Product Family	Package	Flash	RAM
μPD70F3483F1(A2)-JA1	V850E/PHO3	FPBGA 20 × 20 mm	768 KB	60 KB
μPD70F3483W-CAR	V850E/PHO3	Bare Die	768 KB	60 KB
μPD70F3441F1(A2)-JA1	V850E/PHO3	FPBGA 20 × 20 mm	992 KB	60 KB
μPD70F3441W-CAR	V850E/PHO3	Bare Die	992 KB	60 KB

The information in this document is subject to change without notice. Before using this document, please confirm that this is the latest version.

Not all products and/or types are available in every country. Please check with an NEC Electronics sales representative for availability and additional information.

Table of Contents

1.	Electrical Target Specification	3
1.1	Absolute Maximum Ratings	3
1.2	Capacitance	4
1.3	Operation Conditions	4
1.4	Oscillator Characteristics	4
1.5	DC Characteristics	5
1.5.1	Input/Output Level	5
1.5.2	Pin Leak Current	6
1.5.3	Operation and HALT Mode Supply Current	7
1.6	AC Characteristics	8
1.6.1	Power Supply Turning On / Interception Timing	9
1.6.2	Reset And Interrupt Timing	11
1.6.3	External Asynchronous Memory Access Read Timing	12
1.6.4	External Asynchronous Memory Access Write Timing	14
1.6.5	Clocked Serial Interface B (CSIB) Characteristics	16
1.6.6	Clocked Serial Interface E (CSIE) Timing	18
1.6.7	UARTC Timing	25
1.6.8	CAN Timing	25
1.6.9	AD Converter	27
1.6.10	Flash Memory Programming Characteristics	28
2.	Recommended Soldering Conditions	31
3.	Package Drawings	33
4.	Revision History	35

1. Electrical Target Specification

1.1 Absolute Maximum Ratings

$T_a = 25^{\circ}\text{C}$, $V_{SS15x} = CV_{SS15} = V_{SS3x} = AV_{SS0,1} = 0\text{V}$

Table 1-1: Absolute Maximum Ratings

Parameter	Symbol	Conditions		Ratings	Unit
Supply voltage	V_{DD15x}			-0.5 to +2.0	V
	CV_{DD15}			-0.5 to +2.0	V
	V_{DD3x}			-0.5 to +4.6	V
	AV_{DD}			-0.5 to +4.6	V
Input voltage	V_I	The pin X1 is excluded.		-0.5 to $V_{DD3}+0.3$ (Note 1)	V
Analog input voltage	V_{IN}	ANI00 to ANI09 ANI10 to ANI19		-0.3 to $AV_{DD}+0.3$ (Note 1)	V
A/D Converter	$AV_{REF0,1}$			-0.3 to $AV_{DD}+0.3$ (Note 1)	V
High level output current	I_{OH}	For 1 pin	1 pin	-4.0	mA
		Total of all pins (Note 2)	Total	-100.0	mA
Low level output current	I_{OL}	For 1 pin	1 pin	4.0	mA
		Total of all pins (Note 2)	Total	100.0	mA
Operating ambient temperature	T_a	Normal operating mode (Package)		-40 to +125	$^{\circ}\text{C}$
		NBD Operation		-40 to + 80	$^{\circ}\text{C}$
		Flash programming mode, when flash memory is written. (Package)		-40 to +125	$^{\circ}\text{C}$
Operating junction temperature	T_j	Normal operating mode (Bare Die)		-40 to +150	$^{\circ}\text{C}$
		Flash programming mode, when flash memory is written. (Bare Die)		-40 to +150	$^{\circ}\text{C}$
Storage temperature	T_{stg}	In tray.		-65 to +125	$^{\circ}\text{C}$
		Off tray, mounted but not powered.		-65 to + 150	$^{\circ}\text{C}$

Notes: 1. Please do not exceed absolute maximum rating (max. +4.6V) of each power supply voltage.
2. Total sum of all input and output currents of all pins.

Cautions: 1. **Cautions: 1. Do not directly connect output (or I/O) pins of IC products to each other, or to VDD, Vss, and GND.**
2. **Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded. The ratings and conditions shown below for DC characteristics and AC characteristics are within the range for normal operation and quality assurance.**

1.2 Capacitance

$$T_a = 25^{\circ}\text{C}$$

$$V_{DD15} = C V_{DD15} = V_{DD3x} = A V_{DD} = V_{SS15x} = C V_{SS15} = V_{SS3x} = A V_{SS0,1} = 0V$$

Table 1-2: Pin Leak Current

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Input capacitance	C_I	fc=1MHz			15	pF
Input/output capacitance	C_{IO}	All pins are at 0V excluding the pin that is measured.			15	pF
Output capacitance	C_O				15	pF

1.3 Operation Conditions

Table 1-3: Operating Conditions

Internal system clock frequency	Operating Temperature (Topt)		Power Supply Voltage
80MHz, 128MHz	$T_a = -40$ to $+125^{\circ}\text{C}$	Normal operating mode (Package)	$V_{DD15x} = C V_{DD15} = 1.5V \pm 0.15V$ $V_{DD3x} = 3.3V \pm 0.3V$
	$T_j = -40$ to $+150^{\circ}\text{C}$	Normal operating mode (Bare Die)	

1.4 Oscillator Characteristics

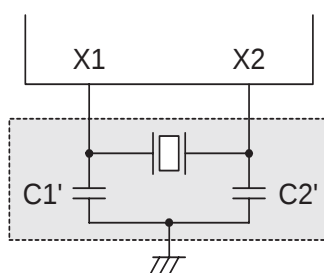


Figure 1-1: Oscillator Recommendations

Remark: Values of capacitors C1' and C2' depend on used crystal and must be specified in cooperation with the crystal manufacturer.

- Cautions:**
1. External clock input is prohibited.
 2. Wire as follows in the area enclosed by the broken lines in the above figure to avoid an adverse effect from wiring capacitance.
 - Place the oscillation circuit as close as possible to X1 and X2 pins.
 - Keep the wiring length as short as possible.
 - Do not cross the wiring with the other signal lines.

- Do not route the wiring near a signal line through which a high fluctuating current flows.
- Always make the ground point of the oscillator capacitor the same potential as CVSS15.
- Do not ground the capacitor to a ground pattern through which a high current flows.
- Do not fetch signals from the oscillator.

Table 1-4: Operating Conditions

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Oscillation frequency	fosc			16		MHz
Oscillation stabilization time	t _{OST}	The oscillation stabilization time depends on the crystal and circuit and must be specified in cooperation with the crystal manufacturer. Ensure that all conditions and tolerances of all components are considered for determination of oscillation stabilization time: Resistance value Capacity value Voltage Temperature Manufacturing range	n/a	n/a	n/a	
PLL lockup time	PSTC	Internal digital counter, counting with fosc (fx=fosc) frequency.		2 ¹⁴ /fx		s

1.5 DC Characteristics

1.5.1 Input/Output Level

T_a = -40 to +125°C

T_j = -40 to +150°C

VDD15x = CVDD15 = 1.5V +/-10%,

VDD3x = 3.3V +/- 0.3V,

VSS15x = CVSS15 = VSS3x = 0V

Table 1-5: Input/Output Level (1/2)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Input voltage, high	V _{IH}	PAL,PAH,PDL,PDH,PCD,PCS,PCM,MODE1,DDI,DMS,DCK	0.7V _{DD3}		V _{DD3} +0.3	V
		P0,P1,P2,P3,P4,P5,P6,P7,P8,P9,P10,P11,ADn_DBG,MODE3,FRXDA,FRXDB,SYNC,CLK_DBG	0.7V _{DD3}		V _{DD3} +0.3	V
		_DRST, MODE_DBG	0.75V _{DD3}		V _{DD3} +0.3	V
		MODE0,MODE2,_RESET	0.8V _{DD3}		V _{DD3} +0.3	V

Table 1-5: Input/Output Level (2/2)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Input voltage, low	V_{IL}	PAL, PAH, PDL, PDH, PCD, PCS, PCM, MODE1, DDI, DMS, DCK	-0.5		$0.3V_{DD3}$	V
		P0, P1, P2, P3, P4, P5, P6, P7, P8, P9, P10, P11, ADn_DBG, MODE3, FRXDA, FRXDB, SYNC, CLK_DBG	-0.5		$0.3V_{DD3}$	V
		_DRST, MODE_DBG	-0.5		$0.3V_{DD3}$	V
		MODE0, MODE2, _RESET	-0.5		$0.2V_{DD3}$	V
Output voltage, high	V_{OH}	$I_{OH} = -2.5$ mA (Note 2)	$V_{DD3} - 1.0$			V
		$I_{OH} = -0.1$ mA	$V_{DD3} - 0.4$			V
Output voltage, low	V_{OL}	$I_{OL} = 2.5$ mA (Note 2)			0.8	V
		$I_{OL} = 0.1$ mA			0.4	V
Build in pull down resistor	R_L	Note 1	10	50	120	K Ω

- Notes:** 1. _DRST, MODE_DBG
 2. Max +/- 2.5 mA x 20 of output current simultaneously.
 Only the output port pins and the FlexRay outputs have to be considered.
 (The output pins of the debugger (NBD/DCU) are excluded).

1.5.2 Pin Leak Current

$T_a = -40$ to $+125^\circ\text{C}$

$T_j = -40$ to $+150^\circ\text{C}$

$V_{DD15x} = CV_{DD15} = 1.5\text{V} \pm 10\%$,

$V_{DD3x} = 3.3\text{V} \pm 0.3\text{V}$,

$V_{SS15x} = CV_{SS15} = V_{SS3x} = 0\text{V}$

Table 1-6: Pin Leak Current

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Input leakage current, high	I_{LIH}	$V_I = V_{DD3x}$ All pins except for the below mentioned			10.0	μA
		$V_I = AV_{DD}$ ANI00 to ANI09, ANI10 to ANI19			3.0	μA
Input leakage current, low	I_{LIL}	$V_I = 0\text{V}$ All pins except for the below mentioned			-10.0	μA
		$V_I = 0\text{V}$ ANI00 to ANI09, ANI10 to ANI19			-3.0	μA
Output leakage current, high	I_{LOH}	$V_O = V_{DD3x}$ All pins			10.0	μA
Output leakage current, low	I_{LOL}	$V_O = 0\text{V}$ All pins			-10.0	μA

1.5.3 Operation and HALT Mode Supply Current

$T_a = -40$ to $+125^{\circ}\text{C}$

$T_j = -40$ to $+150^{\circ}\text{C}$

$V_{DD15x} = CV_{DD15} = 1.5\text{V} \pm 10\%$,

$V_{DD3x} = 3.3\text{V} \pm 0.3\text{V}$,

$V_{SS15x} = CV_{SS15} = V_{SS3x} = 0\text{V}$

Table 1-7: Power Supply Current

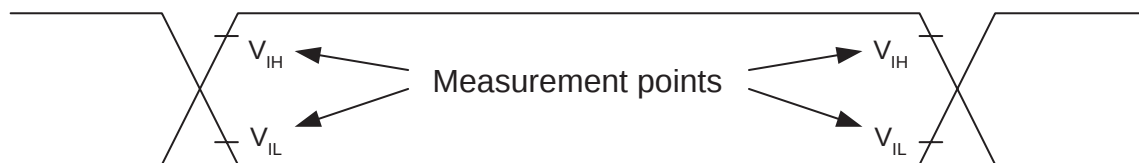
Parameter	Conditions		Symbol	MIN.	TYP. (Note 2)	MAX.	Unit
Supply current (Note 1)	Normal Operation mode	V_{DD15x}, CV_{DD15} $f_{XX} = 128\text{MHz}$	I_{DD15}		220	430	mA
		V_{DD15x}, CV_{DD15} $f_{XX} = 80\text{MHz}$	I_{DD15}		195	400	mA
		V_{DD3x}	I_{DD3}		35	100	mA
	Flash programming mode	V_{DD15x}, CV_{DD15} $f_{XX} = 128\text{MHz}$	I_{DDF15}		230	450	mA
		V_{DD15x}, CV_{DD15} $f_{XX} = 80\text{MHz}$	I_{DDF15}		205	420	mA
		V_{DD3x}	I_{DDF3}		60	100	mA
	Halt mode	V_{DD15x}, CV_{DD15} $f_{XX} = 128\text{MHz}$	I_{DDH15}		200	390	mA
		V_{DD15x}, CV_{DD15} $f_{XX} = 80\text{MHz}$	I_{DDH15}		180	365	mA

Notes: 1. The port output current resulting from built-in pull-up or pull-down resistances is not included.

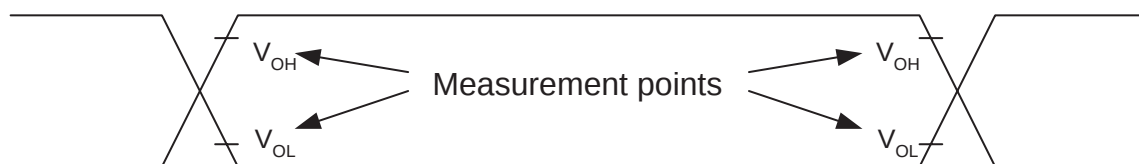
2. The typical value refers to $T_a = 25^{\circ}\text{C}$, $V_{DD15x} = 1.5\text{V}$ and $V_{DD3x} = 3.3\text{V}$

1.6 AC Characteristics

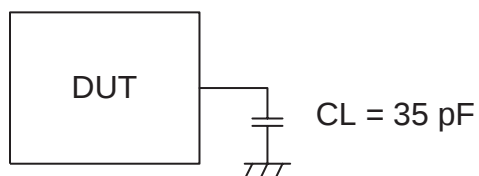
AC Test Input Measurement Points,



AC Test Output Measurement Points



Load Conditions



Caution: If the load capacitance exceeds 35 pF due to the circuit configuration, bring the load capacitance of the device to 35 pF or less by inserting a buffer or by some other means.

1.6.1 Power Supply Turning On / Interception Timing

$T_a = -40$ to $+125^{\circ}\text{C}$

$T_j = -40$ to $+150^{\circ}\text{C}$

$V_{DD15x} = CV_{DD15} = 1.5\text{V} \pm 10\%$,

$V_{DD3x} = 3.3\text{V} \pm 0.3\text{V}$,

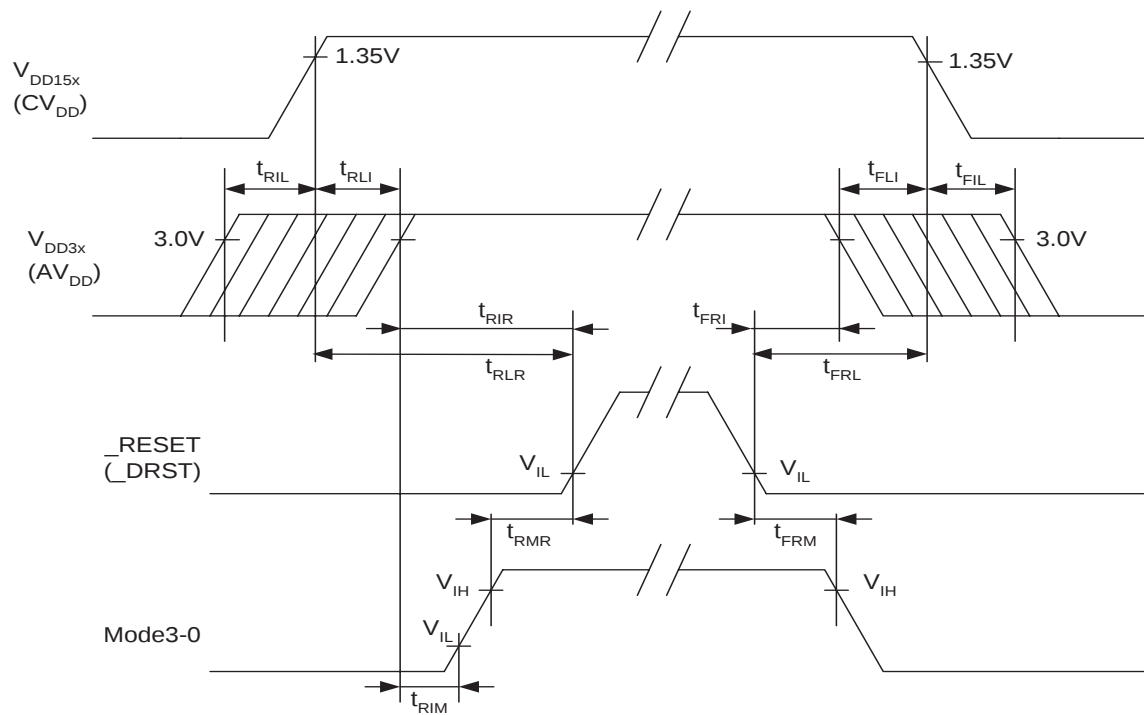
$V_{SS15x} = CV_{SS15} = V_{SS3x} = 0\text{V}$

Table 1-8: Turning On / Interception Timing

Parameter	Symbol	Conditions	MIN.	MAX.	Unit
V_{DD15x} to V_{DD3x}	t_{RLI}		0	1	s
V_{DD3x} to V_{DD15x}	t_{RIL}		0	1	s
V_{DD15x} to $\overline{\text{RESET}}$	t_{RLR}		$0.5+t_{OSC}^{\bar{a}}$		ms
V_{DD3x} to $\overline{\text{RESET}}$	t_{RIR}		$0.5+t_{OSC}^{\bar{b}}$		ms
V_{DD3x} to MODE3-0	t_{RIM}		0.2		ms
MODE3-0 to $\overline{\text{RESET}}$	t_{RMR}		0		ns
$\overline{\text{RESET}}$ to MODE3-0	t_{FRM}		0		ns
$\overline{\text{RESET}}$ to V_{DD3x}	t_{FRI}		500		ns
$\overline{\text{RESET}}$ to V_{DD15x}	t_{FRL}		500		ns
V_{DD3x} to V_{DD15x}	t_{FLI}		0	1	s
V_{DD15x} to V_{DD3x}	t_{FIL}		0	1	s

- t_{OSC} depends on the external oscillator's stabilization time, crystal type and circuit and should be specified / evaluated in cooperation with the oscillator manufacturer.
- t_{OSC} depends on the external oscillator's stabilization time, crystal type and circuit and should be specified / evaluated in cooperation with the oscillator manufacturer.

Figure 1-2: Turning On / Interception Timing



1.6.2 Reset And Interrupt Timing

$T_a = -40$ to $+125^{\circ}\text{C}$

$T_j = -40$ to $+150^{\circ}\text{C}$

$V_{DD15x} = CV_{DD15} = 1.5\text{V} \pm 10\%$,

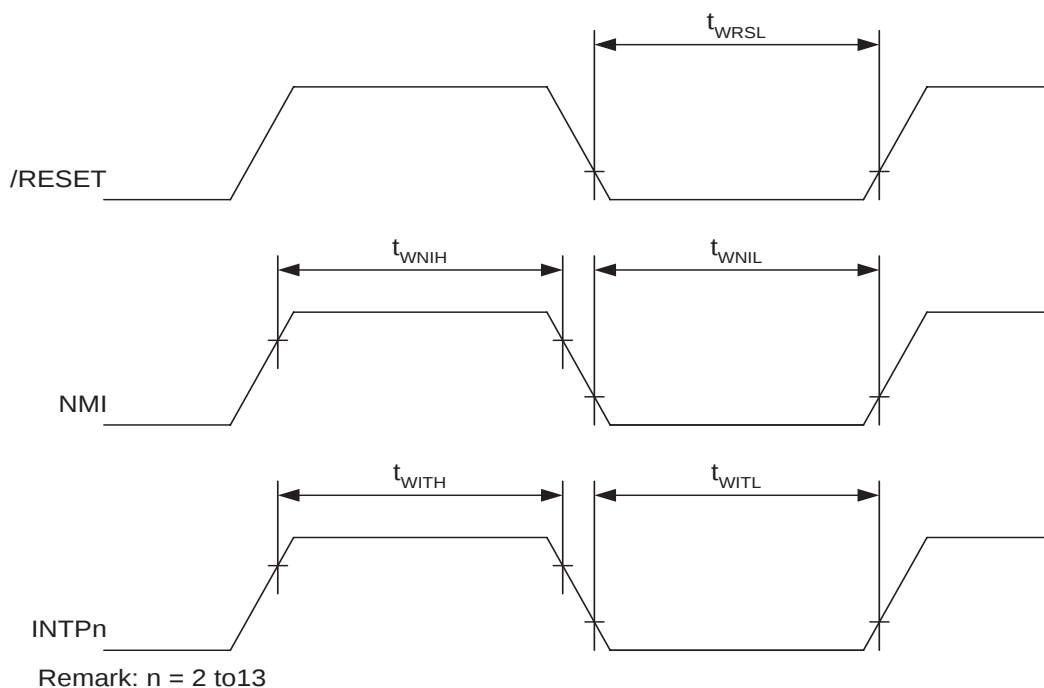
$V_{DD3x} = 3.3\text{V} \pm 0.3\text{V}$,

$V_{SS15x} = CV_{SS15} = V_{SS3x} = 0\text{V}$

Table 1-9: Reset And Interrupt Timing

Parameter	Symbol	Conditions	MIN.	MAX.	Unit
$\overline{\text{RESET}}$ input low level width	t_{WRSL}	except for power on	500		ns
NMI input low level width	t_{WNIL}	(analog filter)	500		ns
NMI input high level width	t_{WNIH}	(analog filter)	500		ns
INTPn input low level width	t_{WITL}	n=0,1 (analog filter)	500		ns
		n=2...13 (digital filter)	Sampling clock $\times 5T$		ns
INTPn input high level width	t_{WITH}	n=0,1 (analog filter)	500		ns
		n=2...13 (digital filter)	Sampling clock $\times 5T$		ns

Figure 1-3: Reset And Interrupt Timing



1.6.3 External Asynchronous Memory Access Read Timing

 $T_a = -40 \text{ to } +125^\circ\text{C}$
 $T_j = -40 \text{ to } +150^\circ\text{C}$
 $V_{DD15x} = CV_{DD15} = 1.5\text{V} \pm 10\%$,

 $V_{DD3x} = 3.3\text{V} \pm 0.3\text{V}$,

 $V_{SS15x} = CV_{SS15} = V_{SS3x} = 0\text{V}$

Table 1-10: External Asynchronous Memory Access Read Timing

Parameter	Symbol	MIN.	MAX.	Unit
Data input set up time (vs. address)	<10> t_{SAID}		$(2 + w_{AS} + w_{AH} + w_D + w) T - 19$	ns
Data input set up time (vs. $\overline{CSn}$, $\overline{BEN0-3}$)	<10> t_{SAID}		$(2 + w_{AS} + w_{AH} + w_D + w) T - 19$	ns
Data input set up time (vs. $\overline{RD}\downarrow$)	<11> t_{SRDID}		$(1.5 + w_D + w) T - 19$	ns
$\overline{RD}$ Low level width	<12> t_{WRDL}	$(1.5 + w_D + w) T - 6$		ns
$\overline{RD}$ High level width	<13> t_{WRDH}	$(0.5 + w_{AS} + i) T - 6$		ns
Address, $\overline{CSn}$, $\overline{BEN0-3} \rightarrow \overline{RD}\downarrow$ delay time	<14> t_{DARD}	$(0.5 + w_{AS}) T - 8.2$		ns
$\overline{RD}\uparrow \rightarrow$ address delay time	<15> t_{DRDA}	$i \cdot T$		ns
$\overline{RD}\uparrow \rightarrow \overline{CSn}$ delay time	<15'> t_{DRDCS}	0		ns
$\overline{RD}\uparrow \rightarrow \overline{BEN0-3}$ delay time	<15''> t_{DRDBEN}	0		ns
Data input hold time (vs. $\overline{RD}\uparrow$)	<16> t_{HRDID}	0		ns
$\overline{RD}\uparrow \rightarrow$ data output delay time	<17> t_{DRDOD}	$(1 + i + w_{AS} + w_{AH}) T - 8$		ns
$\overline{WAIT}$ set up time (vs. address, $\overline{CSn}$, $\overline{BEN0-3}$)	<31> t_{SAW}		$(1 + w_D + w + w_{AS} + w_{AH}) T - 19$	ns
$\overline{WAIT}$ hold time (vs. address, $\overline{CSn}$, $\overline{BEN0-3}$)	<32> t_{WWH}	$(1 + w_D + w + w_{AS} + w_{AH}) T - 3$		ns

Remarks: 1. $T: 1/f_{XX}$

2. i : Number of idle states specified by BCC register

3. w_{AS} : Number of waits specified by AWC register

w_{AH} : Number of waits specified by AWC register

4. w_D : Number of waits specified by DWC0, DWC1 register; $w_D \geq 1$

5. w : Number of waits due to external wait signal ($\overline{WAIT}$)

6. $n = 0, 2, 3, 4$

Figure 1-4: External Asynchronous Memory Access Read Timing

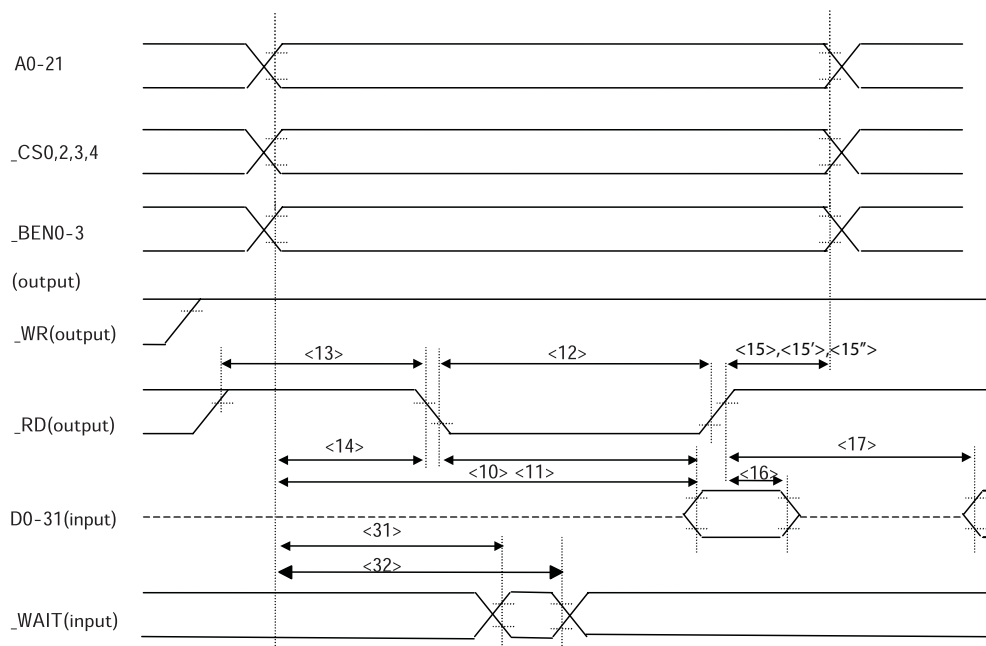
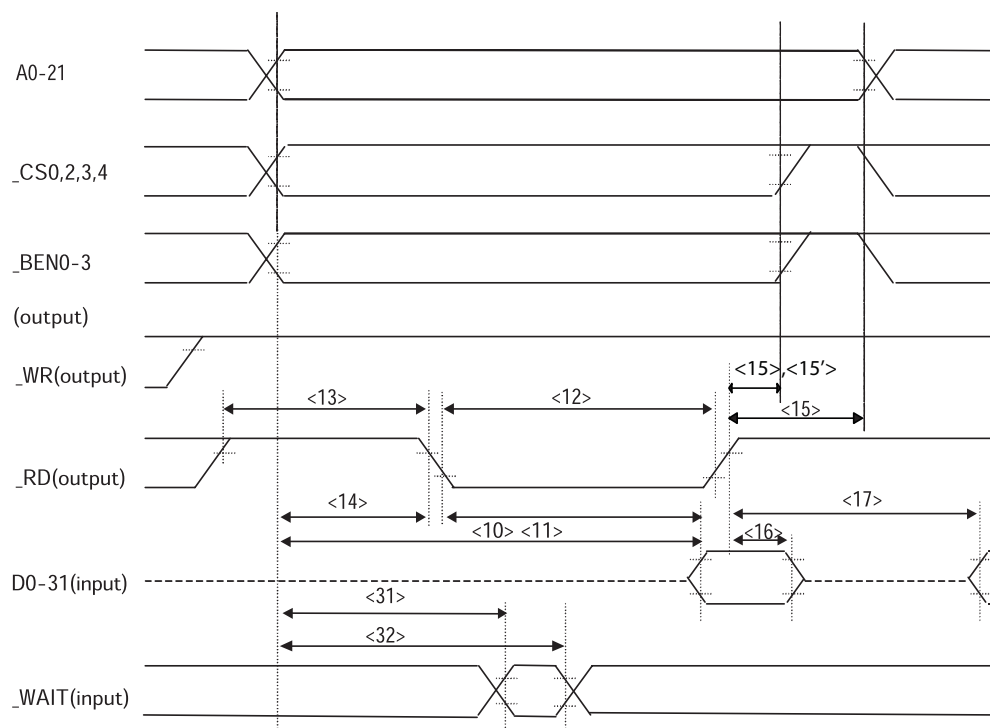


Figure 1-5: External Asynchronous Memory Access Read Timing With Idle Cycle



1.6.4 External Asynchronous Memory Access Write Timing

 $T_a = -40$ to $+125^{\circ}\text{C}$
 $T_j = -40$ to $+150^{\circ}\text{C}$
 $V_{DD15x} = CV_{DD15} = 1.5\text{V} \pm 10\%$,

 $V_{DD3x} = 3.3\text{V} \pm 0.3\text{V}$,

 $V_{SS15x} = CV_{SS15} = V_{SS3x} = 0\text{V}$

Table 1-11: External Asynchronous Memory Access Write Timing

Parameter	Symbol	MIN.	MAX.	Unit
Address, $\overline{\text{CSn}}$, $\overline{\text{BEN0-3}}$ → $\overline{\text{WR}}$ ↓ delay time	<20> T_{DAWR}	$(1 + w_{\text{AS}} + w_{\text{AH}})T - 5$		ns
$\overline{\text{WR}}$ ↓ bus output delay time	<33> T_{DWROD1}	0		ns
$\overline{\text{WR}}$ ↓ data output delay time	<34> T_{DWROD2}		5	ns
$\overline{\text{WR}}$ ↑ data float delay time	<35> T_{FWROD}		$0.5T + 3$	ns
Address, $\overline{\text{CSn}}$, $\overline{\text{BEN0-3}}$ set up (vs. $\overline{\text{WR}}$ ↑)	<21> T_{SAWR}	$(1.5 + w_{\text{AS}} + w_{\text{AH}} + w_{\text{D}} + w)T - 7$		ns
$\overline{\text{WR}}$ ↑ → address delay time	<22> T_{DWRA}	$(0.5 + i)T - 3$		ns
$\overline{\text{WR}}$ ↑ → $\overline{\text{CSn}}$ delay time	<22'> T_{DWRCs}	$0.5T - 3$		ns
$\overline{\text{WR}}$ ↑ → $\overline{\text{BEN0-3}}$ delay time	<22''> T_{DWRBEN}	$0.5T - 3$		ns
$\overline{\text{WR}}$ High level width	<23> T_{WWRH}	$(1.5 + i + w_{\text{AS}} + w_{\text{AH}})T - 6$		ns
$\overline{\text{WR}}$ Low level width	<24> T_{WWRL}	$(0.5 + w + w_{\text{D}})T - 6$		ns
Data output set up time (vs. $\overline{\text{WR}}$ ↑)	<25> T_{SODWR}	$(0.5 + w_{\text{D}} + w)T - 5$		ns
Data output hold time (vs. $\overline{\text{WR}}$ ↑)	<26> T_{HWROD}	$0.5T - 6$		ns
$\overline{\text{WAIT}}$ set up time (vs. address, $\overline{\text{CSn}}$, $\overline{\text{BEN0-3}}$)	<31> T_{SAW}		$(1 + w_{\text{D}} + w + w_{\text{AS}} + w_{\text{AH}})T - 19$	ns
$\overline{\text{WAIT}}$ hold time (vs. address, $\overline{\text{CSn}}$, $\overline{\text{BEN0-3}}$)	<32> T_{WWH}	$(1 + w_{\text{D}} + w + w_{\text{AS}} + w_{\text{AH}})T - 3$		ns

Remarks: 1. T : $1/f_{\text{XX}}$

2. i : Number of idle states specified by BCC register

3. w_{AS} : Number of waits specified by AWC register

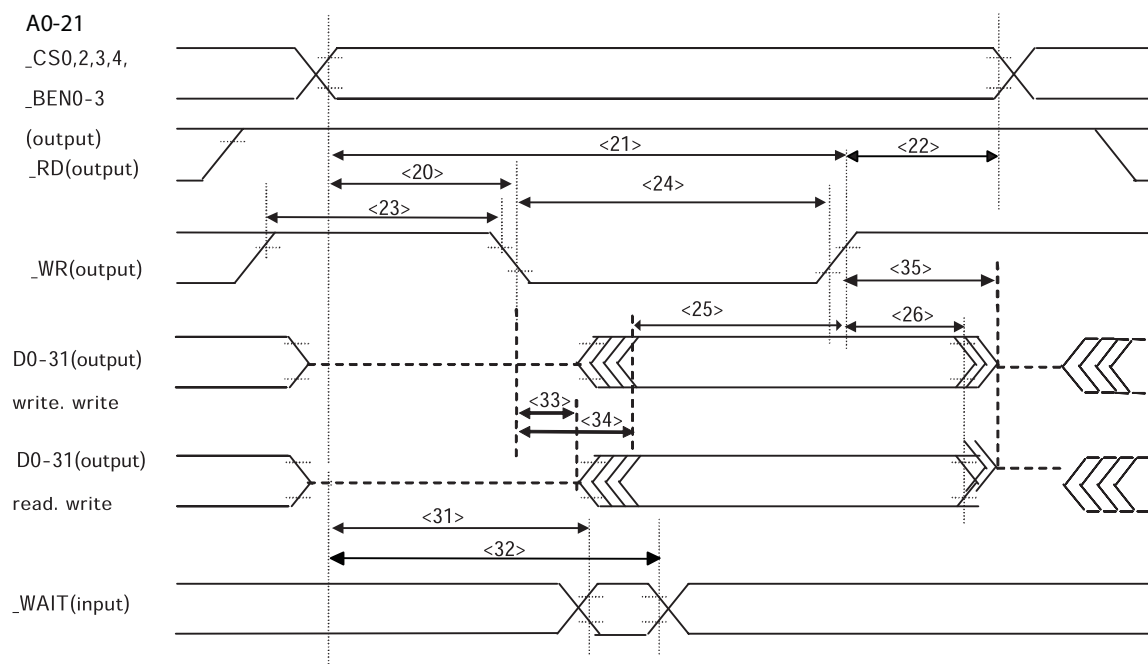
w_{AH} : Number of waits specified by AWC register

4. w_{D} : Number of waits specified by DWC0, DWC1 register; $w_{\text{D}} \geq 1$

5. w : Number of waits due to external wait signal ($\overline{\text{WAIT}}$)

6. $n = 0, 2, 3, 4$

Figure 1-12: External Asynchronous Memory Access Write Timing



1.6.5 Clocked Serial Interface B (CSIB) Characteristics

$T_a = -40$ to $+125^{\circ}\text{C}$

$T_j = -40$ to $+150^{\circ}\text{C}$

$V_{DD15x} = CV_{DD15} = 1.5\text{V} \pm 10\%$,

$V_{DD3x} = 3.3\text{V} \pm 0.3\text{V}$,

$V_{SS15x} = CV_{SS15} = V_{SS3x} = 0\text{V}$

The load capacity of the output terminal is $CL=35\text{pF}$.

Table 1-13: CSIB Characteristics (Master Mode)

CBnCKS2 to CBnCKS0 $\neq$ 111B

Parameter	Symbol	MIN.	MAX.	Unit
$\overline{\text{SCKBn}}$ cycle time	t_{CYSKM}	125		ns
$\overline{\text{SCKBn}}$ high level width	t_{WSKHM}	$0.5 t_{\text{CYSKM}} - 10$		ns
$\overline{\text{SCKBn}}$ low level width	t_{WSKLM}	$0.5 t_{\text{CYSKM}} - 10$		ns
SlBn setup time	t_{SSISKM}	20		ns
SlBn hold time	t_{HSKSIM}	10		ns
SOBn delay	t_{DSKSOM}		10	ns
SOBn hold time	t_{HSKSOM}	$0.5 t_{\text{CYSKM}} - 10$		ns

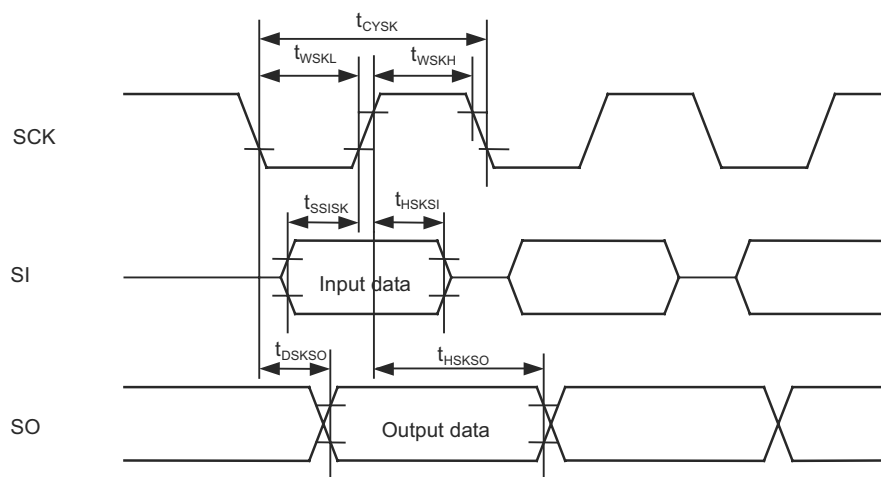
Table 1-14: CSIB Characteristics (Slave Mode)

CBnCKS2 to CBnCKS0 = 111B

Parameter	Symbol	MIN.	MAX.	Unit
$\overline{\text{SCKBn}}$ clock cycle time	t_{CYSKS}	125		ns
$\overline{\text{SCKBn}}$ high level width	t_{WSKHS}	$0.5 t_{\text{CYSKS}} - 10$		ns
$\overline{\text{SCKBn}}$ low level width	t_{WSKLS}	$0.5 t_{\text{CYSKS}} - 10$		ns
SlBn setup time	t_{SSISKS}	5		ns
SlBn hold time	t_{HSKSIS}	10		ns
SOBn delay	t_{DSKSOS}		25	ns
SOBn hold time	t_{HSKSOS}	t_{WSKHS}		ns

Remark: $n = 0, 1$

Figure 1-15: CSIB Master/Slave Mode Timing



1.6.6 Clocked Serial Interface E (CSIE) Timing

$T_a = -40$ to $+125^\circ\text{C}$

$T_j = -40$ to $+150^\circ\text{C}$

$V_{DD15x} = CV_{DD15} = 1.5\text{V} \pm 10\%$,

$V_{DD3x} = 3.3\text{V} \pm 0.3\text{V}$,

$V_{SS15x} = CV_{SS15} = V_{SS3x} = 0\text{V}$

The load capacity of the output terminal is $CL=35\text{pF}$.

Table 1-16: CSIE Characteristics (Master Mode)

Parameter	Symbol	MIN.	MAX.	Unit
Macro operation clock, cycle time	t_{KCY}	31.25		ns
$\overline{SCKEn}$ cycle time	t_{KCYM}	125		ns
$\overline{SCKEn}$ high, low width	t_{KWHM} , t_{KWLM}	$t_{KCYM}/2 - 10$		ns
SIEn input setup time (vs. $\overline{SCKEn}$)	t_{SSIM}	20		ns
SIEn input hold time (vs. $\overline{SCKEn}$)	t_{HSIM}	10		ns
SOEn output delay (vs. $\overline{SCKEn}$)	t_{DSOM}		10	ns
SOEn output hold time (vs. $\overline{SCKEn}$)	t_{HSOM}	$t_{KCYM}/2 - 10$		ns
SCSEn _m inactive (High) width	CEnSIT=x CEnOPE=0 CEnMD=x t_{WSCSB0}	$t_{KCYM}/2 - 10$		ns
	CEnSIT=x CEnOPE=1 CEnMD=x t_{WSCSB1}	$(CS_{IDLE} + 0.5) \cdot t_{KCYM} - 10$		ns
SCSEn _m setup time (vs. $\overline{SCKEn}$)	CEnSIT=x CEnOPE=0 CEnIDL=x CEnMD=0 t_{SSCSB0}	$t_{KCY} - 10$		ns
	CEnSIT=x CEnOPE=1 CEnIDL=0 CEnMD=0 t_{SSCSB1}	$CS_{SETUP} \cdot t_{KCYM} + t_{KCY} - 10$		ns
	CEnSIT=x CEnOPE=1 CEnIDL=1 CEnMD=1 t_{SSCSB2}	$CS_{SETUP} \cdot t_{KCYM} + t_{KCY} - 10$		ns

Table 1-16: CSIE Characteristics (Master Mode)

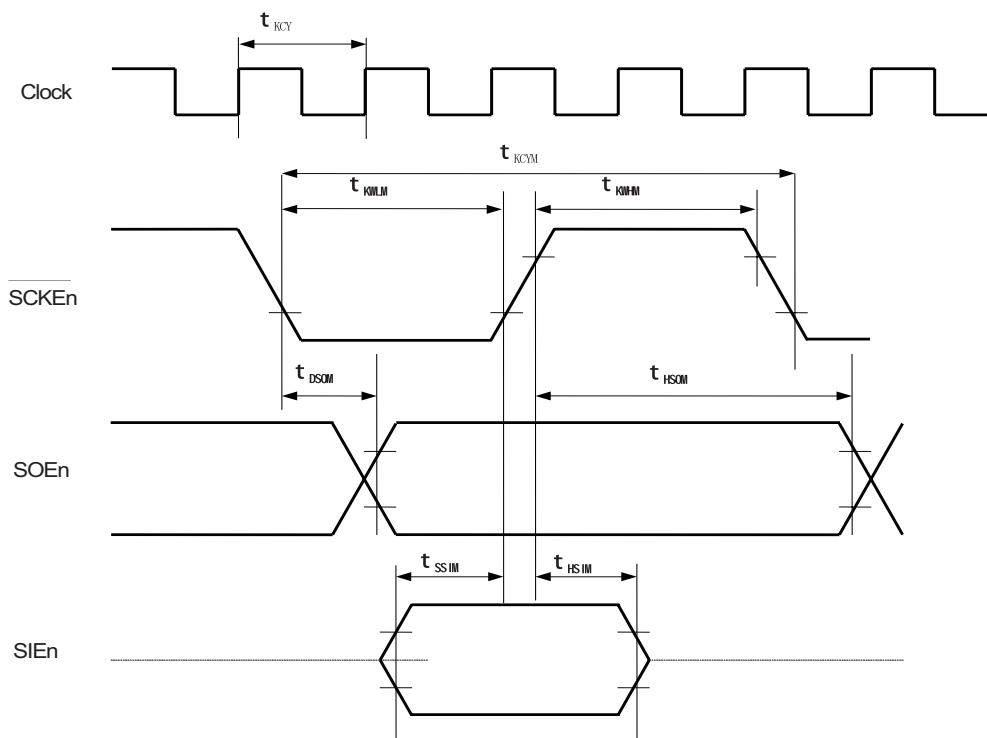
Parameter	Symbol	MIN.	MAX.	Unit
SCSEnm hold time (vs. $\overline{\text{SCKEn}}$)	CEnSIT=0 CEnOPE=0 CEnMD=x t_{HSCSB0}	$t_{\text{KCY}} - 10$		ns
	CEnSIT=1 CEnOPE=0 CEnMD=x t_{HSCSB1}	$t_{\text{KCYM}}/2 - 10$		ns
	CEnSIT=0 CEnOPE=1 CEnMD=x t_{HSCSB2}	$\text{CS}_{\text{HOLD}} * t_{\text{KCYM}} - 10$		ns
	CEnSIT=1 CEnOPE=1 CEnMD=x t_{HSCSB3}	$(\text{CS}_{\text{HOLD}} + 0.5) * t_{\text{KCYM}} - 10$		ns
SCSEnm interframe time	CEnSIT=x CEnOPE=1 CEnMD=x t_{INTER}	$\text{CS}_{\text{INTER}} * t_{\text{KCYM}}$		ns
	CEnSIT=x CEnOPE=0 CEnMD=x -	Not Applicable		ns

Remark: n=0,1
m=7-0(n=0),3-0(n=1)
 $\text{CS}_{\text{SETUP}}, \text{CS}_{\text{INTER}}$: are set by register CEnOPT0
 $\text{CS}_{\text{IDLE}}, \text{CS}_{\text{HOLD}}$: are set by register CEnOPT1

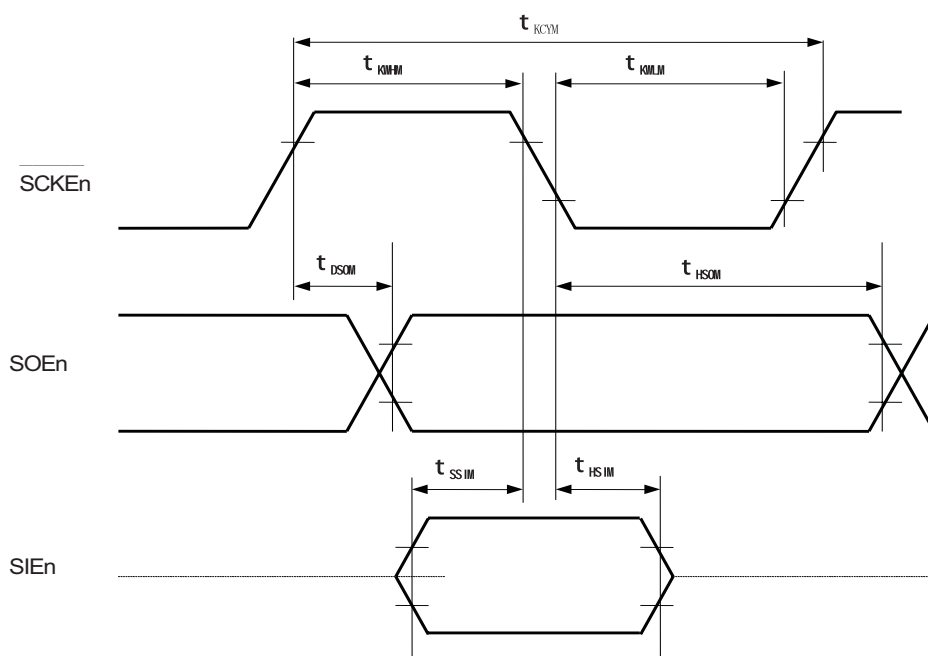
Table 1-17: CSIE Characteristics (Slave Mode)

Parameter	Symbol	MIN.	MAX.	Unit
Macro operation clock, cycle time	t_{KCY}	31.25		ns
$\overline{\text{SCKEn}}$ cycle time	t_{KCYS}	125		ns
$\overline{\text{SCKEn}}$ high, low width	$t_{\text{KWHS}},$ t_{KWLS}	$t_{\text{KCYS}}/2 - 10$		ns
SIEn input setup time (vs. $\overline{\text{SCKEn}}$)	t_{SSIS}	10		ns
SIEn input hold time (vs. $\overline{\text{SCKEn}}$)	t_{HSIS}	$t_{\text{KCY}} * 1.5 + 10$		ns
SOEn output delay (vs. $\overline{\text{SCKEn}}$)	t_{DSOS}		20	ns
SOEn output hold time (vs. $\overline{\text{SCKEn}}$)	t_{HSOS}	$t_{\text{KCYS}}/2 - 10$		ns

Remark: n=0,1

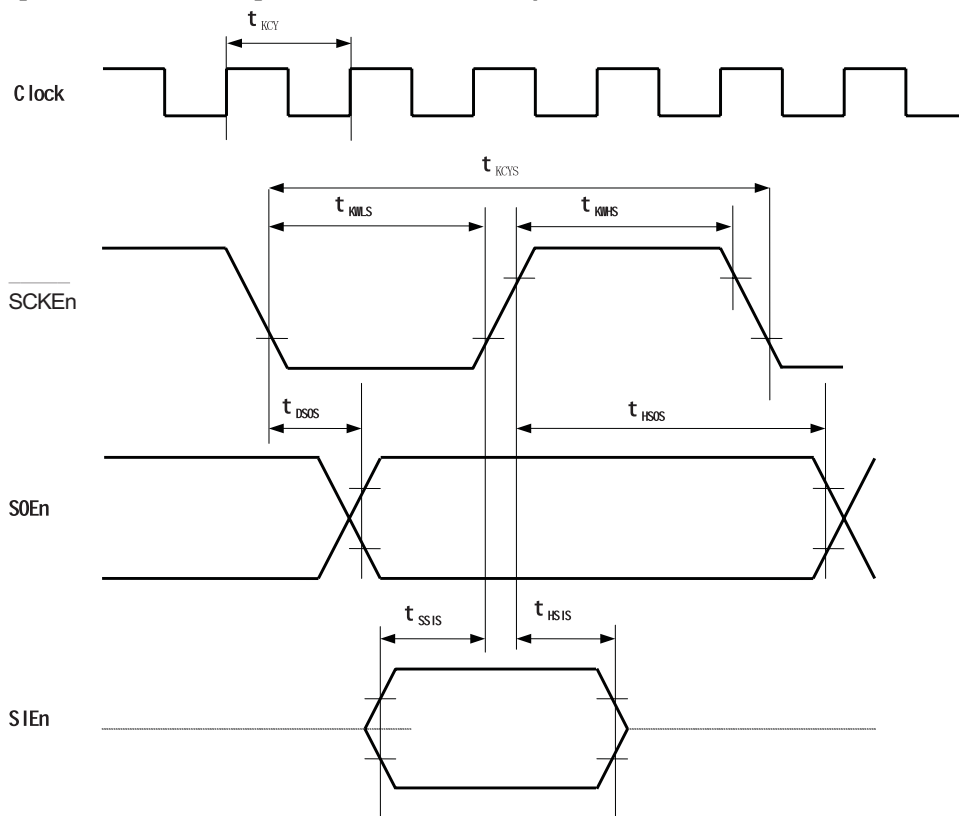
Figure 1-18: CSIE_n Timings(a) $\overline{\text{SCKEn}}/\text{SIEn}/\text{SOEn}$ Pins In Master Mode: (CEnCTL1: CEnCKP/CEnDAP=0/0 or 1/1)

Remark: n=0-1

(b) $\overline{\text{SCKEn}}/\text{SIEn}/\text{SOEn}$ Pins In Master Mode: (CEnCTL1: CEnCKP/CEnDAP=1/0 or 0/1)

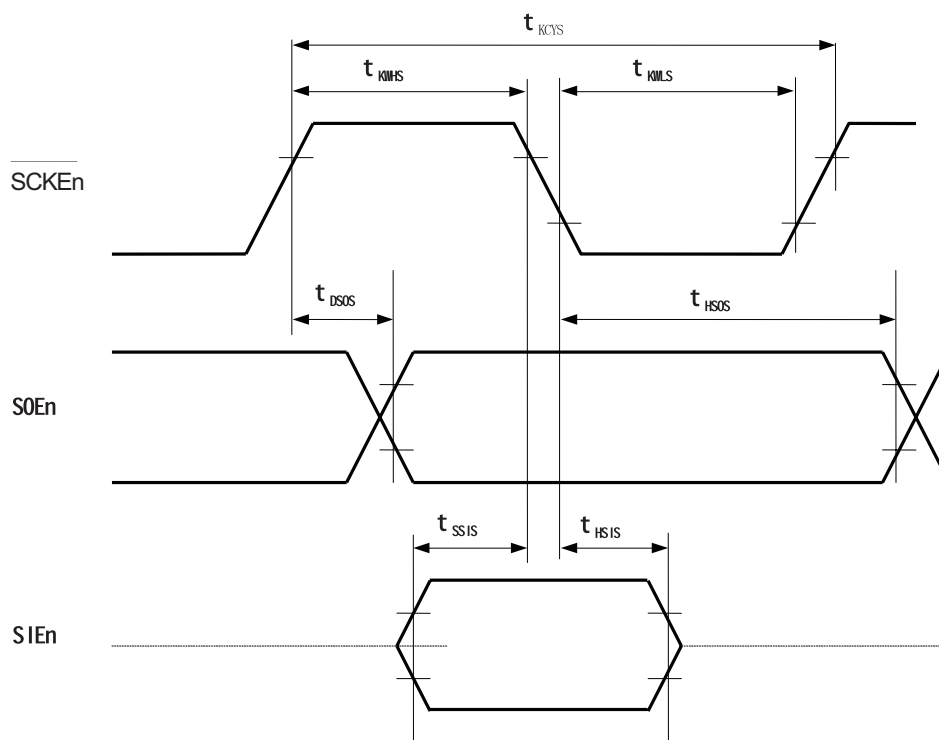
Remark: n=0-1

(c) $[\overline{\text{SCKEn}}/\text{SIEn}/\text{SOEn}]$ Pins In Slave Mode: (CEnCTL1: CEnCKP/CEnDAP=0/0 or 1/1)



Remark: n=0-1

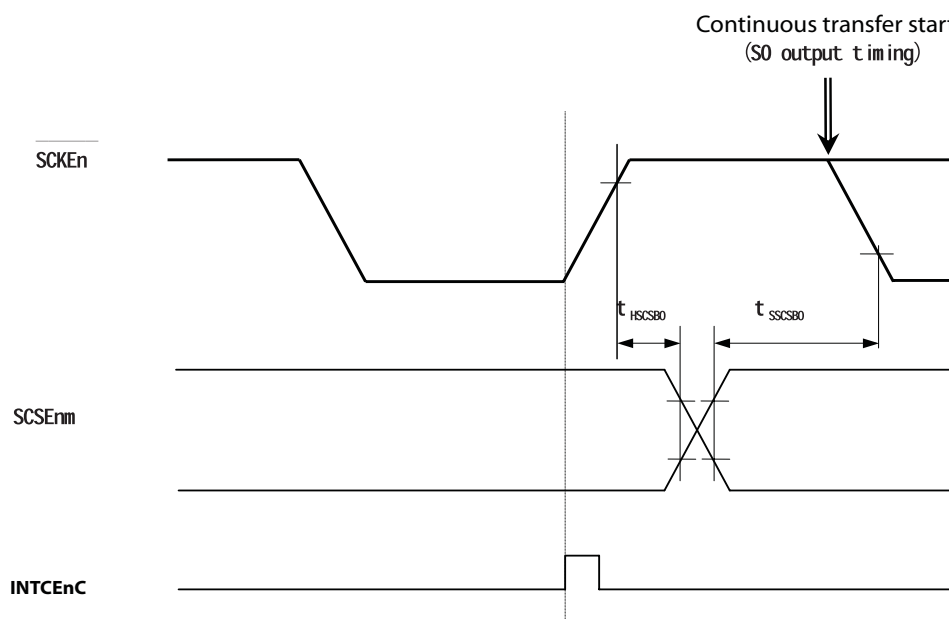
(d) $[\overline{\text{SCKEn}}/\text{SIEn}/\text{SOEn}]$ Pins In Slave Mode: (CEnCTL1: CEnCKP/CEnDAP=1/0 or 0/1)



Remark: n=0-1

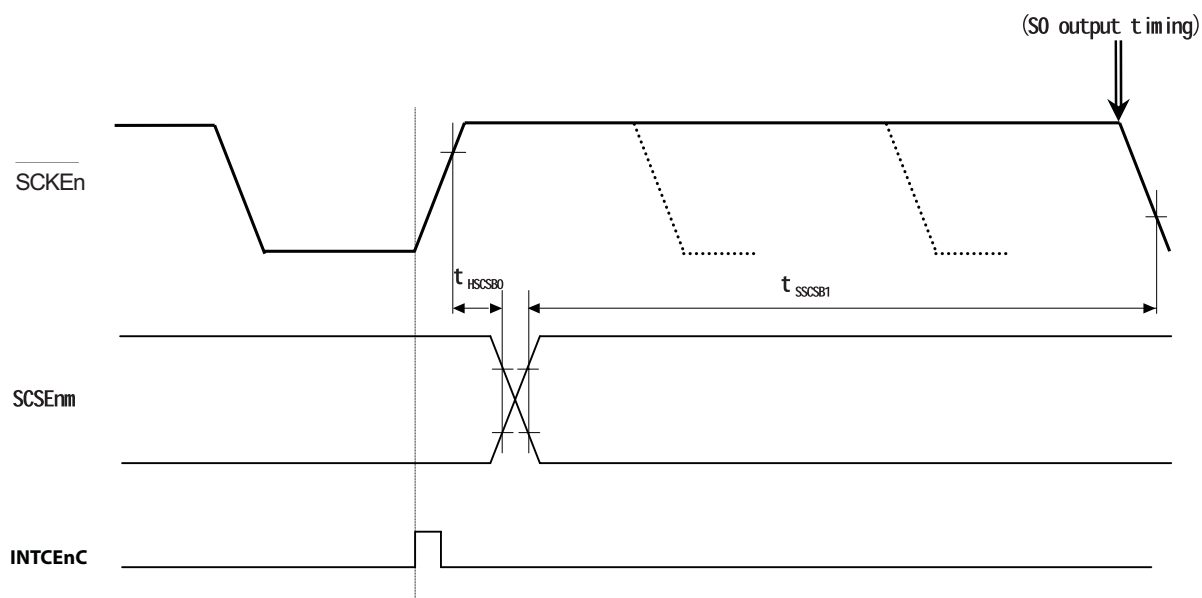
Figure 1-19: CSEn7 - CSEn0 Pin Timings

(e) Only In Master Mode (CEnCTL0:CEnSIT=0 & CEnCTL4:CEnOPE/CEnMD=0/0)



Remark: n=0-1
 m=7-0(n=0),3-0(n=1)
 INTCEnC: CSIE n transfer end interrupt

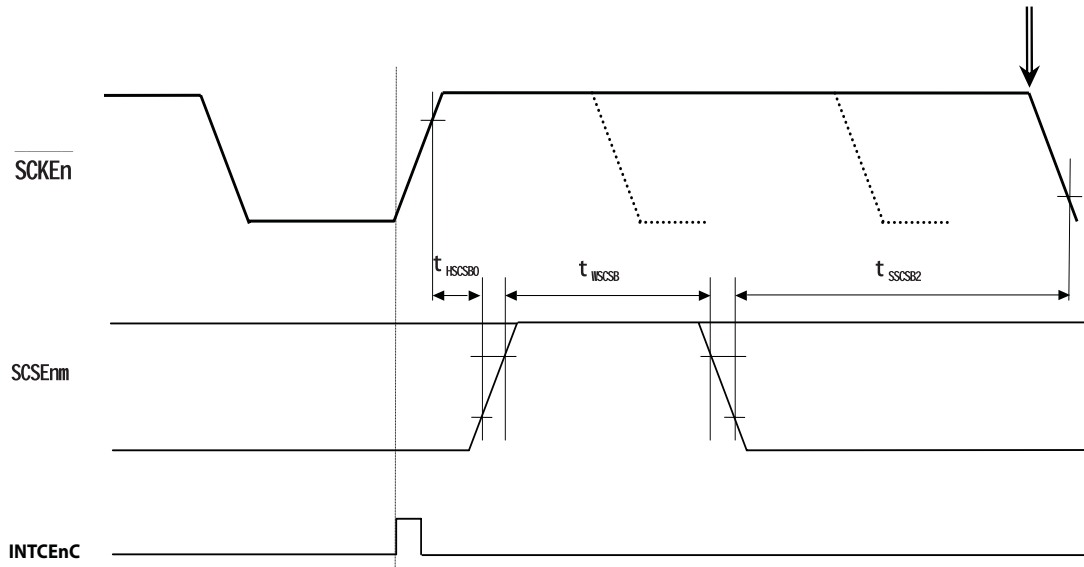
(f) Only In Master Mode (CEnCTL0:CEnSIT=0 & CEnCTL4:CEnOPE/CEnMD=1/0)



Remark: n=0-1
 m=7-0(n=0),3-0(n=1)
 INTCEnC: CSIE n transfer end interrupt

(g) Only In Master Mode (CEnCTL0:CEnSIT=0 & CEnCTL4:CEnOPE/CEnMD=1/1)

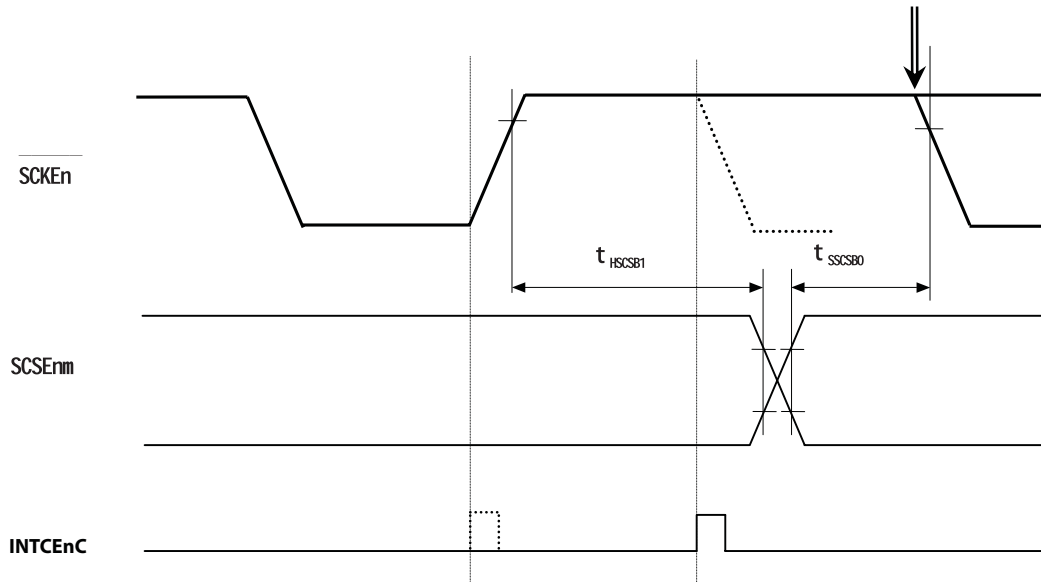
(S0 output timing)



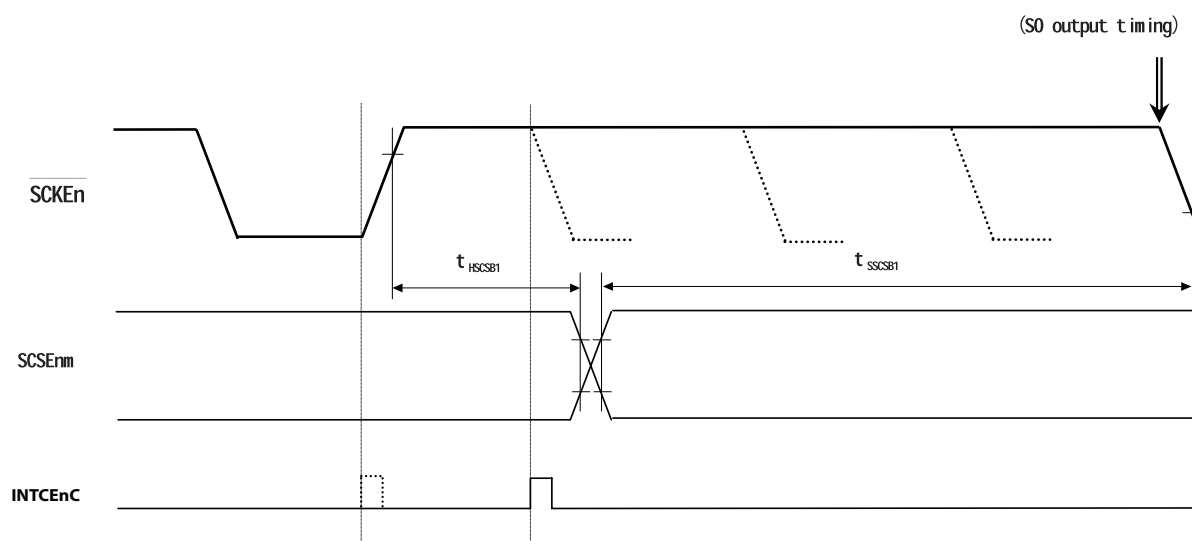
Remark: n=0-1
m=7-0(n=0),3-0(n=1)
INTCEnC: CSIEn transfer end interrupt

(h) Only In Master Mode (CEnCTL0:CEnSIT=1 & CEnCTL4:CEnOPE/CEnMD=0/0)

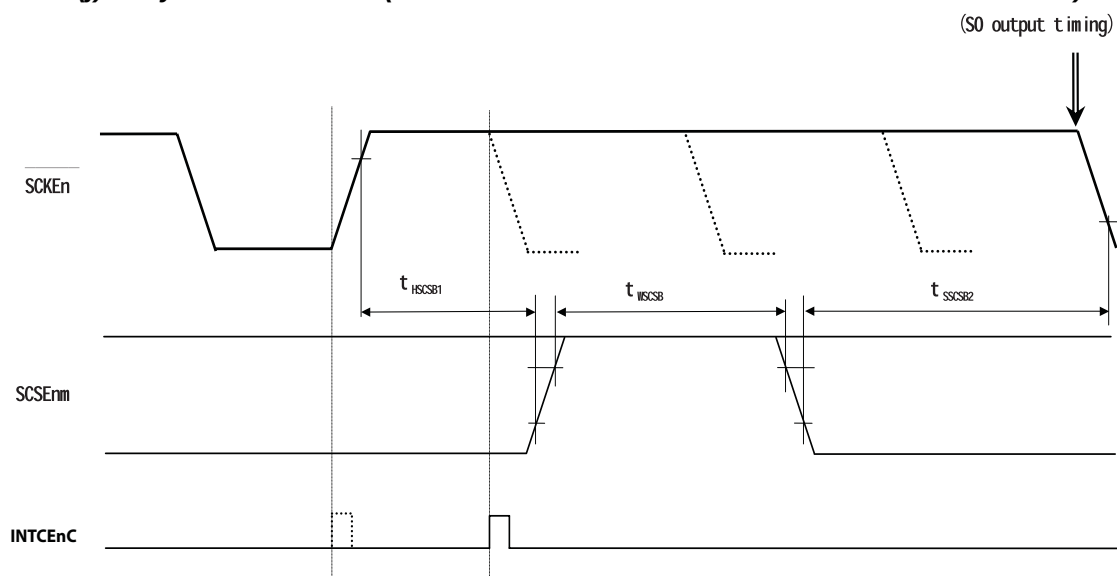
(S0 output timing)



Remark: n=0-1
m=7-0(n=0),3-0(n=1)
INTCEnC: CSIEn transfer end interrupt

(i) Only In Master Mode (CEnCTL0:CEnSIT=1 & CEnCTL4:CEnOPE/CEnMD=1/0)

Remark: n=0-1
 m=7-0(n=0),3-0(n=1)
 INTCEnC: CSIEnc transfer end interrupt

(j) Only In Master Mode (CEnCTL0:CEnSIT=1 & CEnCTL4:CEnOPE/CEnMD=1/1)

Remark: n=0-1
 m=7-0(n=0),3-0(n=1)
 INTCEnC: CSIEnc transfer end interrupt

1.6.7 UARTC Timing

$T_a = -40$ to $+125^{\circ}\text{C}$

$T_j = -40$ to $+150^{\circ}\text{C}$

$V_{DD15x} = CV_{DD15} = 1.5\text{V} \pm 10\%$,

$V_{DD3x} = 3.3\text{V} \pm 0.3\text{V}$,

$V_{SS15x} = CV_{SS15} = V_{SS3x} = 0\text{V}$

The load capacity of the output terminal is $CL=35\text{pF}$.

Table 1-20: UARTC Timing

Parameter	Symbol	Conditions	MIN.	MAX.	Unit
Transfer rate	TUARTC			4	Mbps

1.6.8 CAN Timing

$T_a = -40$ to $+125^{\circ}\text{C}$

$T_j = -40$ to $+150^{\circ}\text{C}$

$V_{DD15x} = CV_{DD15} = 1.5\text{V} \pm 10\%$,

$V_{DD3x} = 3.3\text{V} \pm 0.3\text{V}$,

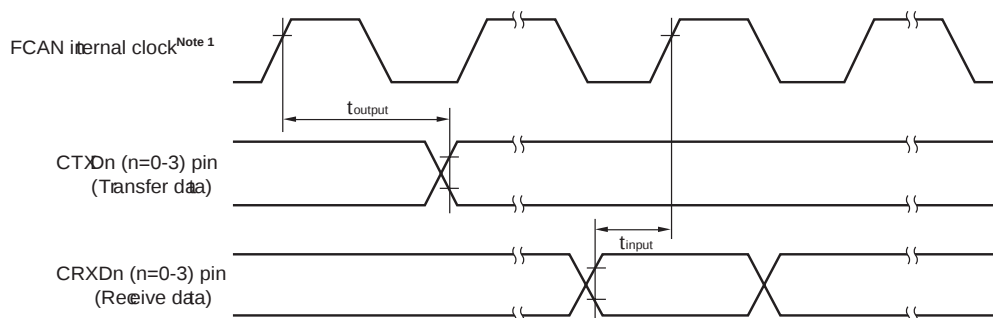
$V_{SS15x} = CV_{SS15} = V_{SS3x} = 0\text{V}$

The load capacity of the output terminal is $CL=35\text{pF}$.

Table 1-21: CAN Timing

Parameter	Symbol	Conditions	MIN.	MAX.	Unit
Internal transmit to receive data delay	t_{node}	$t_{\text{node}} = t_{\text{output}} + t_{\text{input}}$		75	ns

Figure 1-22: CAN Timing



Notes: 1. The FCAN internal clock corresponds to the FCAN macro clock.

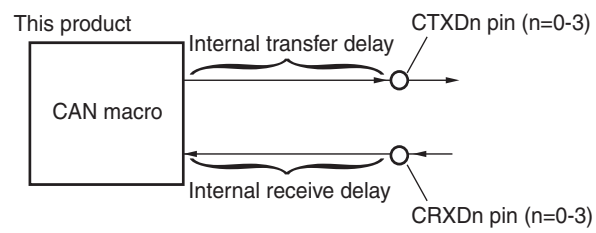
Figure 1-23: Internal Delay

Image figure of internal delay

1.6.9 AD Converter

$T_a = -40$ to $+125^{\circ}\text{C}$

$T_j = -40$ to $+150^{\circ}\text{C}$

$V_{DD15x} = CV_{DD15} = 1.5\text{V} \pm 10\%\text{V}$,

$V_{DD3x} = 3.3\text{V} \pm 0.3\text{V}$,

$AV_{DD} = AV_{REF0,1} = 3.3\text{V} \pm 0.3\text{V}$,

$V_{SS15x} = CV_{SS15} = V_{SS3x} = 0\text{V}$,

Table 1-24: AD Converter

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Resolution				10		bit
Overall error ^a	TOE				± 4	LSB
Quantisation error					± 0.5	LSB
Conversion time (Note 2)	t_{CONV}		2.0		8.0	μs
Sampling time	t_{SAMP}	(Note 1)		$3 \times t_{\text{CONV}} / 16$		s
Analog input voltage	V_{IAN}		$AV_{SS0,1}$		$AV_{REF0,1}$	V
AV_{REFn} input voltage	$AV_{REF0,1}$	$AV_{REF0,1} = AV_{DD}$			AV_{DD}	V
AV_{REFn} input current	$AI_{REF0,1}$			60	300	μA
AV_{DD} electric current	AI_{DD}				6	mA

a. The quantization error is not included.

- Notes:**
1. The conversion time is set by the ADMn1 register. For ADMn1 register setting please refer to the users manual.
 2. The conversion time only in the analog part. The conversion time depends on register setting ADMn1. For ADMn1 register setting please refer to the users manual.

1.6.10 Flash Memory Programming Characteristics

(1) Basic Characteristics

$T_a = -40$ to $+125^{\circ}\text{C}$

$T_j = -40$ to $+150^{\circ}\text{C}$

$V_{DD15x} = CV_{DD15} = 1.5\text{V} \pm 10\%V$,

$V_{DD3x} = 3.3\text{V} \pm 0.3\text{V}$,

$AV_{DD} = AV_{REF0,1} = 3.3\text{V} \pm 0.3\text{V}$,

$V_{SS15x} = CV_{SS15} = V_{SS3x} = 0\text{V}$,

The load capacity of the output terminal is $CL=35\text{pF}$.

Table 1-25: Flash Programming Characteristics

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Operating Frequency	f_{xx}		80		128	MHz
High Level Input Voltage	V_{IH}	FLMD0	$0.7V_{DD3x}$		V_{DD3x}	
Low Level Input Voltage	V_{IL}	FLMD0	-0.5		$0.3V_{DD3x}$	
Code Flash	Reprogramming				100	times
	Data retention				15	years
Data Flash	Reprogramming				10000	times
	Data retention				3	years

(2) Serial Writing Operating Conditions

$T_a = -40$ to $+125^{\circ}\text{C}$

$T_j = -40$ to $+150^{\circ}\text{C}$

$V_{DD15x} = CV_{DD15} = 1.5\text{V} \pm 10\%V$,

$V_{DD3x} = 3.3\text{V} \pm 0.3\text{V}$,

$AV_{DD} = AV_{REF0,1} = 3.3\text{V} \pm 0.3\text{V}$,

$V_{SS15x} = CV_{SS15} = V_{SS3x} = 0\text{V}$,

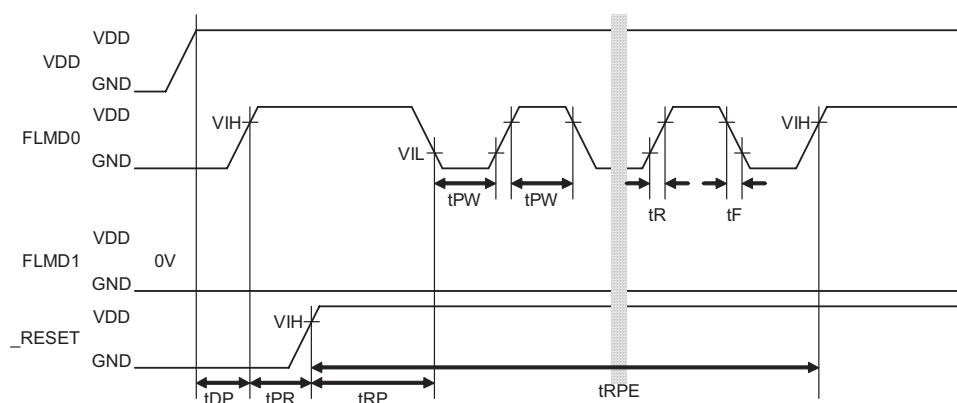
The load capacity of the output terminal is $CL=35\text{pF}$.

Table 1-26: Serial Writing Characteristics

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
FLMD0 setup time (from VDD)	t_{DP}		1			ms
RESET release (from FLMD0)	t_{PR}	(Note 1)	2			ms
Count start time from $\overline{\text{RESET}}$ to FLMD0	f_{RP}		1.2			ms
Count finish time from $\overline{\text{RESET}}$ to FLMD0	f_{RPE}				10	ms
FLMD0 high / low level width	t_{PW}		10		100	μs
FLMD0 raise / fall time	t_R / t_F				1	μs

Notes: 1. Please consider also the power supply turning on to $\overline{\text{RESET}}$ release timing.

Figure 1-27: Serial Write Operation Timing



2. Recommended Soldering Conditions

Solder this product under the following recommended conditions.

For details of the recommended soldering conditions, refer to the Joint Industry Standard:

JEDEC J-STD-020C (MSL=3)

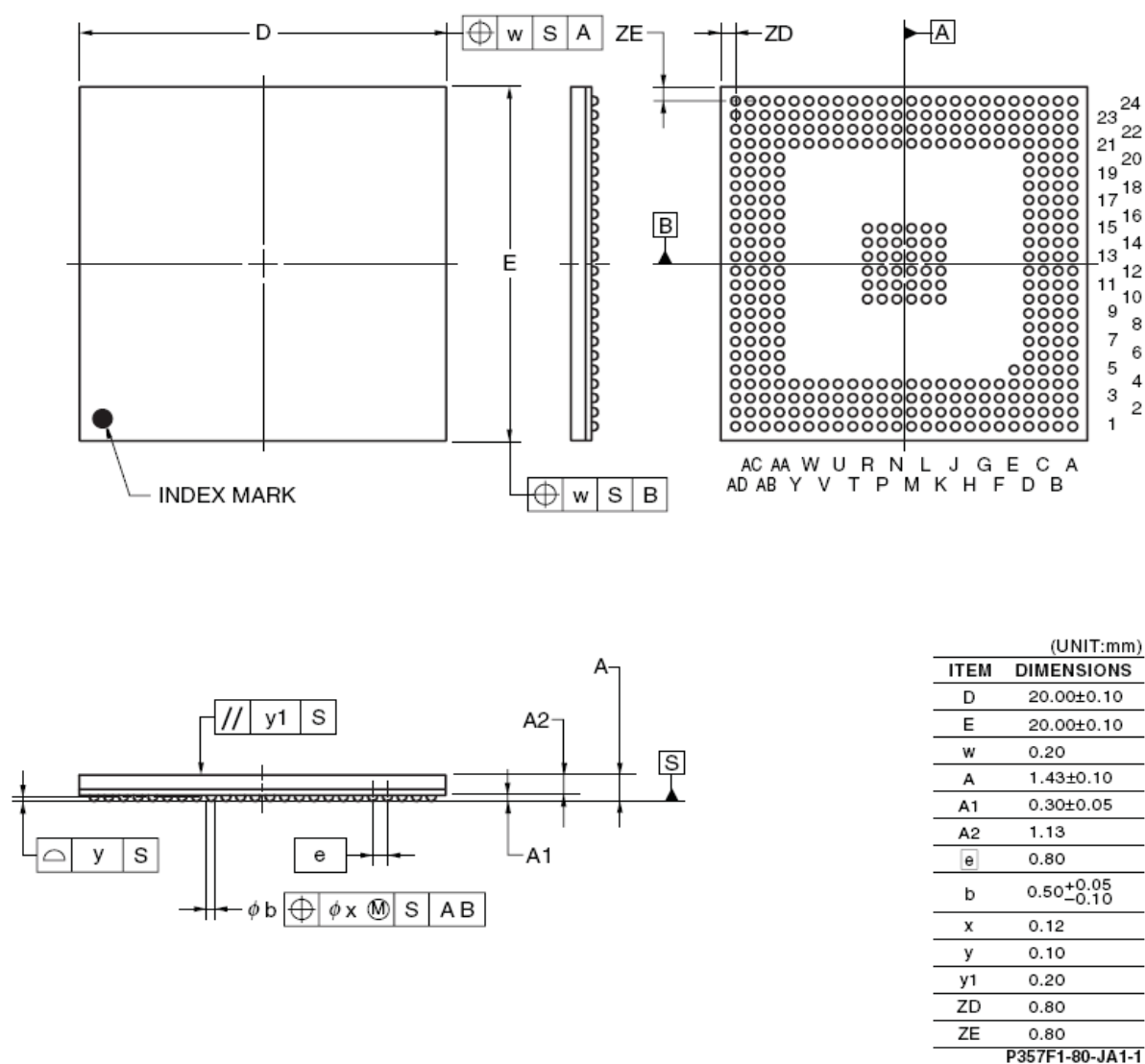
For soldering methods and conditions other than those recommended please consult NEC.

[MEMO]

3. Package Drawings

Figure 3-1: μ PD70F3483F1(A2)-JA1, μ PD70F3441F1(A2)-JA1

357-PIN PLASTIC FBGA (20x20)



© NEC Electronics Corporation 2006

[MEMO]

4. Revision History

Table 4-1: Revision History

Version	Date	Remarks.
1.0	2006/05/31	Initial revision
1.1	2007/07/05	I _{DD} currents for 80 MHz added (Table 1-7 on page 7)
		Revision history added
		Adjusted min timings for tRLR and tRIR
		Flash characteristics added
		Added special storage temperature
		Changed naming from CV _{DD} to CV _{DD15}
		Added reset timing
		NBD operating temperature added
		Junction temperature for bare die added
		External asynchronous memory access timing updated
		CSIB timing updated
		CSIE slave mode, formula of t _{HSIS} corrected
		CSIE master mode, formula of t _{SSCSB2} corrected
		Turning On / Interception timing modified
		Package drawing, parameters A and A1, updated.
2.0	2008/05/19	μPD70F3483 added
		Temperature range for Bare Die added
		MSL for soldering conditions added

[MEMO]

Notes for CMOS Devices

1. Precaution against ESD for semiconductors

Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

2. Handling of unused input pins for CMOS

No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to VDD or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

3. Status before initialization of MOS devices

Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

Legal Notes

- The information in this document is current as of May 2008. The information is subject to change without notice. For actual design-in, refer to the latest publications of NEC Electronics data sheets or data books, etc., for the most up-to-date specifications of NEC Electronics products. Not all products and/or types are available in every country. Please check with an NEC sales representative for availability and additional information.
- No part of this document may be copied or reproduced in any form or by any means without prior written consent of NEC Electronics. NEC Electronics assumes no responsibility for any errors that may appear in this document.
- NEC Electronics does not assume any liability for infringement of patents, copyrights or other intellectual property rights of third parties by or arising from the use of NEC Electronics products listed in this document or any other liability arising from the use of such NEC Electronics products. No license, express, implied or otherwise, is granted under any patents, copyrights or other intellectual property rights of NEC Electronics or others.
- Descriptions of circuits, software and other related information in this document are provided for illustrative purposes in semiconductor product operation and application examples. The incorporation of these circuits, software and information in the design of customer's equipment shall be done under the full responsibility of customer. NEC Electronics assumes no responsibility for any losses incurred by customers or third parties arising from the use of these circuits, software and information.
- While NEC Electronics endeavors to enhance the quality, reliability and safety of NEC Electronics products, customers agree and acknowledge that the possibility of defects thereof cannot be eliminated entirely. To minimize risks of damage to property or injury (including death) to persons arising from defects in NEC Electronics products, customers must incorporate sufficient safety measures in their design, such as redundancy, fire-containment and anti-failure features.
- NEC Electronics products are classified into the following three quality grades: "Standard", "Special" and "Specific".

The "Specific" quality grade applies only to NEC Electronics products developed based on a customer-designated "quality assurance program" for a specific application. The recommended applications of NEC Electronics product depend on its quality grade, as indicated below. Customers must check the quality grade of each NEC Electronics product before using it in a particular application.

"Standard":	Computers, office equipment, communications equipment, test and measurement equipment, audio and visual equipment, home electronic appliances, machine tools, personal electronic equipment and industrial robots.
"Special":	Transportation equipment (automobiles, trains, ships, etc.), traffic control systems, anti-disaster systems, anti-crime systems, safety equipment and medical equipment (not specifically designed for life support).
"Specific":	Aircraft, aerospace equipment, submersible repeaters, nuclear reactor control systems, life support systems and medical equipment for life support, etc.

The quality grade of NEC Electronics products is "Standard" unless otherwise expressly specified in NEC Electronics data sheets or data books, etc. If customers wish to use NEC Electronics products in applications not intended by NEC Electronics, they must contact NEC Electronics sales representative in advance to determine NEC Electronics 's willingness to support a given application.

- Notes:**
1. "NEC Electronics" as used in this statement means NEC Electronics Corporation and also includes its majority-owned subsidiaries.
 2. "NEC Electronics products" means any product developed or manufactured by or for NEC Electronics (as defined above).
 3. SuperFlash[®] is a registered trademark of Silicon Storage Technology, Inc. in several countries including the United States and Japan. This product uses SuperFlash[®] technology licensed from Silicon Storage Technology, Inc.

Regional Information

Some information contained in this document may vary from country to country. Before using any NEC product in your application, please contact the NEC office in your country to obtain a list of authorized representatives and distributors. They will verify:

- Device availability
- Ordering information
- Product release schedule
- Availability of related technical literature
- Development environment specifications (for example, specifications for third-party tools and components, host computers, power plugs, AC supply voltages, and so forth)
- Network requirements

In addition, trademarks, registered trademarks, export restrictions, and other legal issues may also vary from country to country.

NEC Electronics Inc. (U.S.)

Santa Clara, California

Tel: 408-588-6000

800-366-9782

Fax: 408-588-6130

800-729-9288

NEC Electronics (Europe) GmbH

Duesseldorf, Germany

Tel: 0211-65 03 01

Fax: 0211-65 03 327

Sucursal en España

Madrid, Spain

Tel: 091- 504 27 87

Fax: 091- 504 28 60

Succursale Française

Vélizy-Villacoublay, France

Tel: 01-30-67 58 00

Fax: 01-30-67 58 99

Filiale Italiana

Milano, Italy

Tel: 02-66 75 41

Fax: 02-66 75 42 99

Branch The Netherlands

Eindhoven, The Netherlands

Tel: 040-244 58 45

Fax: 040-244 45 80

Branch Sweden

Taeby, Sweden

Tel: 08-63 80 820

Fax: 08-63 80 388

United Kingdom Branch

Milton Keynes, UK

Tel: 01908-691-133

Fax: 01908-670-290

NEC Electronics Hong Kong Ltd.

Hong Kong

Tel: 2886-9318

Fax: 2886-9022/9044

NEC Electronics Hong Kong Ltd.

Seoul Branch

Seoul, Korea

Tel: 02-528-0303

Fax: 02-528-4411

NEC Electronics Singapore Pte. Ltd.

Singapore

Tel: 65-6253-8311

Fax: 65-6250-3583

NEC Electronics Taiwan Ltd.

Taipei, Taiwan

Tel: 02-2719-2377

Fax: 02-2719-5951

NEC do Brasil S.A.

Electron Devices Division

Guarulhos, Brasil

Tel: 55-11-6465-6810

Fax: 55-11-6465-6829

[MEMO]

Facsimile Message

From:

Name

Company

Tel.

FAX

Address

Although NEC has taken all possible steps to ensure that the documentation supplied to our customers is complete, bug free and up-to-date, we readily accept that errors may occur. Despite all the care and precautions we've taken, you may encounter problems in the documentation. Please complete this form whenever you'd like to report errors or suggest improvements to us.

Thank you for your kind support.

North America

NEC Electronics America Inc.
Corporate Communications Dept.
Fax: 1-800-729-9288
1-408-588-6130

Hong Kong, Philippines, Oceania

NEC Electronics Hong Kong Ltd.
Fax: +852-2886-9022/9044

Asian Nations except Philippines

NEC Electronics Singapore Pte. Ltd.
Fax: +65-6250-3583

Europe

NEC Electronics (Europe) GmbH
Market Communication Dept.
Fax: +49(0)-211-6503-1344

Korea

NEC Electronics Hong Kong Ltd.
Seoul Branch
Fax: 02-528-4411

Japan

NEC Semiconductor Technical Hotline
Fax: +81- 44-435-9608

Taiwan

NEC Electronics Taiwan Ltd.
Fax: 02-2719-5951

I would like to report the following error/make the following suggestion:

Document title: _____

Document number: _____ Page number: _____

If possible, please fax the referenced page or drawing.

Document Rating	Excellent	Good	Acceptable	Poor
Clarity	☐	☐	☐	☐
Technical Accuracy	☐	☐	☐	☐
Organization	☐	☐	☐	☐

[MEMO]