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April 1st, 2010 Renesas Electronics Corporation

Issued by: Renesas Electronics Corporation (http://www.renesas.com)

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DATA SHEET



$\frac{\text{MOS FIELD EFFECT TRANSISTOR}}{\text{Phase-out/Discontinued}} \qquad \mu PA1850$

P-CHANNEL MOS FIELD EFFECT TRANSISTOR FOR SWITCHING

DESCRIPTION

The μ PA1850 is a switching device which can be driven directly by a 2.5-V power source.

The μ PA1850 features a low on-state resistance and excellent switching characteristics, and is suitable for applications such as power switch of portable machine and so on.

FEATURES

- Can be driven by a 2.5-V power source
- Low on-state resistance $R_{DS(on)1} = 115 \text{ m}\Omega \text{ MAX}. (V_{GS} = -4.5 \text{ V}, \text{ ID} = -1.5 \text{ A})$ $R_{DS(on)2} = 130 \text{ m}\Omega \text{ MAX}. (V_{GS} = -4.0 \text{ V}, \text{ ID} = -1.5 \text{ A})$ $R_{DS(on)3} = 200 \text{ m}\Omega \text{ MAX}. (V_{GS} = -2.5 \text{ V}, \text{ ID} = -1.5 \text{ A})$
- Built-in G-S protection diode against ESD

ORDERING INFORMATION

PART NUMBER	PACKAGE	
μPA1850GR-9JG	Power TSSOP8	

ABSOLUTE MAXIMUM RATINGS (TA = 25°C)

Drain to Source Voltage	VDSS	-12	
Gate to Source Voltage	Vgss	-10/+5	
Drain Current (DC)	ID(DC)	∓2.5	
Drain Current (pulse) Note1	D(pulse)	∓10	
Total Power Dissipation Note2	Рт	2.0	
Channel Temperature	Tch	150	
Storage Temperature	Tstg	–55 to +150	

Notes 1. PW \leq 10 μ s, Duty Cycle \leq 1 %

2. Mounted on ceramic substrate of 5000 mm² x 1.1 mm

Remark The diode connected between the gate and source of the transistor serves as a protector against ESD. When this device actually used, an additional protection circuit is externally required if a voltage exceeding the rated voltage may be applied to this device.

V

V

A

Α

W

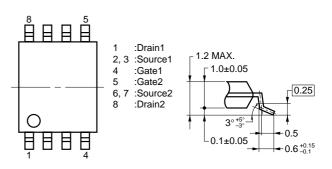
°C °C

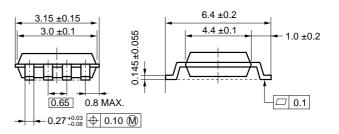
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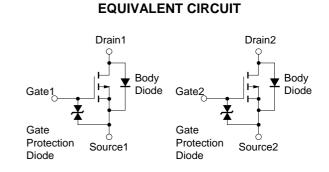
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The mark \star shows major revised points.

PACKAGE DRAWING (Unit : mm)





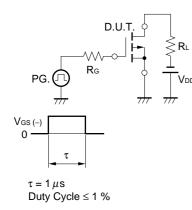


ELECTRICAL CHARACTERISTICS (TA = 25 °C)

	CHARACTERISTICS	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
	Drain Cut-off Current	IDSS	$V_{DS} = -12 V, V_{GS} = 0 V$			-10	μA
	Gate Leakage Current	lgss	$V_{GS} = \mp 10 \text{ V}, \text{ Vds} = 0 \text{ V}$			∓ 10	μA
*	Gate to Source Cut-off Voltage	VGS(off)	$V_{DS} = -10 \text{ V}, \text{ Id} = -1 \text{ mA}$	-0.5	-1.0	-1.5	V
*	Forward Transfer Admittance	y _{fs}	Vds = -10 V, Id = -1.5 A	2.0	5.0		S
	Drain to Source On-state Resistance	RDS(on)1	V _{GS} = -4.5 V, I _D = -1.5 A		80	115	mΩ
		RDS(on)2	V _{GS} = -4.0 V, I _D = -1.5 A		85	130	mΩ
		RDS(on)3	V _{GS} = −2.5 V, I _D = −1.5 A		127	200	mΩ
	Input Capacitance	Ciss	VDS = -10 V		260		pF
	Output Capacitance	Coss	V _{GS} = 0 V		300		pF
	Reverse Transfer Capacitance	Crss	f = 1 MHz		45		pF
	Turn-on Delay Time	td(on)	$V_{DD} = -10 V$		120		ns
	Rise Time	tr	I⊳ = −1.5 A		420		ns
	Turn-off Delay Time	td(off)	$V_{GS(on)} = -4.0 V$		520		ns
	Fall Time	tr	R _G = 10 Ω		430		ns
	Total Gate Charge	Q _G	Vdd = -10 V		12		nC
	Gate to Source Charge	Q _{GS}	I⊳ = −2.5 A		2		nC
	Gate to Drain Charge	Qgd	Vgs = -4.0 V		5		nC
	Diode Forward Voltage	VF(S-D)	IF = 2.5 A, VGS = 0 V		0.80		V
★	Reverse Recovery Time	trr	IF = 2.5 A, VGS = 0 V		750		ns
*	Reverse Recovery Charge	Qrr	di/dt = 10 A/ μ s		950		nC

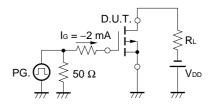
TEST CIRCUIT 1 SWITCHING TIME

Vdd

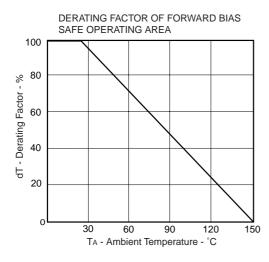


V _{GS} Wave Form	V _{GS} (-) 0 10 %
ID Wave Form	ID (-) 90 % 1D (-) 90 % 1D 10 % 10 %

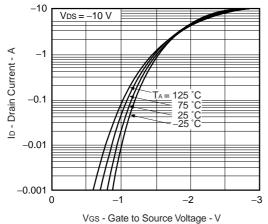
TEST CIRCUIT 2 GATE CHARGE



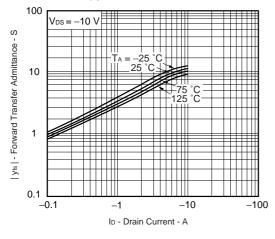
* TYPICAL CHARACTERISTICS (TA = 25°C)



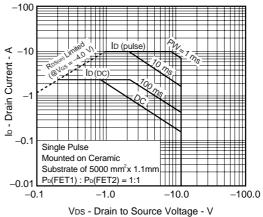




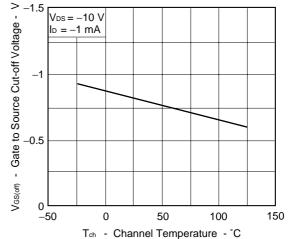
FORWARD TRANSFER ADMMITTANCE vs. DRAIN CURRENT



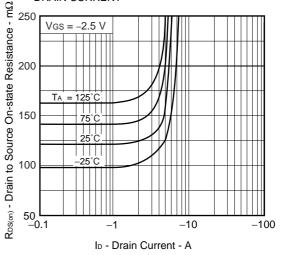
FORWARD BIAS SAFE OPERATING AREA

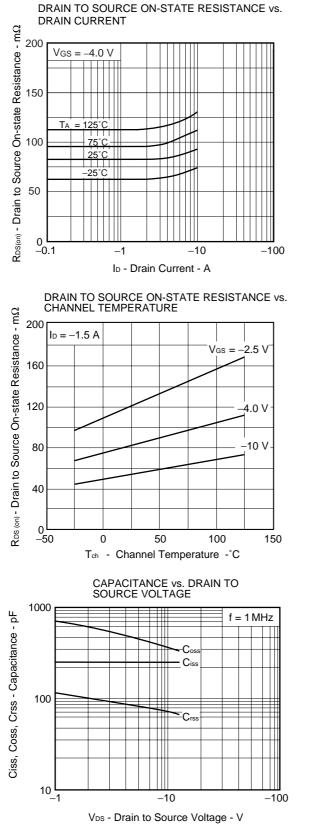


GATE TO SOURCE CUT-OFF VOLTAGE vs. CHANNEL TEMPERATURE

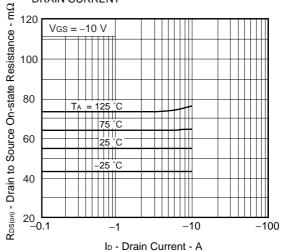


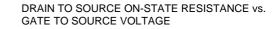
DRAIN TO SOURCE ON-STATE RESISTANCE vs. DRAIN CURRENT

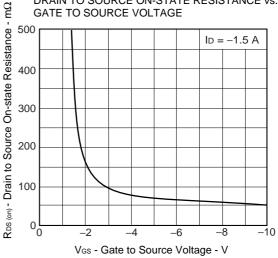




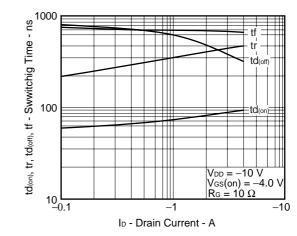
DRAIN TO SOURCE ON-STATE RESISTANCE vs. DRAIN CURRENT



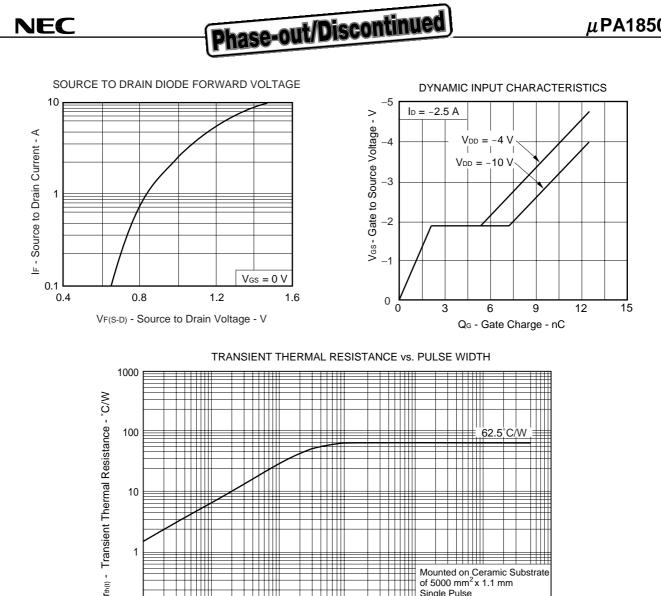








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1

PW - Pulse Width - S

10

Mounted on Ceramic Substrate of 5000 mm² x 1.1 mm Single Pulse $P_D(FET1) : P_D(FET2) = 1:1$

100

1000

10m

0.1

1m

100m

NEC

μ**ΡΑ1850**

[MEMO]

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