

## PMIC with High PSRR, Low Noise, Multi-Output LDOs and Integrated Load Switch

### General Description

SLG51001 contains six compact and customizable low dropout regulators and is designed for high performance camera modules and other small multi-rail applications.

The LDO\_HP is optimized to meet the requirements of high-performance analog circuits. It provides very low output voltage noise characteristics of 13  $\mu\text{V}$  (rms) in addition to high PSRR of 81 dB at 1 MHz and tight output voltage accuracy of  $\pm 1\%$  over temperature.

The 1 A capable LDO\_LV can be configured to operate as a load switch which is optimized to meet the requirements of low  $R_{\text{ON}}$ . By using efficient DC-DC switching regulators upstream in conjunction with SLG51001's linear regulators and load switch downstream, applications can leverage the best characteristics of each to simultaneously achieve low power, low noise, and low voltage dropout, respectively.

Built-in safety protection such as under-voltage lockout, over-temperature protection, and current limit ensures that the ICs are operating under nominal conditions. SLG51001 has an I<sup>2</sup>C-compatible interface for flexible power control. SLG51001 is available in a small 16-pin WLCSP package with a wide ambient operating temperature range of -40 °C to 85 °C.

### Key Features

- Input voltage range:
  - 2.8 V to 5.0 V (1 x HP LDO)
  - 1.7 V to 5.0 V (4 x HV LDO)
  - 0.8 V to 1.5 V (1 x LV LDO)
  - 0.5 V to 1.25 V (1 x load switch)
- Separate input supply and enable pins for flexible power configurations
- Output voltage range:
  - 2.4 V to 3.3 V (1 x HP LDO)
  - 1.2 V to 3.75 V (4 x HV LDO)
  - 0.5 V to 1.2 V (1 x LV LDO)
- Output current levels:
  - Up to 475 mA (1 x HP LDO)
  - Up to 500 mA (4 x HV LDO)
  - Up to 1 A (1 x LV LDO)
  - Up to 1 A (1 x load switch)
- High PSRR of 102 dB at 1 kHz and 81 dB at 1 MHz (1 x HP LDO)
- Ultra-low output voltage noise of 13  $\mu\text{V}$  (1 x HP LDO)
- Low dropout voltage (10 mV per 100 mA of load) for high current LDO supply rail (LV LDO)
- Ultra-low  $R_{\text{ON}}$  load switch with low leakage and slew rate control for low  $V_{\text{IN}}$  supplies
- Tight output voltage accuracy of  $\pm 1\%$  over-temperature
- Low shutdown current of 300 nA
- Low quiescent current of 14  $\mu\text{A}$
- User configurable settings via I<sup>2</sup>C interface and OTP
  - Including output voltage, power sequencing, soft-start timing, and current limit threshold
- Soft start and soft shutdown
- Under-voltage lockout (UVLO)
- Thermal shutdown
- Configurable temperature alerts
- Wide -40 °C to +85 °C operating temperature
- 16-pin WLCSP: 1.675 mm x 1.675 mm x 0.465 mm, 0.4 mm pitch

### Applications

- High End Camera Module Applications
- Smartphones
- Digital Cameras
- Smart Devices with Imaging

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1 Block Diagram

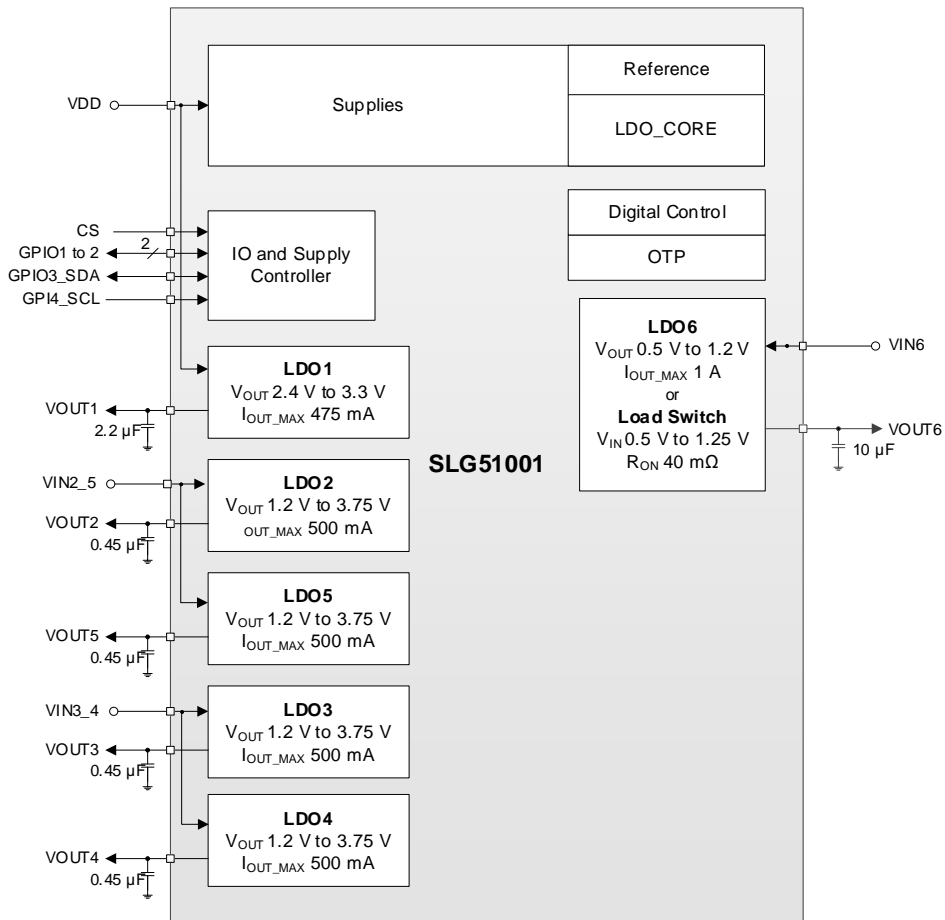


Figure 1: Block Diagram

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2 Pinout

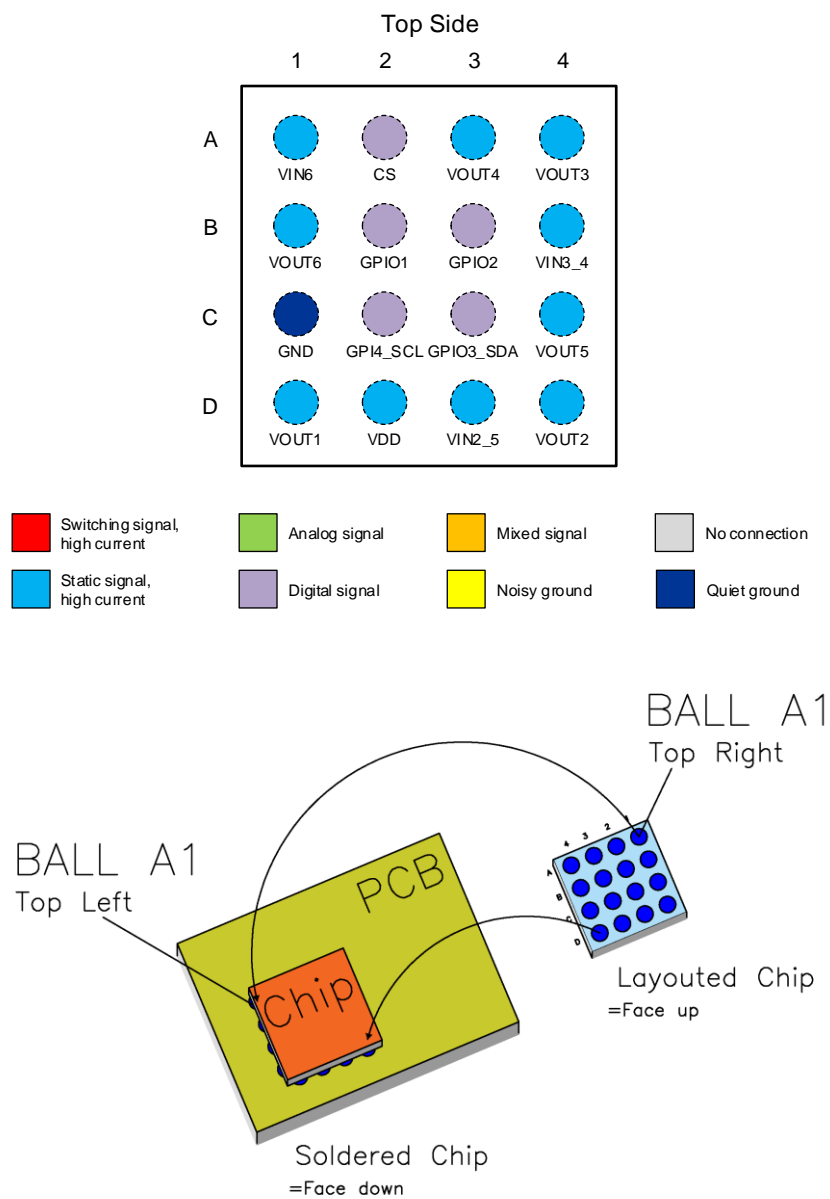


Figure 2: Pinout Diagram (Top View, Face Down)

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**Table 1: Pin Description**

Pin No.	Pin Name	Type (Table 2)	Drive (mA)	Reset State	Description
A2	CS	DI/PWR			Chip select. Also used as the OTP programming power supply.
C1	GND	GND			Ground.
C2	GPI4_SCL	DI			1.2 V/1.8 V input cell, or I <sup>2</sup> C Serial Clock Line (SCL).
B2	GPIO1	DIOD			1.2 V/1.8 V input cell, open-drain output.
B3	GPIO2	DIOD			1.2 V/1.8 V input cell, open-drain output.
C3	GPIO3_SDA	DIOD			1.2 V/1.8 V input cell, open-drain output, or I <sup>2</sup> C Serial Data Line (SDA).
D2	VDD	PWR			Supply voltage for overall chip control. Controller and power FET supply voltage for low noise LDO (LDO1).
D3	VIN2_5	PWR			Controller and power FET supply voltage for LDO2 and LDO5.
B4	VIN3_4	PWR			Controller and power FET supply voltage for LDO3 and LDO4.
A1	VIN6	PWR			Controller and power FET supply voltage for LDO6. LDO6 can be configured as a load switch
D1	VOUT1	PWR			LDO1 power output.
D4	VOUT2	PWR			LDO2 power output.
A4	VOUT3	PWR			LDO3 power output.
A3	VOUT4	PWR			LDO4 power output.
C4	VOUT5	PWR			LDO5 power output.
B1	VOUT6	PWR			LDO6 power output. LDO6 can be configured as a load switch.

**Table 2: Pin Type Definition**

Pin Type	Description	Pin Type	Description
DI	Digital input	AI	Analog input
DO	Digital output	AO	Analog output
DIO	Digital input/output	AIO	Analog input/output
DIOD	Digital input/output open drain	BP	Back drive protection
PU	Pull-up resistor (fixed)	SPU	Switchable pull-up resistor
PD	Pull-down resistor (fixed)	SPD	Switchable pull-down resistor
PWR	Power	GND	Ground

## 2.1 Input Pins

### 2.1.1 CS – Chip Select

This active-high pin is used to wake SLG51001 from a low-power reset state

To guarantee correct operation, CS must be de-asserted whenever the voltage at the VDD pin is out of the operating conditions boundary (that is  $VDD < 2.8\text{ V}$ , or  $VDD > 5.0\text{ V}$ ). See [Guidelines for Reliable Operation](#).

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When de-asserting the CS pin, it can have a programmable shutdown debounce time (from 0  $\mu$ s to 256  $\mu$ s, register CS\_T\_DEB).

### 2.1.2 SCL – I<sup>2</sup>C Clock

The SCL signal is the I<sup>2</sup>C clock.

## 2.2 Bidirectional Pins

### 2.2.1 GPIO1 to GPIO3 and GPI4 – General Purpose Input/Output

The general-purpose input/output pins are configurable by dedicated registers (IO\_GPIO<x>\_CONF). GPIO1 to GPIO3 can be configured as an input or an open-drain output. GPI4 is always an input pin. In the LOW IQ RESET state, all GPIOs are configured as inputs with no pull-down.

The user-configurable input levels are 1.2 V and 1.8 V.

### 2.2.2 SDA – I<sup>2</sup>C Data

The SDA signal is the I<sup>2</sup>C data signal. It is an open-drain signal so that either side can pull it down to a logic low level.

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### 3 Characteristics

#### 3.1 Absolute Maximum Ratings

Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, so functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification are not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

**Table 3: Absolute Maximum Ratings**

Parameter	Description	Conditions	Min	Max	Unit
T <sub>STG</sub>	Storage temperature	Non operational	-40	+150	°C
T <sub>J</sub>	Junction temperature		-25	+125	°C
T <sub>A</sub>	Ambient temperature		-40	+85	°C
V <sub>DD</sub>	Power supply voltage on VDD pin		-0.3	+6.0	V
	Power supply voltage on VIN2_5, VIN3_4 pins		-0.3	+6.0	V
	Power supply voltage on VIN5_6 pin		-0.3	+1.8	V
V <sub>PIN_LV</sub>	Voltage on low-voltage pins	GPIO1 to GPIO3 and GPI4	-0.3	+1.98	V
V <sub>PIN_HV</sub>	Voltage on high-voltage pins	CS	-0.3	V <sub>DD</sub> + 0.3	V
ESD	ESD Protection (Human Body Model)		2000		V
	ESD Protection (Charged Device Model)		500		V

##### 3.1.1 Guidelines for Reliable Operation

- Low Voltage Pins: take care that the low voltage pins (GPIO1 to GPIO3, GPI4, and VIN6) do not exceed their Abs. Max. ratings, even briefly. Transients both positive (above max) and negative (below min) can cause EOS (Electrical Overstress) damage.
- Power sequencing: CS should not be asserted high before VDD is powered up. CS pin should be de-asserted before VDD falls out of operating range. VIN supplies for LDO\_HV and LDO\_LV channels (VIN2\_5, VIN3\_4, VIN6) can be safely biased even if VDD is not present. VIN supplies should be powered up before enabling their respective LDO channels. GPIO's configured as inputs are allowed to be forced high before VDD is powered up.

#### 3.2 Recommended Operating Conditions

**Table 4: Recommended Operating Conditions**

Parameter	Description	Conditions	Min	Typ	Max	Unit
T <sub>A</sub>	Ambient temperature		-40		+85	°C
V <sub>DD</sub>	Power supply voltage on VDD pin		2.8		5.0	V
	Power supply voltage on VIN2_5, VIN3_4 pins		1.7		5.0	V
	Power supply voltage on VIN6 pin	LDO Mode	0.8		1.5	V

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Parameter	Description	Conditions	Min	Typ	Max	Unit
	Power supply voltage on VIN6 pin	Load Switch Mode	0.5		1.25	V
V <sub>PIN_LV</sub>	Voltage on low-voltage pins	GPIO1 to GPIO3 and GPI4	0		1.8	V
V <sub>PIN_HV</sub>	Voltage on high-voltage pins	CS	0		VDD	V

### 3.3 Thermal Characteristics

Table 5: Package Ratings

Parameter	Description	Conditions	Min	Typ	Max	Unit
R <sub>e_JA</sub>	Package thermal resistance	Junction to ambient JEDEC standard PCB		64.3		K/W

### 3.4 Current Consumption

Note: Current consumption electrical characteristics apply over the full operating temperature range.

Table 6: Current Consumption

Parameter	Description	Conditions	Min	Typ	Max	Unit
<b>Electrical Performance</b>						
IQ_SLEEP	Current consumption in SLEEP. IQ_SLEEP is the IQ in LOW IQ RESET State	VIN = 3.8 V VIN6 = 0 V All references disabled I2C interface disabled All rails disabled		0.15	0.65	μA
IQ_READY_DIS	Current consumption in READY State	VIN = 3.8 V, VIN6 = 0 V All references enabled I2C interface enabled All rails disabled		14	24	μA
IQ_READY_EN	Current consumption in READY State	VIN = 3.8 V All references enabled I2C interface enabled All rails enabled, no load		390	630	μA
IQ_OFF_25C	Quiescent current in OFF Mode	TA = 25 °C			1	μA
IQ_OFF	Quiescent current in OFF Mode	TA = -40 °C to 85 °C			7.6	μA

### 3.5 Chip Select Digital I/O Characteristics

Digital I/O electrical characteristics apply over the full operating temperature range, see Section 3.1.1.



**PMIC with High PSRR, Low Noise, Multi-Output LDOs  
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Parameter	Description	Conditions	Min	Typ	Max	Unit
<b>Electrical Performance</b>						
VIH	CS input high voltage		0.9		VDD	V
VIL	CS input low voltage		0		0.2	V
ILKG	CS input leakage current	CS < 2V			1	μA
tON_READ Y	Turn-on time from CS HIGH to Ready State				10	ms

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### 3.6 1.2 V/1.8 V Digital I/O Characteristics

1.2 V/1.8 V digital I/O electrical characteristics apply over the full operating temperature range, see Section 3.1.1. The voltage thresholds for all I/Os are referenced to VDDIO, where VDDIO can be 1.2 V or 1.8 V. The supply configuration options depend on the I/O, see Register Definition.

**Table 8: 1.2 V/1.8 V Digital I/O Characteristics**

Parameter	Description	Conditions	Min	Typ	Max	Unit
<b>Electrical Performance</b>						
<b>GPIO1 to GPIO2</b>						
VTHR_PO S	Positive going threshold voltage		0.4*V DDIO		0.7*V DDIO	V
VTHR_NEG	Negative going threshold voltage		0.3*V DDIO		0.6*V DDIO	V
VOL	Output low voltage	IOUT ≤ IOL	0		0.3	V
IOL	Output current	VOL = 0.3 V	2	13		mA
ILKG	Input leakage				500	nA
<b>SCL, SDA, GPIO3 and GPI4</b>						
VTHR_PO S	Positive going threshold voltage		0.4*V DDIO		0.7*V DDIO	V
VTHR_NEG	Negative going threshold voltage		0.3*V DDIO		0.6*V DDIO	V
VHYS	Schmitt trigger hysteresis		0.1*V DDIO			V
VOL	Output low voltage SDA, GPIO5	IOUT ≤ IOL	0		0.3	V
IOL	Output current	VOL = 0.3 V	20			mA
ILKG	Input leakage				500	nA
CIN	Pin capacitance				10	pF

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### 3.7 LDO\_HP Characteristics

Table 9: LDO\_HP (LDO1) Electrical Characteristics

Parameter	Description	Conditions	Min	Typ	Max	Unit
<b>External Electrical Conditions</b>						
V <sub>IN</sub>	Input voltage		2.8		5	V
C <sub>OUT</sub>	Output capacitance	Effective capacitance after derating	2.2	4.7	10	μF
I <sub>OUT_MAX</sub>	Maximum output current	V <sub>IN</sub> = 3.3 V V <sub>OUT</sub> drops 50 mV	475			mA
<b>Programmable Conditions</b>						
V <sub>OUT</sub>	Selectable output voltage		2.4	2.85	3.3	V
V <sub>OUT_LSB</sub>	LSB of output voltage programming DAC (8-bit control)			5		mV
I <sub>OUT_STARTUP_LIM</sub>	Start-up current limit, programmable range <a href="#">Note 1</a>	At 90 % V <sub>OUT</sub>	11	140	240	mA
<b>Electrical Performance</b>						
<b>Static Parameters</b>						
V <sub>OUT_PP</sub>	Part to part output voltage accuracy <a href="#">Note 2</a>	I <sub>OUT</sub> = 1 mA T <sub>A</sub> = 25 °C	-5		5	mV
V <sub>OUT_TEMP</sub>	Temperature dependence of V <sub>OUT</sub> <a href="#">Note 2</a>	I <sub>OUT</sub> = 1 mA	-0.65		0.65	%
V <sub>OUT_STATIC_LINE</sub>	Static line regulation <a href="#">Note 2</a>	I <sub>OUT</sub> = 1 mA V <sub>IN</sub> = V <sub>OUT</sub> + V <sub>DROPOUT (Max)</sub> to V <sub>IN (Max)</sub>	-2		2	mV
V <sub>OUT_STATIC_LD</sub>	Static load regulation <a href="#">Note 2</a>	1 mA < I <sub>OUT</sub> < 300 mA	-7.5		5.5	mV
V <sub>DROPOUT</sub>	Dropout voltage	@ V <sub>OUT</sub> = V <sub>OUT (V<sub>IN (Max)</sub>)</sub> - 10 mV I <sub>OUT</sub> = 300 mA			200	mV
<b>Dynamic Parameters</b>						
V <sub>OUT_TR_LINE</sub>	Line transient response	V <sub>IN</sub> = V <sub>OUT</sub> + V <sub>DROPOUT (Max)</sub> + 100 mV to V <sub>IN</sub> = V <sub>OUT</sub> + V <sub>DROPOUT (Max)</sub> V <sub>OUT</sub> = V <sub>OUT (Typ)</sub> I <sub>OUT</sub> = 300 mA t <sub>R</sub> = t <sub>F</sub> = 1 μs			0.3	mV

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Parameter	Description	Conditions	Min	Typ	Max	Unit
$V_{OUT\_TR\_LD\_1}$ mA	Load transient response	$V_{IN} = V_{OUT} + V_{DROPOUT} (Max)$ $V_{OUT} = V_{OUT} (Typ)$ $I_{OUT} = 1 \text{ mA to } 300 \text{ mA}$ $t_R = t_F = 1 \mu s$			20	mV
$t_{ON}$	Turn-on time	Time to 90 % of $V_{OUT}$ $I_{OUT} = 0 \text{ mA}$		0.15		ms
$t_{OFF}$	Turn-off time	Time to 10 % of $V_{OUT}$ $I_{OUT} = 0 \text{ mA}$			2	ms
<b>AC Parameters</b>						
$PSRR_{1kHz}$	Power supply rejection ratio	$f = 1 \text{ kHz}$ $V_{IN} = 3.2 \text{ V}$ $V_{OUT} = V_{OUT} (Typ)$ $I_{OUT} = 150 \text{ mA}$ $C_{OUT} = 4.7 \mu F$ <a href="#">Note 3</a>		102		dB
$PSRR_{100kHz}$	Power supply rejection ratio	$f = 100 \text{ kHz}$ $V_{IN} = 3.2 \text{ V}$ $V_{OUT} = V_{OUT} (Typ)$ $I_{OUT} = 150 \text{ mA}$ $C_{OUT} = 4.7 \mu F$ <a href="#">Note 3</a>		87		dB
$PSRR_{1MHz}$	Power supply rejection ratio	$f = 1 \text{ MHz}$ $V_{IN} = 3.2 \text{ V}$ $V_{OUT} = V_{OUT} (Typ)$ $I_{OUT} = 150 \text{ mA}$ $C_{OUT} = 4.7 \mu F$ <a href="#">Note 3</a>		81		dB
$V_{N\_100kHz}$	Output noise	$f = 10 \text{ Hz to } 100 \text{ kHz}$ $V_{IN} = 3.2 \text{ V}$ $V_{OUT} = V_{OUT} (Typ)$ $I_{OUT} > 30 \text{ mA}$		13		$\mu V$
$V_{N\_1MHz}$	Output noise	$f = 10 \text{ Hz to } 1 \text{ MHz}$ $V_{IN} = 3.2 \text{ V}$ $V_{OUT} = V_{OUT} (Typ)$ $I_{OUT} > 10 \text{ mA}$		21		$\mu V$
<b>Current Limit Accuracy</b>						
$I_{OUT\_FUNC\_LIM}$	Functional current limit		500			mA
$I_{OUT\_STARTUP\_LIM\_ACC}$	Start-up current limit accuracy	$I_{OUT\_STARTUP\_LIM} > 11 \text{ mA}$	-50		50	%
$I_{OUT\_STARTUP\_LIM\_ACC\_11}$	Start-up current limit accuracy	$I_{OUT\_STARTUP\_LIM} = 11 \text{ mA}$	-75		75	%

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Parameter	Description	Conditions	Min	Typ	Max	Unit
<b>Quiescent Current Specifications</b>						
I <sub>Q_ON_0mA</sub>	Quiescent current	I <sub>OUT</sub> = 0 mA		380	600	μA
I <sub>Q_ON_1mA</sub>	Quiescent current	I <sub>OUT</sub> = 1 mA		400	600	μA
I <sub>Q_ON_300mA</sub>	Quiescent current	I <sub>OUT</sub> = 300 mA		2.8	3.2	mA
R <sub>PD_OFF</sub>	Output pull down resistance	V <sub>OUT</sub> = 0.5 V LDO disabled			40	Ω

**Note 1** For programmable selections, refer to Section 4.4.1

**Note 2** The overall accuracy can be calculated by summing V<sub>OUT\_PP</sub> + V<sub>OUT\_TEMP</sub> + V<sub>OUT\_STATIC\_LD</sub> + V<sub>OUT\_STATIC\_LINE</sub>

**Note 3** For V<sub>IN</sub> - V<sub>OUT</sub> < 350 mV, PSRR will be degraded.

### 3.8 LDO\_HV Characteristics

In the LDO\_HV electrical characteristics table, unless otherwise specified, all specifications are guaranteed for VDD above 2.5 V and below 5 V, for V<sub>IN</sub> as defined in the table, and apply over the full operating temperature range, see Section 3.1.1.

**Table 10: LDO\_HV (LDO2, 3, 4, and 5) Electrical Characteristics**

Parameter	Description	Conditions	Min	Typ	Max	Unit
<b>External Electrical Conditions</b>						
V <sub>IN</sub>	Input voltage		1.7 <a href="#">Note 1</a>	3.8	5	V
C <sub>OUT</sub>	Output capacitance	Effective capacitance after derating	0.45	2.2	20	μF
I <sub>OUT_MAX</sub>	Maximum output current	V <sub>OUT</sub> drops 50 mV <a href="#">Note 2</a>	500			mA
<b>Programmable Conditions</b>						
V <sub>OUT</sub>	Selectable output voltage		1.2	3.3	3.75	V
V <sub>OUT_LSB</sub>	LSB of output voltage programming DAC (8-bit control)			10		mV
I <sub>OUT_STA RTUP_LIM</sub>	Start-up current limit, programmable in 12 mA steps <a href="#">Note 3</a>	At 90 % V <sub>OUT</sub>	30	150	606	mA
I <sub>OUT_FUN C_LIM</sub>	Functional current limit, programmable in 12 mA steps <a href="#">Note 3</a>		30	550	606	mA

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Parameter	Description	Conditions	Min	Typ	Max	Unit
<b>Electrical Performance</b>						
<b>Static Parameters</b>						
VOUT_PP	Part to part output voltage accuracy <a href="#">Note 4</a>	IOUT = 1 mA TA = 25 °C	-10 <a href="#">Note 5</a>		10 <a href="#">Note 5</a>	mV
VOUT_TEMP	Temperature dependence of VOUT <a href="#">Note 4</a>	IOUT = 1 mA <a href="#">Note 6</a>	-0.65		0.65	%
VOUT_STATIC_LINE	Static line regulation <a href="#">Note 4</a>	IOUT = 1 mA VIN = VOUT + VDROPOUT (Max) to VIN (Max)	-2		2	mV
VOUT_STATIC_LD	Static load regulation <a href="#">Note 4</a>	1 mA < IOUT < IOUT_MAX	-7		2	mV
VDROPOUT	Dropout voltage	@ VOUT = VOUT (VIN (Max)) - 10 mV IOUT = 250mA <a href="#">Note 7</a>			200 <a href="#">Note 8</a>	mV
RON	On resistance	@ VIN = VOUT (VIN (Max)) - 50 mV IOUT = IOUT_MAX <a href="#">Note 7</a>			800	mΩ
<b>Dynamic Parameters</b>						
VOUT_TRANSIENT_LINE	Line transient response	VIN = VOUT + VDROPOUT (Max) + 0.6 V to VIN = VOUT + VDROPOUT (Max) VOUT = VOUT (Typ) IOUT = IOUT_MAX tR = tF = 100 mV/μs		2	5 <a href="#">Note 9</a>	mV
VOUT_TRANSIENT_LD_1mA	Load transient response	VIN = VOUT + VDROPOUT (Max) VOUT = VOUT (Typ) IOUT = 1 mA to IOUT_MAX/2 tR = tF = 1 μs		28	37	mV
tON	Turn-on time	Time to 90 % of VOUT IOUT = 0 mA		0.2		ms
tOFF	Turn-off time	Time to 10 % of VOUT IOUT = 0 mA		0.2	10	ms

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Parameter	Description	Conditions	Min	Typ	Max	Unit
<b>AC Parameters</b>						
PSRR1kHz	Power supply rejection ratio	f = 1 kHz VIN = VOUT + 500 mV VOUT = VOUT (Typ) IOUT = IOUT_MAX/2 COUT = 4.7 μF		80		dB
PSRR100k Hz	Power supply rejection ratio	f = 100 kHz VIN = VOUT + 500 mV VOUT = VOUT (Typ) IOUT = IOUT_MAX/2 COUT = 4.7 μF		54		dB
PSRR1MHz	Power supply rejection ratio	f = 1 MHz VIN = VOUT + 500 mV VOUT = VOUT (Typ) IOUT = IOUT_MAX/2 COUT = 4.7 μF		47		dB
VN	Output noise	f = 10 Hz to 100 kHz IOUT = IOUT_MAX/2		152		μV
<b>Current Limit Accuracy</b>						
IOV_SINK	Current sink at over-voltage	VOV = VOUT + 100 mV <a href="#">Note 10</a>	10	77		mA
<b>Quiescent Current Specifications</b>						
IQ_ON_0mA	Quiescent current	IOUT = 0 mA <a href="#">Note 11</a>		13	19	μA
IQ_ON_1mA	Quiescent current	IOUT = 1 mA <a href="#">Note 11</a>		36	48	μA
IQ_ON_IMAX	Quiescent current	IOUT = IOUT_MAX <a href="#">Note 11</a>		2.25	3.5	mA
RPD_OFF	Output pull down resistance	VOUT = 0.5 V LDO disabled		30	100	Ω

- Note 1** IOUT\_MAX below 2.1 V is limited to 200 mA. For VIN above 2.1 V, IOUT\_MAX of 500 mA is guaranteed.
- Note 2** Guaranteed for VIN > 2.1 V, between 1.7 V and 2.1 V the IOUT\_MAX guaranteed is 200 mA.
- Note 3** Accuracy ±30 %
- Note 4** The overall accuracy can be calculated by summing VOUT\_PP + VOUT\_TEMP + VOUT\_STATIC\_LD + VOUT\_STATIC\_LINE.
- Note 5** +10 mV / -10 mV accuracy applies to factory-trimmed VOUT values targeted between 1.23 V to 3.72 V. VOUT targets from 1.20 V to 1.22 V can be trimmed to +24 mV / -10 mV accuracy. VOUT targets from 3.73 V to 3.75 V can be trimmed to +10 mV / -30 mV accuracy
- Note 6** Guaranteed for VIN ≥ 2.5 V.
- Note 7** Guaranteed for VIN > 1.8 V.

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## PMIC with High PSRR, Low Noise, Multi-Output LDOs and Integrated Load Switch

- Note 8** Dropout voltage is linear with the load current. If using a lower IOUT\_MAX than specified, the dropout can be calculated using 80 mV per 100 mA of load.
- Note 9** Guaranteed for VIN > 2.1 V. Otherwise, maximum line transient is 20 mV.
- Note 10** Guaranteed for VIN > 2.35 V.
- Note 11** Internal regulator current flowing to ground.



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### 3.9 LDO\_LV Characteristics

In the LDO\_LV electrical characteristics table, unless otherwise specified, all specifications are guaranteed for VDD above 2.5 V and below 4.9 V, for V<sub>IN</sub> as defined in the table, and apply over the full operating temperature range, see Section 3.1.1.

The characteristics for the LDOs in Load Switch Mode are given in Section 3.9.1.

**Table 11: LDO\_LV (LDO6) Electrical Characteristics**

Parameter	Description	Conditions	Min	Typ	Max	Unit
<b>External Electrical Conditions</b>						
V <sub>IN</sub>	Input supply (pass device + part of controller)		0.8	1.25	1.5	V
VDD_CTRL	Supply for controller (VDD)		2.3	3.8	5	V
C <sub>OUT</sub>	Output capacitance	Effective capacitance after derating	10 Note 1	20	80	μF
ESLC <sub>OUT</sub>	Output capacitor series inductance	f > 100 kHz			1	nH
I <sub>OUT_MAX</sub>	Maximum output current	V <sub>OUT</sub> drops 50 mV	1000			mA
<b>Programmable Conditions</b>						
V <sub>OUT</sub>	Selectable output voltage		0.5 Note 2	1.175	1.2	V
V <sub>OUT_LSB</sub>	LSB of output voltage programming DAC (8-bit control)			5		mV
I <sub>OUT_STA</sub> RTUP_LIM	Start-up current limit, programmable in 13 mA steps Note 3	At 90 % V <sub>OUT</sub>	15	150	1434	mA
I <sub>OUT_FUN</sub> C_LIM	Functional current limit, programmable in 13 mA steps Note 3		15	1250	1434	mA
<b>Electrical Performance</b>						
<b>Static Parameters</b>						
V <sub>OUT_PP</sub>	Part to part output voltage accuracy Note 4	I <sub>OUT</sub> = 1 mA T <sub>A</sub> = 25 °C	-5		5	mV
V <sub>OUT_TE</sub> MP	Temperature dependence of V <sub>OUT</sub> Note 4	I <sub>OUT</sub> = 1 mA Note 5	-0.65		0.65	%
V <sub>OUT_STA</sub> TIC_LINE	Static line regulation Note 4	I <sub>OUT</sub> = 1 mA V <sub>IN</sub> = V <sub>OUT</sub> + VDROPOUT (Max) to V <sub>IN</sub> (Max)	-2		2	mV

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Parameter	Description	Conditions	Min	Typ	Max	Unit
VOUT_STA TIC_LD	Static load regulation <a href="#">Note 4</a>	$1 \text{ mA} < \text{IOUT} < \text{IOUT\_MAX}$	-8		2	mV
VDROPOU T	Dropout voltage	@ $\text{VOUT} = \text{VOUT (VIN (Max))} - 10 \text{ mV}$ $\text{IOUT} = \text{IOUT\_MAX}$ <a href="#">Note 5</a>			100 <a href="#">Note 6</a>	mV
<b>Dynamic Parameters</b>						
VOUT_TR_ LINE	Line transient response	$\text{VIN} = \text{VOUT} + \text{VDROPOUT (Max)} + 100 \text{ mV}$ to $\text{VIN} = \text{VOUT} + \text{VDROPOUT (Max)}$ $\text{VOUT} = \text{VOUT (Typ)}$ $\text{IOUT} = \text{IOUT\_MAX}$ $tR = tF = 100 \text{ mV}/\mu\text{s}$		2	5	mV
VOUT_TR_ LD_1mA	Load transient response	$\text{VIN} = \text{VOUT} + \text{VDROPOUT (Max)}$ $\text{VOUT} = \text{VOUT (Typ)}$ $\text{IOUT} = 1 \text{ mA}$ to $\text{IOUT\_MAX}/2$ $tR = tF = 1 \mu\text{s}$		21	29	mV
tON	Turn-on time	Time to 90 % of VOUT $\text{IOUT} = 0 \text{ mA}$ $\text{COUT} = 20 \mu\text{F}$		0.15		ms
tOFF	Turn-off time	Time to 10 % of VOUT $\text{IOUT} = 0 \text{ mA}$ $\text{COUT} = 20 \mu\text{F}$		2	5 <a href="#">Note 7</a>	ms
<b>AC Parameters</b>						
PSRR1kHz	Power supply rejection ratio	$f = 1 \text{ kHz}$ $\text{VIN} = \text{VOUT} + \text{VDROPOUT (Max)} + 200 \text{ mV}$ $\text{VOUT} = \text{VOUT (Typ)}$ $\text{IOUT} = \text{IOUT\_MAX}/2$ $\text{COUT} = 20 \mu\text{F}$		76		dB
PSRR100k Hz	Power supply rejection ratio	$f = 100 \text{ kHz}$ $\text{VIN} = \text{VOUT} + \text{VDROPOUT (Max)} + 200 \text{ mV}$ $\text{VOUT} = \text{VOUT (Typ)}$ $\text{IOUT} = \text{IOUT\_MAX}/2$ $\text{COUT} = 20 \mu\text{F}$		54		dB
VN	Output noise	$f = 10 \text{ Hz}$ to $100 \text{ kHz}$ $\text{IOUT} = \text{IOUT\_MAX}/2$		100		$\mu\text{V}$

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Parameter	Description	Conditions	Min	Typ	Max	Unit
<b>Current Limit Accuracy</b>						
IOV_SINK	Current sink at over-voltage	VOV = VOUT + 100 mV	10			mA
<b>Quiescent Current Specifications</b>						
IQ_ON_0mA	Quiescent current, no load	IOUT = 0 mA Note 8		8	15	μA
IQ_ON_1mA	Quiescent current, low load	IOUT = 1 mA Note 8		10	16	μA
IQ_ON_IMAX	Quiescent current, IOUT_MAX	IOUT = IOUT_MAX Note 8		0.35	1.5	mA
RPD_OFF	Output pull down resistance	VOUT = 0.5 V LDO disabled		35	100	Ω

**Note 1** For currents less than 400 mA, a minimum of 1.2 μF (after derating) can be used.

**Note 2** Output is capable down to 0.4 V at reduced accuracy. Please contact Renesas for more information

**Note 3** Accuracy ±30 %

**Note 4** The overall accuracy can be calculated by summing VOUT\_PP + VOUT\_TEMP + VOUT\_STATIC\_LD + VOUT\_STATIC\_LINE.

**Note 5** Spec guaranteed for VDD\_CTRL ≥ 2.8 V.

**Note 6** Dropout voltage is linear with the load current. If using a lower IOUT\_MAX than specified, the dropout can be calculated using 10 mV per 100 mA of load.

**Note 7** Max tOFF of 20 ms achieved for COUT = 80 μF.

**Note 8** Internal regulator current flowing to ground.

### 3.9.1 Load Switch Mode Characteristics

**Table 12: Load Switch Mode Electrical Characteristics**

Parameter	Description	Conditions	Min	Typ	Max	Unit
<b>External Electrical Conditions</b>						
VIN	Input voltage		0.5 Note 1 Note 2		1.25	V
IOUT_MAX	Maximum output current		1000			mA
<b>Programmable Conditions</b>						
SR	Slew rate, programmable to (4, 6, 8, 10) mV/μs		4		10	mV/μs
ILIM	Current limit, programmable from 15 mA to 1.434 A in 13 mA steps Note 3		15		1434	mA

## PMIC with High PSRR, Low Noise, Multi-Output LDOs and Integrated Load Switch

Parameter	Description	Conditions	Min	Typ	Max	Unit
<b>Electrical Performance</b>						
RON	On resistance			40		mΩ
SRACC	Slew rate accuracy		-35		35	%
ILIM_ACC	Current limit accuracy		-35		35	%
IQ_OFF	Quiescent current in off mode	TA = 25 °C			2	μA

**Note 1** Input is capable down to 0.4 V. Please contact Renesas for more information

**Note 2** Register bit SEL\_BYP\_VGATE must be set to 0 for VIN between 0.5 V and 0.8 V, and is recommended to be set to 1 for VIN between 0.8 V and 1.25 V.

**Note 3** Current limit is guaranteed for VIN > 0.7 V. Below 0.7 V, a functional current limit is not guaranteed.

### 3.10 VREF, IREF, Temperature Supervision Characteristics

**Table 13: VREF, IREF, Temperature Supervision Electrical Characteristics**

Parameter	Description	Conditions	Min	Typ	Max	Unit
<b>Programmable Conditions</b>						
VREF	Reference voltage	Internal VREF		1.2		V
TWARN	Warning temperature threshold, programmable to (90, 100, 110, 120) °C		90		120	°C
TWARN_HYS	Warning temperature hysteresis, programmable to (0, 14) °C			14		°C
<b>Electrical Performance</b>						
VREF_ACC	Reference voltage accuracy	Internal VREF	-1		1	%
TOT	Thermal shutdown over-temperature		125	140	155	°C
TWARN_ACC	Warning temperature threshold accuracy		-5		5	°C

## PMIC with High PSRR, Low Noise, Multi-Output LDOs and Integrated Load Switch

### 3.11 Internal Oscillator Characteristics

Table 14: Internal Oscillator Electrical Characteristics

Parameter	Description	Conditions	Min	Typ	Max	Unit
<b>Electrical Performance</b>						
fCLK	Internal clock frequency		7.2	8	8.8	MHz

### 3.12 UVLO Characteristics

Table 15: UVLO Electrical Characteristics

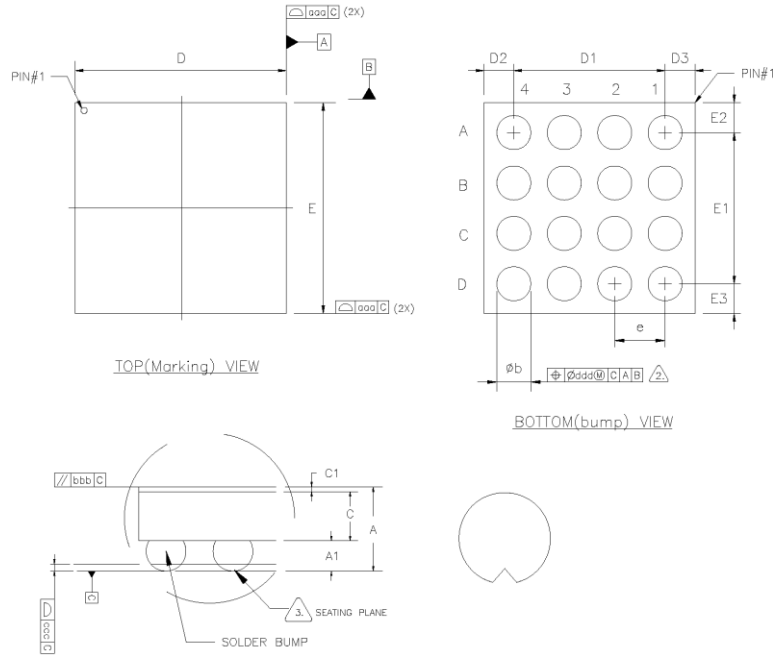
Parameter	Description	Conditions	Min	Typ	Max	Unit
<b>Programmable Conditions</b>						
VDD_UVL O_LWR	Under-voltage lower threshold (falling edge) <a href="#">Note 1</a>		2.215		2.658	V
VDD_UVL O_UPPER	Under-voltage upper threshold (rising edge)			VDD_UVLO_LWR + 3 %		V
<b>Electrical Performance</b>						
VDD_POR _UPPER	Deep discharge lockout upper threshold			2.1	2.2	V
VDD_POR _LWR	Deep discharge lockout lower threshold			1.9		V
VDD_UVL O_STAT_A CC	Under-voltage lower threshold static accuracy with flip gate bandgap reference		-1.5		1.5	%

**Note 1** This voltage is programmed from OTP.

PMIC with High PSRR, Low Noise, Multi-Output LDOs and Integrated Load Switch

4 Package Information

4.1 Package Outlines



Symbol	Dimensions in mm			Dimensions in inch		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.4350	0.4650	0.4950	0.0171	0.0183	0.0195
A1	0.1750	0.1900	0.2050	0.0069	0.0075	0.0081
c	0.2250	0.2500	0.2750	0.0089	0.0098	0.0108
c1	0.0220	0.0250	0.0280	0.0009	0.0010	0.0011
D	1.6500	1.6750	1.7000	0.0650	0.0659	0.0669
E	1.6500	1.6750	1.7000	0.0650	0.0659	0.0669
b	0.2400	0.2700	0.3000	0.0094	0.0106	0.0118
D1	---	1.2000	---	---	0.0472	---
D2	---	0.2375	---	---	0.0094	---
D3	---	0.2375	---	---	0.0094	---
E1	---	1.2000	---	---	0.0472	---
E2	---	0.2375	---	---	0.0094	---
E3	---	0.2375	---	---	0.0094	---
e	---	0.4000	---	---	0.0157	---
aaa	---	0.0250	---	---	0.0010	---
bbb	---	0.0600	---	---	0.0024	---
ccc	---	0.0300	---	---	0.0012	---
ddd	---	0.0150	---	---	0.0006	---

NOTE:

1. CONTROLLING DIMENSION : MILLIMETER.

2. DIMENSION IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER, PARALLEL TO PRIMARY DATUM C

3. PRIMARY DATUM C AND SEATING PLANE ARE DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS

Figure 3: Package Outline Drawing

PMIC with High PSRR, Low Noise, Multi-Output LDOs and Integrated Load Switch

4.2 PCB Landing Pattern

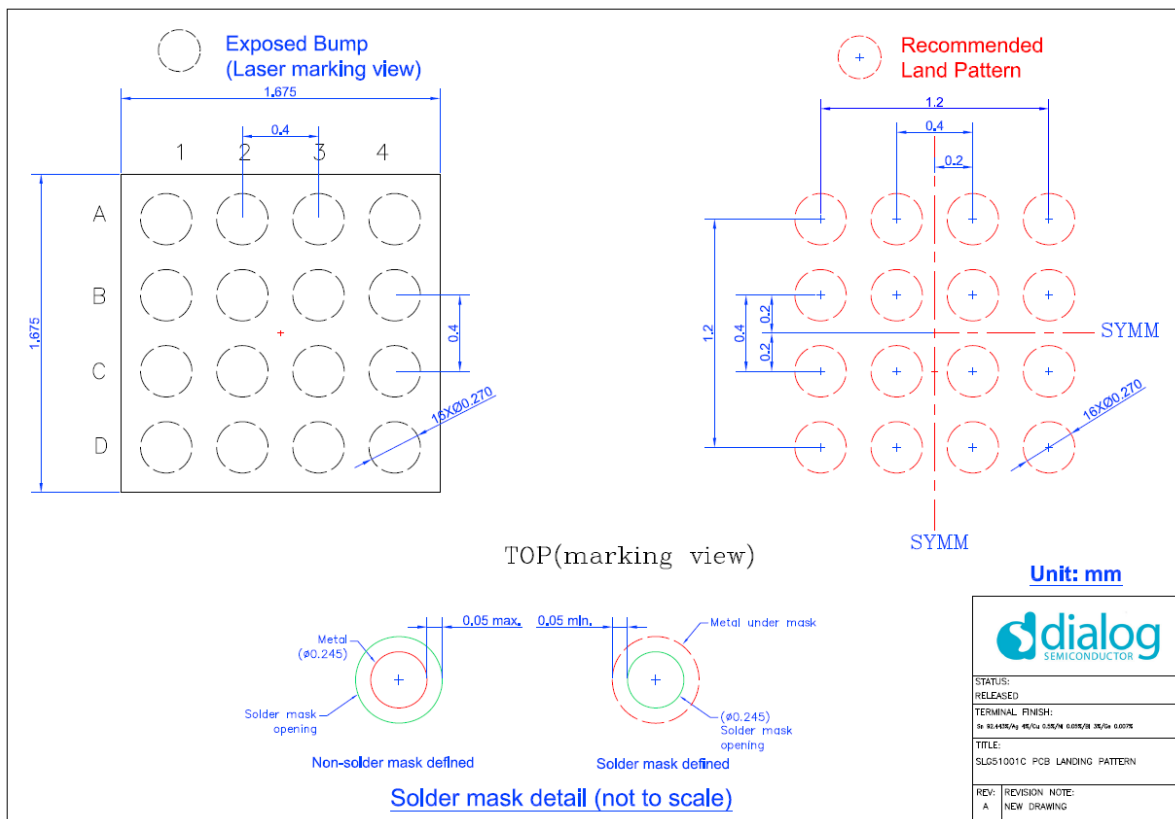


Figure 4: PCB Landing Pattern

4.3 Moisture Sensitivity Level

The Moisture Sensitivity Level (MSL) is an indicator for the maximum allowable time period (floor lifetime) in which a moisture sensitive plastic device, once removed from the dry bag, can be exposed to an environment with a specified maximum temperature and a maximum relative humidity before the solder reflow process. The MSL classification is defined in

Table 16.

For detailed information on MSL levels refer to the IPC/JEDEC standard J-STD-020, which can be downloaded from <http://www.jedec.org>.

MSL rating does not apply to this device as it is not plastic encapsulated.

Table 16: MSL Classification

MSL Level	Floor Lifetime	Conditions
MSL 4	72 hours	30 °C / 60 % RH
MSL 3	168 hours	30 °C / 60 % RH
MSL 2A	4 weeks	30 °C / 60 % RH
MSL 2	1 year	30 °C / 60 % RH
MSL 1	Unlimited	30 °C / 85 % RH

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## PMIC with High PSRR, Low Noise, Multi-Output LDOs and Integrated Load Switch

### 4.4 WLCSP Handling

Manual handling of WLCSP packages should be reduced to the absolute minimum. In cases where it is still necessary, a vacuum pick-up tool should be used. In extreme cases plastic tweezers could be used, but metal tweezers are not acceptable, since contact may easily damage the silicon chip.

Removal of a WLCSP package will cause damage to the solder balls. Therefore a removed sample cannot be reused.

WLCSP packages are sensitive to visible and infrared light. Precautions should be taken to properly shield the chip in the final product.

### 4.5 Soldering Information

Refer to the IPC/JEDEC standard J-STD-020 for relevant soldering information. This document can be downloaded from <http://www.jedec.org>.



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**PMIC with High PSRR, Low Noise, Multi-Output LDOs  
and Integrated Load Switch**

## 5 Ordering Information

The ordering number consists of the part number followed by a suffix indicating the packing method. For details and availability, please consult Renesas [customer support portal](#) or your local sales representative.

**Table 17: Ordering Information**

Part Number	Package	Size (mm)	Shipment Form	Pack Quantity
SLG51001CTR	WLCSP-16	1.675 x 1.675	T & R	3,000