Data Sheet

RAA730101

R02DS0014EJ0200
Rev.2.00
Feb 27, 2015

16-bit ΔΣ A/D converter IC with programmable gain instrumentation amplifier

Overview

The RAA730101 is a 16-bit ΔΣ A/D converter IC with a programmable gain instrumentation amplifier ideal for differential output sensors used for measuring flow and pressure. The RAA730101 incorporates a temperature sensor, a power supply for external sensor, and an internal reference voltage generator. Using Serial Peripheral Interface (SPI) communication or Universal Asynchronous Receiver Transmitter (UART) communication, the RAA730101 controls system configurations for each function block from an external device and outputs measured data to the external device. The RAA730101 also incorporates flash memory for storing system configurations for each function block. The RAA730101 uses a 36-pin FBGA package, which enables a more compact set design for measuring flow and pressure.

Features

- 16-bit ΔΣ A/D converter
- Programmable gain instrumentation amplifier (capable of gain adjustment from x1 to x32 and adjustment of offset voltage)
- Four analog input channels (differential input mode or single-ended input mode can be specified for each input channel)
- Temperature sensor (internally connected to 16-bit ΔΣ A/D converter)
- Power supply for external sensor (output voltage: 1.2 to 2.2 V)
- Internal system clock (OSC) oscillator (clock frequency: 20 MHz (Typ.))
- Power-on reset (POR) circuit
- Serial interface (SPI or UART communication is selectable)
- 256-byte flash memory for storing system configuration data
- Operating voltage range: 2.7 V $\leq V_{DD} \leq$ 5.5 V
- Operating temperature range:
  - 125°C models: −40°C $\leq T_A \leq$ 125°C (during normal operation)
    105°C models: −40°C $\leq T_A \leq$ 105°C (during normal operation)
  - 125°C and 105°C models: 10°C $\leq T_A \leq$ 85°C (during flash memory programming)
- Package: 36-pin plastic FBGA (4 mm × 4 mm, 0.5-mm pitch)

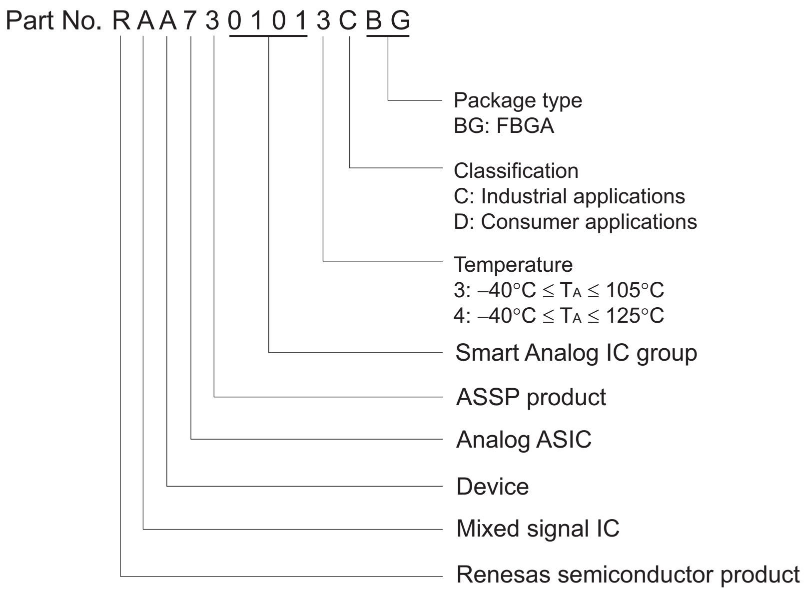
Caution Flash memory programming refers to erasing or writing of data in the flash memory.

Applications

- Industrial equipment for measuring items such as pressure, flow, and temperature
- Healthcare equipment for measuring items such as blood pressure and weight

Ordering Information

Pin count	Package	Part Number
36 pins	36-pin plastic FBGA (4 × 4)	RAA7301013CBG, RAA7301014CBG



How to Read This Manual

It is assumed that the readers of this manual have general knowledge of electrical engineering, logic circuits, and microcontrollers.

- To gain a general understanding of functions
  → Read this manual in the order of the Contents.
- Revised points
  → The mark "<R>" shows major revised points.
  The revised points can be easily searched by copying an "<R>" in the PDF file and specifying it in the "Find what:" field.

Conventions

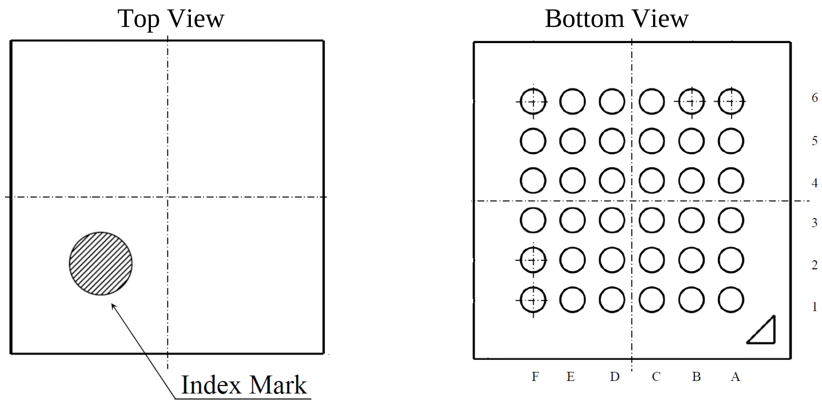
Data significance:	Higher digits on the left and lower digits on the right
Active low representations:	$\overline{\times\times\times}$ (overscore over pin and signal name)
Note:	Footnote for item marked with Note in the text
Caution:	Information requiring particular attention
Remark:	Supplementary information
Numerical representations:	Binary … ×××× or ××××B
	Decimal … ××××
	Hexadecimal … ××××H

Contents

1. Pin Connection

1.1 Pin layout (Top View)

- 4 × 4 mm / 36-pin TFBGA (0.50 mm pitch)



6	AGND1	SBIAS	AIN2N	AIN2P	AIN1P	AGND6
5	VREF	AGND2	AGND3	AGND5	AIN3N	AIN1N
4	CREG	AV_{DD}	DGND3	AGND4	AIN4N	AIN3P
3	AREG	IOV_{DD1}	SMODE	DGND4	ADV_{DD}	AIN4P
2	RV_{DD}	IOV_{DD2}	INT	TX_B	MCLK	DV_{DD}
1	DGND1	MOSI_RX	MISO_TX	SCLK	CS_B	DGND2
	A	B	C	D	E	F

Cautions 1. Make the potential of AGND (AGND1 to AGND6) and DGND (DGND1 to DGND4) the same.

2. Make the potential of ADV_{DD} and DV_{DD} the same.

3. Connect IOV_{DD1} and IOV_{DD2} directly.

4. Make RV_{DD} greater than or equal to IOV_{DD}.

5. Connect RV_{DD} to AGND via a capacitor (0.47 μF recommended).

6. Connect AREG to AGND via a capacitor (0.47 μF recommended).

7. Connect CREG to AGND via a capacitor (0.22 μF recommended).

8. Connect SBIAS to AGND via a capacitor (0.22 μF recommended).

9. Connect VREF to AGND via a capacitor (0.1 μF recommended).

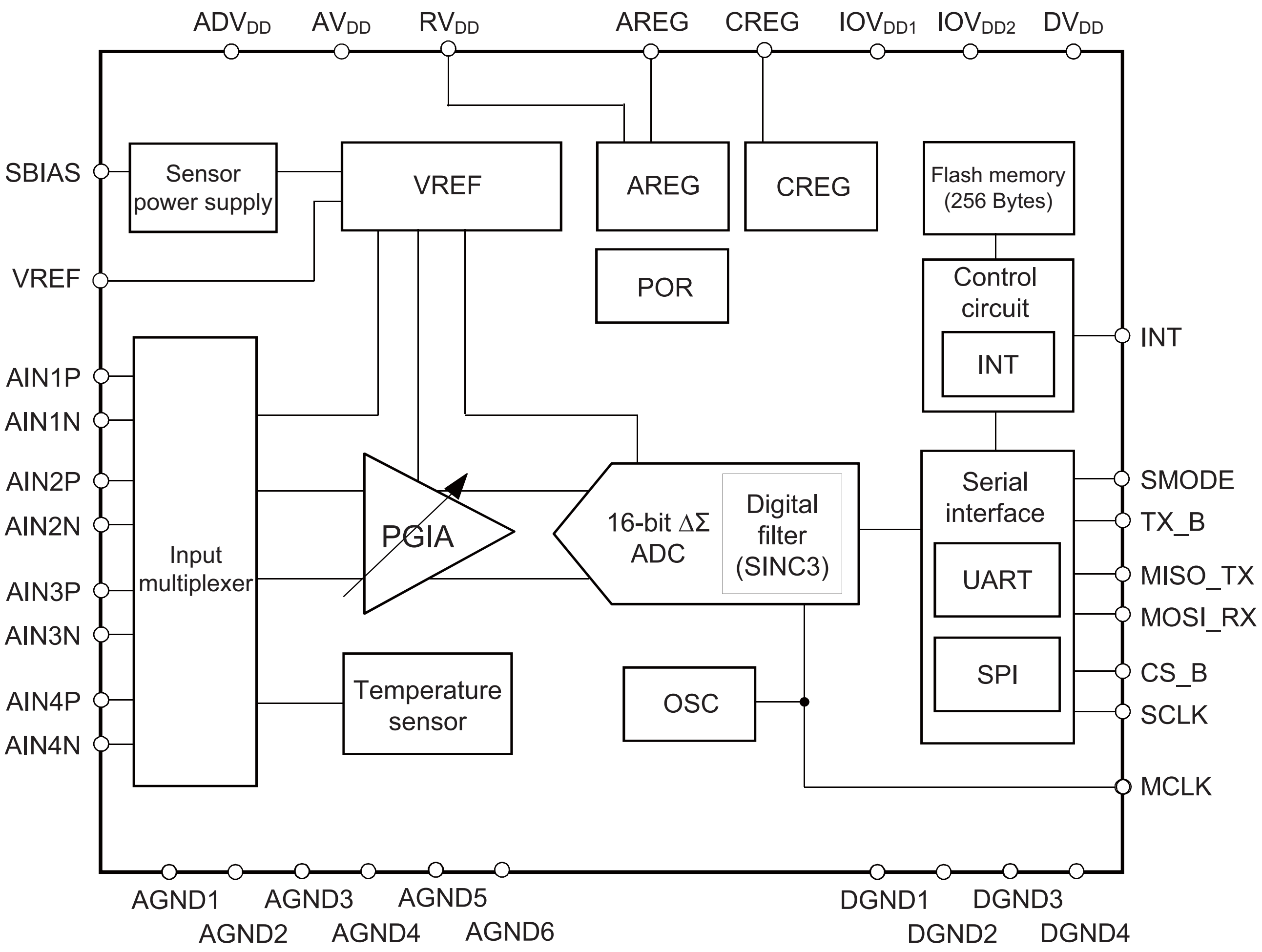
10. Connect ADV_{DD} to AGND via a capacitor (0.1 μF recommended).

Remarks 1. In this document, AGND1, AGND2, AGND3, AGND4, AGND5, and AGND6 are referred to as *AGND*.

2. In this document, DGND1, DGND2, DGND3, and DGND4 are referred to as *DGND*.

3. In this document, IOV_{DD1} and IOV_{DD2} are referred to as *IOV_{DD}*.

1.2 Block diagram



1.3 Pin functions

Table 1.1 Pin functions

Pin No.	Pin name	Analog/ digital	I/O	I/O level	Description
A1	DGND1	–	–	–	Digital circuit ground pin 1
A2	RV_{DD}	–	–	–	Regulator power supply
A3	AREG	A	Output	RV_{DD}	3.0 V LDO output pin for supplying AV_{DD}
A4	CREG	A	Output	AV_{DD}	2.1 V LDO output pin for supplying ADV_{DD}
A5	VREF	A	Output	AV_{DD}	VREF voltage monitor pin
A6	AGND1	–	–	–	Analog circuit ground pin 1
B1	MOSI_RX	D	Input	IOV_{DD}	SPI serial data input/UART data reception pin
B2	IOV_{DD2}	–	–	–	I/O circuit power supply pin 2
B3	IOV_{DD1}	–	–	–	I/O circuit power supply pin 1
B4	AV_{DD}	–	–	–	Analog circuit power supply pin
B5	AGND2	–	–	–	Analog circuit ground pin 2
B6	SBIAS	A	Output	AV_{DD}	Externally-connected sensor power supply pin
C1	MISO_TX	D	Output	IOV_{DD}	SPI serial data input/UART data transmission pin
C2	INT	D	Output	IOV_{DD}	Interrupt signal output pin
C3	SMODE	D	Input	IOV_{DD}	Serial interface mode select pin
C4	DGND3	–	–	–	Digital circuit ground pin 3
C5	AGND3	–	–	–	Analog circuit ground pin 3
C6	AIN2N	A	Input	AV_{DD}	Input multiplexer 2 (programmable gain instrumentation amplifier input pin 2 (negative))
D1	SCLK	D	Input	IOV_{DD}	SPI serial clock input pin
D2	TX_B	D	Output	IOV_{DD}	UART data transmission pin
D3	DGND4	–	–	–	Digital circuit ground pin 4
D4	AGND4	–	–	–	Analog circuit ground pin 4
D5	AGND5	–	–	–	Analog circuit ground pin 5
D6	AIN2P	A	Input	AV_{DD}	Input multiplexer 2 (programmable gain instrumentation amplifier input pin 2 (positive))
E1	CS_B	D	Input	IOV_{DD}	SPI chip select/UART reception mode select pin
E2	MCLK	D	I/O	IOV_{DD}	Oscillator clock monitor pin (1 MHz)/external clock input pin (4 MHz)
E3	ADV_{DD}	–	–	–	A/D converter power supply
E4	AIN4N	A	Input	AV_{DD}	Input multiplexer 4 (programmable gain instrumentation amplifier input pin 4 (negative))
E5	AIN3N	A	Input	AV_{DD}	Input multiplexer 3 (programmable gain instrumentation amplifier input pin 3 (negative))
E6	AIN1P	A	Input	AV_{DD}	Input multiplexer 1 (programmable gain instrumentation amplifier input pin 1 (positive))
F1	DGND2	–	–	–	Digital circuit ground pin 2
F2	DV_{DD}	–	–	–	Digital circuit power supply pin
F3	AIN4P	A	Input	AV_{DD}	Input multiplexer 4 (programmable gain instrumentation amplifier input pin 4 (positive))
F4	AIN3P	A	Input	AV_{DD}	Input multiplexer 3 (programmable gain instrumentation amplifier input pin 3 (positive))
F5	AIN1N	A	Input	AV_{DD}	Input multiplexer 1 (programmable gain instrumentation amplifier input pin 1 (negative))
F6	AGND6	–	–	–	Analog circuit ground pin 6

Remark The digital I/O pins are compatible with the CMOS interface and Schmitt-triggered input.

1.4 Connection of unused pins

Table 1.2 shows the connection of unused pins.

Table 1.2 Connection of unused pins

Pin name	Analog/ digital	I/O	I/O level	Description
AREG	A	Output	RV_{DD}	Connect to AGND via a capacitor (0.47 μF recommended). (When AREGPD = 1, connect it to RV_{DD}.)
CREG	A	Output	AV_{DD}	Connect to AGND via a capacitor (0.22 μF recommended).
VREF	A	Output	AV_{DD}	Connect to AGND via a capacitor (0.1 μF recommended).
SBIAS	A	Output	AV_{DD}	Connect to AGND via a capacitor (0.22 μF recommended).
AIN1P	A	Input	AV_{DD}	Directly connect to AGND.
AIN1N	A	Input	AV_{DD}	
AIN2P	A	Input	AV_{DD}	
AIN2N	A	Input	AV_{DD}	
AIN3P	A	Input	AV_{DD}	
AIN3N	A	Input	AV_{DD}	
AIN4P	A	Input	AV_{DD}	
AIN4N	A	Input	AV_{DD}	
CS_B Note	D	Input	IOV_{DD}	Directly connect to IOV_{DD} or DGND.
SCLK	D	Input	IOV_{DD}	Directly connect to DGND.
MOSI_RX	D	Input	IOV_{DD}	Directly connect to IOV_{DD}
MISO_TX	D	Output	IOV_{DD}	Leave this pin open.
TX_B	D	Output	IOV_{DD}	Leave this pin open.
SMODE	D	Input	IOV_{DD}	Directly connect to IOV_{DD} or DGND.
INT	D	Output	IOV_{DD}	Leave this pin open.
MCLK	D	I/O	IOV_{DD}	Leave this pin open.

Note In SPI communication, the CS_B pin is surely used. In UART communication, the CS_B pin is used only when PWM direct input function is used. For details about PWM direct input function, see ***6. 7 PWM direct input***.

1.5 I/O circuits

Figure 1.1 I/O circuit type (1/2)

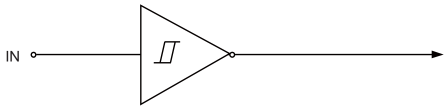
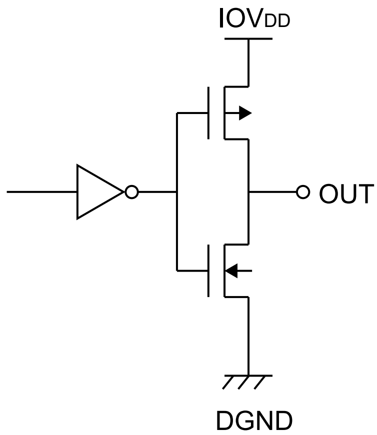
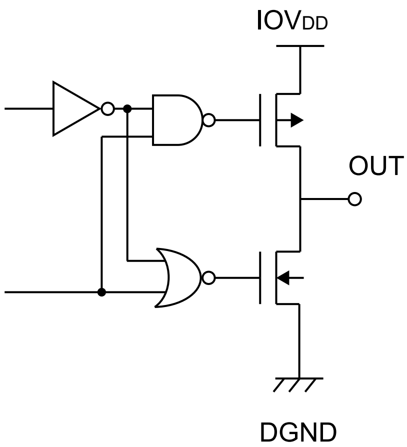
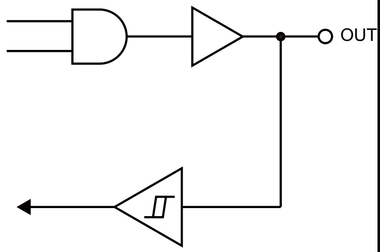
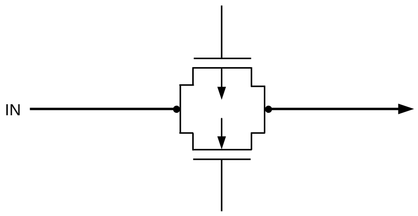
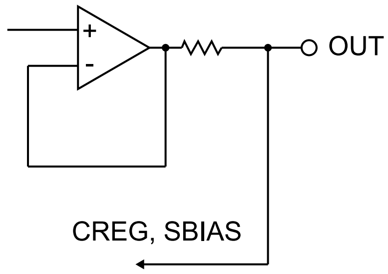
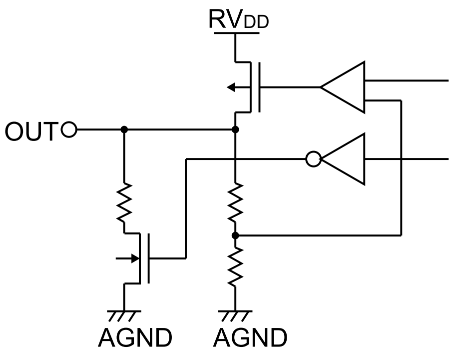
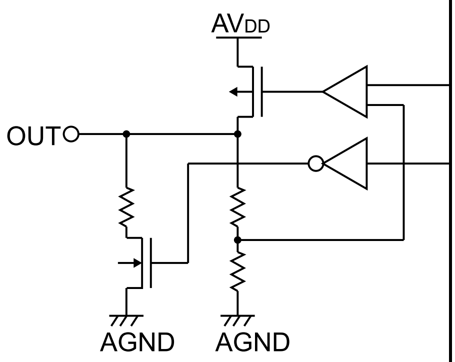
Pin name	Equivalent circuit	Pin name	Equivalent circuit
CS_B SCLK MOSI_RX SMODE	 Schmitt-triggered input with hysteresis characteristics	INT	
MISO_TX TX_B		MCLK	 Schmitt-triggered input with hysteresis characteristics

Figure 1.1 I/O circuit type (2/2)

Pin name	Equivalent circuit	Pin name	Equivalent circuit
AIN1P AIN1N AIN2P AIN2N AIN3P AIN3N AIN4P AIN4N		VREF	
AREG		CREG SBIAS	

2. Input Multiplexer

2.1 Overview

The input multiplexer has five analog input channels, four of which (input multiplexers 1 to 4) can be used to input an external signal, and the remaining one of which (input multiplexer 5) is connected to the internal temperature sensor. For input multiplexers 1 to 4, differential input mode or single-ended input mode can be selected for each channel. If single-ended input mode is selected, an internal bias voltage (VBIAS) is connected to the channel.

An internal bias voltage (VBIAS) is also connected to the channel to which the output from the internal temperature sensor is connected. For details about the internal bias voltage, see ***8. Power Supply Circuit***.

2.2 Block diagram

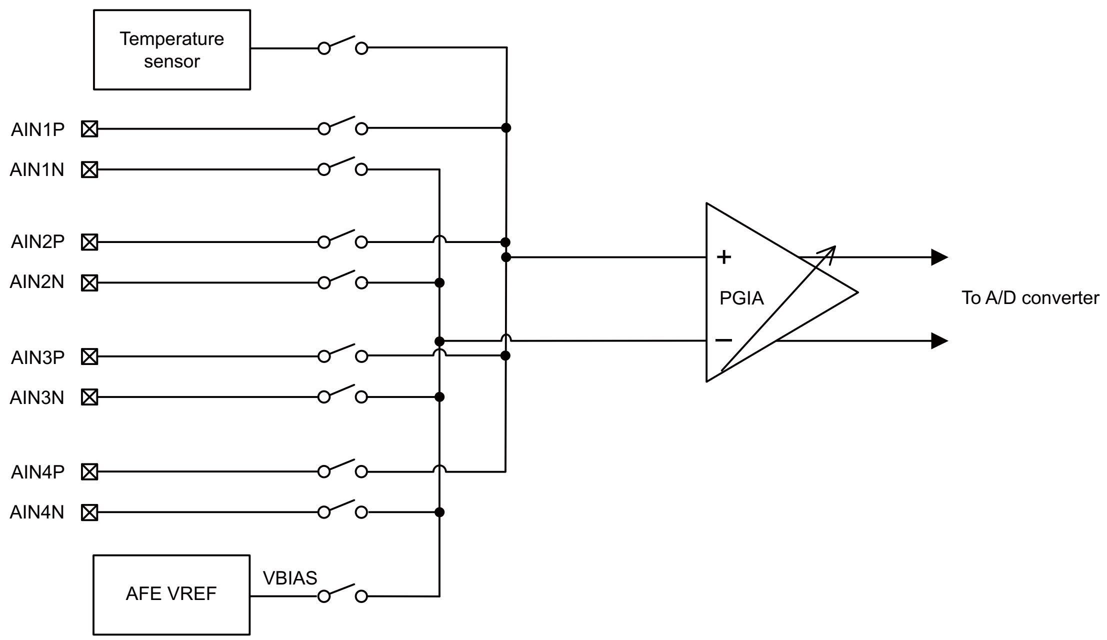


Figure 2.1 Block diagram of input multiplexer

2.3 Registers controlling input multiplexers

The following kind of register is used to control input multiplexers.

- Input multiplexer x (x = 1 to 4) A/D conversion setting register 2 (CHxCNT2)

(1) Input multiplexer x (x = 1 to 4) A/D conversion setting register 2 (CHxCNT2)

These registers are used to specify differential input mode or single-ended input mode for each input multiplexer. After reset, these registers are initialized to 10H.

Address: 11H After reset: 10H R/W

	7	6	5	4	3	2	1	0
CH1CNT2	AINSEL1	0	0	AIN1OFT4	AIN1OFT3	AIN1OFT2	AIN1OFT1	AIN1OFT0

AINSEL1	Control of input multiplexer 1
0	Differential input
1	Single-ended input

Caution Bits 6 and 5 are read-only. (When these bits are read, 0 is always returned.)

Address: 14H After reset: 10H R/W

	7	6	5	4	3	2	1	0
CH2CNT2	AINSEL2	0	0	AIN2OFT4	AIN2OFT3	AIN2OFT2	AIN2OFT1	AIN2OFT0

AINSEL2	Control of input multiplexer 2
0	Differential input
1	Single-ended input

Caution Bits 6 and 5 are read-only. (When these bits are read, 0 is always returned.)

Address: 17H After reset: 10H R/W

	7	6	5	4	3	2	1	0
CH3CNT2	AINSEL3	0	0	AIN3OFT4	AIN3OFT3	AIN3OFT2	AIN3OFT1	AIN3OFT0

AINSEL3	Control of input multiplexer 3
0	Differential input
1	Single-ended input

Caution Bits 6 and 5 are read-only. (When these bits are read, 0 is always returned.)

Address: 1AH After reset: 10H R/W

	7	6	5	4	3	2	1	0
CH4CNT2	AINSEL4	0	0	AIN4OFT4	AIN4OFT3	AIN4OFT2	AIN4OFT1	AIN4OFT0

AINSEL4	Control of input multiplexer 4
0	Differential input
1	Single-ended input

Caution Bits 6 and 5 are read-only. (When these bits are read, 0 is always returned.)

3. Programmable Gain Instrumentation Amplifier (PGIA)

3.1 Overview

The programmable gain instrumentation amplifier (PGIA) features low offset voltage, low 1/f noise, and high impedance. The PGIA operates in differential input mode, single-ended input mode, or internal temperature sensor input mode, according to the setting of the input multiplexer used.

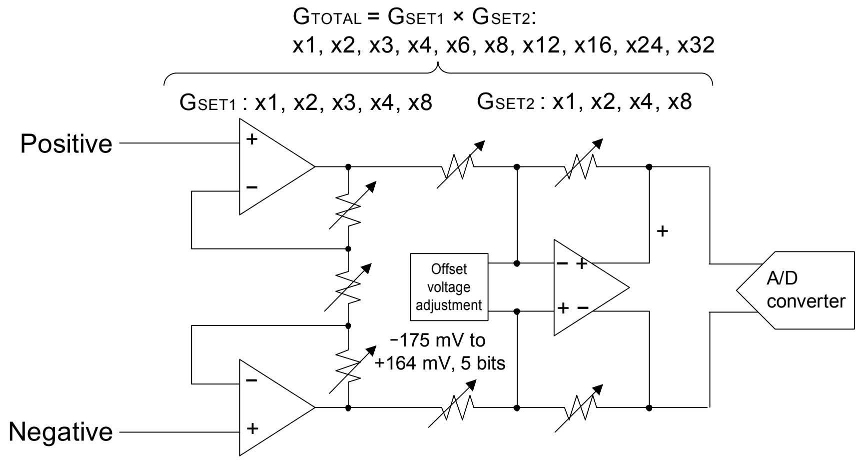
In differential input mode, a gain from x1 to x32 (G_{TOTAL}) can be specified by combining the gain in the preamplifier (G_{SET1}) and the gain in the post amplifier (G_{SET2}) in the instrumentation amplifier. In single-ended input mode, it is recommended that you set to 1x gain. The gain cannot be changed in internal temperature sensor input mode. G_{SET1} and G_{SET2} are internally fixed to 1 (G_{TOTAL} = 1).

A D/A converter for adjusting the offset voltage is connected to the post amplifier. In differential input mode and single-ended input mode, the offset voltage can be adjusted (from –175 mV to +164 mV, in 32 steps (5 bits)) by using this D/A converter. In internal temperature sensor input mode, the offset voltage cannot be adjusted. The D/A converter output is internally fixed to 0 mV.

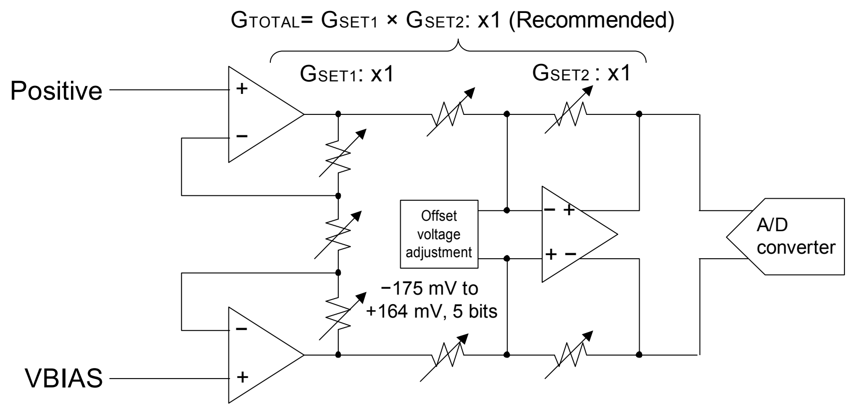
For details about controlling the programmable gain instrumentation amplifier (PGIA), see ***4.4 Operation of A/D converter (AUTOSCAN)***.

3.2 Block diagram

Differential input mode



Single-ended input mode



Internal temperature sensor input mode

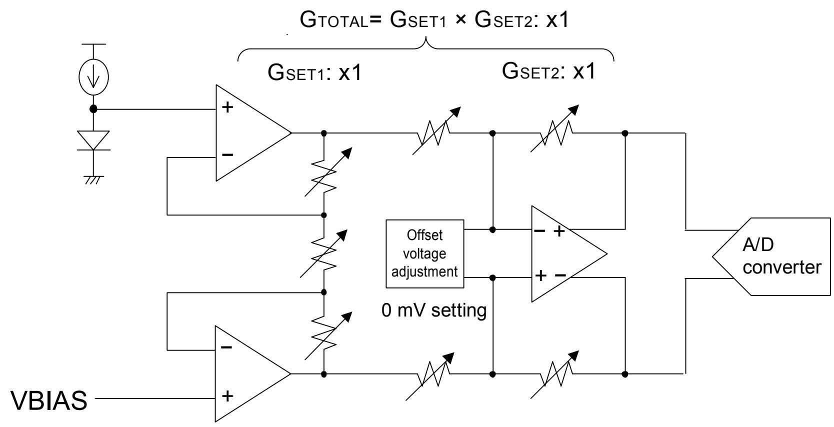


Figure 3.1 Block diagram of programmable gain instrumentation amplifier (PGIA)

3.3 Input voltage range

This section describes the range of voltage input to the programmable gain instrumentation amplifier (PGIA). Figure 3.2 shows the input voltage range in differential input mode, single-ended input mode, and internal temperature sensor input mode.

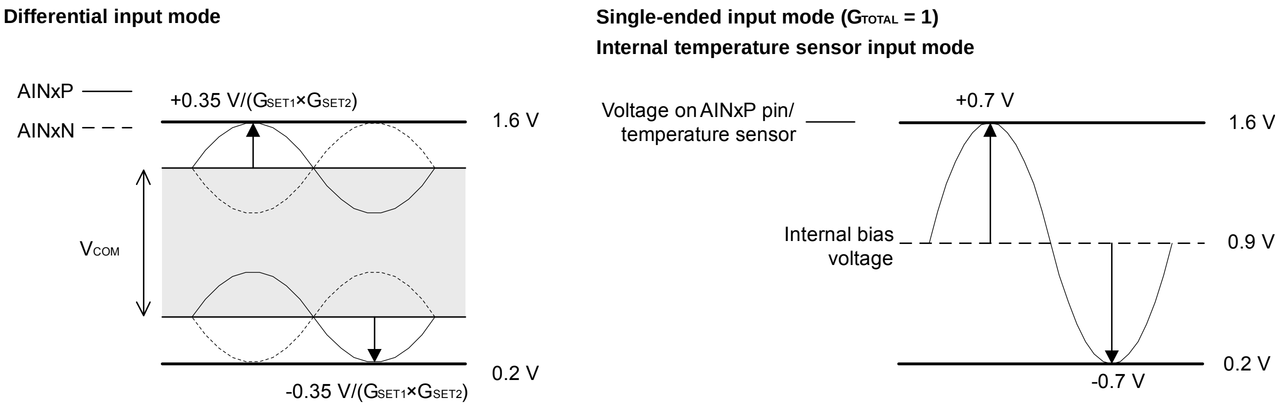


Figure 3.2 Input voltage range

3.3.1 Input voltage range in differential input mode

V_{SIG} indicates the input-referred amplitude of the differential voltage input signal, V_{COM} indicates the input-referred common mode input voltage, and d_{OFR} indicates the input-referred D/A converter output voltage for adjusting the offset voltage. The voltage input to an amplifier should be 0.2 to 1.6 V. Therefore, the signal that passes through the preamplifier in the instrumentation amplifier and is then input to the post amplifier must satisfy the conditions in Formula 3.1.

The signal that passes through the preamplifier in the instrumentation amplifier and is then output from the post amplifier must satisfy the conditions in Formula 3.2.

$$0.2\ \text{V} + \frac{|V_{SIG}| \times G_{SET1}}{2} \leqq V_{COM} \leqq 1.6\ \text{V} - \frac{|V_{SIG}| \times G_{SET1}}{2}$$ ... Formula 3.1

$$-0.7\ \text{V} \leqq (V_{SIG} + d_{OFR}) \times G_{TOTAL} \leqq 0.7\ \text{V}$$ ... Formula 3.2

When d_{OFR} = 0 mV, the input signal is equivalent to the full-scale differential input voltage. V_{COM} can be expressed by using Formula 3.3, where $V_{SIG} = V_{ID}$ (full-scale differential input voltage).

$$0.2\ \text{V} + \frac{|V_{ID}| \times G_{SET1}}{2} \leqq V_{COM} \leqq 1.6\ \text{V} - \frac{|V_{ID}| \times G_{SET1}}{2}$$ ... Formula 3.3

Figure 3.3 shows the transition of the differential input voltage level in each phase in the programmable gain instrumentation amplifier (PGIA).

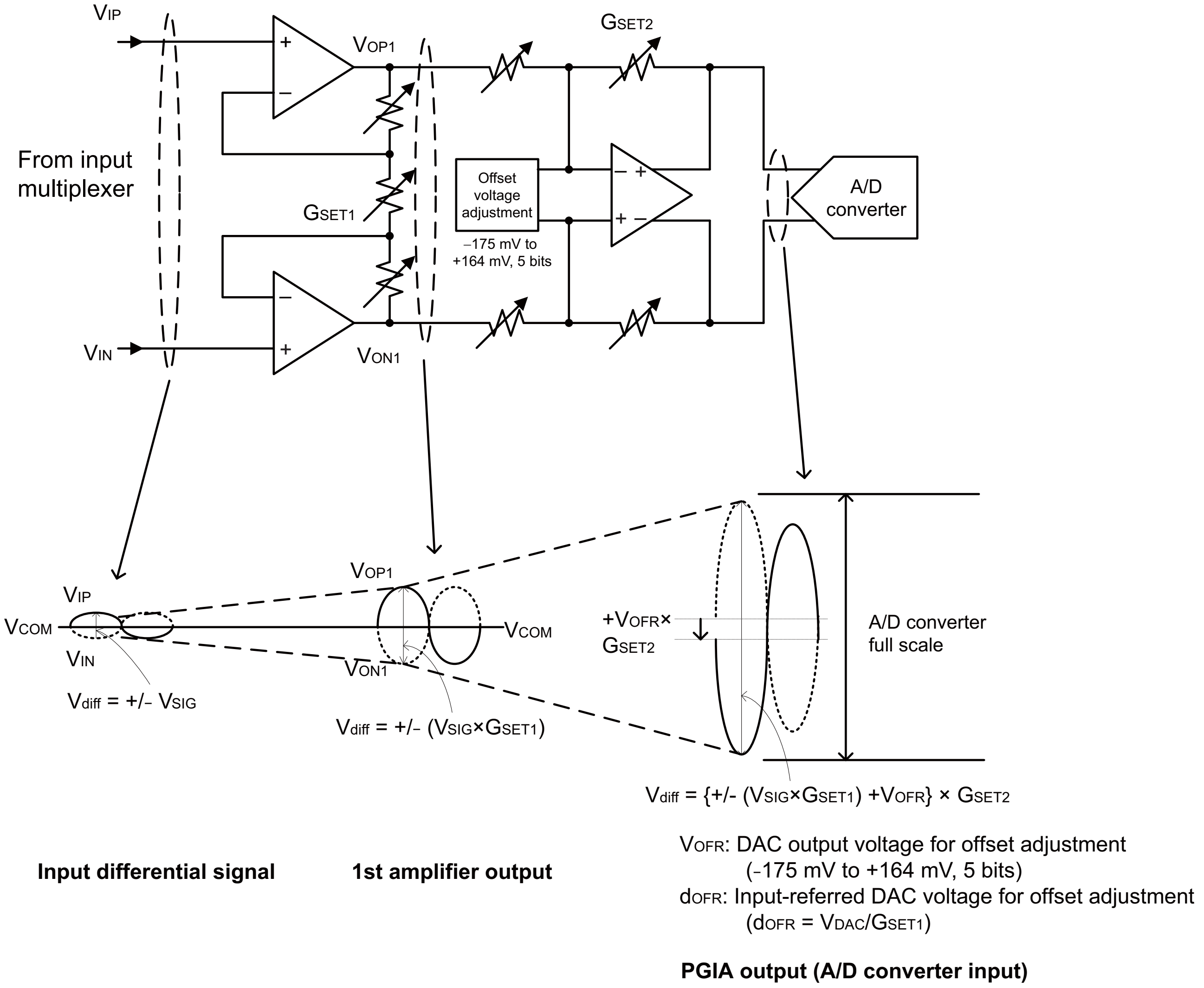


Figure 3.3 Transition of the differential input voltage level in the PGIA

3.3.2 Input voltage range in single-ended input mode and internal temperature sensor input mode

In single-ended input mode and internal temperature sensor input mode, the internal bias voltage (VBIAS = 0.9 V (Typ.)) is connected to the inverting input in the programmable gain instrumentation amplifier (PGIA) as a reference voltage. On the other hand, the signal from input multiplexer x (x = 1 to 5) is connected to the non-inverting input in the PGIA.

A differential signal in the range of 0.2 to 1.6 V is output based on the reference voltage in G_{TOTAL}=1 (in settings of G_{SET1}=1 and G_{SET2}=1). Because VBIAS offset gains by G_{TOTAL},and affects the accuracy of ADC conversion results in higher gain setting, it is recommended to set G_{TOTAL}=1 (G_{SET1}=1 and G_{SET2}=1) in single-ended mode.

For details about the internal bias voltage, see ***8. Power Supply Circuit.***

3.4 Registers controlling the programmable gain instrumentation amplifier (PGIA)

The following two kinds of registers are used to control the programmable gain instrumentation amplifier (PGIA).

- Input multiplexer x (x = 1 to 4) A/D conversion setting register 1 (CHxCNT1)
- Input multiplexer x (x = 1 to 4) A/D conversion setting register 2 (CHxCNT2)

(1) Input multiplexer x (x = 1 to 4) A/D conversion setting register 1 (CHxCNT1)

These registers are used to specify the gain of the programmable gain instrumentation amplifier for input multiplexer x (x = 1 to 4). After reset, these registers are initialized to 40H.

For details, see ***4.4 Operation of A/D converter (AUTOSCAN)***.

Address: 10H (x = 1), 13H (x = 2), 16H (x = 3), 19H (x = 4) After reset: 40H R/W

	7	6	5	4	3	2	1	0
CHxCNT1	AINxOSR2	AINxOSR1	AINxOSR0	AINxGC4	AINxGC3	AINxGC2	AINxGC1	AINxGC0

AINxGC4	AINxGC3	AINxGC2	AINxGC1	AINxGC0	Gain setting		
					GSET1	GSET2	GTOTAL
0	0	0	0	0	1	1	1
0	0	1	0	0	2	1	2
0	1	0	0	0	3	1	3
0	1	1	0	0	4	1	4
1	0	0	0	0	8	1	8
0	0	0	0	1	1	2	2
0	0	1	0	1	2	2	4
0	1	0	0	1	3	2	6
0	1	1	0	1	4	2	8
1	0	0	0	1	8	2	16
0	0	0	1	0	1	4	4
0	0	1	1	0	2	4	8
0	1	0	1	0	3	4	12
0	1	1	1	0	4	4	16
1	0	0	1	0	8	4	32
0	0	0	1	1	1	8	8
0	0	1	1	1	2	8	16
0	1	0	1	1	3	8	24
0	1	1	1	1	4	8	32
Other than above					Setting prohibited		

(2) Input multiplexer x (x = 1 to 4) A/D conversion setting register 2 (CHxCNT2)

These registers are used to adjust the offset voltage for input multiplexer x (x = 1 to 4). The d_{OFR} (d_{OFR} is the input-referred value) which is the output voltage from D/A converter for adjusting the offset voltage is calculated by using the following formula:

(Input-referred) D/A converter output voltage d_{OFR} (mV) = $(-175 + 350/32 \times m) \times 1/G_{SET1}$
(m = 0 to 31: A value set to the CHxCNT2 register)

After reset, these registers are initialized to 10H.
For details, see ***4.4 Operation of A/D converter (AUTOSCAN)***.

Address: 11H (x = 1), 14H (x = 2), 17H (x = 3), 1AH (x = 4) After reset: 10H R/W

	7	6	5	4	3	2	1	0
CHxCNT2	AINSELx	0	0	AINxOFT4	AINxOFT3	AINxOFT2	AINxOFT1	AINxOFT0

AINxOFT4	AINxOFT3	AINxOFT2	AINxOFT1	AINxOFT0	*m* (steps)	d_{OFR} (mV)
0	0	0	0	0	0	$-175.00 / G_{SET1}$
0	0	0	0	1	1	$-164.06 / G_{SET1}$
0	0	0	1	0	2	$-153.13 / G_{SET1}$
... ...	... ...	... ...	... ...	... ...	... ...	... ...
1	0	0	0	0	16	0
... ...	... ...	... ...	... ...	... ...	... ...	... ...
1	1	1	0	1	29	$+142.19 / G_{SET1}$
1	1	1	1	0	30	$+153.13 / G_{SET1}$
1	1	1	1	1	31	$+164.06 / G_{SET1}$

Caution1. Bits 6 and 5 are read-only. (When these bits are read, 0 is always returned.)
2. d_{OFR} (mV) is fixed to 0 (Number of steps (*m*) = 16) in internal temperature sensor input mode.

4. 16-bit ΔΣ A/D Converter

4.1 16-bit ΔΣ A/D converter

4.1.1 Overview

The RAA730101 incorporates a 16-bit ΔΣ A/D converter. The signal from input multiplexer x (x = 1 to 5) is input to the 16-bit ΔΣ A/D converter via the programmable gain instrumentation amplifier (PGIA). The A/D conversion result is filtered by the SINC3 digital filter and is then stored in an output register.

A/D conversion is performed based on the clock generated in the internal system clock (OSC) oscillator (sampling frequency = 1 MHz (Typ.)). An external clock can also be used. (For details, see ***10. Clock configuration***.) A/D conversion is performed based on a built-in sequencer called AUTOSCAN. The data rate (A/D conversion speed) can be specified for each channel. For details, see ***4.4 Operation of A/D converter (AUTOSCAN)***.

4.1.2 Block diagram

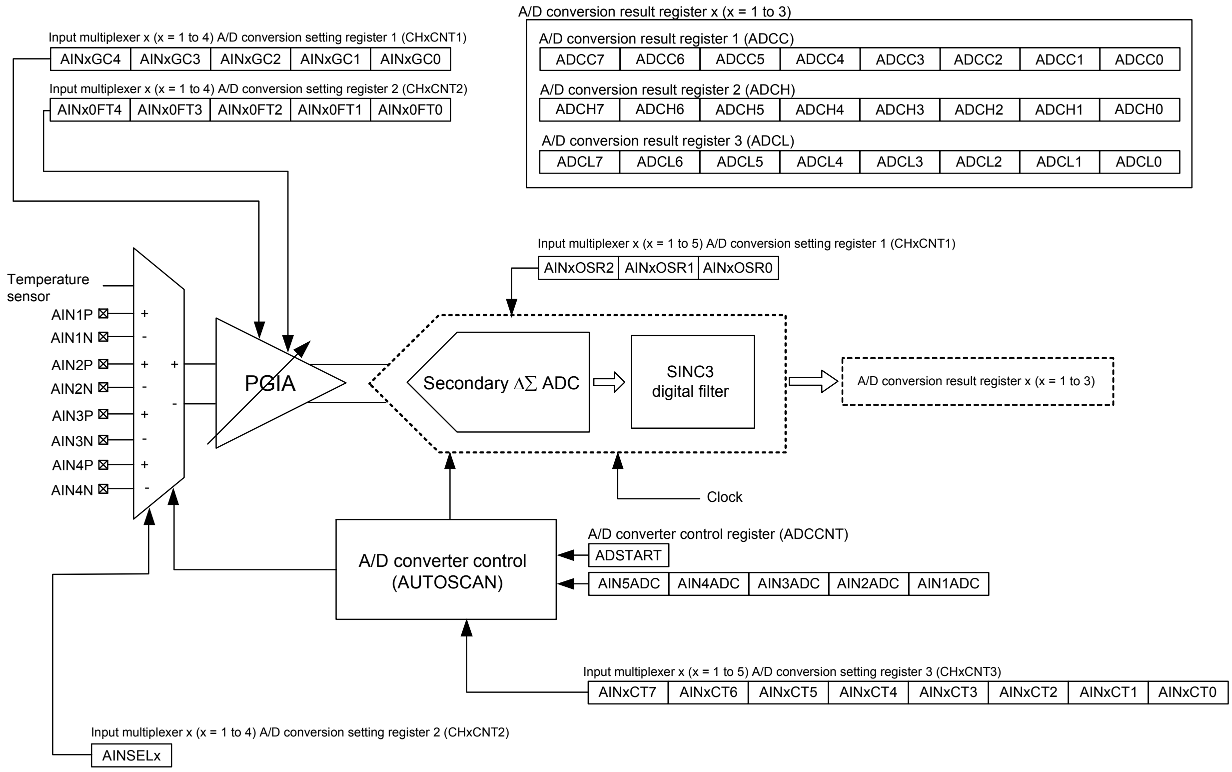


Figure 4.1 Block diagram of 16-bit ΔΣ A/D converter

4.1.3 Voltage input to the 16-bit ΔΣ A/D converter and A/D conversion result

This section describes the relationship between the voltage input to the 16-bit ΔΣ A/D converter and A/D conversion result. Figure 4.2 and Table 4.1 show the A/D conversion result when the full-scale range of voltage can be input to the A/D converter.

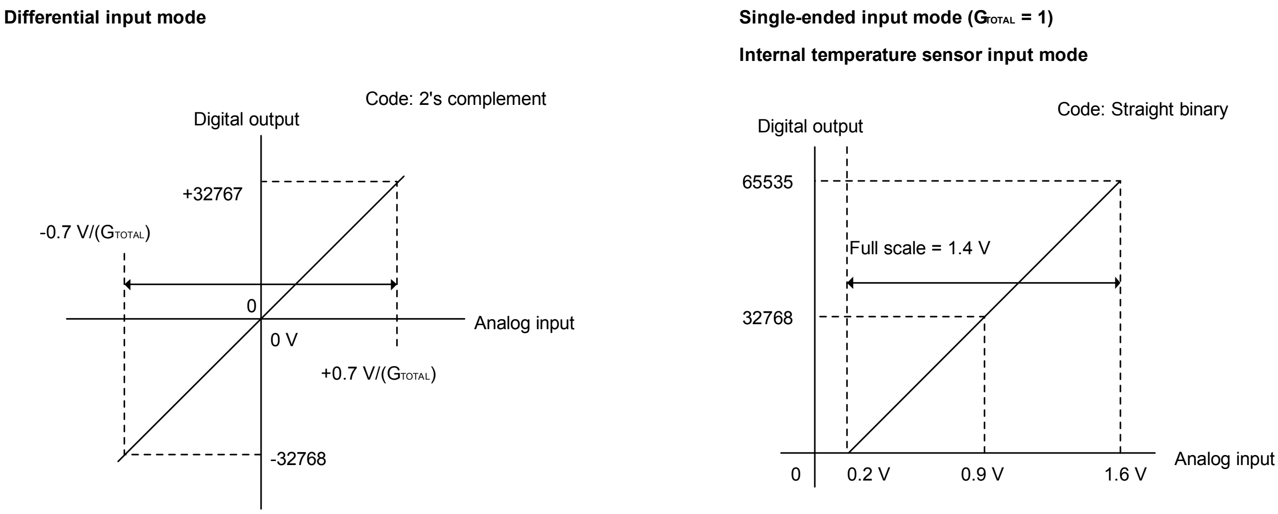


Figure 4.2 Digital output (A/D conversion result) and analog input (voltage input to the A/D converter)

Table 4.1 A/D-converted data

Differential input mode		Single-ended input mode(G_{TOTAL}=1) and internal temperature sensor input mode	
Voltage input to A/D converter	**A/D conversion result (2's complement)**	**Voltage input to A/D converter**	**A/D conversion result (straight binary)**
+700 mV / (G_{TOTAL})	32767	1.6 V	65535
0 V	0	0.9 V	32768
–700 mV / (G_{TOTAL})	–32768	0.2 V	0

The A/D conversion result shown in Table 4.1 can be calculated by using the following formulas.

- Differential input mode
  Voltage input to A/D converter = (1.4 V/G_{TOTAL}) × (ADCDATA1 / 2^{16})
  ADCDATA1: 16-bit A/D conversion result (higher 8 bits stored in ADCH and lower 8 bits stored in ADCL) expressed as 2's complement

- Single-ended input mode(G_{TOTAL}=1) and internal temperature sensor input mode
  Voltage input to A/D converter = (1.4 V/G_{TOTAL}) × (ADCDATA2 / 2^{16}) + 0.2 V
  ADCDATA2: 16-bit A/D conversion result (higher 8 bits stored in ADCH and lower 8 bits stored in ADCL) expressed as straight binary

4.2 Digital filter

4.2.1 Overview

A SINC3 digital filter is used to downsample A/D conversion results. The digital filter transfer function is expressed by using the following equation. M in the equation of the transfer function represents the factor of decimation by the digital filter, which is itself determined by the OSR (oversampling ratio) set in the AINxOSRn register (x = 0 to 5, n = 0 to 2).

$$H(z) = \left(\frac{1}{M} \cdot \frac{1 - z^{-M}}{1 - z^{-1}} \right)^3$$

4.2.2 Block diagram

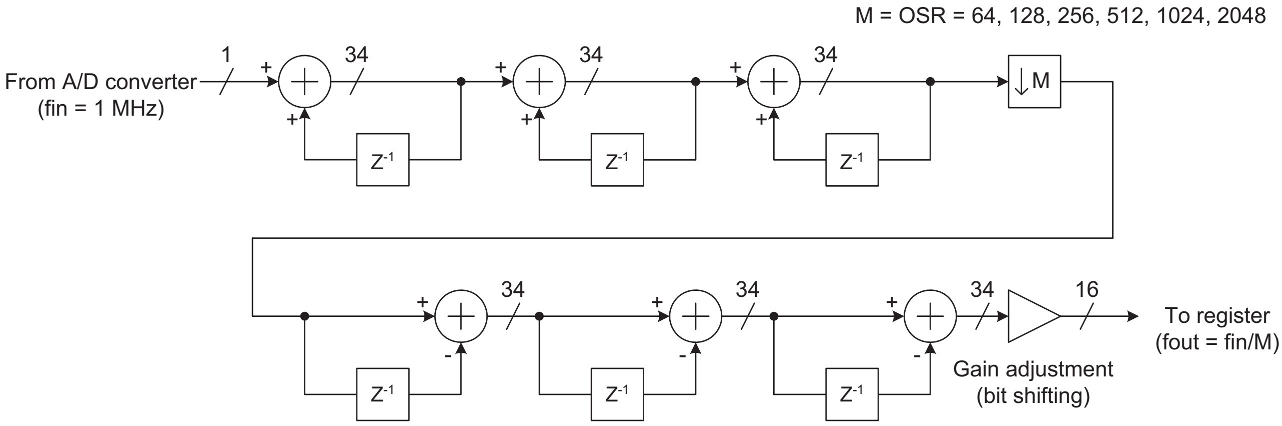


Figure 4.3 Block diagram of digital filter

Figure 4.3 shows the block diagram of the digital filter. Three integrators and three differentiators are cascaded. Considering the A/D converter stabilization time, clock synchronization at the input stage in the digital filter, and a delay caused due to three stages of the differentiator, four times the sampling period (= 4 x 1/fout) is required as the settling time. (Because the A/D converter stabilization time is fixed to 64 µs or longer, it takes five times the sampling period when M = 64.)

Remark The settling time is automatically generated in a built-in sequencer called AUTOSCAN

Figure 4.4 shows the SINC3 filter frequency response.

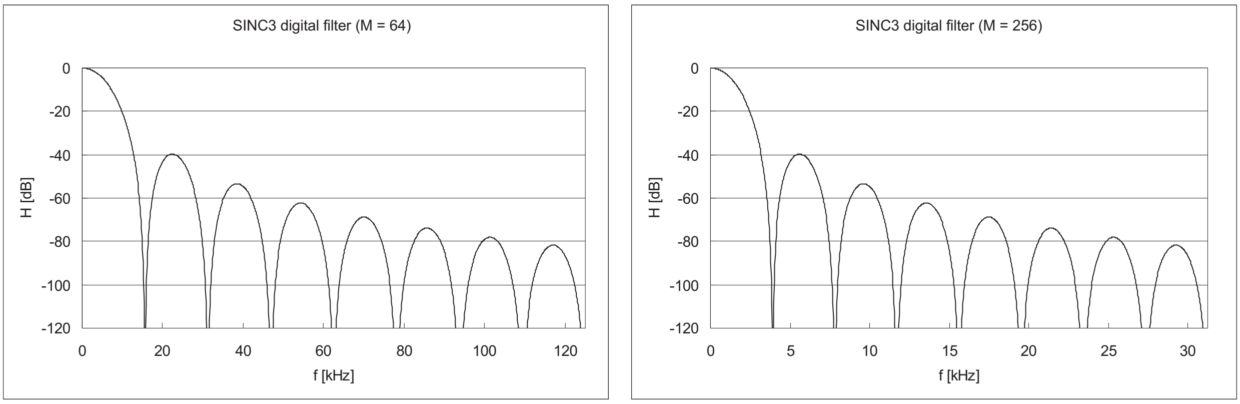


Figure 4.4 SINC3 filter frequency response where M = 64 and M = 256

4.3 Registers controlling the 16-bit ΔΣ A/D converter

The following six kinds of registers are used to control the 16-bit ΔΣ A/D converter.

- A/D converter control register (ADCCNT)
- Input multiplexer x (x = 1 to 5) A/D conversion setting register 1 (CHxCNT1)
- Input multiplexer x (x = 1 to 5) A/D conversion setting register 3 (CHxCNT3)
- A/D conversion result register 1 (ADCC)
- A/D conversion result register 2 (ADCH)
- A/D conversion result register 3 (ADCL)

(1) A/D converter control register (ADCCNT)

This register is used to start and stop A/D converter operation. This register is also used to enable or disable A/D conversion of input signals for each input multiplexer channel.

After reset, this register is cleared to 00H.

For details, see ***4.4 Operation of A/D converter (AUTOSCAN)***.

Address: 0FH After reset: 00H R/W

	7	6	5	4	3	2	1	0
ADCCNT	ADSTART	0	0	AIN5ADC	AIN4ADC	AIN3ADC	AIN2ADC	AIN1ADC

AIN1ADC	Signal from input multiplexer 1
0	Enable A/D conversion.
1	Disable A/D conversion.

AIN2ADC	Signal from input multiplexer 2
0	Enable A/D conversion.
1	Disable A/D conversion.

AIN3ADC	Signal from input multiplexer 3
0	Enable A/D conversion.
1	Disable A/D conversion.

AIN4ADC	Signal from input multiplexer 4
0	Enable A/D conversion.
1	Disable A/D conversion.

AIN5ADC	Signal from input multiplexer 5 (temperature sensor)
0	Enable A/D conversion.
1	Disable A/D conversion.

ADSTART	Control of A/D converter
0	Stop A/D conversion.
1	Start A/D conversion.

Caution Bits 6 and 5 are read-only. (When these bits are read, 0 is always returned.)

(2) Input multiplexer x (x = 1 to 5) A/D conversion setting register 1 (CHxCNT1)
These registers are used to specify the data rate (A/D conversion speed) for input multiplexer x (x = 1 to 5).
After reset, these registers are initialized to 40H.
For details, see ***4.4 Operation of A/D converter (AUTOSCAN)***.

Address: 10H (x = 1), 13H (x = 2), 16H (x = 3), 19H (x = 4) After reset: 40H R/W

	7	6	5	4	3	2	1	0
CHxCNT1	AINxOSR2	AINxOSR1	AINxOSR0	AINxGC4	AINxGC3	AINxGC2	AINxGC1	AINxGC0

Address: 1CH (x = 5) After reset: 40H R/W

	7	6	5	4	3	2	1	0
CH5CNT1	AIN5OSR2	AIN5OSR1	AIN5OSR0	0	0	0	0	0

Caution Bits 4 to 0 are read-only. (When these bits are read, 0 is always returned.)

AINxOSR2	AINxOSR1	AINxOSR0	OSR (oversampling ratio)	Data rate (sps)
0	0	0	64	15625.000
0	0	1	128	7812.500
0	1	0	256	3906.250
0	1	1	512	1953.125
1	0	0	1024	976.563
1	0	1	2048	488.281
Other than above			Setting prohibited	

Remark The A/D converter sampling clock frequency is set to 1 MHz (Typ.).

(3) Input multiplexer x (x = 1 to 5) A/D conversion setting register 3 (CHxCNT3)

These registers are used to specify the number of A/D conversions per AUTOSCAN cycle for input multiplexer x (x = 1 to 5). The number of A/D conversions N can be expressed by using the formula below.

After reset, these registers are cleared to 00H.

For details, see ***4.4 Operation of A/D converter (AUTOSCAN)***.

$N = 32 \times (2^n - 1) + m \times 2^n$ (*m* and *n* correspond to the values set to the CHxCNT3 register)

Address: 12H (x = 1), 15H (x = 2), 18H (x = 3), 1BH (x = 4), 1EH (x = 5) After reset: 00H R/W

	7	6	5	4	3	2	1	0
CHxCNT3	AINxCT7	AINxCT6	AINxCT5	AINxCT4	AINxCT3	AINxCT2	AINxCT1	AINxCT0

AINxCT4	AINxCT3	AINxCT2	AINxCT1	AINxCT0	m
0	0	0	0	0	0
0	0	0	0	1	1
0	0	0	1	0	2
...	...	...	...	...	...
1	0	0	0	0	16
...	...	...	...	...	...
1	1	1	0	1	29
1	1	1	1	0	30
1	1	1	1	1	31

AINxCT7	AINxCT6	AINxCT5	n
0	0	0	0
0	0	1	1
0	1	0	2
0	1	1	3
1	0	0	4
1	0	1	5
1	1	0	6
1	1	1	7

Up to 256 levels can be selected by combining *m* and *n*. The following figure shows the correlation between the number of A/D conversions and the number of levels (0 to 255) calculated by using the register value.

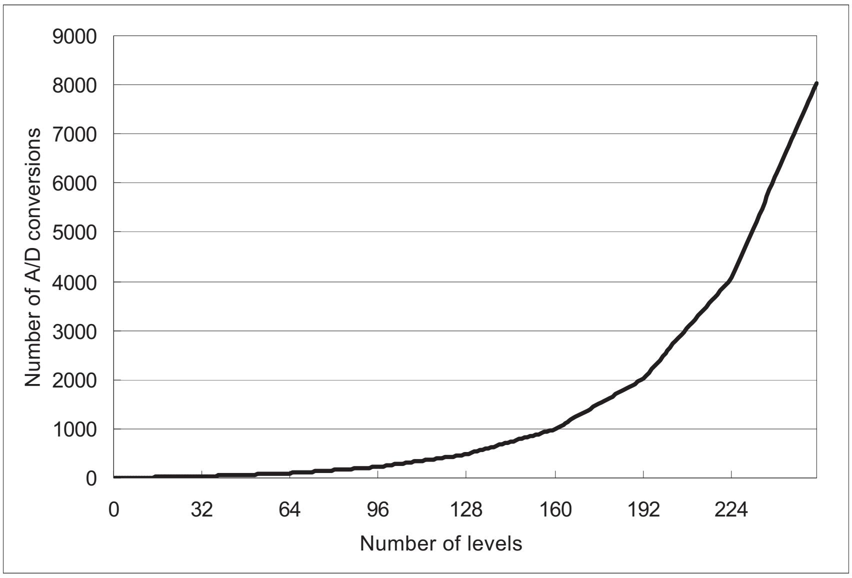


Figure 4.5 The number of A/D conversions and the number of levels calculated by using the register value (0 to 255)

(4) A/D conversion result register 1 (ADCC)

This is a read-only register that is used to check the A/D conversion result. You can check the A/D conversion result parameters including the checksum, overflow flag, and the channel of input multiplexer corresponding to the conversion result. For details about a checksum, see ***6. UART***.

After reset, this register is cleared to 00H.

For details, see ***4.4 Operation of A/D converter (AUTOSCAN)***.

Address: 0CH After reset: 00H R/–

	7	6	5	4	3	2	1	0
ADCC	ADCC7	ADCC6	ADCC5	ADCC4	ADCC3	ADCC2	ADCC1	ADCC0

ADCC3	ADCC2	ADCC1	ADCC0	Checksum calculated from A/D conversion result
1 / 0	1 / 0	1 / 0	1 / 0	Checksum

ADCC4	Flag that indicates whether A/D conversion result overflowed
0	No overflow (within range)
1	Overflow occurred (causing the register value to be the maximum value)

ADCC7	ADCC6	ADCC5	The channel corresponding to the conversion result
0	0	0	Invalid
0	0	1	Input multiplexer 1 (AIN1P/AIN1N)
0	1	0	Input multiplexer 2 (AIN2P/AIN2N)
0	1	1	Input multiplexer 3 (AIN3P/AIN3N)
1	0	0	Input multiplexer 4 (AIN4P/AIN4N)
1	0	1	Input multiplexer 5 (temperature sensor)
1	1	0	Invalid
1	1	1	Invalid

(5) A/D conversion result register 2 (ADCH)

This is a read-only register that is used to check the A/D conversion result. This register stores the higher 8 bits of the 16-bit conversion result.

After reset, this register is cleared to 00H.

For details, see ***4.4 Operation of A/D converter (AUTOSCAN)***.

Address: 0DH After reset: 00H R/–

	7	6	5	4	3	2	1	0
ADCH	ADCH7	ADCH6	ADCH5	ADCH4	ADCH3	ADCH2	ADCH1	ADCH0

(6) A/D conversion result register 3 (ADCL)

This is a read-only register that is used to check the A/D conversion result. This register stores the lower 8 bits of the 16-bit conversion result.

After reset, this register is cleared to 00H.

For details, see ***4.4 Operation of A/D converter (AUTOSCAN)***.

Address: 0EH After reset: 00H R/–

	7	6	5	4	3	2	1	0
ADCL	ADCL7	ADCL6	ADCL5	ADCL4	ADCL3	ADCL2	ADCL1	ADCL0

4.4 Operation of A/D converter (AUTOSCAN)

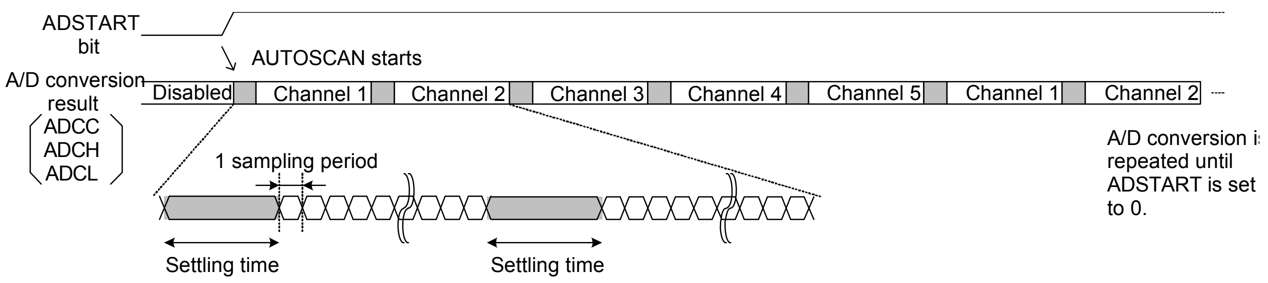
All operations controlling the A/D conversion are based on a built-in sequencer called AUTOSCAN. The AUTOSCAN operation starts when "1" is written to the ADSTART bit of the A/D converter control register (ADCCNT). The signal from input channels is A/D-converted in round-robin fashion.

Use the AIN5ADC, AIN4ADC, AIN3ADC, AIN2ADC, and AIN1ADC bits of the A/D converter control register (ADCCNT) to control whether to A/D-convert the signal from each input channel.

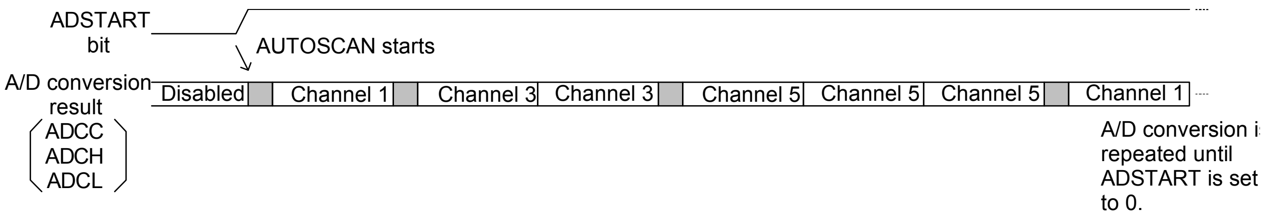
Use input multiplexer x (x = 1 to 5) A/D conversion setting register 3 (CHxCNT3) to specify the number of times A/D conversion is to be performed in an active channel until execution shifts to the next channel. If CHxCNT3 is set to 00H, it specifies single-shot operation, which stops A/D conversion each time when a conversion ends.

Use the AINxOSR2, AINxOSR1, and AINxOSR0 bits of input multiplexer x (x = 1 to 5) A/D conversion setting register 1 (CHxCNT1) to specify the data rate (A/D conversion speed) on a conversion channel.

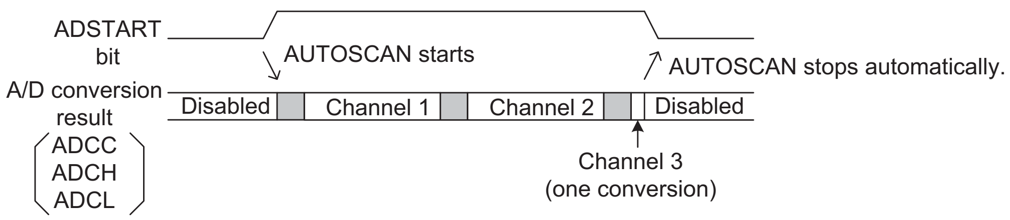
The A/D conversion result is stored in read-only registers ADCC (for storing the checksum, overflow status, and the A/D-converted channel of the input multiplexer), ADCH (for storing the higher 8 bits of the conversion result), and ADCL (for storing the lower 8 bits of the conversion result).



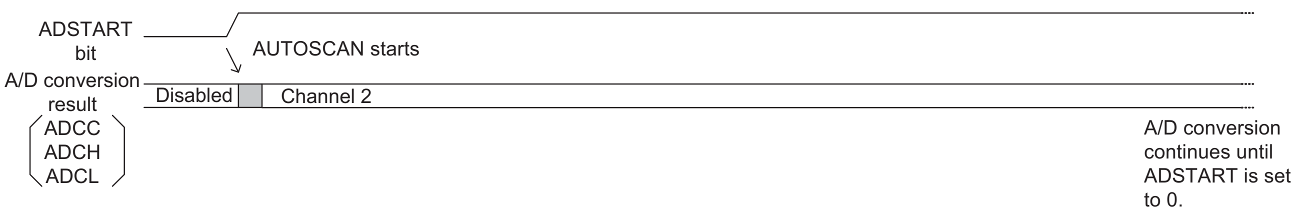
Example 1 When skipping A/D conversion of the signal from input channels
AIN5ADC = AIN3ADC = AIN1ADC = 0, AIN4ADC = AIN2ADC = 1
AIN1CTn [7:0] = 1, AIN3CTn [7:0] = 2, AIN5CTn [7:0] = 3



Example 2 To perform single-shot A/D conversion of the signal from channel 3
AIN3ADC = AIN2ADC = AIN1ADC = 0, AIN5ADC = AIN4ADC = 1
AINxCTn [7:0] > 0 (x = 1, 2) *Value of input multiplexer x (x = 1 or 2) A/D conversion setting register
AIN3CTn [7:0] = 0 *Value of input multiplexer 3 A/D conversion setting register



Example 3 When only the signal from channel 2 is A/D converted successively
AIN2ADC = 0, AIN5ADC = AIN4ADC = AIN3ADC = AIN1ADC = 1
AIN2CTn [7:0] > 0 *Value of input multiplexer 2 A/D conversion setting register



Remark The settling time is automatically generated in a built-in sequencer called AUTOSCAN

Figure 4.6 AUTOSCAN sequence

To transfer the A/D conversion result to a microcontroller, three types of communication, UART, SPI, and SPI which does not use an interrupt signal (INT), can be used. The simplified timing charts for each communication type are shown below. For details, see ***5. SPI*** and ***6. UART***.

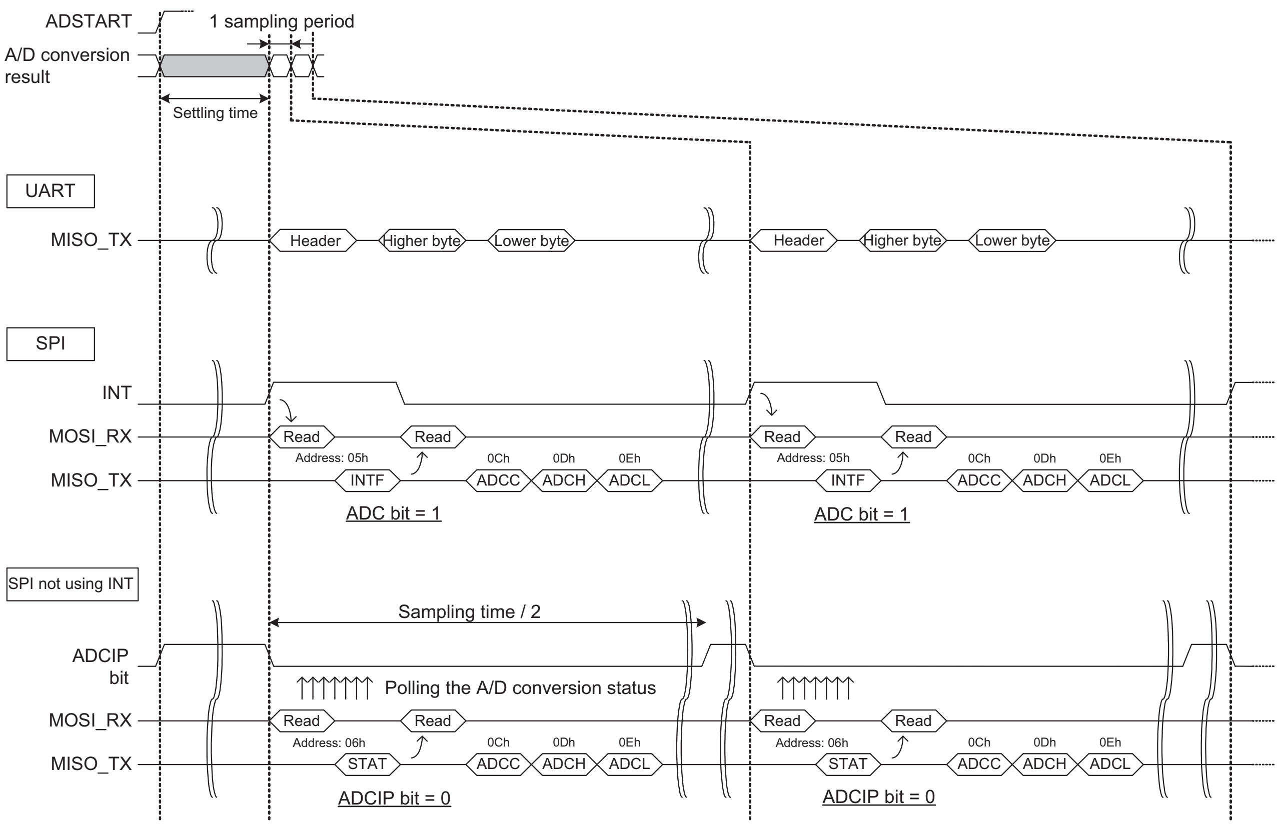


Figure 4.7 AUTOSCAN interface timing

5. SPI

5.1 Overview

The SPI interface is used to allow control from external devices by using clocked communication via four lines: a serial clock line (SCLK), a serial data input line (MOSI_RX), a serial data output line (MISO_TX), and a chip select input line (CS_B).

SPI communication or UART communication is selected according to the SMODE pin setting. If a high level is input to the SMODE pin, SPI communication is selected. If a low level is input to the SMODE pin, UART communication is selected. Some SPI pins are also used as UART pins, which are selected according to the SMODE pin setting (exclusive use).

- SMODE = 1: SPI communication (TGLSM = 0)
- SMODE = 0: UART communication (TGLSM = 0)

<R> There is a point to note when using the SPI of the RAA730101. For details, see ***5.5 Note on Using the SPI***.

Caution Clear the TGLSM bit of the startup sequence/communication control register (STARTUP) to "0". For details, see ***13. Flash Memory***.

5.2 SPI command format

An SPI access is established by using a short access command or long access command. Which to use is determined according to the command used. For the detailed command definitions, see the table *SPI commands*. Because reading data from the flash memory takes a long time to start, the flash read command requires an access cycle equivalent to two commands.

Short access command

Command (8 bits)								Data (8 bits)							
R/W	R/F	1	C4	C3	C2	C1	C0	D7	D6	D5	D4	D3	D2	D1	D0
C7	C6	C5													

Long access command

Command (8 bits)								Extension (8 bits)								Data (8 bits)							
R/W	R/F	0	C4	C3	C2	C1	C0	E7	E6	E5	E4	E3	E2	E1	E0	D7	D6	D5	D4	D3	D2	D1	D0
C7	C6	C5																					

R/W 0: Read mode 1: Write mode

R/F 0: Register 1: Flash memory

The following table shows the SPI commands.

Table 5.1 SPI commands

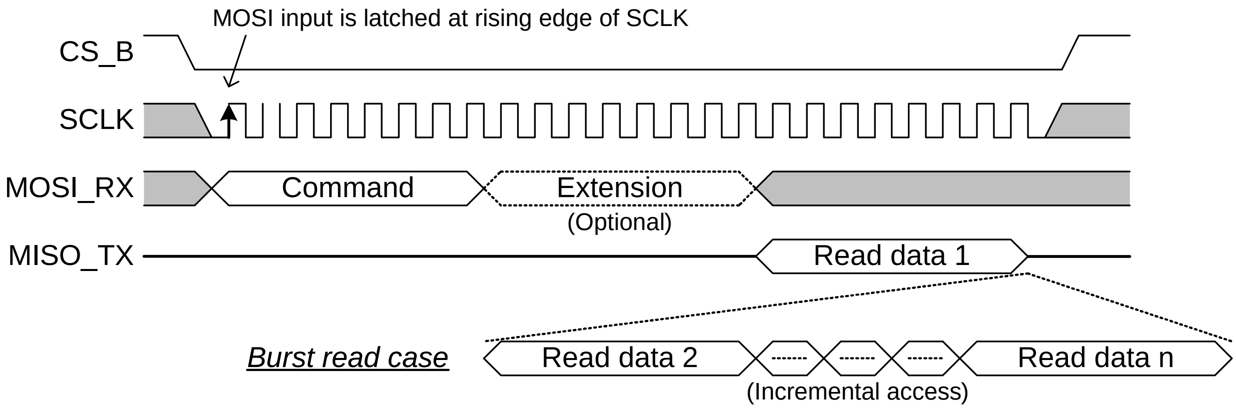
No.	Name	Command				Extension	Description
		C7	C6	C5	C4 to C0	E7 to E0	
1	Register Read	0	0	1	Address: 00h to 1Fh	–	Reads 1 byte of data from the specified register.
2	Register Write	1	0	1	Address: 00h to 1Fh	–	Writes 1 byte of data to the specified register.
3	Register Burst Read	0	0	0	Data length 1xxxx Note 1	Start address 00h to 1Fh	Reads the specified length of data from the specified register successively. (Starting from the specified address)
4	Register Burst Write	1	0	0	Data length 1xxxx Note 1	Start address 00h to 1Fh	Writes the specified length of data to the specified register successively. (Starting from the specified address)
5	Register All Write from Flash	1	0	0	01111	–	Copies all data stored in the register shadow in the flash memory to the specified register.
6	Buffer Refresh	1	0	0	01100	–	Copies the default configuration data to the register buffer.
7	Flash (Burst) Read Note 3	0	1	0	11111	Start address 00h to FFh	Reads data from the flash memory. Specifies the address from which to start reading data. (First command)
		0	1	0	11100	Data length 00h to FFh Note 2	Reads data from the flash memory. Specifies the length of data to be read. (Second command)
8	Flash Write	1	1	0	11111	Address: 00h to FFh	Writes 1 byte of data to the flash memory.
9	Flash All Erase Note 3	1	1	1	11010	–	Erases all data in the flash memory. (First command)
		1	1	1	01011	–	Erases all data in the flash memory. (Second command)

Notes
1. Data length = "sum of C3 to C0 values" + 1 (Up to 16 bytes)
2. Data length = "sum of E7 to E0 values" + 1 (Up to 256 bytes)
3. To (burst) read and erase data in the flash memory, accessing the flash memory by successively using two commands is required.

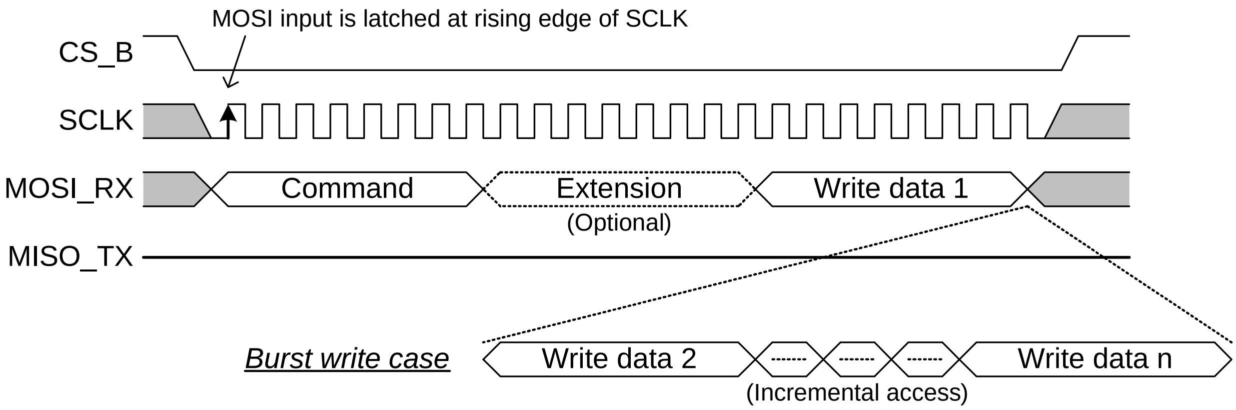
5.3 Timing of SPI communication operations

The timing of SPI communication operations is shown below.

< Register Read / Register Burst Read >



< Register Write / Register Burst Write / Flash Write [Note] >



Notes There is not *burst function* for Flash write. Only writing 1 Byte data is available.

< Register All Write from Flash / Buffer Refresh >

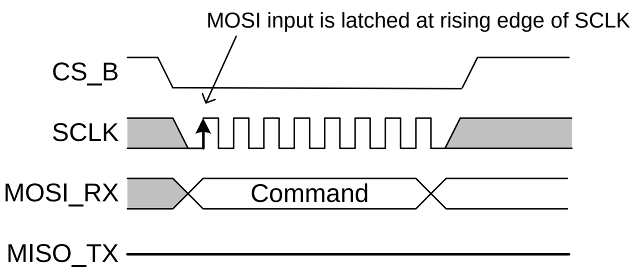


Figure 5.1 Timing of SPI communication operations

< Flash (Burst) Read >

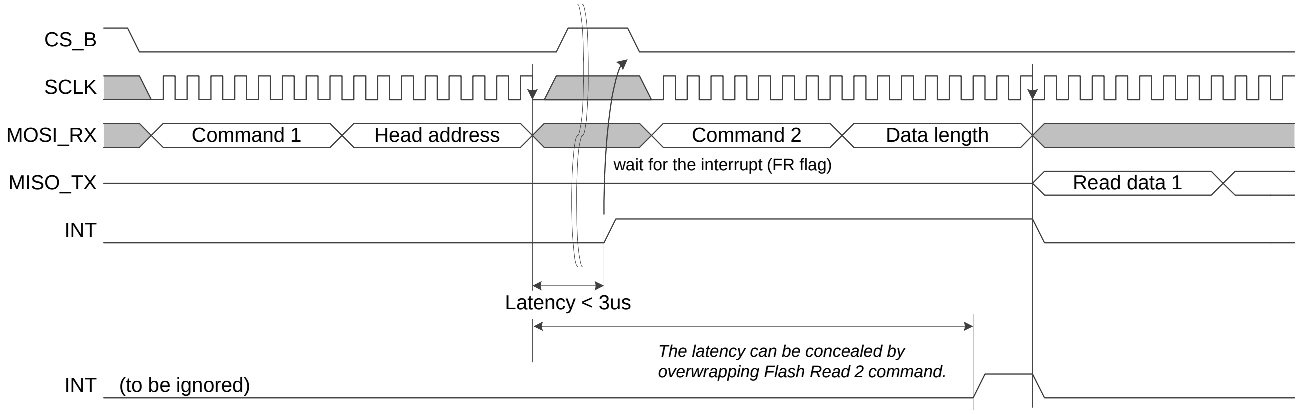


Figure 5.2 Timing of SPI communication operations (read access to the flash memory)

< Flash Erase >

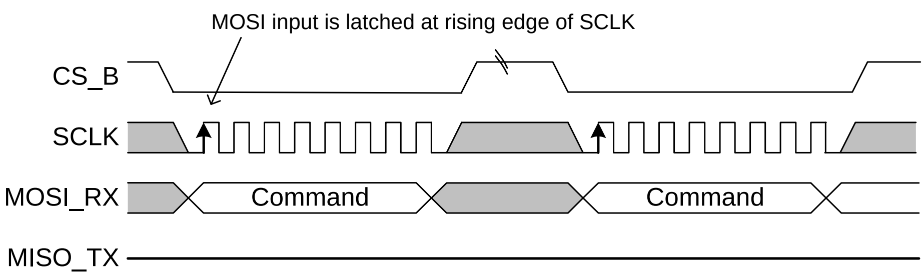


Figure 5.3 Timing of SPI communication operations (erasing all the data of the flash memory)

5.4 Registers controlling SPI communication

The following register is used to control SPI communication.

- Startup sequence/communication control register (STARTUP)

(1) Startup sequence/communication control register (STARTUP)
This register is used to control flash memory access during the startup sequence and select the communication mode. After reset, this register is cleared to 00H. For details, see ***13. Flash Memory***.
Be sure to clear the TGLSM bit to “0”.

Address: 1FH After reset: 00H R/–

	7	6	5	4	3	2	1	0
STARTUP	0	0	0	TGLSM	0	0	SDCOR	CPSOR

TGLSM	Control of SMODE pin function
0	UART communication is selected when SMODE = 0, and SPI communication is selected when SMODE = 1.
1	Setting prohibited

Caution Bits 7, 6, 5, 3, and 2 are read-only. (When these bits are read, 0 is always returned.)

<R> 5.5 Note on Using the SPI

Pay attention to the following point when using the SPI.
When the communicating node enters the reset state, the levels on the CS_B and SCLK pins become undefined and the result of the first SPI communication after the other party is released from the reset state may be failure.
When using a communication mode where the level on the SCLK pin becomes high while the level on CS_B pin is high, confirm that the CHIPID can be read correctly after the other party is released from the reset state, and then start the communications that are actually required.

6. UART

6.1 Overview

A full duplex operational communication interface is available by using two lines: a serial data transmission line (TxD) and a serial data reception line (RxD). Using these two communication lines, a data frame (a packet ; its character length = 10-12bits), which consists of a start bit, data, parity bit, and stop bit, is transmitted and received asynchronously (using an internal baud rate) with a communicating node.

There is a point to note when using the UART of the RAA730101. For details, see ***6.6 Note on Using the UART***.

SPI communication or UART communication is selected according to the SMODE pin setting. If a high level is input to the SMODE pin, SPI communication is selected. If a low level is input to the SMODE pin, UART communication is selected. Some UART pins are also used as SPI pins, which are selected according to the SMODE pin setting (exclusive used).

- SMODE = 1: SPI communication (TGLSM = 0)
- SMODE = 0: UART communication (TGLSM = 0)

Caution Clear the TGLSM bit of the startup sequence/communication control register (STARTUP) to "0". For details, see *13. Flash Memory*.

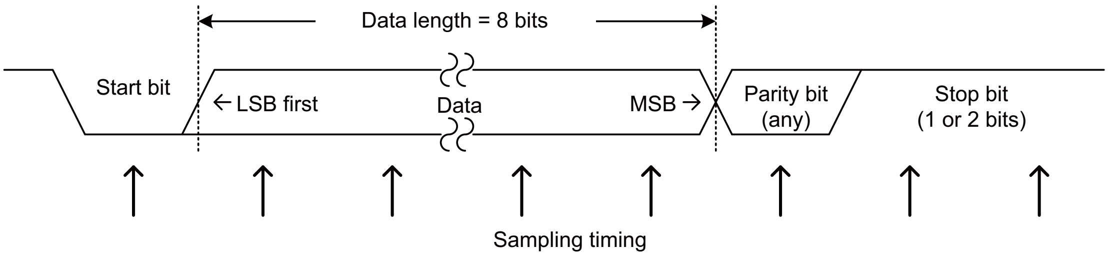


Figure 6.1 UART packet format

By default, the baud rate is 4.8 kbps, no parity, and the number of stop bits is 1. This default setting is used for the first communication after a power-on reset. If you want to use a setting other than the default for the first communication after a power-on reset, store the configuration data you want to use in the register shadow in the flash memory in advance. For details, see ***13. Flash Memory***.

UART communication parameters such as the baud rate, parity bit, and stop bit can be selected by using a register. For details, see ***6.2 Registers controlling UART communication***.

As special features, PWM direct input using the Rx pin and differential output using the Tx pin are available. For details, see ***6.7 PWM direct input*** and ***6.8 Differential output***.

There is a time out feature for UART reception and transmission. For details, see ***6.3 UART reception (UART command format)*** and ***6.4 UART transmission***.

The following shows an overview of the UART.

Table 6.1 Overview of UART

	Receiver side (Rx communication)	Transmitter side (Tx communication)
Baud rate	4.8 kbps (default) or 250 kbps (Selectable by using the RXBR bit in the setting register)	4.8 kbps (default) or 250 kbps (Selectable by using the TXBR bit in the setting register)
Signal format	NRZ[Note 1] or PWM[Note 2] (Selected according to the CS_B pin level)	NRZ[Note 1]
Packet format (character length = 10-12bits)	Start bit - 1 bit (fixed)	
	Data length - 8 bits (fixed) - LSB first	
	Parity setting - No parity (default) - Odd parity (Selectable by using the PEN and EPS bits in the setting register) - Even parity (Selectable by using the PEN and EPS bits in the setting register)	
	Number of stop bits - 1 bit (default) - 2 bits (Selectable by using the STB bit in the setting register register)	
Time-out time	Character length × 2	
Special function	PWM direct input	Differential output

Notes 1. NRZ: Non Return to Zero

2. PWM: Pulse Width Modulation

6.2 Registers controlling UART communication

The following two kinds of registers are used to control UART communication.

- Startup sequence/communication control register (STARTUP)
- Clock/UART control register (UARTCNT)

(1) Startup sequence/communication control register (STARTUP)

This register is used to control flash memory access during the startup sequence and select the communication mode. After reset, this register is cleared to 00H. For details, see ***13. Flash Memory***.
Be sure to clear the TGLSM bit to “0”.

Address: 1FH After reset: 00H R/–

	7	6	5	4	3	2	1	0
STARTUP	0	0	0	TGLSM	0	0	SDCOR	CPSOR

TGLSM	Control of SMODE pin function
0	UART communication is selected when SMODE = 0, and SPI communication is selected when SMODE = 1.
1	Setting prohibited

Caution Bits 7, 6, 5, 3, and 2 are read-only. (When these bits are read, 0 is always returned.)

(2) Clock/UART control register (UARTCNT)

This register is used to specify UART parameters and control the clock configuration.
After reset, this register is cleared to 00H.

Address: 08H After reset: 00H R/W

	7	6	5	4	3	2	1	0
UARTCNT	EXTCLK	MONIOUT	DIFFOUT	STB	EPS	PEN	TXBR	RXBR

RXBR	Baud rate during reception
0	4.8 kbps (default)
1	250 kbps

TXBR	Baud rate during transmission
0	4.8 kbps (default)
1	250 kbps

PEN	Enabling/disabling the parity bit
0	No parity (default)
1	A parity bit is generated (checked)

EPS	Parity bit selection
0	Odd parity (default): The number of 1s in each set of written bits must be an odd number.
1	Even parity: The number of 1s in each set of written bits must be an even number.

STB	Number of stop bits
0	1 bit (default)
1	2 bits

DIFFOUT	Differential output during transmission
0	Disable differential output (default)
1	Enabled differential output

Remark When DIFFOUT is set to 0, the output of the TX_B pin becomes high impedance. The TX_B pin can be left open when it is not used. For details, see ***1.4 Connection of unused pins***.

6.3 UART reception (UART command format)

Like SPI commands, UART commands require a 1- or 2-byte packet for each command (see ***5.2 SPI command format***). Message reception might take a time-out if the interval of each packet that makes up a message could not be within a period of two character length. If packet reception fails due to a time-out, the UART receiver is initialized.

There are two commands dedicated to UART communication. One is a "baud rate correction" command. If this command is received, a message that consists of 9-bits logical low level (= start bit + 0000_0000b) is output from the transmission output pin. An external device can adjust the baud rate by counting the number of low cycles.

The other is a "Send request" command. If this command is received, a message that was transmitted last is transmitted again. By using this command, an external device can regain a message which was lost due to a parity error or checksum error. "Send request" is available only for a deferred response, which is described in a later section.

There is a point to note regarding the UART reception. For details, see ***6.6 Note on Using the UART***.

Short access command

Command (8 bits)								Data (8 bits)							
R/W	R/F	1	C4	C3	C2	C1	C0	D7	D6	D5	D4	D3	D2	D1	D0
C7	C6	C5													

Long access command

Command (8 bits)								Extension (8 bits)								Data (8 bits)							
R/W	R/F	0	C4	C3	C2	C1	C0	E7	E6	E5	E4	E3	E2	E1	E0	D7	D6	D5	D4	D3	D2	D1	D0
C7	C6	C5																					

R/W 0: Read mode 1: Write mode

R/F 0: Register 1: Flash memory

The following table shows the UART commands.

Table 6.2 UART commands

No.	Name	Command				Extension	Description
		C7	C6	C5	C4 to C0	E7 to E0	
1	Register Read	0	0	1	Address: 00h to 1Fh	–	Reads 1 byte of data from the specified register.
2	Register Write	1	0	1	Address: 00h to 1Fh	–	Writes 1 byte of data to the specified register.
3	Register Burst Read	0	0	0	Data length 1xxxx Note 1	Start address 00h to 1Fh	Reads the specified length of data from the specified register successively. (Starting from the specified address)
4	Register Burst Write	1	0	0	Data length 1xxxx Note 1	Start address 00h-1Fh	Writes the specified length of data to the specified register successively. (Starting from the specified address)
5	Register All Write from Flash	1	0	0	01111	–	Copies all data stored in the register shadow in the flash memory to the specified register.
6	Buffer Refresh	1	0	0	01100	–	Copies the default configuration data to the register buffer.
7	Flash (Burst) Read Note 3	0	1	0	11111	Start address 00h to FFh	Reads data from the flash memory. Specifies the address from which to start reading data. (First command)
		0	1	0	11100	Data length 00h to FFh Note 2	Reads data from the flash memory. Specifies the length of data to be read. (Second command)
8	Flash Write	1	1	0	11111	Address 00h to FFh	Writes 1 byte of data to the flash memory.
9	Flash All Erase Note 3	1	1	1	11010	–	Erases all data in the flash memory. (First command)
		1	1	1	01011	–	Erases all data in the flash memory. (Second command)
10	Baud rate correction	0	0	0	00000	–	Corrects the baud rate. (Only available in UART communication)
11	Send request	0	0	0	01111	–	Requests re-transmission of the message transmitted last. (Only available in UART communication)

Notes **1.** Data length = "sum of C3 to C0 values" + 1 (Up to 16 bytes)

2. Data length = "sum of E7 to E0 values" + 1 (Up to 256 bytes)

3. To (burst) read and erase data in the flash memory, accessing the flash memory by successively using two commands is required.

6.4 UART transmission

A UART transmission message has three types of the structures shown below.

A type 1 message is transmitted in response to Register Read, Register Burst Read or Flash (Burst) Read command shown in the table of *UART commands*. A type 2 message is transmitted automatically when A/D conversion ends. A type 3 message is transmitted automatically when an interrupt request is generated. A type 3 message is equivalent to the INT signal used in SPI communication. (For details, see ***7. Interrupt signal output function (for SPI communication)***.)

Message transmission might take a time-out if the interval of each packet that makes up a message could not be within a period of two character length.

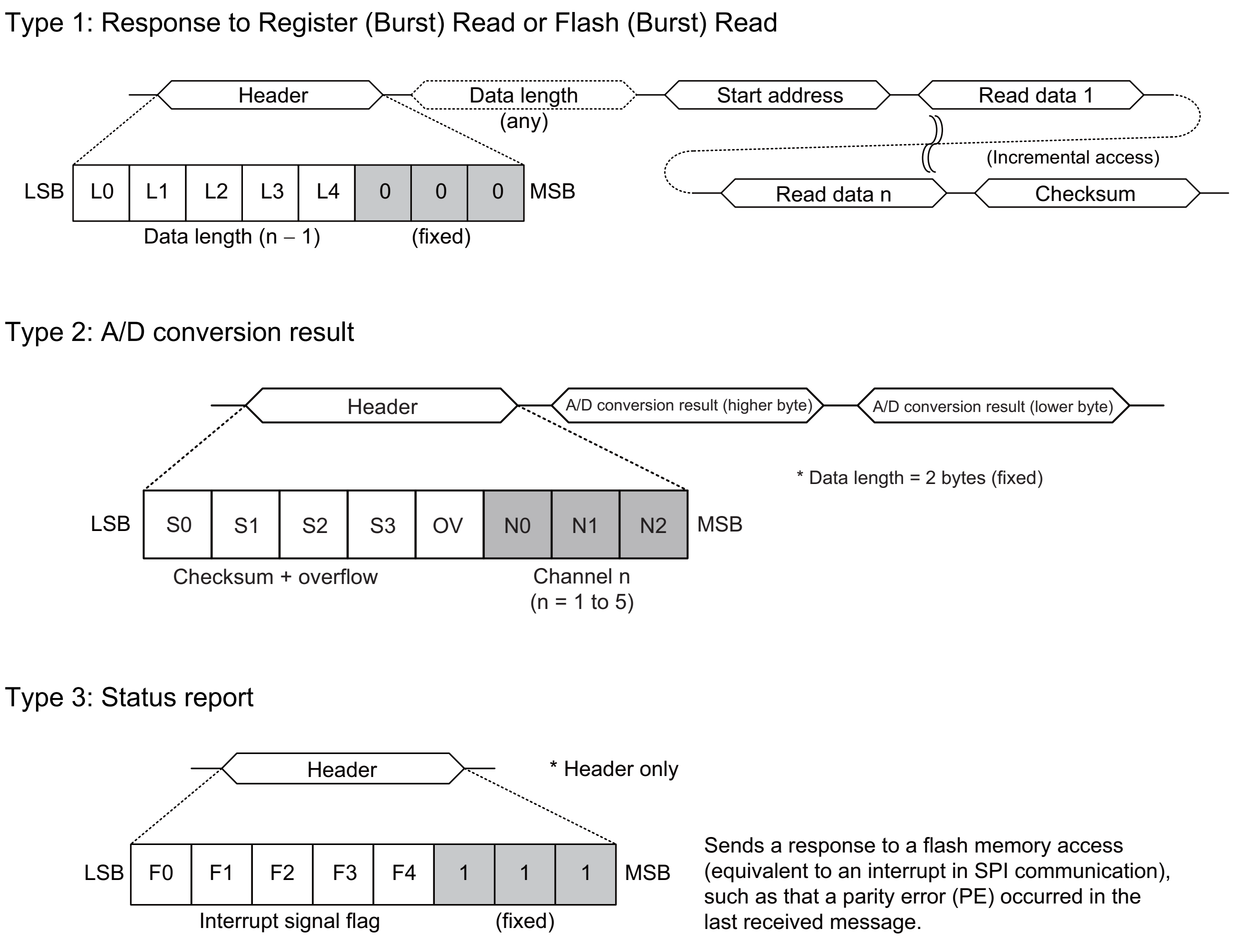


Figure 6.2 Transmission message structure

The type 1 message consists of the header which describes the data length of read data, the start address of read data and read data. The maximum data length which the header can describe is 32 bytes. If the data length of read data is 32 bytes or more, an additional packet that indicates the actual data length (data length = n-1; 32 to 256 bytes) is inserted following to the header in the message.

The type 2 message consists of the header, A/D conversion result (higher bytes) and A/D conversion result (lower bytes). These three contents corresponds to the information of A/D conversion result register 1 (ADCC), A/D conversion result register 2 (ADCH), A/D conversion result register 3 (ADCL). The header of the type 2 message reserves the information of the checksum, the overflow status and the input channel which is A/D converted. The overflow flag in a type 2 header indicates whether the A/D conversion result has been clipped to the maximum value that can be stored in the register.

The type 3 message consists of the header which describes the status. The definitions of flags included in type 3 are shown below. These flags have the same meaning as that indicated in the interrupt signal flag indication register (INTFLAG). (For details, see ***7.3 Registers controlling the interrupt signal output function***.) Note, however, that the F4 bit is not the ADC flag but the PE flag. This is because the A/D conversion result is transmitted automatically when the A/D conversion ends in UART communication, and therefore the ADC flag is not required.

Like SPI communication, the RAW flag is also set when the Buffer Refresh command (see No. 6 in the table *UART commands*) is executed.

F0: Flash Read ready (FR flag)
F1: Flash Write (FW flag)
F2: Flash All Erase (FAE flag)
F3: Register All Write (RAW flag)
F4: Parity Error at the last reception (PE flag)

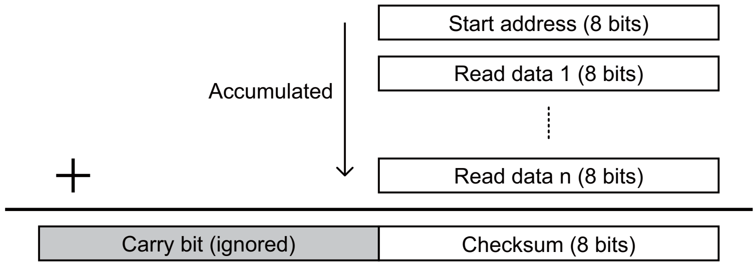
If the logic of one of the five flags included in a message becomes high, transmitting an interrupt request is enabled and the message is automatically transmitted. A communication error can be detected by checking the bit arrangement, even if a parity bit is disabled.

To transmit an A/D conversion result successively by using the UART, the baud rate must be set to 250 kbps. Even though the baud rate is set to 250 kbps, the communication speed becomes insufficient and UART transmission fails under the condition when the oversampling ratio (OSR) for A/D conversion is set to 64, or when the oversampling ratio (OSR) is set to 128 with the parity bit enabled or with the number of stop bits set to 2.

If A/D conversion result is not transmitted successively (but by just one time, or by single-shot), there is no restriction on the communication speed.

The checksum can be calculated as follows. When verifying the checksum from an external device, see the relevant checksum calculation.

How to calculate a checksum for type 1 (response to Register Read or Flash Read)



How to calculate a checksum for type 2 (A/D conversion result)

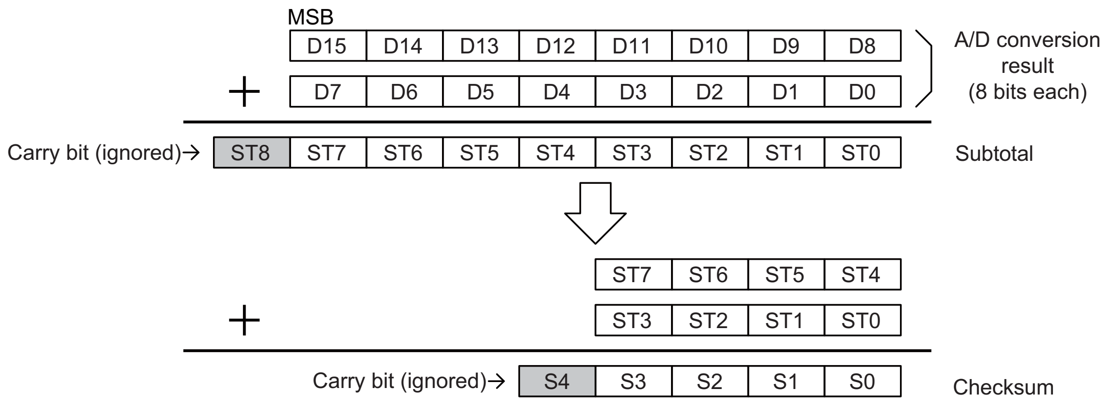


Figure 6.3 Checksum calculation

6.5 Communication flow

Some instant responses always occur, regardless of the command conditions including whether the command has finished normally or abnormally. In addition to instant responses, deferred responses are also sent asynchronously in terms of some commands.

Any new command is ignored until a series of command and response (including a deferred response) is completed. The table below shows the relationship between received commands and transmitted responses.

Abnormal end shown for type 3 (PE) indicates that an error such as a parity error and framing error has occurred, or an execution error such as a flash memory access being attempted while flash memory access is prohibited has occurred.

Because A/D conversion results are transmitted asynchronously, a *conflict* might occur. The messages of responses (data) are retained in the transmission buffer as much as possible. If the *conflict* continues for a long time, however, the transmission buffer becomes full, which causes the A/D conversion results to be lost because the transmission buffer is updated periodically. Therefore, it is not recommended to issue a reception command while A/D conversion results are transmitted.

Table 6.3 Relationship between reception commands and transmitted responses

Reception command			Transmitted response				
No.	**Name**	**→**	**Instant response (normal end)**Note 1	**or**	**Instant response (abnormal end)**Note 2	**→**	**Deferred response**Note 3
1	Register Read	→	Type 1	or	Type 3 (PE)		
2	Register Write	→	Type 3 (normal end)	or	Type 3 (PE)		
3	Register Burst Read	→	Type 1	or	Type 3 (PE)		
4	Register Burst Write	→	Type 3 (normal end)	or	Type 3 (PE)		
5	Register All Write from Flash	→	Type 3 (normal end)	or	Type 3 (PE)	→	Type 3 (RAW)
6	Buffer Refresh	→	Type 3 (normal end)	or	Type 3 (PE)	→	Type 3 (RAW)
7	Flash (Burst) Read (First command)	→	Type 3 (normal end)	or	Type 3 (PE)	→	Type 3 (FR)
	Flash (Burst) Read (Second command)	→	Type 1	or	Type 3 (PE)		
8	Flash Write	→	Type 3 (normal end)	or	Type 3 (PE)	→	Type 3 (FW)
9	Flash All Erase	→	Type 3 (normal end)	or	Type 3 (PE)	→	Type 3 (FAE)
10	Baud rate correction	→	Zero data (0000_0000b)	or	Type 3 (PE)Note 4		
11-1	Send request (when ADSTART = 0)	→	Type 3, excluding PE	or	Type 3 (PE)		
11-2	Send request (when ADSTART = 1)	→	Type 2	or	Type 3 (PE)		
A/D conversion results (when ADSTART = 1) -No reception command is required since A/D conversion results are transmitted automatically.						→	Type 2

Notes 1. The type-3 (normal end) message indicates interrupt flag Fx = 0 (x = 0 to 4). (“00000111” in LSB first)

2. A type-3 (PE) response is transmitted if an error occurs during command reception or command execution. (A type-3 (PE) response = “00001111” in LSB first)

3. A deferred response is transmitted asynchronously when a flash memory access finished or the A/D conversion result is updated.

4. Four-bit zero data (“0000xxxx” in LSB first) always occurs, even if a command ends abnormally. Therefore, zero data (“00000000” in LSB first) that occurs when a command ends normally must be distinguished when adjusting the baud rate.

6.6 Note on Using the UART

Pay attention to the following point when using the UART.

<R> (1) Disabling the reception by the UART

The receiver of UART turns to be disabled under the condition both Non parity (PEN = 0) and low-level signal is input to the pin of MOSI_Rx for the period of the three times of character length or more. Once the receiver of UART becomes disabled, only power on reset by external power supply can make the receiver of UART enabled again.

The examples of condition which make the receiver of UART disabled are described below.

- After powered on, low-level signal continued to be input to the pin of MOSI_Rx for more than 5ms.

- After the baud rate of the RAA730101 is set to be 250kbps (RXBR = 1), the external device tries to communicate with the RAA730101 using the baud rate of 4.8kbps.

To avoid the unexpected situation that the receiver of UART is disabled, be sure to carry the operations as described below into effect.

1. Connect the pin of MOSI_Rx and the pin of MISO_Tx to IOV_{DD} via a resistor.

2. When the baud rate of the RAA730101 is set to be 250kbps (RXBR = 1), be sure to set the parity bit enabled (PEN = 1).

The parity bit enabled (PEN = 1) is recommended even if the baud rate of the RAA730101 is 4.8kbps (RXBR = 0). If you use the copy function from Register shadow of flash memory to register to set the baud rate 250kbps (RXBR = 1), you must set the parity bit enabled (PEN = 1) by the copy function, too. For details about the copy function from Register shadow of flash memory to register, see ***13. Flash Memory***.

<R> (2) Reading the ADSTART bit

While communications by the UART are in progress, and only then, the value of ADSTART bit cannot be read correctly. To check for the start of A/D conversion (whether writing to the ADSTART bit was successful or failed), check whether a type 3 normal end was returned as the instant response to the writing.
To check for the state of operation of the A/D converter (the value of the ADSTART bit), read the bit twice and treat the second value as the true value.

6.7 PWM direct input

In the RAA730101, the logic level of the NRZ signal can be set to high (= 1) or low (= 0) according to the duty ratio of the PWM signal. This feature assumes use in isolated communication. The PWM direct input feature is enabled by inputting a high level to the CS_B pin. The logic level of the NRZ signal becomes high (= 1) when the duty of the PWM signal is 75%, and becomes low (= 0) when the duty of the PWM signal is 25%.

Conventionally, an analog filter has been used to demodulate the PWM signal to the NRZ signal. In the RAA730101, a digital PWM filter is used to directly input PWM, instead of the analog filter.

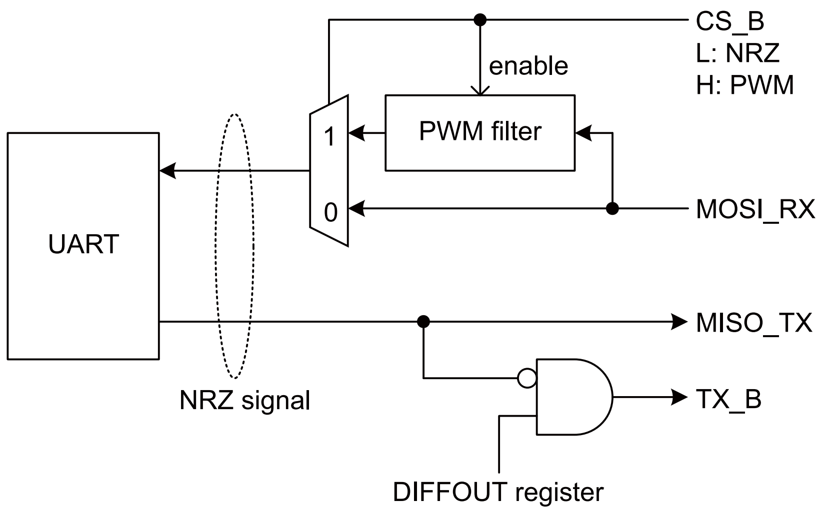


Figure 6.4 Special UART feature 1 - PWM direct input

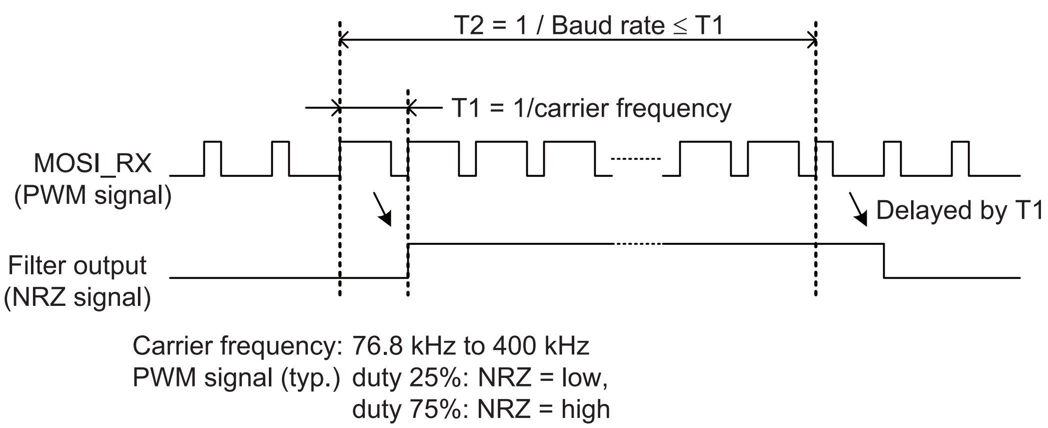


Figure 6.5 Timing of PWM filtering

6.8 Differential output

Differential output is used to enlarge the output amplitude and improve noise robustness. Differential output can be enabled by setting the DIFFOUT bit of the Clock/UART control register (UARTCNT). For details, see *6.2 Registers controlling UART communication*.

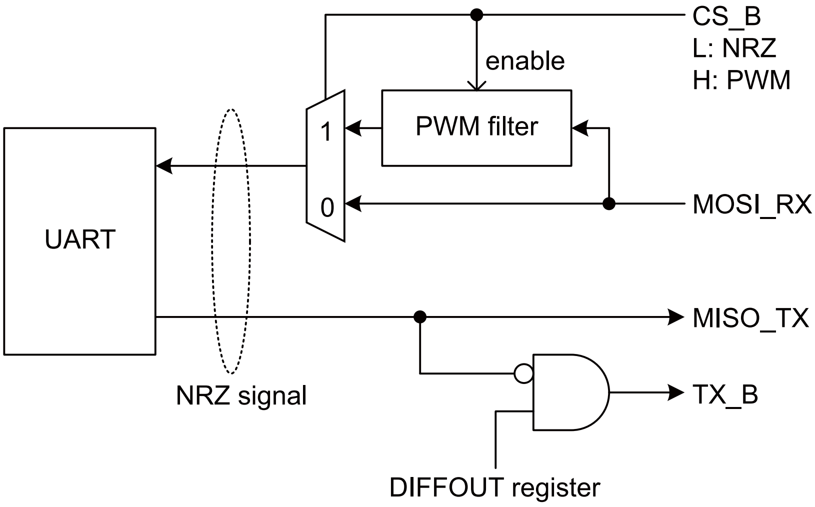


Figure 6.6 Special UART feature 2 - Differential output

7. Interrupt Signal Output Function (for SPI Communication)

7.1 Overview

The RAA730101 has an interrupt signal output function. This feature is available only when using SPI communication. The interrupt signal output function outputs a high level from the INT pin when A/D conversion or flash memory access finishes. By inputting this output signal to an external device connected to the RAA730101 as an interrupt (INT) signal, the status of A/D conversion or flash memory access can be reported to the external device. For details, see ***7.4 Operation of interrupt signal output function***.

7.2 Block diagram

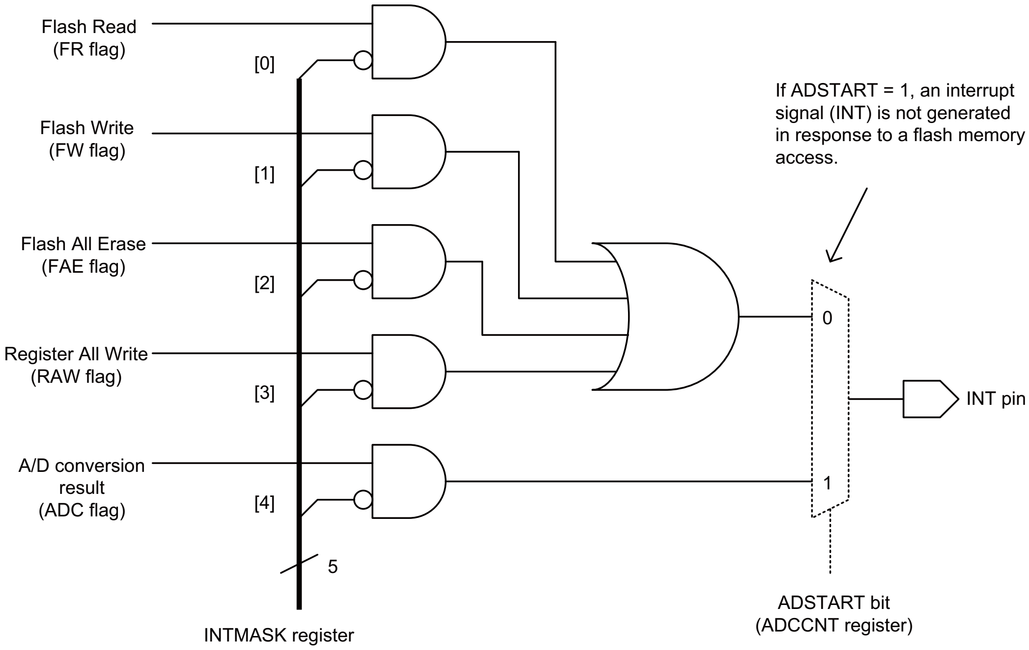


Figure 7.1 Structure of interrupt (INT) signal output function

7.3 Registers controlling the interrupt signal output function

The following three kinds of registers are used to control the interrupt signal output function.

- Interrupt mask setting register (INTMASK)
- Interrupt flag indication register (INTFLAG)
- Processing status indication register (STATUS)

(1) Interrupt mask setting register (INTMASK)
This register is used to enable or disable the output of interrupt signals.
After reset, this register is cleared to 00H.

Address: 04H After reset: 00H R/W

	7	6	5	4	3	2	1	0
INTMASK	0	0	0	MADC	MRAW	MFAE	MFW	MFR

MFR	Outputting an interrupt signal in response to Flash Read
0	Enable output of interrupts.
1	Disable output of interrupts. (Mask output of interrupts.)

MFW	Outputting an interrupt signal in response to Flash Write
0	Enable output of interrupts.
1	Disable output of interrupts. (Mask output of interrupts.)

MFAE	Outputting an interrupt signal in response to Flash All Erase
0	Enable output of interrupts.
1	Disable output of interrupts. (Mask output of interrupts.)

MRAW	Outputting an interrupt signal in response to Register All Write
0	Enable output of interrupts.
1	Disable output of interrupts. (Mask output of interrupts.)

MADC	Outputting an interrupt signal in response to A/D conversion
0	Enable output of interrupts.
1	Disable output of interrupts. (Mask output of interrupts.)

Caution Bits 7 to 5 are read-only. (When these bits are read, 0 is always returned.)

(2) Interrupt flag indication register (INTFLAG)

This is a flag register that indicates whether an interrupt signal is ready to be output.
After reset, this register is cleared to 00H.

Address: 05H After reset: 00H R/–

	7	6	5	4	3	2	1	0
INTFLAG	0	0	0	ADC	RAW	FAE	FW	FR

FR	Interrupt flag indication for Flash Read
0	Output is not ready
1	Output is ready

FW	Interrupt flag indication for Flash Write
0	Output is not ready
1	Output is ready

FAE	Interrupt flag indication for Flash All Erase
0	Output is not ready
1	Output is ready

RAW	Interrupt flag indication for Register All Write
0	Output is not ready
1	Output is ready

ADC	Interrupt flag indication for A/D conversion
0	Output is not ready
1	Output is ready

Caution When bits 7 to 5 are read, 0 is always returned.

(3) Processing status indication register (STATUS)

This register indicates the processing status of Flash Write, Flash ALL Erase, Register All Write, and A/D conversion. After reset, this register is cleared to 00H.

Address: 06H After reset: 00H R/–

	7	6	5	4	3	2	1	0
STATUS	0	0	0	ADCIP	RAWIP	FAEIP	FWIP	0

FWIP	Flash Write processing status
0	Processing finished
1	Processing in progress

FAEIP	Flash All Erase processing status
0	Processing finished
1	Processing in progress

RAWIP	Register All Write processing status
0	Processing finished
1	Processing in progress

ADCIP	A/D conversion processing status
0	Processing finished
1	Processing in progress

Caution When bits 7 to 5 and 0 are read, 0 is always returned.

7.4 Operation of interrupt signal output function

When any of the commands Flash Write, Flash ALL Erase, and Register All Write, or a command that triggers A/D conversion is executed by using SPI communication, the corresponding bit in the processing status indication register (STATUS) is set to 1. When the above processing has finished, the corresponding bit in the processing status indication register (STATUS) is cleared to 0. At this time, the corresponding bit in the interrupt flag indication register (INTFLAG) is set to 1, and a high-level interrupt (INT) signal is output from the INT pin. When the interrupt flag indication register (INTFLAG) is read, it is cleared to 0, and the output of the INT pin goes low.

When the first command of Flash Read is executed, the corresponding bit in the interrupt flag indication register (INTFLAG) is set to 1, and a high-level interrupt (INT) signal is output from the INT pin. When the second command of Flash Read is executed, the interrupt flag indication register (INTFLAG) is cleared to 0, and the output of the INT pin goes low.

The interrupt mask setting register (INTMASK) controls the high-level interrupt (INT) signal output from the INT pin. (See Figure *7.1 Structure of interrupt signal output function*.) If operation of Flash Read, Flash Write, Flash ALL Erase, Register All Write, or A/D conversion is masked by using the interrupt mask setting register (INTMASK), a high-level interrupt (INT) signal is not output even when the operation has finished. Outputting an interrupt (INT) signal for A/D conversion and an accessing to the flash memory is exclusive. If the ADSTART bit of the A/D converter control register (ADCCNT) is set to 1, an interrupt (INT) signal for a flash memory access is not output. (For details, see ***4.3 Registers controlling the 16-bit ΔΣ A/D converter***.)

Like SPI communication, the RAW flag is also set when the Buffer Refresh command (see No. 6 in the table *UART commands*) is executed. When the Buffer Refresh command is executed and its processing has finished, the corresponding bit in the interrupt flag indication register (INTFLAG) is set to 1, and a high-level interrupt (INT) signal is output from the INT pin.

Instead of using the INT pin, you can check the status of A/D conversion or an accessing to the flash memory by constantly monitoring the processing status indication register (STATUS).

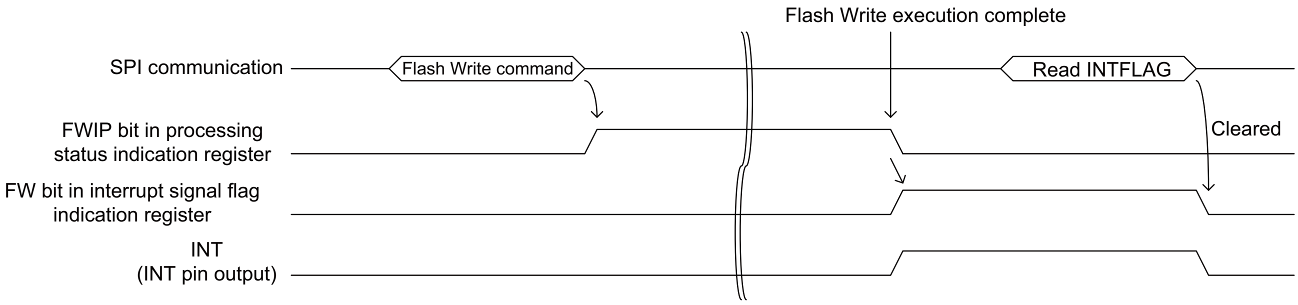


Figure 7.2 Interrupt signal (INT) output timing (for Flash Write command)

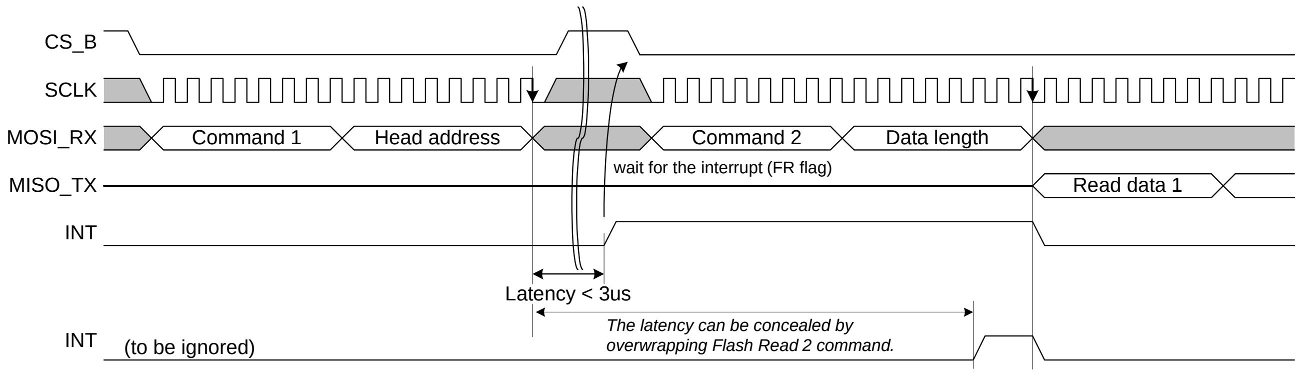


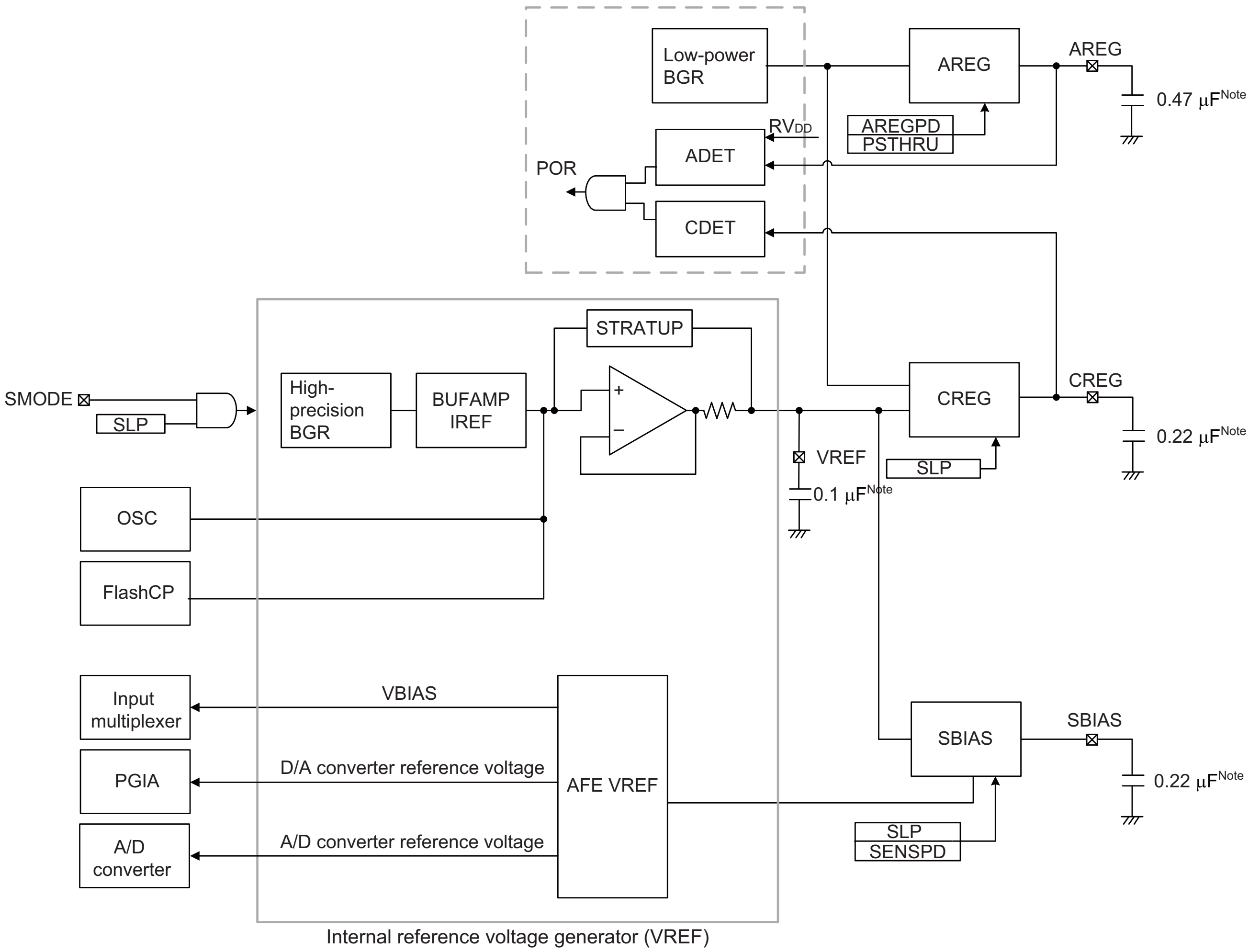
Figure 7.3 Interrupt signal (INT) output timing (for Flash (Burst) Read command)

8. Power Supply Circuit

8.1 Overview

The RAA730101 has a power supply circuit for supplying power to internal circuits and external devices. The power supply circuit consists of a 2-channel bandgap reference circuit (high-precision BGR and low-power BGR), 2-channel LDO regulator (AREG and CREG), and a sensor (external device) power supply (SBIAS). For details about the power supply configuration, see ***9. Power Supply Configuration***.

8.2 Block diagram of power supply circuit



Note Capacitance values are recommended values.

Figure 8.1 Block diagram of power supply circuit

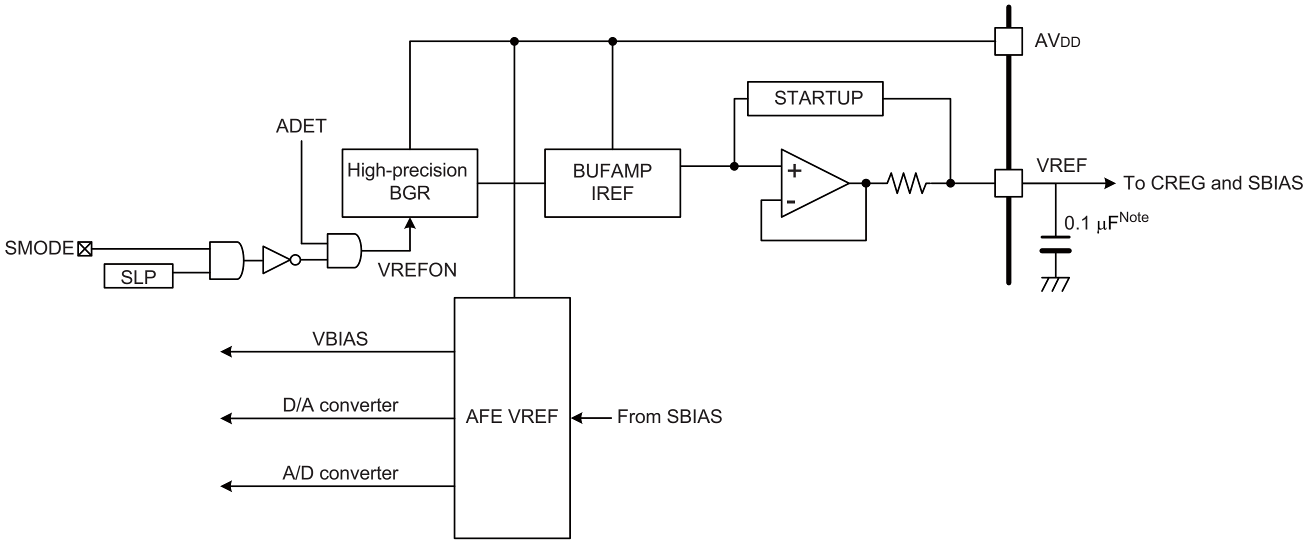
8.3 Internal reference voltage generator (VREF)

8.3.1 Overview

The internal reference voltage generator (VREF) consists of a high-precision BGR and an analog circuit reference voltage generator (AFE VREF). VREF generates a reference voltage for CREG and SBIAS based on the voltage output from the high-precision BGR. The voltage output from the high-precision BGR passes through SBIAS and AFE VREF, and is then used as a reference voltage in the A/D converter and D/A converter, and as an internal bias voltage (VBIAS) to be connected to input multiplexers. The high-precision BGR can achieve high precision in the output voltage because it is less dependent on the temperature.

By connecting an external capacitor of 0.1 μF (recommended) to the VREF pin, the internal reference voltage generator (VREF) is equipped with a low-pass filter that consists of an on-chip resistor and this external capacitor.

8.3.2 Block diagram



Note Capacitance values are recommended values.

Figure 8.2 Block diagram of internal reference voltage generator (VREF)

8.3.3 Registers controlling the internal reference voltage generator (VREF)

The following register is used to control the internal reference voltage generator (VREF).

- Power/mode control register (CHIPCNT)

(1) Power/mode control register (CHIPCNT)

This register is used to set the internal reference voltage generator (VREF) to normal operation or sleep mode.

After reset, this register is cleared to 00H.

For details, see ***8.3.4 Operation of internal reference voltage generator (VREF)***.

Address: 01H After reset: 00H R/W

	7	6	5	4	3	2	1	0
CHIPCNT	0	0	PSTHRU	AREGPD	0	0	SENSPD	SLP

SLP	Control of sleep mode
0	Normal operation
1	Sleep mode

Caution Bits 7, 6, 3, and 2 are read-only. (When these bits are read, 0 is always returned.)

8.3.4 Operation of internal reference voltage generator (VREF)

The SLP bit of the power/mode control register (CHIPCNT) sets the high-precision BGR to sleep mode. To shift to sleep mode, the result of logical operations using data of the SLP bit and data input to the SMODE pin is used. When "1" is written to the SLP bit of the power/mode control register (CHIPCNT) during SPI communication (SMODE = 1), the high-precision BGR shifts to sleep mode and stops operating. During UART communication (SMODE = 0), on the other hand, the high-precision BGR is in normal operating mode.

When SBIAS stops operating, AFE VREF also stops operating even if the high-precision BGR operates normally. As a result, a reference voltage in the A/D converter and D/A converter, and an internal bias voltage (VBIAS) to be connected to input multiplexers, are not generated. For details about SBIAS, see ***8.4 Sensor power supply (SBIAS)***.

8.4 Sensor power supply (SBIAS)

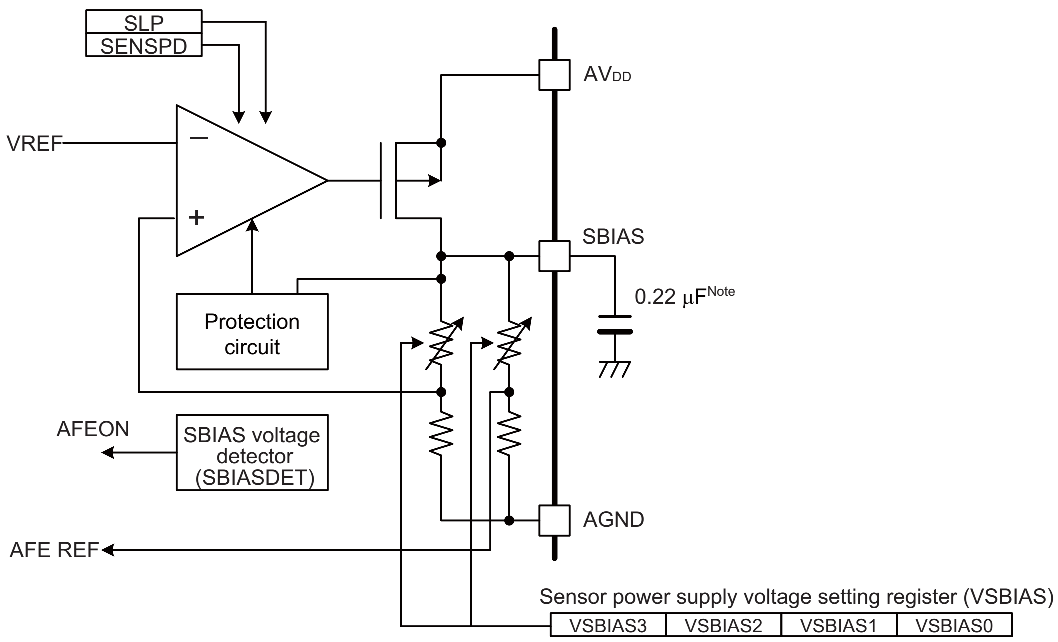
8.4.1 Overview

SBIAS supplies power to the sensor connected to the RAA730101. A reference voltage is input from VREF. SBIAS outputs a voltage between 1.2 and 2.2 V, which can be specified in units of 0.1 V. Output current of 5 mA or less can be provided. An external capacitor of 0.22 µF (recommended) must be connected to the SBIAS pin.

SBIAS has a protection circuit against an overcurrent. When an overcurrent occurs, the protection circuit works to protect the internal circuits. SBIAS also has a circuit that monitors and detects the voltage output by SBIAS.

The reference voltage output from VREF passes through SBIAS and is then used as a reference voltage in the A/D converter and D/A converter, and as an internal bias voltage (VBIAS) to be connected to input multiplexers. For details, see ***8.4.4 Operation of sensor power supply (SBIAS)***.

8.4.2 Block diagram



Note Capacitance values are recommended values

Figure 8.3 Block diagram of sensor power supply (SBIAS)

8.4.3 Registers controlling the sensor power supply (SBIAS)

The following two kinds of registers are used to control the sensor power supply (SBIAS).

- Power/mode control register (CHIPCNT)
- Sensor power supply voltage setting register (VSBIAS)

(1) Power/mode control register (CHIPCNT)

This register is used to set the sensor power supply (SBIAS) to normal operation or sleep mode, or stop the operation.
After reset, this register is cleared to 00H.
For details, see ***8.4.4 Operation of sensor power supply (SBIAS)***.

Address: 01H After reset: 00H R/W

	7	6	5	4	3	2	1	0
CHIPCNT	0	0	PSTHRU	AREGPD	0	0	SENSPD	SLP

SLP	Control of sleep mode
0	Normal operation
1	Sleep mode

SENSPD	Control of SBIAS operation
0	Normal operation
1	Stops operation.

Caution Bits 7, 6, 3, and 2 are read-only. (When these bits are read, 0 is always returned.)

(2) Sensor power supply voltage setting register (VSBIAS)

This register is used to specify the SBIAS output voltage. After reset, this register is cleared to 00H.

Address: 02H After reset: 00H R/W

	7	6	5	4	3	2	1	0
VSBIAS	0	0	0	0	VSBIAS3	VSBIAS2	VSBIAS1	VSBIAS0

VSBIAS3	VSBIAS2	VSBIAS1	VSBIAS0	Voltage output from sensor power supply (SBIAS) (in V)
0	0	0	0	1.2
0	0	0	1	1.3
0	0	1	0	1.4
0	0	1	1	1.5
0	1	0	0	1.6
0	1	0	1	1.7
0	1	1	0	1.8
0	1	1	1	1.9
1	0	0	0	2.0
1	0	0	1	2.1
1	0	1	0	2.2
Other than above				Setting prohibited

Caution Bits 7, 6, 5, and 4 are read-only. (When these bits are read, 0 is always returned.)

8.4.4 Operation of sensor power supply (SBIAS)

In addition to supplying power to the sensor connected to the RAA730101, SBIAS is involved in generating reference voltages used in analog circuits, such as the reference voltage used in the A/D converter and D/A converter and an internal bias voltage (VBIAS) to be connected to input multiplexers.

SBIAS has a circuit that monitors and detects the voltage output by SBIAS (SBIASDET), and is used to start analog circuits such as AFE VREF, programmable gain instrumentation amplifier (PGIA), and A/D converter. When SBIASDET detects the SBIAS output voltage, SBIASDET is released, which enables analog circuits to start operating. When SBIASDET detects that the SBIAS output voltage has not risen normally, analog circuits stop operating.

When "1" is written to the SLP bit of the power/mode control register (CHIPCNT), SBIAS shifts to sleep mode and stops operating. When "1" is written to the SENSPD bit of the power/mode control register (CHIPCNT), SBIAS stops operating. In both cases, SBIASDET detects the SBIAS output voltage and analog circuits such as AFE VREF, PGIA, and A/D converter stop operating. When AFE VREF stops operating, a reference voltage in the A/D converter and D/A converter and an internal bias voltage (VBIAS) to be connected to input multiplexers are not generated.

8.5 LDO regulator

The LDO regulator consists of AREG (AV_{DD}/IOV_{DD} power supply circuit) and CREG (ADV_{DD}/DV_{DD} power supply circuit). For how to use AREG and CREG, see ***9. Power Supply Configuration***.

8.5.1 AREG (AV_{DD}/IOV_{DD} power supply circuit)

8.5.1.1 Overview

AREG generates a voltage based on the voltage output from the low-power BGR, and supplies power to AV_{DD} and IOV_{DD}. Output voltage is 3.0 V (Typ.). Output current of 50 mA or less can be provided. An external capacitor of 0.47 µF (recommended) must be connected to the AREG output pin.

AREG has a protection circuit against an overcurrent and a low output voltage detector (ADET). For details about the AREG operation, see ***8.5.1.4 Operation of AREG (AV_{DD}/IOV_{DD} power supply circuit)***.

8.5.1.2 Block diagram

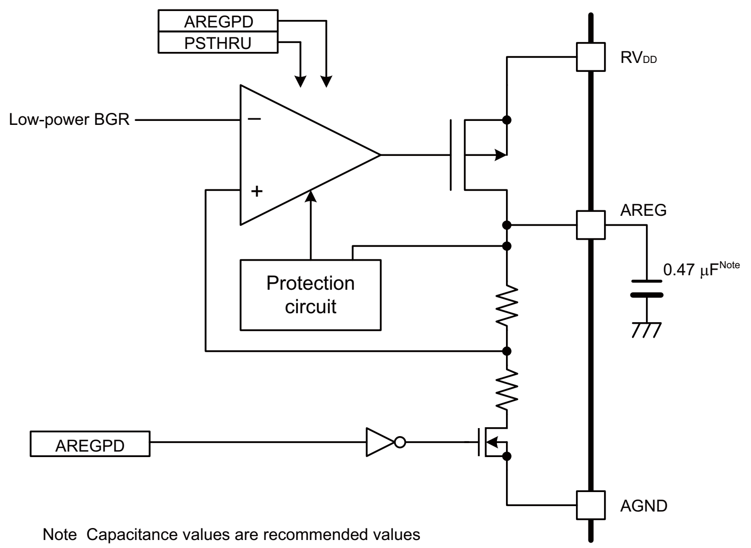


Figure 8.4 Block diagram of AREG

8.5.1.3 Registers controlling AREG (AV_{DD}/IOV_{DD} power supply circuit)

The following register is used to control AREG (AV_{DD}/IOV_{DD} power supply circuit).

- Power/mode control register (CHIPCNT)

(1) Power/mode control register (CHIPCNT)

This register is used to set AREG to normal operation or sleep mode, and controls the output status.
After reset, this register is cleared to 00H.
For details, see ***8.5.1.4 Operation of AREG (AV_{DD}/IOV_{DD} power supply circuit)***.

Address: 01H After reset: 00H R/W

	7	6	5	4	3	2	1	0
CHIPCNT	0	0	PSTHRU	AREGPD	0	0	SENSPD	SLP

PSTHRU	AREGPD	AREG operating status	Voltage output from AREG pin
0	0	Normal operation	3.0 V
1	0	Operation stops.	RV_{DD}
*	1	Operation stops.	Hi-Z

Caution Bits 7, 6, 3, and 2 are read-only. (When these bits are read, 0 is always returned.)

Remark * ; don't care

8.5.1.4 Operation of AREG (AV_{DD}/IOV_{DD} power supply circuit)

The AREGPD and PSTHRU bits of the power/mode control register (CHIPCNT) are used to set AREG to normal operation or sleep mode, and controls the output status.

AREG can be stopped and its output made invalid (high impedance) by writing "1" to the AREGPD bit after AREG starts operating normally. In this case, the AREG and RV_{DD} pins must be connected externally so that oscillation does not start. In addition, power must be supplied to RV_{DD}, AV_{DD}, and IOV_{DD} externally. For details, see ***9. Power Supply Configuration***.

When "1" is written to the PSTHRU bit, AREG stops operating and the output from AREG is bypassed to RV_{DD} inside the circuit. This bypass feature can be used when a voltage of 3.0 V or higher needs to be supplied to IOV_{DD} during flash memory programming. For details, see ***9. Power Supply Configuration***.

For details about the low output voltage detector (ADET), see ***12. Power-on-Reset (POR) Circuit***.

Caution Flash memory programming refers to erasing or writing of data in the flash memory.

8.5.2 CREG (ADV_{DD}/DV_{DD} power supply circuit)

8.5.2.1 Overview

CREG generates a voltage based on the voltage output from the high-precision BGR, and supplies power to ADV_{DD} and DV_{DD}. Output voltage is 2.1 V (Typ.). Output current of 20 mA or less can be provided. An external capacitor of 0.22 μF (recommended) must be connected to the CREG output pin.

CREG has a protection circuit against an overcurrent and a low output voltage detector (CDET). For details about the CREG operation, see ***8.5.2.4 Operation of CREG (ADV_{DD}/DV_{DD} power supply circuit)***.

8.5.2.2 Block diagram

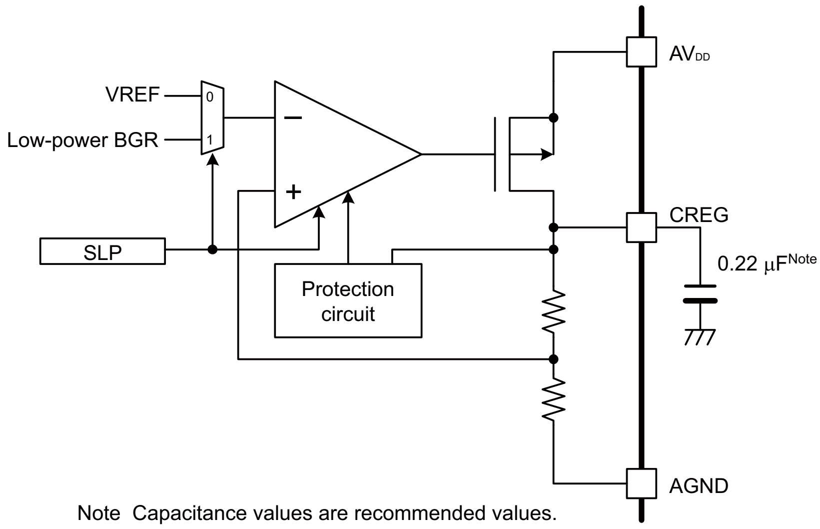


Figure 8.5 Block diagram of CREG

8.5.2.3 Registers controlling CREG (ADV_{DD}/DV_{DD} power supply circuit)

The following register is used to control CREG (ADV_{DD}/DV_{DD} power supply circuit).

- Power/mode control register (CHIPCNT)

(1) Power/mode control register (CHIPCNT)

This register is used to set CREG to normal operation or sleep mode.
After reset, this register is cleared to 00H.
For details, see ***8.5.2.4 Operation of CREG (ADV_{DD}/DV_{DD} power supply circuit)***.

Address: 01H After reset: 00H R/W

	7	6	5	4	3	2	1	0
CHIPCNT	0	0	PSTHRU	AREGPD	0	0	SENSPD	SLP

SLP	Control of sleep mode
0	Normal operation
1	Sleep mode

Caution Bits 7, 6, 3, and 2 are read-only. (When these bits are read, 0 is always returned.)

8.5.2.4 Operation of CREG (ADV_{DD}/DV_{DD} power supply circuit)

The SLP bit of the power/mode control register (CHIPCNT) sets CREG to sleep mode. When "1" is written to the SLP bit of the power/mode control register (CHIPCNT), CREG shifts to sleep mode and enters the standby state. In the standby state, CREG operates at low power and outputs a current of 2 mA or less. The reference voltage source is switched from the high-precision BGR to the low-power BGR. Even in this state, power is supplied to the protection circuit and the low output voltage detector (CDET).

For details about the low output voltage detector (CDET), see ***12. Power-on-Reset (POR) Circuit***.

8.5.3 LDO regulator operation in sleep mode

How the LDO regulator operates in sleep mode differs depending on which of the SPI communication and UART communication is selected.

When "1" is written to the SLP bit of the power/mode control register (CHIPCNT) during SPI communication (SMODE = 1), the power supply circuits other than the low-power BGR, AREG, and CREG stop operating. When "1" is written to the SLP bit of the power/mode control register (CHIPCNT) during UART communication (SMODE = 0), the high-precision BGR, in addition to the low-power BGR, AREG, and CREG, can operate. The high-precision BGR operates during UART communication (SMODE = 0) so as to operate the internal system clock (OSC) oscillator.

In sleep mode, CREG is in standby mode (operates at low power) during SPI communication (SMODE = 1) and UART communication (SMODE = 0), whichever is selected.

9. Power Supply Configuration

9.1 Overview

The RA730101 can use the three power supply configurations shown below.

Configuration 1: External power supply (3.3 V to 5.5 V) = RV_{DD} = IOV_{DD}, AREG = AV_{DD}, CREG = ADV_{DD} = DV_{DD}

Configuration 2: External power supply (3.3 V to 5.5 V) = RV_{DD}, AREG = AV_{DD} = IOV_{DD}, CREG = ADV_{DD} = DV_{DD}

Configuration 3: External power supply (2.7 V to 3.6 V) = RV_{DD} = AV_{DD} = IOV_{DD}, AREG disabled (AREGPD = 1), CREG = ADV_{DD} = DV_{DD}

Table 9.1 shows the power supply configurations. For details, see ***9.2 Block diagrams of power supply configurations***.

Table 9.1 Overview of power supply configuration

Settings specified in:	External power supply is connected to: (External power supply voltage)	AREG is connected to: (AREG = 3.0 V)	CREG is connected to: (CREG = 2.1 V)	See:
Configuration 1	RV_{DD}, IOV_{DD} (3.3 to 5.5 V)	AV_{DD}	ADV_{DD}, DV_{DD}	Figure 9.1
Configuration 2	RV_{DD} (3.3 to 5.5 V)	AV_{DD}, IOV_{DD}	ADV_{DD}, DV_{DD}	Figure 9.2
Configuration 3	RV_{DD}, AV_{DD}, IOV_{DD} (2.7 to 3.6 V)	RV_{DD} (AREGPD = 1: Output disabled)	ADV_{DD}, DV_{DD}	Figure 9.3

Caution The power supply voltage range of IOV_{DD} determines the range of the input and output voltages used for serial communication.

During flash memory programming, 5 V (Typ.) must be supplied to IOV_{DD}. To perform flash memory programming in any of the above power supply configurations, the settings need to be changed as shown in Table 9.2. For details, see ***9.4 Settings for flash programming***.

Table 9.2 Overview of power supply configuration (for flash memory programming)

Settings specified in:	External power supply is connected to: (External power supply voltage)	AREG is connected to: (AREG = 3.0 V)	CREG is connected to: (CREG = 2.1 V)	See:
Configuration 1	RV_{DD}, IOV_{DD} (**4.5** to **5.5 V**)	AV_{DD}	ADV_{DD}, DV_{DD}	-
Configuration 2	RV_{DD} (**4.6** to **5.5 V**)	AV_{DD}, IOV_{DD} (**PSTHRU = 1: AREG stops operating and the AREG output is bypassed to RVDD.)**	ADV_{DD}, DV_{DD}	-
Configuration 3	RV_{DD}, AV_{DD}, IOV_{DD} (**4.5** to **5.5 V**)	RV_{DD} (AREGPD = 1: AREG stopped)	ADV_{DD}, DV_{DD}	-

Cautions 1. Flash memory programming refers to erasing or writing of data in the flash memory.

2. The power supply voltage range of IOV_{DD} determines the range of the input and output voltages used for serial communication.

9.2 Block diagrams of power supply configurations

Configuration 1: External power supply (3.3 V to 5.5 V) = RV_{DD} = IOV_{DD}, AREG = AV_{DD}, CREG = ADV_{DD} = DV_{DD}

- Supply 3.3 V to 5.5 V from an external power source to RV_{DD} and IOV_{DD}. (Short RV_{DD} and IOV_{DD} externally.)
- Supply AV_{DD} from AREG (3.0 V).
- Supply ADV_{DD} and DV_{DD} from CREG (2.1 V).

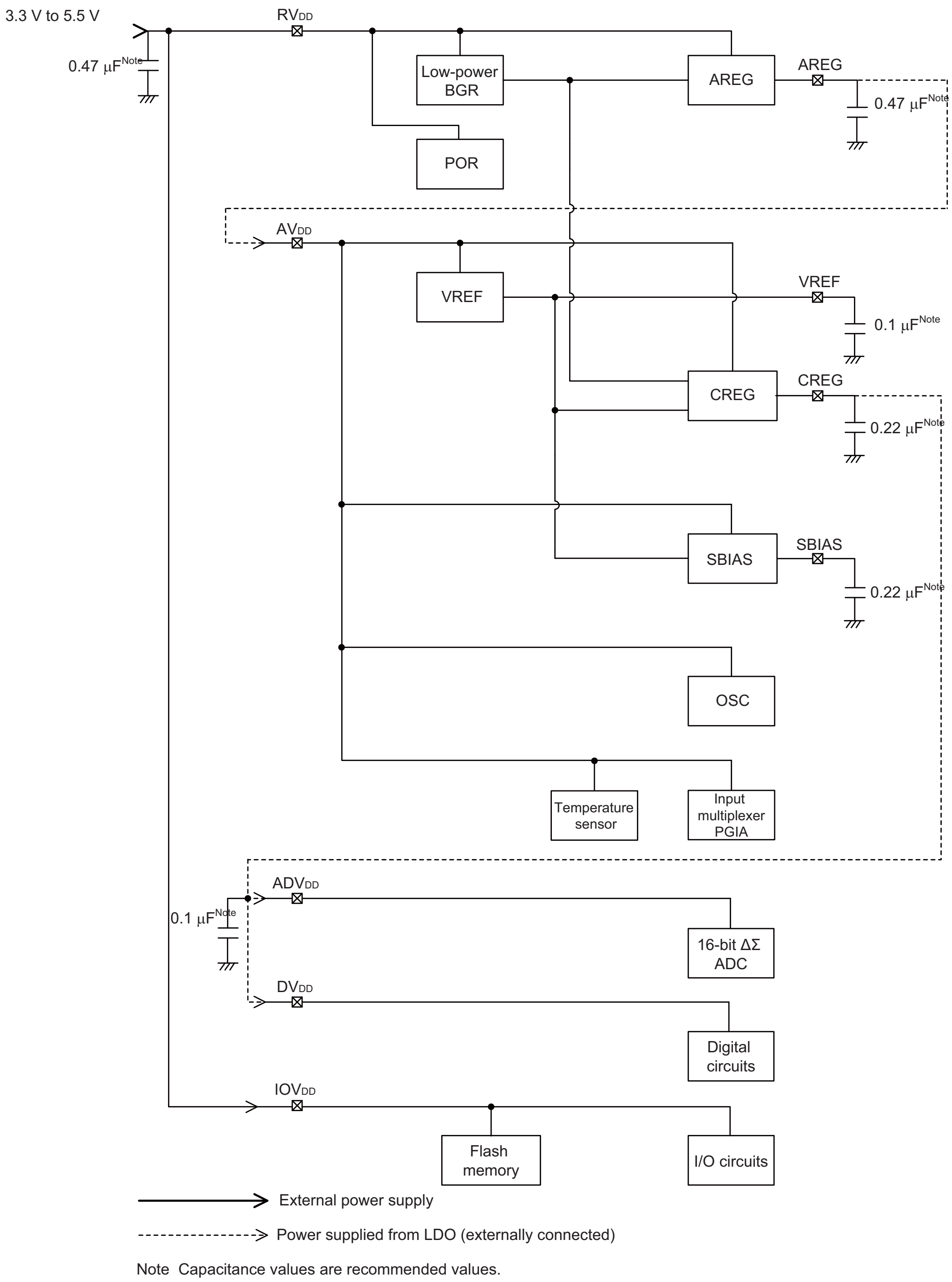


Figure 9.1 Block diagram of power supply configuration 1

Configuration 2: External power supply (3.3 V to 5.5 V) = RV_{DD}, AREG = AV_{DD} = IOV_{DD}, CREG = ADV_{DD} = DV_{DD}

- Supply 3.3 V to 5.5 V from an external power source to RV_{DD}.
- Supply AV_{DD} and IOV_{DD} from AREG (3.0 V).
- Supply ADV_{DD} and DV_{DD} from CREG (2.1 V).

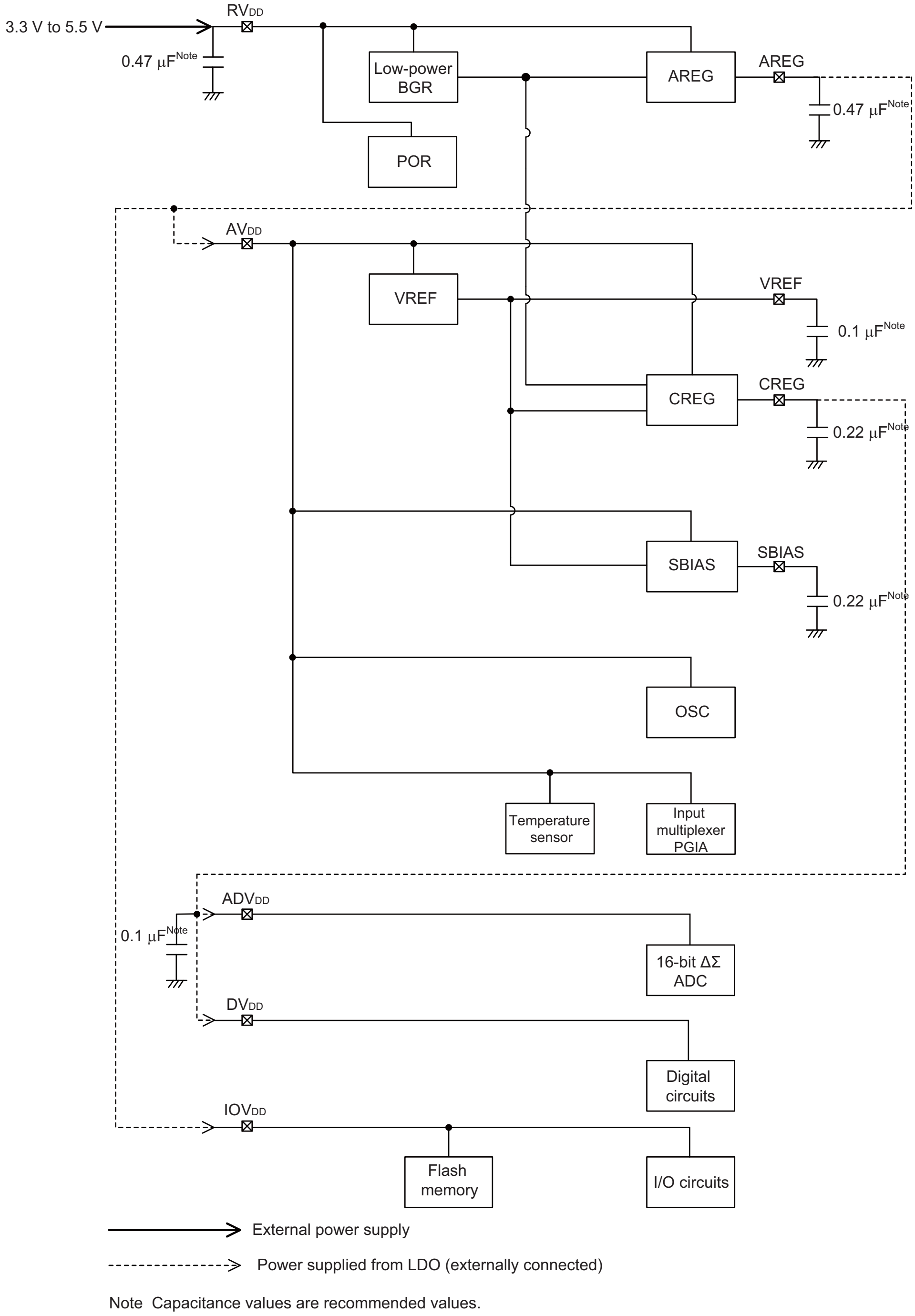


Figure 9.2 Block diagram of power supply configuration 2

Configuration 3: External power supply (2.7 V to 3.6 V) = RV_{DD} = AV_{DD} = IOV_{DD}, AREG disabled (AREGPD = 1), CREG = ADV_{DD} = DV_{DD}

- Supply 2.7 V to 3.6 V from an external power source to RV_{DD}, AV_{DD}, and IOV_{DD}. (Short RV_{DD}, AV_{DD}, and IOV_{DD} externally.)
- Set the AREGPD bit to 1 after circuits start operating normally. (Short AREG and RV_{DD} externally.)
- Supply ADV_{DD} and DV_{DD} from CREG (2.1 V).

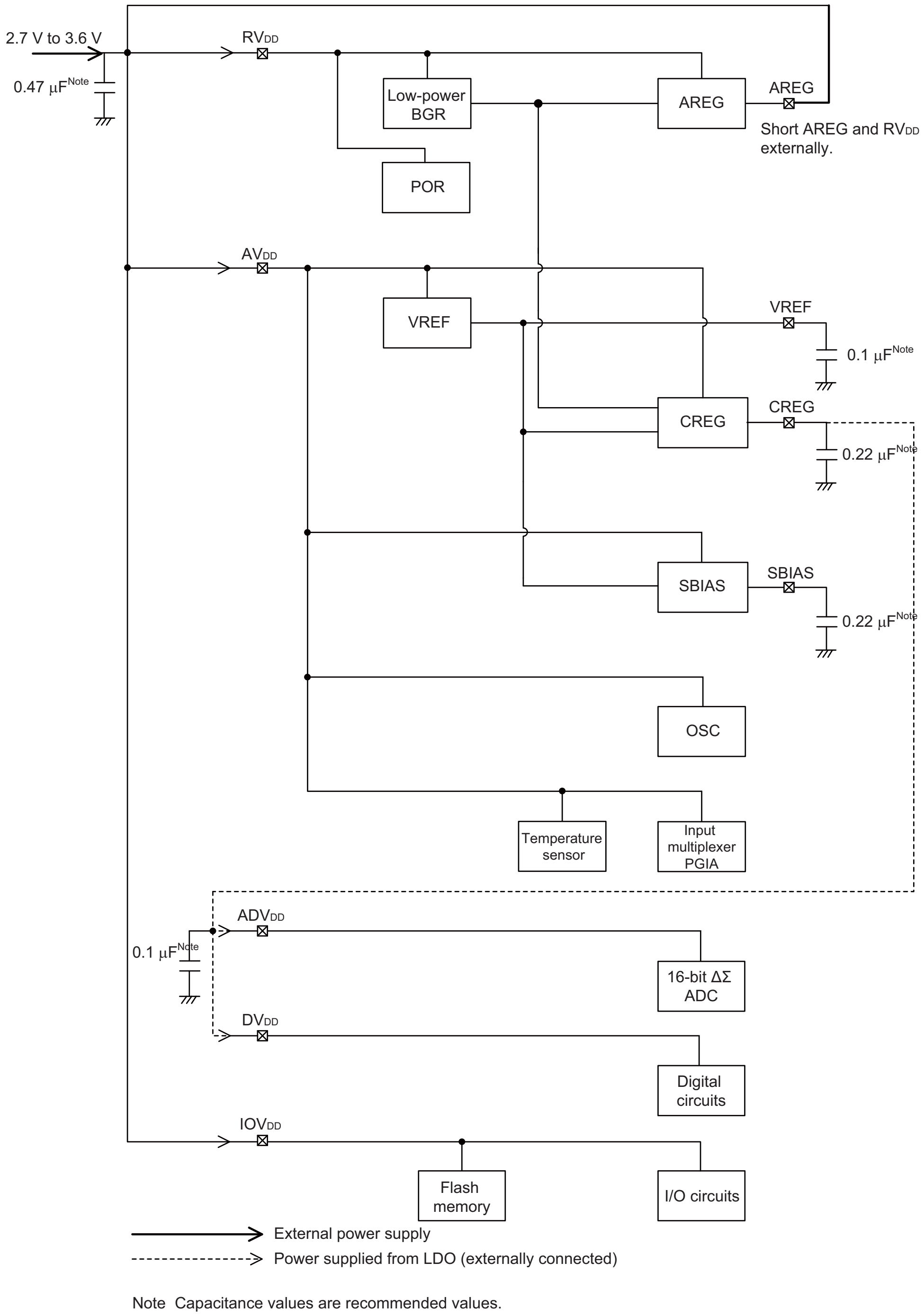


Figure 9.3 Block diagram of power supply configuration 3

9.3 Sequence of power-on, power-off, and switching to standby mode

Figures 9.4 to 9.7 show the timing at which to power on, power off, and switch to standby mode.

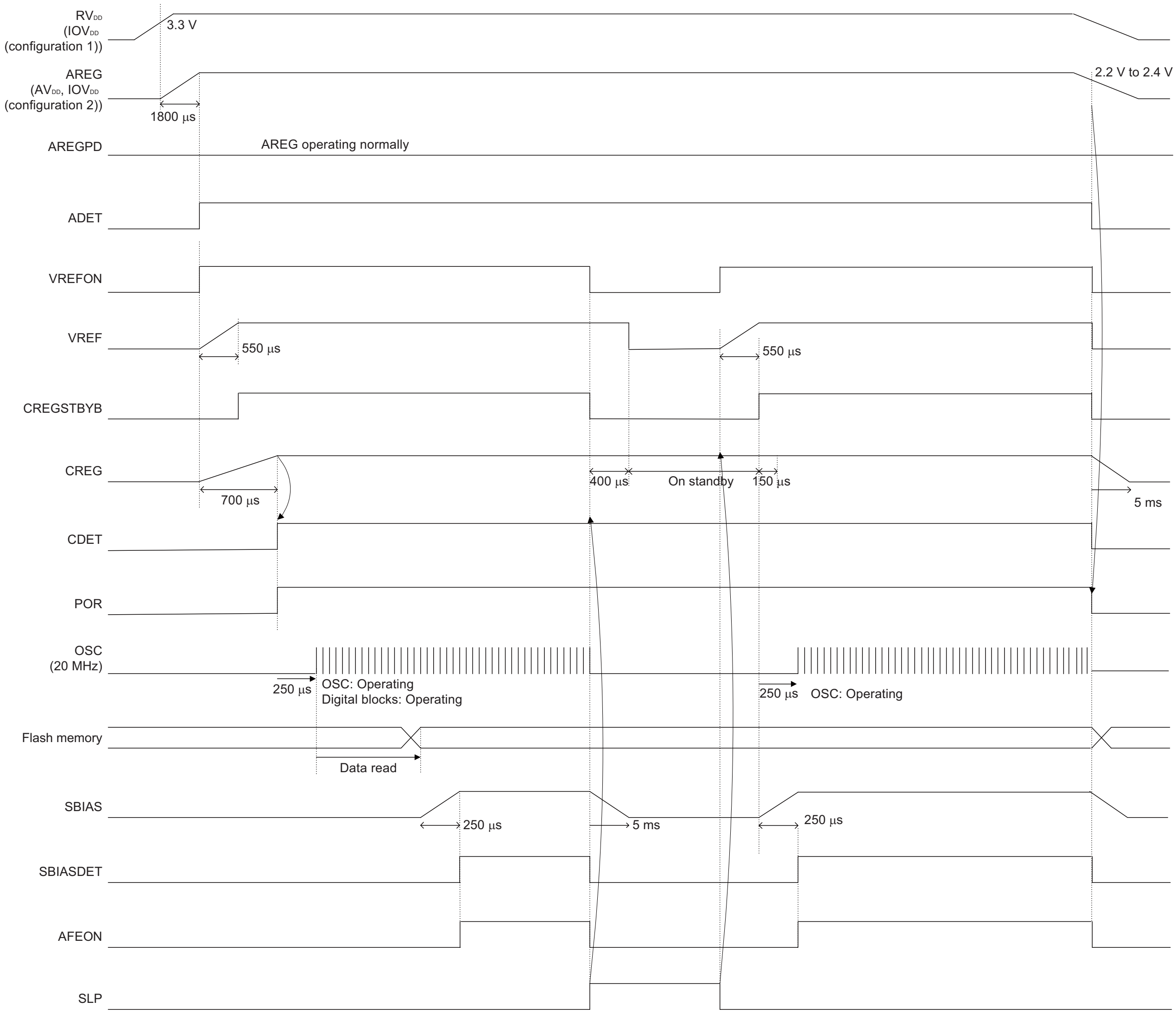


Figure 9.4 Timing chart 1 (for configurations 1 and 2, during SPI communication (SMODE = 1))

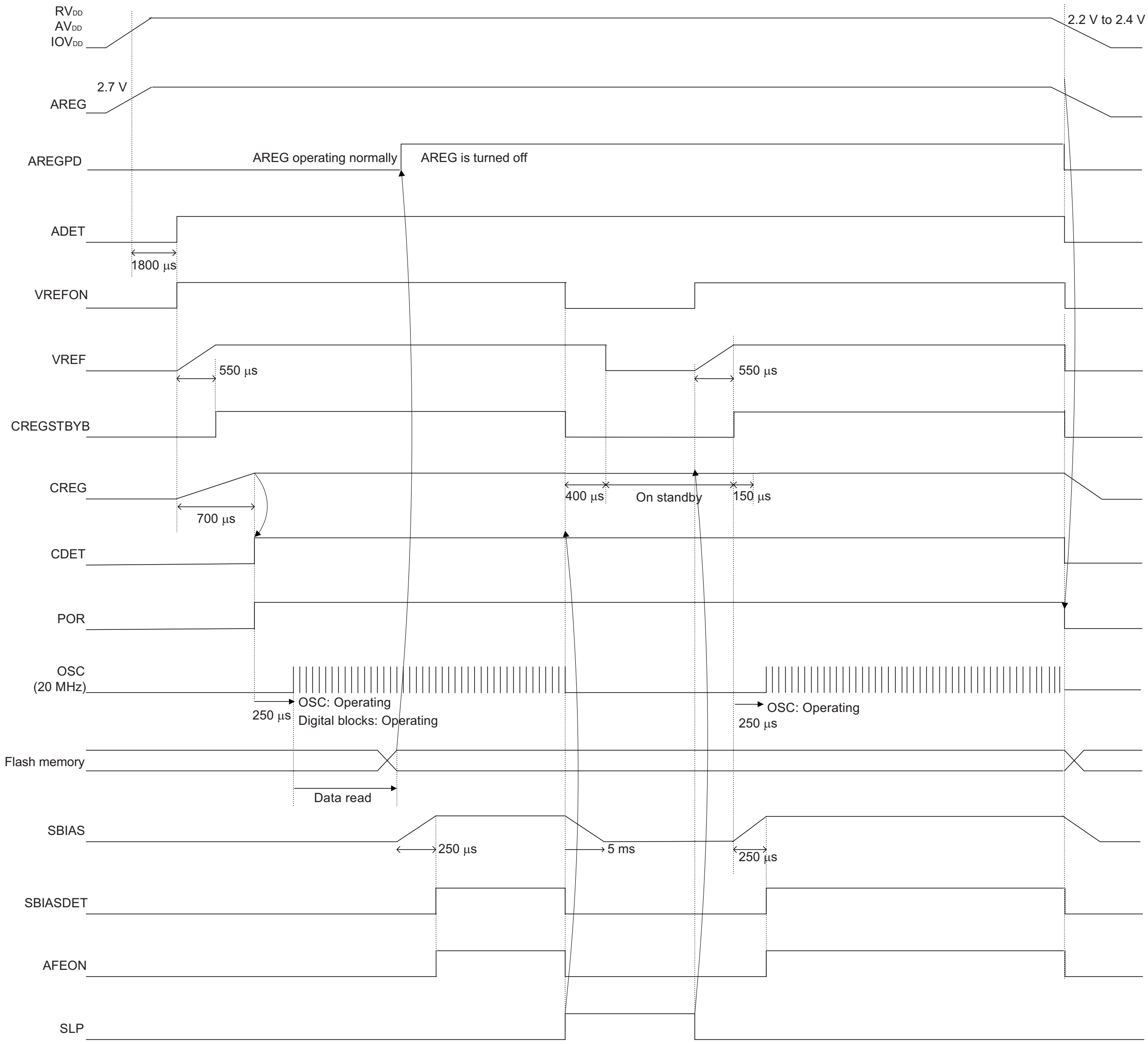


Figure 9.5 Timing chart 2 (for configuration 3, during SPI communication (SMODE = 1))

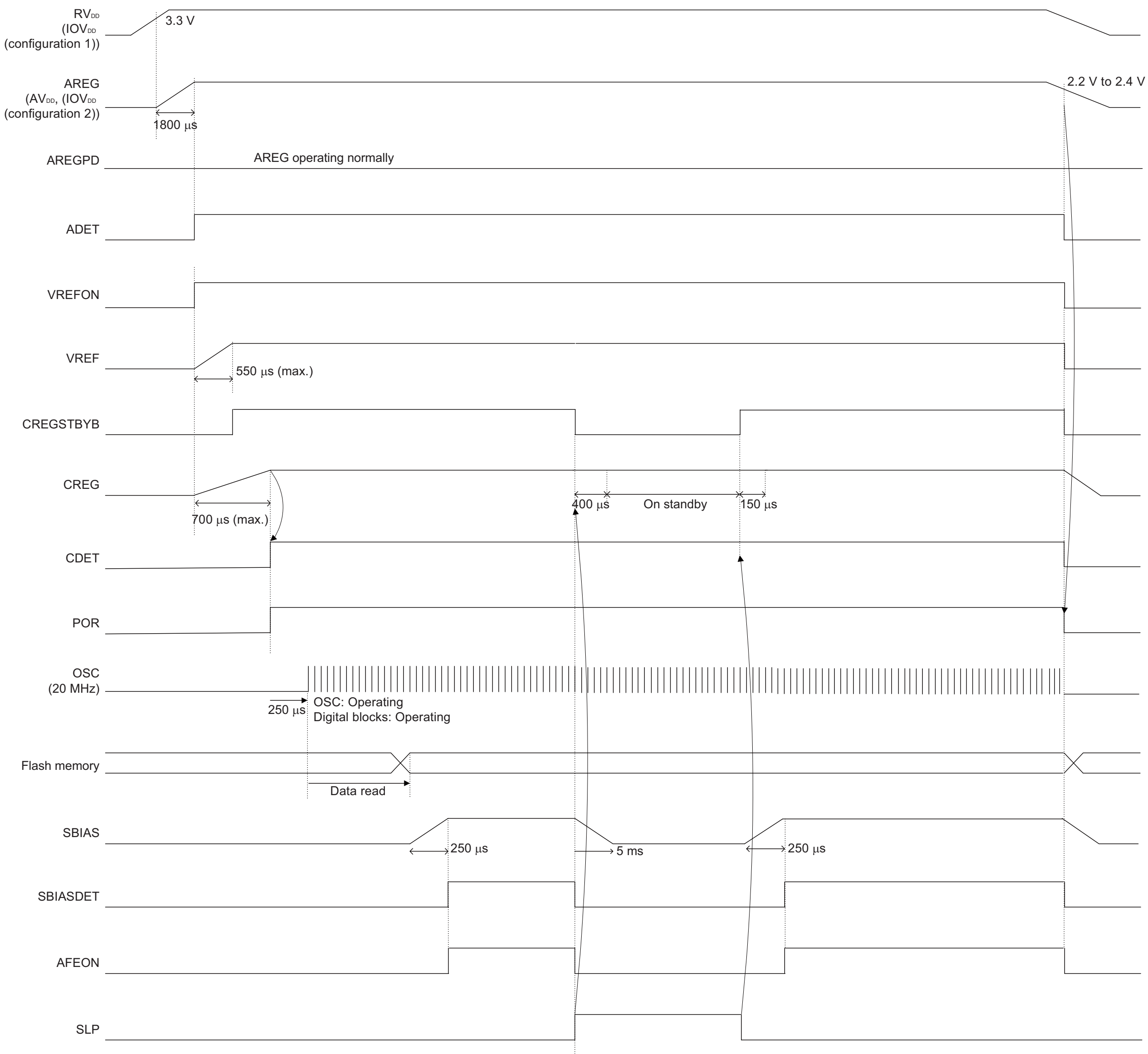


Figure 9.6 Timing chart 3 (for configurations 1 and 2, during UART communication (SMODE = 0))

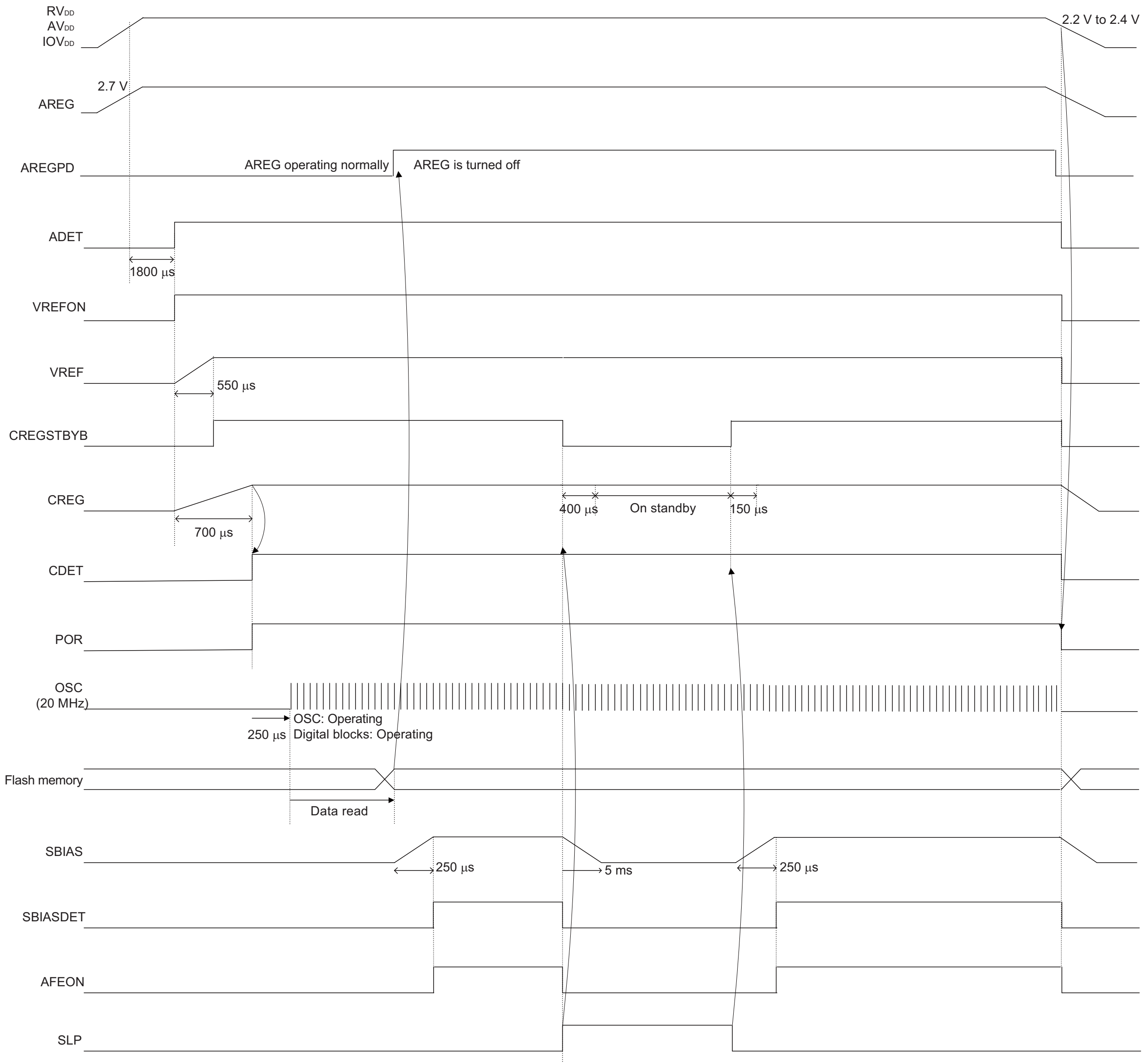


Figure 9.7 Timing chart 4 (for configuration 3, during UART communication (SMODE = 0))

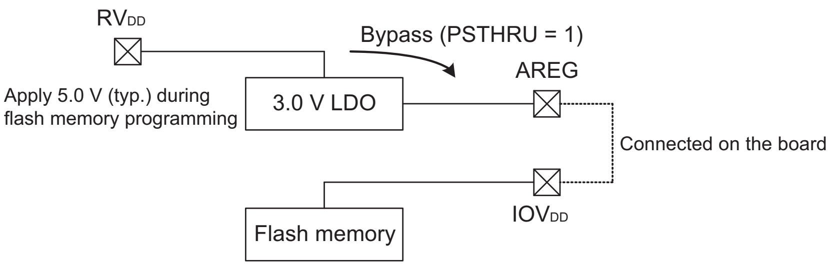
9.4 Settings for flash memory programming

9.4.1 Low-power access (mainly for read access)

Setting the SENSPD bit of the power/mode control register (CHIPCNT) enables accessing (mainly for reading) the flash memory at low power. When "1" is written to the SENSPD bit of the power/mode control register (CHIPCNT), SBIAS stops operating and analog circuits such as the PGIA and A/D converter stop operating. These analog circuits are not used for accessing the flash memory, so power supply to these circuits can be stopped to reduce power consumption. For details, see ***8.4.3 Registers controlling the sensor power supply (SBIAS)*** and ***8.4.4 Operation of sensor power supply (SBIAS)***.

9.4.2 Settings for bypassing AREG to RV_{DD} (for power supply configuration 2)

Even if IOV_{DD} is connected to the AREG output as shown in power supply configuration 2, flash memory programming can be performed by setting the PSTHRU bit of the power/mode control register (CHIPCNT). When "1" is written to the PSTHRU bit of the power/mode control register (CHIPCNT), AREG stops operating and the output from AREG is bypassed to RV_{DD} inside the circuit. For details, see ***8.5.1.3 Registers controlling AREG (AV_{DD}/IOV_{DD} power supply circuit)*** and ***8.5.1.4 Operation of AREG (AV_{DD}/IOV_{DD} power supply circuit)***.



Caution 5.0 V (typ.) is also applied to the serial communication pins.

Figure 9.8 Bypassing AREG to RV_{DD}

9.4.3 Protection of power/mode control register (CHIPCNT)

If the value of the AREGPD or PSTHRU bit changes accidentally during operation, a critical error or a malfunction that cannot be detected easily might occur. To prevent such a problem, the power/mode control register (CHIPCNT) has two protective features.

One is write-protection of the AREGPD bit of the power/mode control register (CHIPCNT). This protects the AREGPD bit from being written, thus ensuring that its data is retained. The setting of the SLP bit of the power/mode control register (CHIPCNT) affects writing to the AREGPD bit. The SLP bit must be set to 1 to enable writing to the AREGPD bit. If the SLP bit is not set to 1, writing to the AREGPD bit is disabled and thus the current data of the AREGPD bit is retained. Note, however, that this protection does not work when the register data in the flash memory is copied.

The other protective feature is masking of the PSTHRU bit of the power/mode control register (CHIPCNT). The setting of the ADSTART bit of the A/D converter control register (ADCCNT) affects writing to the PSTHRU bit. If "1" is written to the ADSTART bit to start A/D conversion, the PSTHRU bit is masked and thus retains 0. Writing to the PSTHRU bit is enabled again when a power-on reset (POR) occurs.

Figure 9.9 shows an example for accessing the power/mode control register (CHIPCNT).

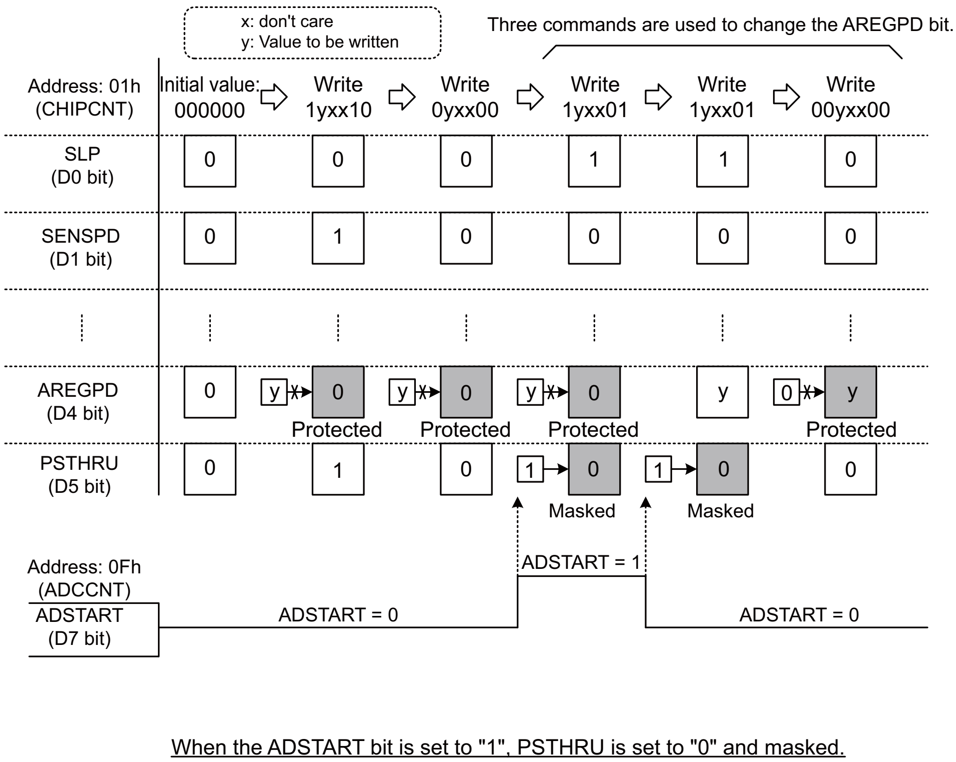


Figure 9.9 Protection of CHIPCNT register

10. Clock Configuration

10.1 Overview

The RAA730101 has an internal system clock (OSC) oscillator. This oscillator generates all the clocks required in each circuit (clock frequency = 20 MHz (Typ.)). The generated clock is divided and distributed to the A/D converter, UART, and flash memory controller. The ADC logic generates a clock for the A/D converter. The clock for the A/D converter can be monitored by using the MCLK pin.

An external clock can also be input to the A/D converter. In this case, the MCLK pin is used to input the external clock. An external clock is valid only during SPI communication (SMODE = 1). An external clock cannot be input during UART communication (SMODE = 0). For details, see ***10.3 Registers controlling clocks***.

10.2 Block diagram

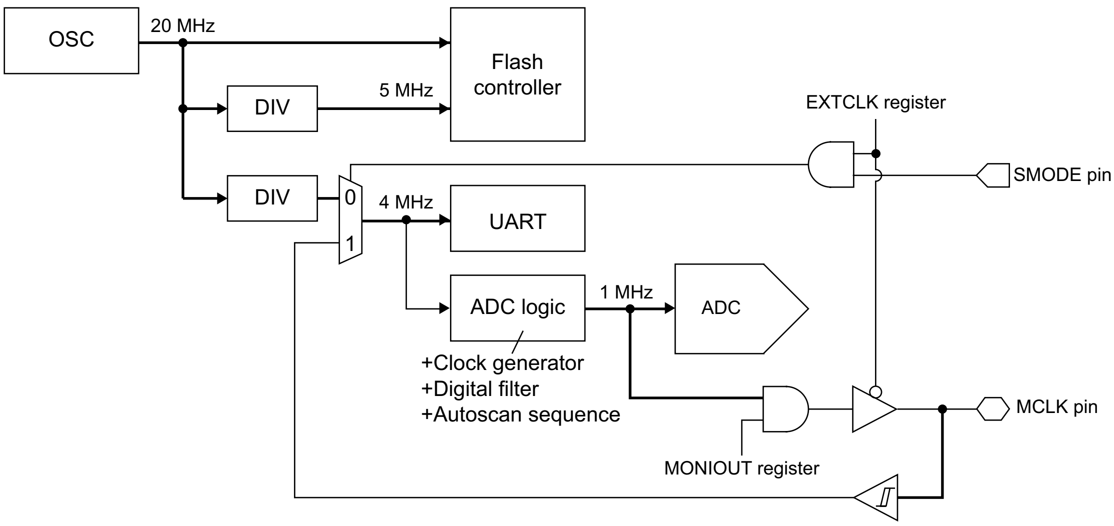


Figure 10.1 Clock configuration

Remark For details about MONIOUT and EXTCLK, see ***10.3 Registers controlling clocks***.

10.3 Registers controlling clocks

The following register is used to control the clocks.

- Clock/UART control register (UARTCNT)

(1) Clock/UART control register (UARTCNT)
This register is used to specify UART parameters and control the clock configuration.
After reset, this register is cleared to 00H.

Address: 08H After reset: 00H R/W

	7	6	5	4	3	2	1	0
UARTCNT	EXTCLK	MONIOUT	DIFFOUT	STB	EPS	PEN	TXBR	RXBR

MONIOUT	Monitoring the MCLK pin output
0	Disable monitoring (default).
1	Enable monitoring.

EXTCLK	External clock input to the A/D converter
0	Disable external clock input (default).
1	Enable external clock input.

Remark When MONIOUT is set to 0, the logic level of the MCLK pin output is fixed to low (pulled down to DGND inside the IC.) When not using this pin, see ***1.4 Connection of unused pins***.

11. Temperature Sensor

11.1 Overview

The RAA730101 has one on-chip temperature sensor channel. The output from the on-chip temperature sensor passes through input multiplexer 5 and the programmable gain instrumentation amplifier, and is then input to the A/D converter.

11.2 Registers controlling the temperature sensor

The following six kinds of registers are used to control the temperature sensor.

- A/D converter control register (ADCCNT)
- Input multiplexer 5 A/D conversion setting register 1 (CH5CNT1)
- Input multiplexer 5 A/D conversion setting register 3 (CH5CNT3)
- A/D conversion result register 1 (ADCC)
- A/D conversion result register 2 (ADCH)
- A/D conversion result register 3 (ADCL)

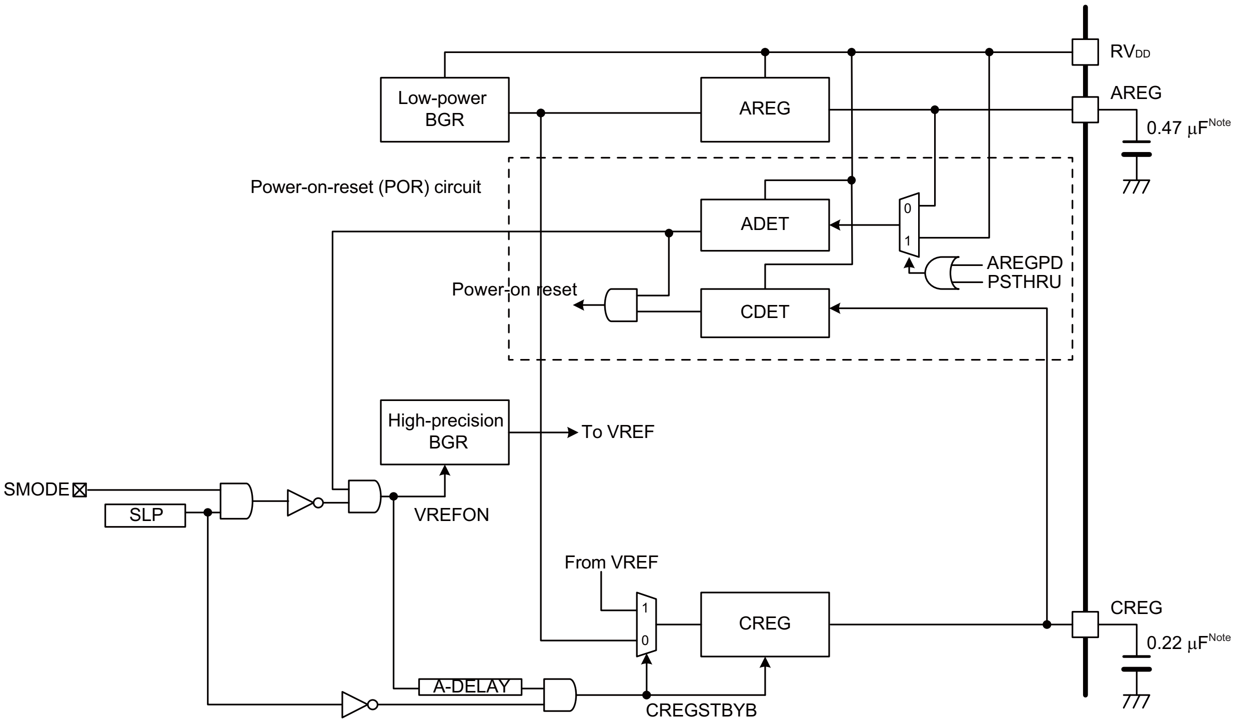
For details, see ***4.3 Registers controlling the 16-bit ΔΣ A/D converter***.

12. Power-on-Reset (POR) Circuit

12.1 Overview

The RAA730101 has a power-on-reset (POR) circuit. The POR circuit is built in as part of the power supply circuit and is used to monitor and detect the voltage output from the LDO regulators (AREG and CREG). The POR circuit consists of ADET, a circuit that monitors and detects the voltage output from AREG (or RVDD when AREG is bypassed) and CDET, a circuit that monitors and detects the voltage output from CREG. For details about the operation, see ***12.4 Operation of power-on-reset (POR) circuit***.

12.2 Block diagram



Note Capacitance values are recommended values.

Figure 12.1 Block diagram of power-on-reset (POR) circuit

12.3 Registers controlling the power-on-reset (POR) circuit

The following register is used to control the power-on-reset (POR) circuit

- Power/mode control register (CHIPCNT)

(1) Power/mode control register (CHIPCNT)

This register is used to switch the voltage to be monitored and detected by ADET, a circuit that monitors and detects the voltage output from AREG (or RV_{DD} when AREG is bypassed).

After reset, this register is cleared to 00H.

For details, see ***12.4 Operation of power-on-reset (POR) circuit***.

Address: 01H After reset: 00H R/W

	7	6	5	4	3	2	1	0
CHIPCNT	0	0	PSTHRU	AREGPD	0	0	SENSPD	SLP

PSTHRU	AREGPD	AREG operating status	ADET monitoring/detection target
0	0	Normal operation	Voltage output from AREG
1	0	Operation stops.	Voltage applied to RV_{DD}
*	1	Operation stops.	Voltage applied to RV_{DD}

Caution Bits 7, 6, 3, and 2 are read-only. (When these bits are read, 0 is always returned.)

Remark * ; don't care

12.4 Operation of power-on-reset (POR) circuit

The POR signal is generated based on the results of voltage detection by ADET and CDET. If both circuits detect a voltage higher than the removal voltage, the POR signal goes high and the internal blocks becomes active. If either circuit detects a voltage lower than the detection voltage, the POR signal goes low and the internal blocks are reset.

The AREGPD and PSTHRU bits of the power/mode control register (CHIPCNT) are used to switch the voltage to be monitored and detected by ADET. When "1" is written to the AREGPD or PSTHRU bit, the voltage to be monitored and detected by ADET is switched from the AREG output voltage to the voltage applied to RV_{DD}.

The POR circuit operates normally even if "1" is written to the SLP bit of the power/mode control register (CHIPCNT) and the power supply circuit enters sleep mode. For details, see ***8. Power Supply Circuit***.

13. Flash Memory

13.1 Overview

The RAA730101 has a 256-byte flash memory for storing information specific to the sensor connected to the RAA730101, such as the sensor ID, initial values, calibration data, and RAA730101 internal register settings specified for the sensor.

The lower 32 bytes of the address space are defined as a register shadow that can be used to store the data to be copied to registers. Data stored in the register shadow is copied to the relevant registers in the startup sequence that starts after power-on. Data stored in the register shadow can also be copied to the relevant registers by using an SPI or UART command in response to a request during normal operation.

The flash memory can be read and written in bytes, but should be erased all at once.

Flash memory programming is prohibited while A/D conversion is being performed (ADSTART = 1). Flash memory programming in sleep mode (SLP = 1) is also prohibited.

For details about the operation, see ***13.3 Startup (power-on) sequence***.

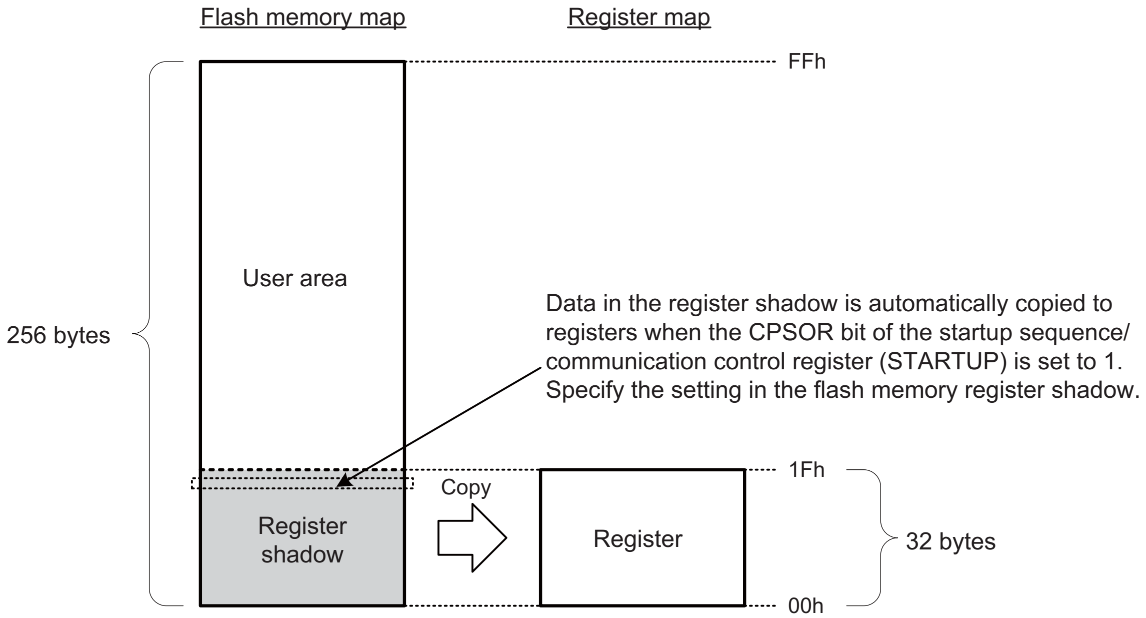


Figure 13.1 Address space

Cautions 1. Flash memory programming refers to erasing or writing of data in the flash memory.

2. If more than 30 days have passed since the data of flash memory was erased last, be sure to erase the data of flash memory again, and then write the required data to flash memory.

13.2 Registers controlling the flash memory

The following register is used to control the flash memory.

- Startup sequence/communication control register (STARTUP)

(1) Startup sequence/communication control register (STARTUP)

This register is used to control flash memory access during the startup sequence and select the communication mode. After reset, this register is cleared to 00H. For details, see ***13.3 Startup (power-on) sequence***.

This is a read-only register and cannot be written by using an SPI or UART command. However, this register is updated when data in the register shadow is copied during the startup sequence. The updated value then becomes valid.

Be sure to clear the TGLSM bit to "0". The TGLSM bit is also updated when data in the register shadow is copied. The updated value then becomes valid.

Address: 1FH After reset: 00H R/–

	7	6	5	4	3	2	1	0
STARTUP	0	0	0	TGLSM	0	0	SDCOR	CPSOR

CPSOR	Copying data in the register shadow
0	Disable operation.
1	Enable operation.

SDCOR	Data transmission to an external device using UART communication
0	Disable operation.
1	Enable operation.

TGLSM	Control of SMODE pin function
0	UART communication is selected when SMODE = 0, and SPI communication is selected when SMODE = 1.
1	Setting prohibited

Caution Bits 7, 6, 5, 3, and 2 are read-only. (When these bits are read, 0 is always returned.)

13.3 Startup (power-on) sequence

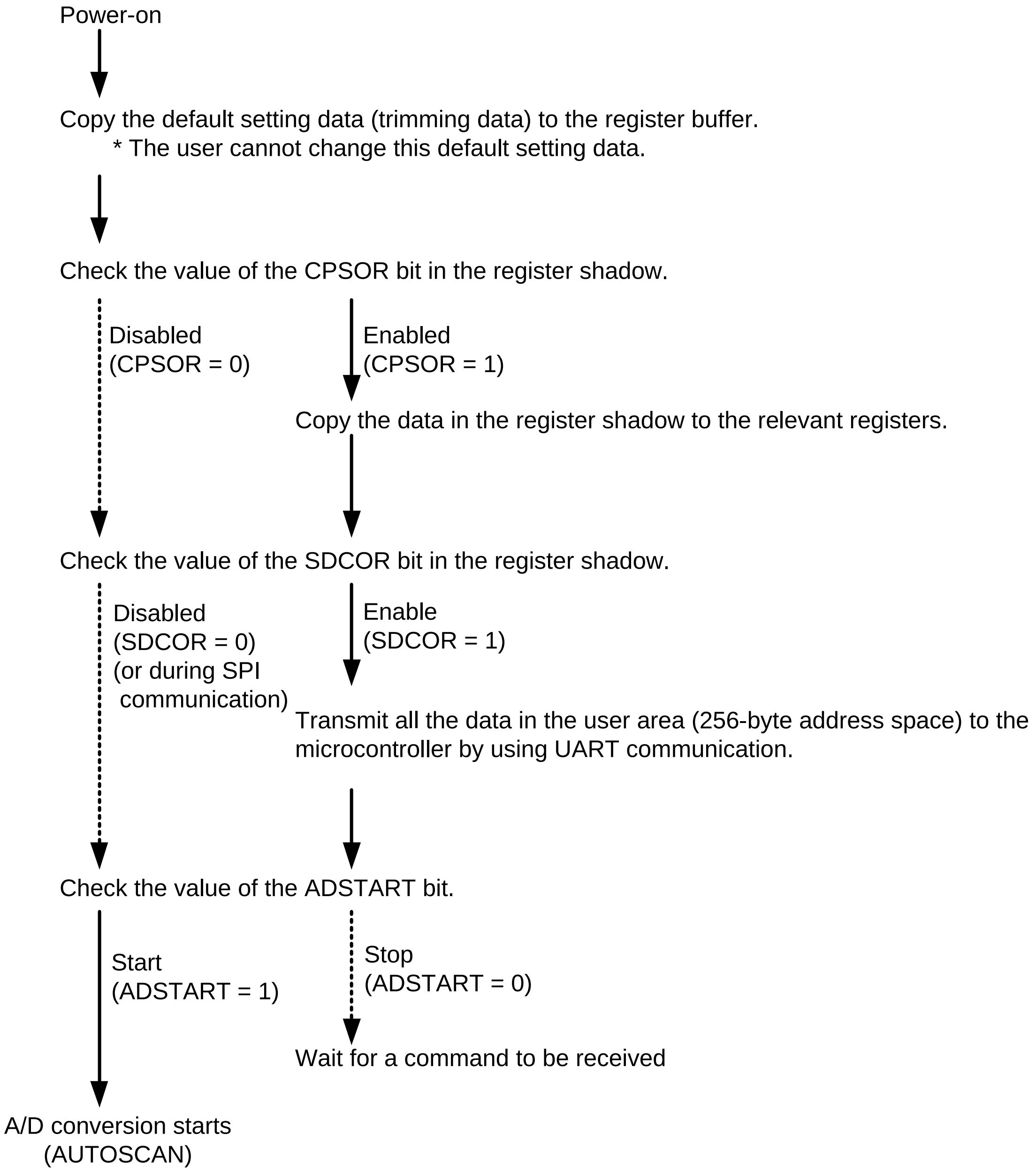


Figure 13.2 Startup (power-on) sequence

After power-on reset, the default setting data of the RAA730101 such as trimming data is copied to the register buffer area automatically. (The default setting data is always copied automatically.) The default setting data can also be copied to the register buffer area by using an SPI or UART command during normal operation. For details, see ***5. SPI*** and ***6. UART***.

Next, the CPSOR bit value stored in the register shadow is checked. If CPSOR is 1, the data in the register shadow are copied to the relevant registers. Then, the SDCOR bit value stored in the register shadow is checked. If SDCOR is 1, all 256 bytes of data in the user area in the flash memory are transmitted to the microcontroller connected to the RAA730101 by using UART communication. (This data is not transmitted in SPI communication.) The processes up to this point are automatically performed after power-on reset.

There is a programming window period in the interval from when the system starts up after power-on reset to when the first A/D conversion starts. Flash memory programming can only be performed in this period.

When ADSTART is set to 1 to trigger A/D conversion, flash memory programming can no longer be performed. This prevents the flash memory from being erased and overwritten unintentionally during operation. Flash memory programming is enabled again when power-on reset (POR) occurs.

Note that this operation occurs when ADSTART has been set to 1 by using an SPI or UART command. Flash memory programming is not disabled just by copying the value of ADSTART set to 1 in the register shadow to the relevant register.

Cautions 1. Flash memory programming refers to erasing or writing of data in the flash memory.

2. When the copy function from the register shadow to the registers is used, see *6.6 Note on Using the UART*.

13.4 Commands controlling the flash memory

13.4.1 Controlling the flash memory by using SPI commands

Table 13.1 SPI commands

No.	Name	Command				Extension	Description
		C7	C6	C5	C4 to C0	E7 to E0	
1	Register Read	0	0	1	Address: 00h to 1Fh	–	Reads 1 byte of data from the specified register.
2	Register Write	1	0	1	Address: 00h to 1Fh	–	Writes 1 byte of data to the specified register.
3	Register Burst Read	0	0	0	Data length 1xxxx Note 1	Start address 00h to 1Fh	Reads the specified length of data from the specified register successively. (Starting from the specified address)
4	Register Burst Write	1	0	0	Data length 1xxxx Note 1	Start address 00h to 1Fh	Writes the specified length of data to the specified register successively. (Starting from the specified address)
5	Register All Write from Flash	1	0	0	01111	–	Copies all data stored in the register shadow in the flash memory to the specified register.
6	Buffer Refresh	1	0	0	01100	–	Copies the default configuration data to the register buffer.
7	Flash (Burst) Read Note 3	0	1	0	11111	Start address 00h to FFh	Reads data from the flash memory. Specifies the address from which to start reading data. (First command)
		0	1	0	11100	Data length 00h to FFh Note 2	Reads data from the flash memory. Specifies the length of data to be read. (Second command)
8	Flash Write	1	1	0	11111	Address: 00h to FFh	Writes 1 byte of data to the flash memory.
9	Flash All Erase Note 3	1	1	1	11010	–	Erase all data in the flash memory. (First command)
		1	1	1	01011	–	Erase all data in the flash memory. (Second command)

Notes
1. Data length = "sum of C3 to C0 values" + 1 (Up to 16 bytes)
2. Data length = "sum of E7 to E0 values" + 1 (Up to 256 bytes)
3. To (burst) read and erase data in the flash memory, accessing the flash memory by successively using two commands is required.

13.4.2 Controlling the flash memory by using UART commands

Table 13.2 UART commands

No.	Name	Command				Extension	Description
		C7	C6	C5	C4 to C0	E7 to E0	
1	Register Read	0	0	1	Address: 00h to 1Fh	–	Reads 1 byte of data from the specified register.
2	Register Write	1	0	1	Address: 00h to 1Fh	–	Writes 1 byte of data to the specified register.
3	Register Burst Read	0	0	0	Data length 1xxxx Note 1	Start address 00h to 1Fh	Reads the specified length of data from the specified register successively. (Starting from the specified address)
4	Register Burst Write	1	0	0	Data length 1xxxx Note 1	Start address 00h to 1Fh	Writes the specified length of data to the specified register successively. (Starting from the specified address)
5	Register All Write from Flash	1	0	0	01111	–	Copies all data stored in the register shadow in the flash memory to the specified register.
6	Buffer Refresh	1	0	0	01100	–	Copies the default configuration data to the register buffer.
7	Flash (Burst) Read Note 3	0	1	0	11111	Start address 00h to FFh	Reads data from the flash memory. Specifies the address from which to start reading data. (First command)
		0	1	0	11100	Data length 00h to FFh Note 2	Reads data from the flash memory. Specifies the length of data to be read. (Second command)
8	Flash Write	1	1	0	11111	Address 00h to FFh	Writes 1 byte of data to the flash memory.
9	Flash All Erase Note 3	1	1	1	11010	–	Erase all data in the flash memory. (First command)
		1	1	1	01011	–	Erase all data in the flash memory. (Second command)
10	Baud rate correction	0	0	0	00000	–	Corrects the baud rate. (Only available in UART communication)
11	Send request	0	0	0	01111	–	Requests re-transmission of the message transmitted last. (Only available in UART communication)

Notes
1. Data length = "sum of C3 to C0 values" + 1 (Up to 16 bytes)
2. Data length = "sum of E7 to E0 values" + 1 (Up to 256 bytes)
3. To (burst) read and erase data in the flash memory, accessing the flash memory by successively using two commands is required.

14. Application Examples

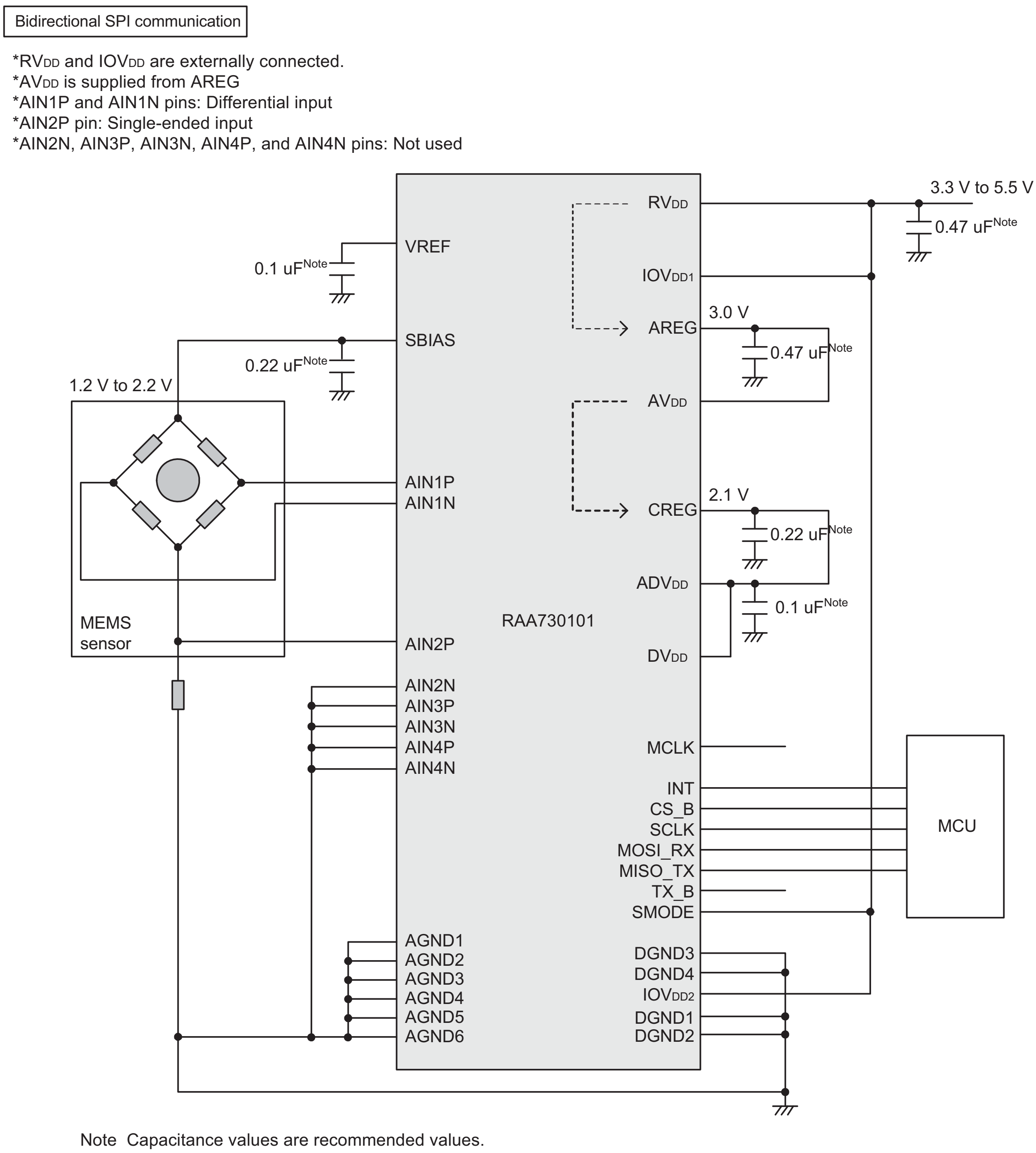
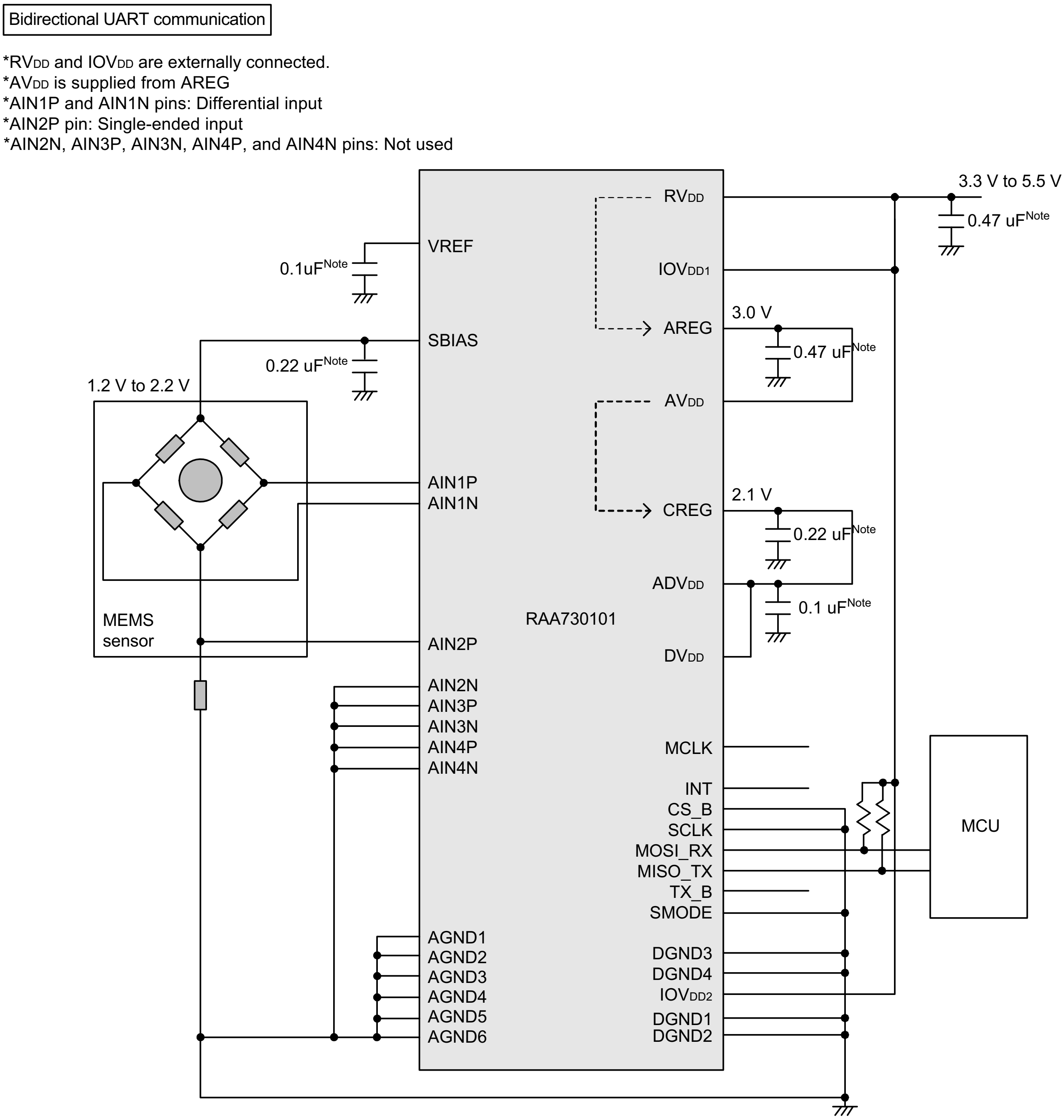


Figure 14.1 Example of connecting a sensor to a microcontroller (for SPI communication)



Note Capacitance values are recommended values.

Figure 14.2 Example of connecting a sensor to a microcontroller (for UART communication)

15. Electrical Specifications

The electrical specifications shown in this section are verified under the following conditions unless otherwise specified.

- The temperature ranges are −40°C ≤ T_A ≤ 125°C (for 125 °C models), −40°C ≤ T_A ≤ 105°C (for 105 °C models).
- The power supply voltage ranges satisfy the values prescribed in ***15.2 Operating conditions***.
- The Typ. value is the value when T_A = 25°C.
- Differential input mode, F_S = 1 MHz, F_{DATA} = 3.90625 ksps, SBIAS = 1.2 V, d_{OFR} = 0 mV, EXTCLK = 0, and V_{COM} = 0.9 V.

15.1 Absolute maximum ratings

Parameter	Symbol	Conditions	Ratings	Unit
Supply voltage	V_{DD1}	RV_{DD}, AV_{DD}, IOV_{DD}	−0.3 to +6.5	V
	V_{DD2}	ADV_{DD}, DV_{DD}	−0.3 to +2.8	V
	V_{SS}	AGND, DGND	−0.3 to +0.3	V
Input voltage	V_{I2}	AIN1P, AIN1N, AIN2P, AIN2N, AIN3P, AIN3N, AIN4P, AIN4N	−0.3 to AV_{DD} + 0.3 Note	V
	V_{I1}	CS_B, SCLK, MOSI_RX, SMODE, MCLK	−0.3 to IOV_{DD} + 0.3 Note	V
Output voltage	V_{O1}	AREG	−0.3 to RV_{DD} + 0.3 Note	V
	V_{O2}	CREG, SBIAS, VREF	−0.3 to AV_{DD} + 0.3 Note	V
	V_{O3}	MISO_TX, TX_B, INT, MCLK	−0.3 to IOV_{DD} + 0.3 Note	V
Output current, low	I_{OL}	MISO_TX	10	mA
Operating ambient temperature	T_A	In normal operating mode (for 125 °C models)	−40 to +125	°C
		In normal operating mode (for 105 °C models)	−40 to +105	°C
		During flash memory programming (for both 125 °C models and 105 °C models)	10 to 85	°C
Storage temperature	T_{STG}		−55 to +150	°C

Note Must be 6.5 V or lower.

15.2 Operating conditions

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Range of power supply voltage for regulator	RV_{DD}	AREG is operating	3.3	5.0	5.5	V
		AREG operation stopped	2.7	3.0	3.6	V
Range of power supply voltage for analog circuits	AV_{DD}		2.7	3.0	3.6	V
Power supply voltage input to the A/D converter	ADV_{DD}		2.0	2.1	2.2	V
Range of power supply voltage for digital circuits	DV_{DD}		2.0	2.1	2.2	V
Range of power supply voltage for I/O circuits	IOV_{DD}	$RV_{DD} \geq IOV_{DD}$ [Note 1]	2.7	5.0	5.5	V
Range of voltage for flash memory programming 1	V_{FP1}	When $V_{FP1} = IOV_{DD}$ [Note 2]	4.5		5.5	V
Range of voltage for flash memory programming 2	V_{FP2}	When $V_{FP2} = RV_{DD}$ [Note 3]	4.6		5.5	V

Notes **1.** Make RV_{DD} greater than or equal to IOV_{DD}.
2. For power supply configurations 1 and 3
3. For power supply configuration 2 and when PSTHRU = 1

Caution Flash memory programming refers to erasing or writing of data in the flash memory.

15.3 Supply current characteristics

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Current consumption in sleep mode (total of analog and digital circuits)	I_{DDS1}	SMODE = 1, SLP = 1, AREGPD = 0		3	20	μA
	I_{DDS2}	SMODE = 1, SLP = 1, AREGPD = 1		1.5	15	μA
	I_{DDS3}	SMODE = 0, SLP = 1, AREGPD = 0		550	850	μA
Analog power supply current ($RV_{DD} + AV_{DD} + ADV_{DD}$)	I_{DDA1}	During A/D conversion AREGPD = 0, SBIAS I_{OUT} = 0 mA		1.3	1.7	mA
	I_{DDA2}	SENSPD = 1, SLP = 0, AREGPD = 0		0.35	0.5	mA
Digital power supply current (DV_{DD})	I_{DDD1}	During A/D conversion		0.25	0.4	mA
	I_{DDD2}	When reading from flash memory [Note]		1.3	1.7	mA
Current consumption in flash memory programming ($IOV_{DD} + DV_{DD}$)	I_{DDF1}	When writing to flash memory $10°C \leq T_A \leq 85°C$		1.2	3	mA
	I_{DDF2}	When erasing flash memory $10°C \leq T_A \leq 85°C$		1.2	2	mA

Note The current consumption under the condition that some data are written to flash memory.

Caution Flash memory programming refers to erasing or writing of data in the flash memory.

15.4 Electrical specifications of each block

15.4.1 Programmable gain instrumentation amplifier and 16-bit ΔΣ A/D converter

Analog input in differential input mode

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Full-scale differential input voltage range	V_{ID}	V_{ID} = (AINxP − AINxN) (x = 1, 2, 3, 4)		± 700 /G_{TOTAL}		mV
Input voltage range	V_I	Each of AINxP and AINxN pins (x = 1, 2, 3, 4)	0.2		1.6	V
Common mode input voltage	V_{COM}	d_{OFR} = 0 mV	0.2 + (|V_{ID}|x G_{SET1})/2		1.6 − (|V_{ID}|x G_{SET1})/2	V
Input impedance	Z_{IN}		5			MΩ

Analog input in single-ended input mode

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Input voltage	V_I	G_{SET1} = 1, G_{SET2} = 1	0.2		1.6	V
Input impedance	Z_{IN}		5			MΩ

Programmable gain instrumentation amplifier and 16-bit ΔΣ A/D converter (1/2)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Sampling frequency	F_S			1		MHz
Output data rate	F_{DATA}		(0.48828)		(15.625)	ksps
Gain setting range	G_{TOTAL}	G_{TOTAL} = G_{SET1} x G_{SET2}	1		32	V/V
1st gain setting range	G_{SET1}			1, 2, 3, 4, 8		V/V
2nd gain setting range	G_{SET2}			1, 2, 4, 8		V/V
Offset adjustment bit range	d_{OFFB}			5		bit
Offset adjustment range	d_{OFR}	Referred to input	−175/G_{SET1}		+164/G_{SET1}	mV
Offset adjustment steps	d_{OFS}	Referred to input		11/G_{SET1}		mV

Remark In the specification column, values in parentheses are the target design values and therefore are not tested for shipment.

Programmable gain instrumentation amplifier and 16-bit ΔΣ A/D converter (2/2)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Gain error	E_G		–10		10	%
Gain drift[Note]	dE_G	G_{SET1} = 1, G_{SET2} = 1 Excluding SBIAS drift			(22)	ppm/°C
Offset error	E_{OS}	G_{SET1} = 1, G_{SET2} = 1	–5		5	mV
Offset drift[Note]	dE_{OS}	G_{SET1} = 1, G_{SET2} = 1			(16)	μV/°C
S/N	SNR	G_{SET1} = 1, G_{SET2} = 1 Excluding MEMS noise	82	85		dB
Common mode rejection ratio	CMRR	f_{in} = 50 Hz, G_{SET1} = 1, G_{SET2} = 1	40	60		dB
Power supply rejection ratio	PSRR	AV_{DD} = 3.0 V + 0.1 $V_{pp\ ripple}$ f_{in} = 50 Hz, G_{SET1} = 1, G_{SET2} = 1	(60)	(70)		dB
A/D converter input clock frequency	f_{ADC}	EXTCLK = 1	3.8	4	4.2	MHz

Note Calculate the gain drift and offset drift by using the following expression:

(for 125 °C models)

For gain drift: $(MAX(E_G(T_{(-40)}$ to $T_{(125)})) – MIN(E_G(T_{(-40)}$ to $T_{(125)}))) / (125°C – (–40°C))$

For offset drift: $(MAX(E_{OS}(T_{(-40)}$ to $T_{(125)})) – MIN(E_{OS}(T_{(-40)}$ to $T_{(125)}))) / (125°C – (–40°C))$

$MAX(E_G(T_{(-40)}$ to $T_{(125)})$: The maximum value of gain error when the temperature range is –40°C to 125°C

$MIN(E_G(T_{(-40)}$ to $T_{(125)})$: The minimum value of gain error when the temperature range is –40°C to 125°C

$MAX(E_{OS}(T_{(-40)}$ to $T_{(125)})$: The maximum value of offset error when the temperature range is –40°C to 125°C

$MIN(E_{OS}(T_{(-40)}$ to $T_{(125)})$: The minimum value of offset error when the temperature range is –40°C to 125°C

(for 105 °C models)

For gain drift: $(MAX(E_G(T_{(-40)}$ to $T_{(105)})) – MIN(E_G(T_{(-40)}$ to $T_{(105)}))) / (105°C – (–40°C))$

For offset drift: $(MAX(E_{OS}(T_{(-40)}$ to $T_{(105)})) – MIN(E_{OS}(T_{(-40)}$ to $T_{(105)}))) / (105°C – (–40°C))$

$MAX(E_G(T_{(-40)}$ to $T_{(105)})$: The maximum value of gain error when the temperature range is –40°C to 105°C

$MIN(E_G(T_{(-40)}$ to $T_{(105)})$: The minimum value of gain error when the temperature range is –40°C to 105°C

$MAX(E_{OS}(T_{(-40)}$ to $T_{(105)})$: The maximum value of offset error when the temperature range is –40°C to 105°C

$MIN(E_{OS}(T_{(-40)}$ to $T_{(105)})$: The minimum value of offset error when the temperature range is –40°C to 105°C

Remark In the specification column, values in parentheses are the target design values and therefore are not tested for shipment.

15.4.2 Internal reference voltage generator (VREF)

(C_{OUT} = 0.1 μF)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Output voltage	V_{OUT}		0.76	0.8	0.84	V
Turn-on time	T_{ON}	V_{OUT} > 90%			(550)	μs

Remark Values in parentheses are the target design values and therefore are not tested for shipment.

15.4.3 Sensor power supply (SBIAS)

(C_{OUT} = 0.22 μF)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Output voltage range	V_{OUT}		1.2		2.2	V
Output voltage setting steps	V_{STEP}			0.1		V
Output voltage range	V_A	0 mA ≤ I_{OUT} ≤ 5 mA	–5		+5	%
Output current	I_{OUT}		5			mA
Output current limit	I_{LIMIT}			(40)	(60)	mA
Short-circuit current	I_{SHORT}	V_{OUT} = 0 V		40	65	mA
Load regulation	L_R	0 mA ≤ I_{OUT} ≤ 5 mA			15	mV
Power supply rejection ratio	PSRR	AV_{DD} = 3.0 V + 0.1 $V_{pp\ ripple}$ f = 100 Hz, I_{OUT} = 2.5 mA	(45)	(50)		dB
Turn-on time	T_{ON}	V_{OUT} > 90%			(250)	μs
Turn-off time	T_{OFF}	V_{OUT} < 10%			(5)	ms

Remark Values in parentheses are the target design values and therefore are not tested for shipment.

15.4.4 AREG (AV_{DD}/IOV_{DD} power supply circuit)

(C_{OUT} = 0.47 μF)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Output voltage	V_{OUT}	0 mA ≤ I_{OUT} ≤ 50 mA	2.85	3	3.15	V
Output current	I_{OUT}		50			mA
Output current limit	I_{LIMIT}			(110)	(150)	mA
Short-circuit current	I_{SHORT}	V_{OUT} = 0 V		40	65	mA
Load regulation	L_R	1 mA ≤ I_{OUT} ≤ 50 mA			40	mV
Power supply rejection ratio	PSRR	RV_{DD} = 5.0 V + 0.1 $V_{pp\ ripple}$ f = 100 Hz, I_{OUT} = 25 mA	(35)	(45)		dB
Turn-on time	TON	RV_{DD} ≥ 3.3 V, V_{OUT} > 90%, I_{OUT} = 0 mA			(1800)	μs

Remark Values in parentheses are the target design values and therefore are not tested for shipment.

15.4.5 CREG (ADV_{DD}/DV_{DD} power supply circuit)

(C_{OUT} = 0.22 μF, in normal operating mode)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Output voltage	V_{OUT}	0 mA ≤ I_{OUT} ≤ 20 mA	2	2.1	2.2	V
Output current	I_{OUT}		20			mA
Output current limit	I_{LIMIT}			(60)	(90)	mA
Short-circuit current	I_{SHORT}	V_{OUT} = 0 V		40	65	mA
Load regulation	L_R	1 mA ≤ I_{OUT} ≤ 20 mA			20	mV
Power supply rejection ratio	PSRR	AV_{DD} = 3.0 V + 0.1 $V_{pp\ ripple}$ f = 100 Hz, I_{OUT} = 10 mA	(45)	(50)		dB
Turn-on time	T_{ON}	V_{OUT} > 90%, I_{OUT} = 0 mA including VREF turn-on time			(700)	μs
Turn-off time	T_{OFF}	V_{OUT} < 10%, I_{OUT} = 0 mA			(5)	ms
Mode switching time 1	T_{SW1}	Operating to Standby			(400)	μs
Mode switching time 2	T_{SW2}	Standby to Operating Excluding VREF turn-on time			(150)	μs

Remark Values in parentheses are the target design values and therefore are not tested for shipment.

(C_{OUT} = 0.22 μF, on standby)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Output voltage	V_{OUT}	0 mA ≤ I_{OUT} ≤ 2 mA	2	2.1	2.2	V
Output current	I_{OUT}		2			mA

15.4.6 Power-on-reset (POR) circuit

ADET (AREG/RV_{DD} voltage monitor and detector)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Removal voltage	V_{POR}	When AREG output voltage rises	2.4	2.5	2.6	V
Detection voltage 1	V_{PDR1}	When AREG output voltage falls AREGPD = 0	2.2	2.3	2.4	V
Detection voltage 2	V_{PDR2}	When RV_{DD} input voltage falls AREGPD = 1	2.2	2.3	2.4	V

CDET (CREG voltage monitor and detector)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Removal voltage	V_{POR}	When CREG output voltage rises	1.82	1.9	1.98	V
Detection voltage	V_{PDR}	When CREG output voltage falls	1.75	1.83	1.91	V

15.4.7 Temperature sensor

Parameter	Symbol	Conditions	Min.	Typ.	Max	Unit
Temperature coefficient for sensor	TC_{SNS}		(–2.1)	(–1.8)	(–1.5)	mV/°C
Temperature sensor output voltage	V_{TEMP}	T_A = 25°C	580	680	780	mV

Remark Values in parentheses are the target design values and therefore are not tested for shipment.

15.4.8 Internal system clock (OSC) oscillator

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Clock frequency	f_{OSC}		19	20	21	MHz

15.4.9 Flash memory

($10°C \leq T_A \leq 85°C$, 4.5 (4.6) V[Note] $\leq IOV_{DD} \leq RV_{DD} \leq 5.5$ V)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Erase time	T_{ER}			(5)		ms
Write time	T_{WR}			(100)		μs
Number of rewrite times	C_{EW}		(100)			Times
Data retention period	T_{DR}		(10)			Years

Note Specify the voltage to be applied according to the power supply configuration used. For details, see ***9 Power Supply Configuration*** and see ***15.2 Operating conditions*** about the power supply voltage ranges.

Remark Values in parentheses are the target design values and therefore are not tested for shipment.

15.4.10 Digital I/O

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Input voltage, high	V_{IH}	CS_B, SCLK, MOSI_RX, SMODE MCLK (EXTCLK = 1)	0.7 × IOV_{DD}		IOV_{DD}	V
Input voltage, low	V_{IL}	CS_B, SCLK, MOSI_RX, SMODE MCLK (EXTCLK = 1)	0		0.3 × IOV_{DD}	V
Output voltage, high	V_{OH}	MISO_TX, TX_B, INT, MCLK, IOH = –1 mA, 2.7 V ≤ IOV_{DD} ≤ 5.5 V	IOV_{DD} – 0.5		IOV_{DD}	V
Output voltage, low 1	V_{OL1}	MISO_TX, TX_B, INT, MCLK, IOL = 1 mA, 2.7 V ≤ IOV_{DD} ≤ 5.5 V	0		0.4	V
Output voltage, low 2	V_{OL2}	MISO_TX, IOL = 5 mA, 2.7 V ≤ IOV_{DD} ≤ 5.5 V	0		0.7	V
Input leakage current	I_{INL}	CS_B, SCLK, MOSI_RX, SMODE MCLK (EXTCLK = 1)	–1		1	μA

15.5 SPI access timing

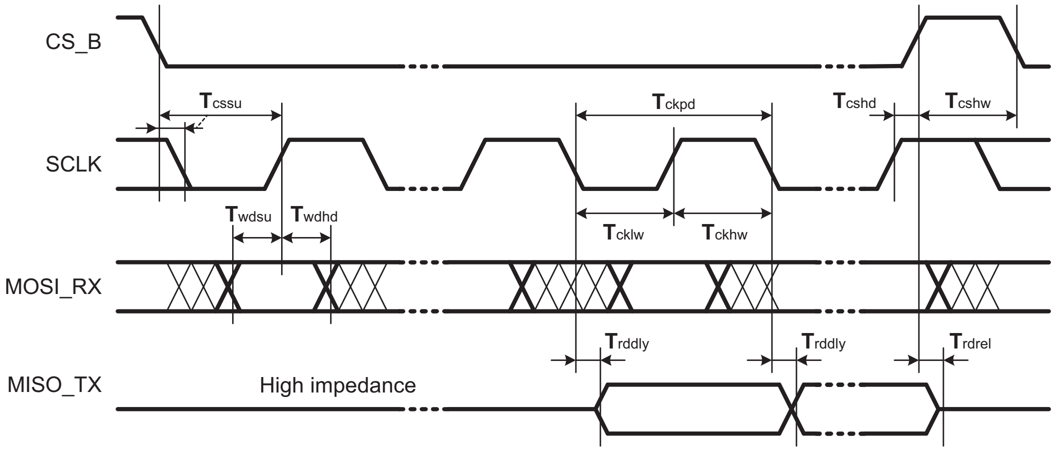


Figure 15.1 SPI access timing

IOVDD = 2.7 V to 5.5 V, C = 15 pF

Symbol	Description	Min.	Typ.	Max.	Unit
Tcssu	From CS_B↓ to first SCLK↓ or to first SCLK↑	20			ns
Tcshd	From SCLK↑ to CS_B↑	20			ns
Tcshw	CS_B high-level width between transfers	80			ns
Tckpd	SCLK clock cycle	200 (500)Note			ns
Tckhw	SCLK high-level width	80			ns
Tcklw	SCLK low-level width	80			ns
Twdsu	MOSI_RX setup time (to SCLK↑)	20			ns
Twdhd	MOSI_RX hold time (from SCLK↑)	20			ns
Trddly	From SCLK↓ to MISO_TX stabilizes			40	ns
Trdrel	From CS_B↑ to MISO_TX released			40	ns

Note The maximum clock cycle of the burst read access to the flash memory is 2 MHz.

15.6 Cumulative power-on time and wake-up time

CPSOR = SDCOR = 0

	Power-on time (μs)	**Wake-up time (μs)**	
		During SPI communication (SMODE = 1)	**During UART communication** (SMODE = 0)
Until serial communication is ready	(3300)	–	–
Until A/D conversion is ready	(3570)	(820)	(270)
Until the first A/D conversion ends	(3698 + 3T) Note	(948 + 3T) Note	(398 + 3T) Note
Based on	Power-on	SLP = 1 → 0	

Note T: Sampling time (= $1/f_{OUT}$)

Remark Values in parentheses are the target design values and therefore are not tested for shipment.

The figure 15.2 shows the status transition at power-on and the figure 15.3 shows the status transition at wake-up. Estimate the cumulative power-on time and wake-up time referring to the figure 15.2 and to the figure 15.3. It is possible to make a sufficient allowance of time as a safety margin according to the actual system of use. For details about each function in the figures below, see the relevant section described about that function.

In the figures below, it is assumed that ADSTART is set to 1 during the SBIAS stabilization time. If ADSTART is not set to 1 during that time, the timing when the actual A/D conversion starts is delayed according to the timing when ADSTART is set to 1.

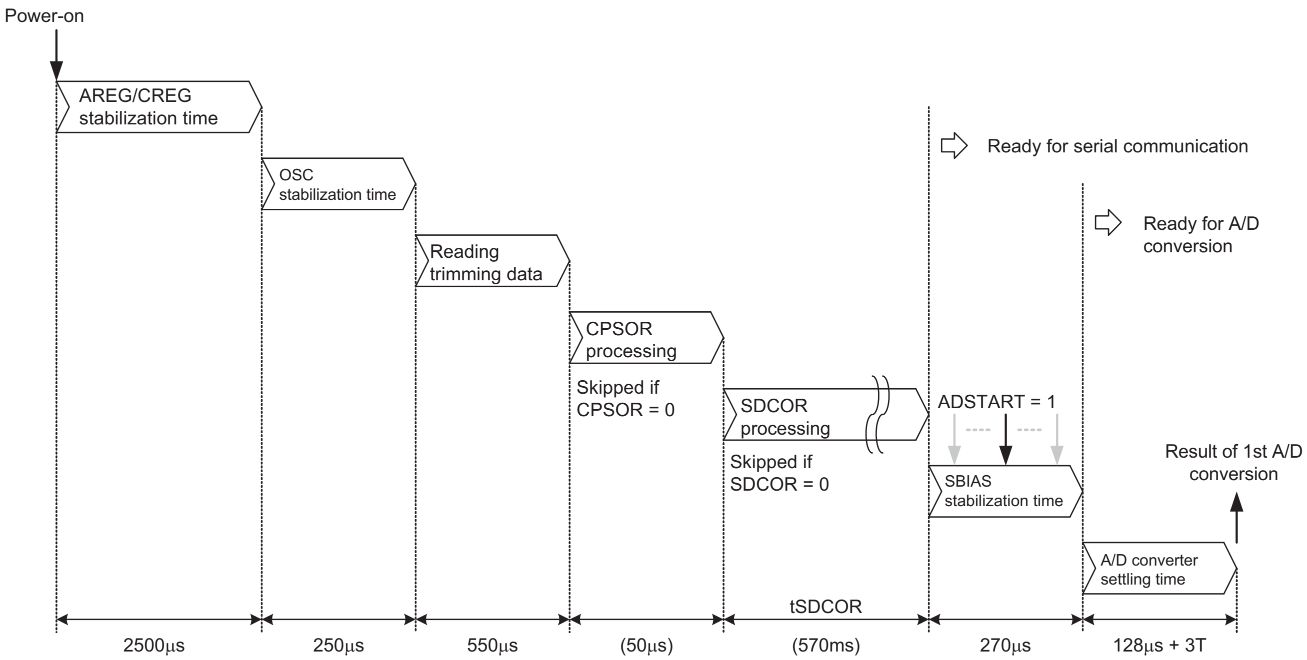


Figure 15.2 Cumulative power-on time

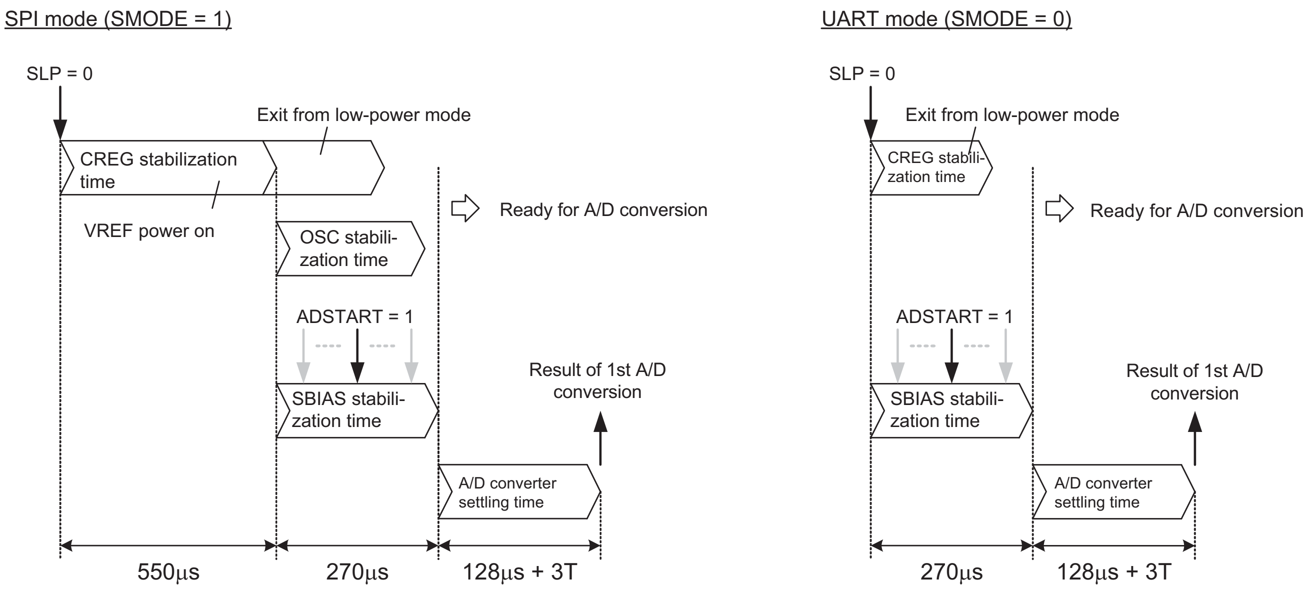


Figure 15.3 Cumulative wake-up time

The example is added for explanation about the time required for SDCOR processing.

As the time required for SDCOR processing varies depending on the UART setting, calculate the SDCOR processing time by using the following equation:

$$t_{SDCOR}\ [\text{sec.}] = (1/\text{baud rate [bps]}) \times \text{packet length [bits]} \times (256 + 4)\ [\text{packets}]$$

In the figure 15.2, it is assumed that baud rate is 4.8 kbps, no parity bit, number of stop bits is 1, and then

$$t_{SDCOR}\ [\text{sec.}] = (1 / 4800) \times 10 \times (256 + 4) = 0.54\ [\text{sec.}]$$

Considering the accuracy of clock frequency, add about +5% of 0.54 [sec.] as a safety margin and use the resulting 0.57 [sec.] for the setting.

16. Chip Identification

16.1 Overview

The RAA730101 has a chip identification register.

16.2 Register for chip identification

The following register is used for chip identification.

- Chip identification register (CHIPID)

(1) Chip identification register (CHIPID)

This is a read-only register storing chip ID. The initial value is 3AH.

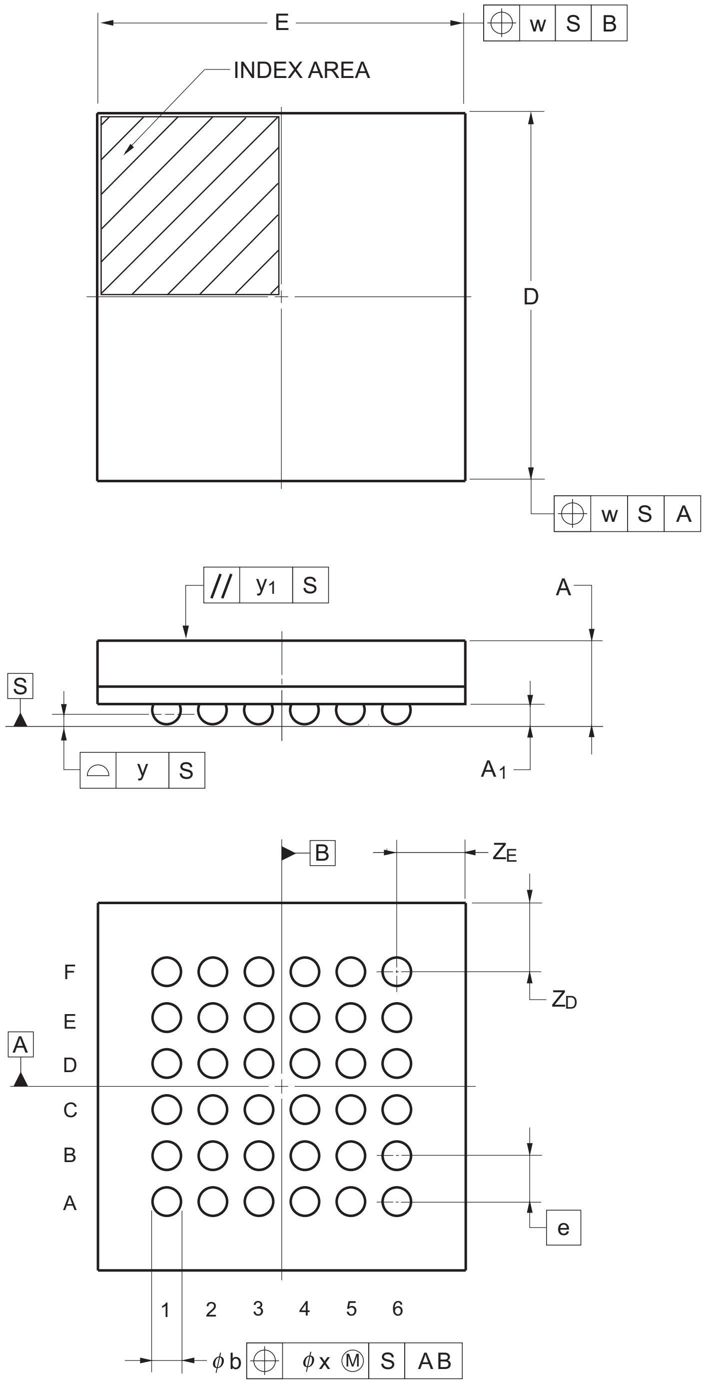
Address: 00H After reset: 3AH R/–

	7	6	5	4	3	2	1	0
CHIPID	0	0	1	1	1	0	1	0

17. Package Drawings

4 × 4 mm/36-pin FBGA (0.50 mm pitch)

JEITA Package code	RENESAS code	Previous code	MASS(TYP.)[g]
P-TFBGA36-4x4-0.50	PTBG0036KA-A	P36F1-50-AA6	0.027

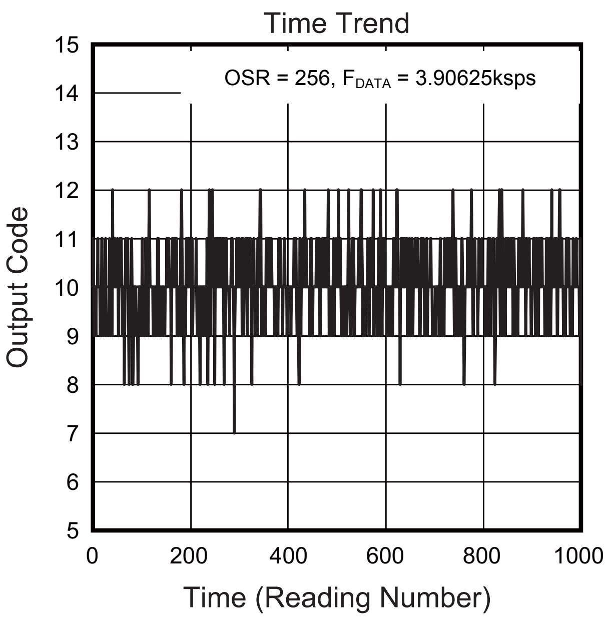


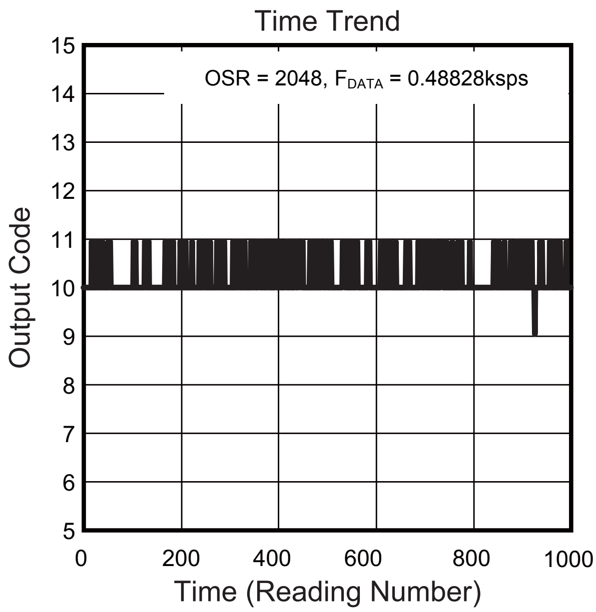
Referance Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	3.90	4.00	4.10
E	3.90	4.00	4.10
A	—	—	1.10
A_1	0.17	0.22	0.27
e	—	0.50	—
b	0.26	0.31	0.36
x	—	—	0.05
y	—	—	0.08
y_1	—	—	0.20
Z_D	—	0.75	—
Z_E	—	0.75	—
w	—	—	0.20

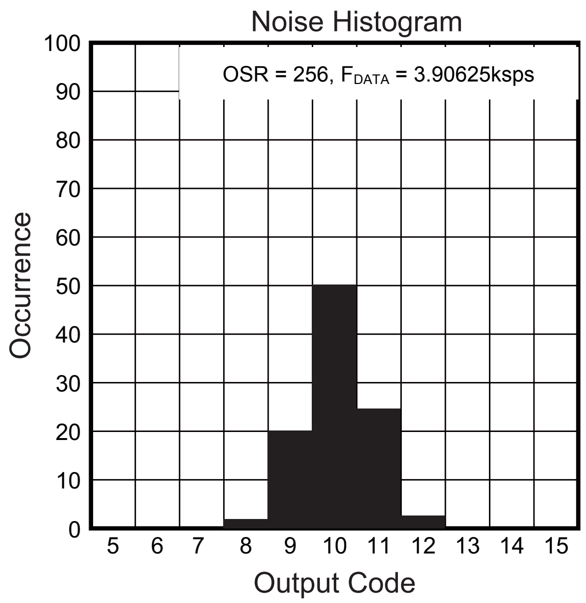
Characteristics Curve (T_A = 25°C, TYP.) (reference value)

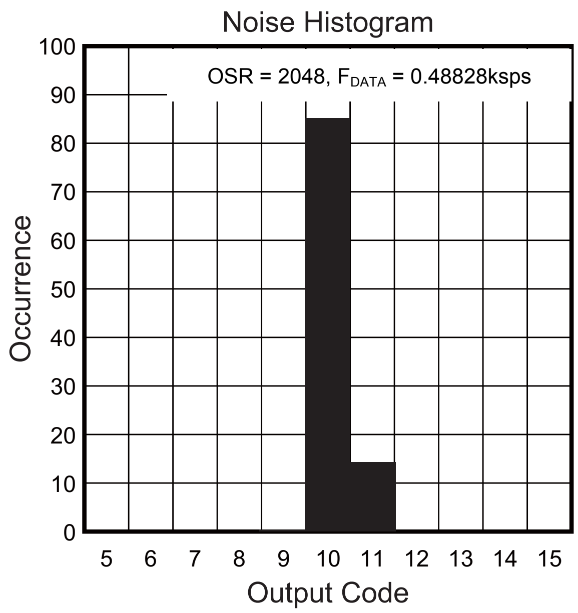
- Programmable gain instrumentation amplifier and 16-bit ΔΣ A/D converter

RV_{DD} = IOV_{DD} = 5.0V, AV_{DD} = 3.0V, ADV_{DD} = DV_{DD} = 2.1V,
differential input mode, FS = 1MHz, SBIAS = 1.2V, d_{OFR} = 0mV, G_{TOTAL}=1

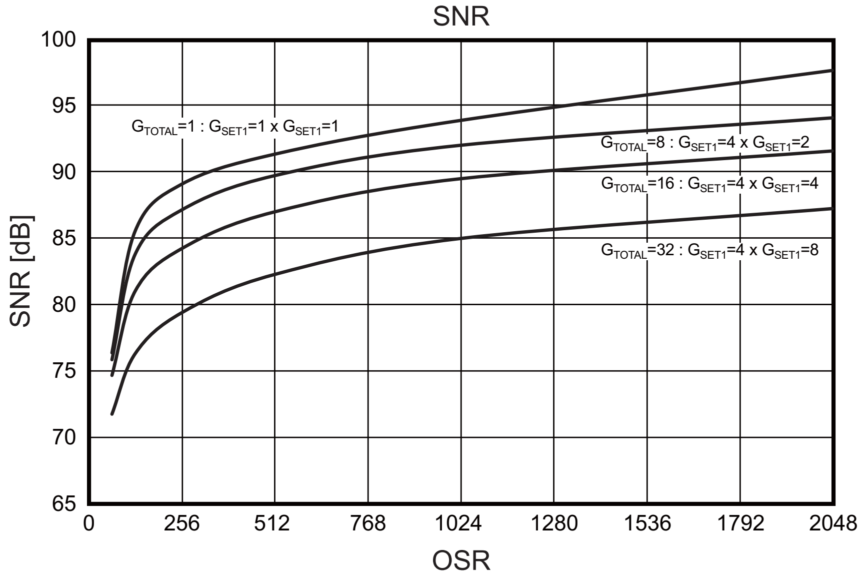


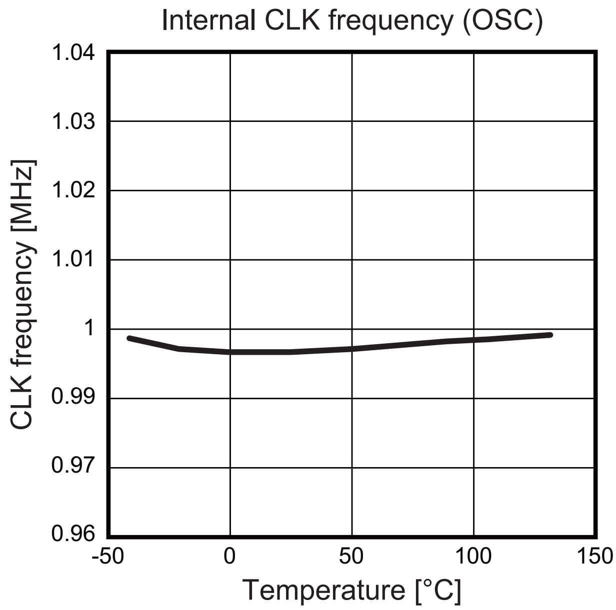






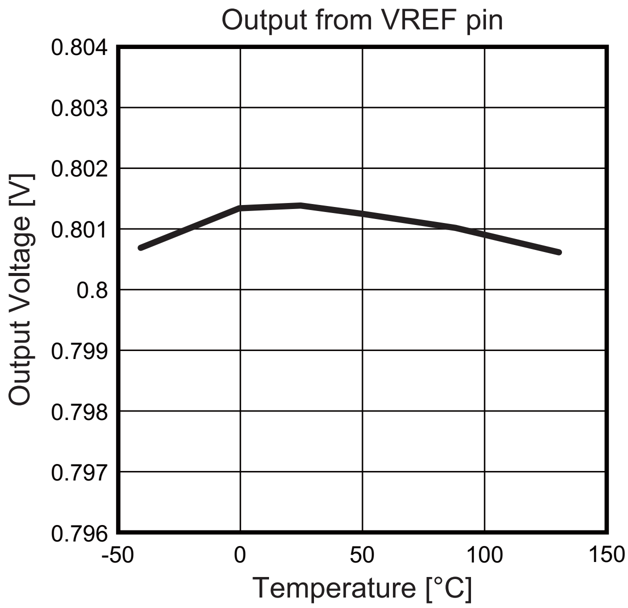
RV_{DD} = IOV_{DD} = 5.0V, AV_{DD} = 3.0V, ADV_{DD} = DV_{DD} = 2.1V, differential input mode, FS = 1MHz, F_{DATA} = 3.90625ksps, SBIAS = 1.2V, d_{OFR} = 0mV, OSR = 256, G_{TOTAL}=1





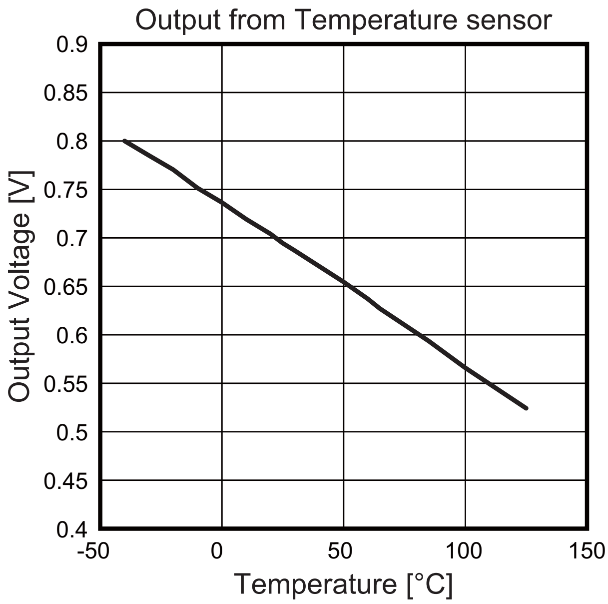
- Internal reference voltage generator（VREF）

$RV_{DD} = IOV_{DD} = 5.0V$, $AV_{DD} = 3.0V$, $ADV_{DD} = DV_{DD} = 2.1V$, differential input mode, FS = 1MHz, $F_{DATA} = 3.90625ksps$, SBIAS = 1.2V, $d_{OFR} = 0mV$, OSR = 256, $G_{TOTAL}=1$



- Temperature Sensor

$RV_{DD} = IOV_{DD} = 5.0V$, $AV_{DD} = 3.0V$, $ADV_{DD} = DV_{DD} = 2.1V$, differential input mode, FS = 1MHz, $F_{DATA} = 3.90625ksps$, SBIAS = 1.2V, $d_{OFR} = 0mV$, OSR = 256, $G_{TOTAL}=1$



Revision Record	RAA730101 16-bit ΔΣ A/D converter IC with programmable gain instrumentation amplifier

Rev.	Date	Description	
		Page	**Summary**
1.00	Mar 31, 2014	–	First edition issued
1.10	Jul 31, 2014	14	Modification of description in 3.1 Function of Programmable Gain Instrumentation Amplifier
		15	Addition of description in 3.2 Function of Single-ended input mode
		16	Addition of description in 3.3 Function of Single-ended input mode
		17	Addition of description in 3.3.2 Function of Single-ended input mode
		18	Deletion of note in A/D conversion setting register 1
		21	・Addition of description in 4.1.3 Function of Single-ended input mode ・Addition of description in 4.1 table of Single-ended input mode
		32	Modification of Figure in Example 1
		92	Addition of Condition in Input voltage at single-ended input mode
2.00	Feb 27, 2015	All	The English expression has been corrected.
		34	Addition of description in 5.1 Overview
		38	Addition of 5.5 Note on Using the SPI
		49	Addition of title (1) Disabling the reception by the UART and description of (2) Reading the ADSTART bit in 6.6 Note on Using the UART

Caution: This product uses SuperFlash® technology licensed from Silicon Storage Technology, Inc.

NOTES FOR CMOS DEVICES

① VOLTAGE APPLICATION WAVEFORM AT INPUT PIN

Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (MAX) and V_{IH} (MIN) due to noise, etc., the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (MAX) and V_{IH} (MIN).

② HANDLING OF UNUSED INPUT PINS

Unconnected CMOS device inputs can be cause of malfunction. If an input pin is unconnected, it is possible that an internal input level may be generated due to noise, etc., causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND via a resistor if there is a possibility that it will be an output pin. All handling related to unused pins must be judged separately for each device and according to related specifications governing the device.

③ PRECAUTION AGAINST ESD

A strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it when it has occurred. Environmental control must be adequate. When it is dry, a humidifier should be used. It is recommended to avoid using insulators that easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors should be grounded. The operator should be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with mounted semiconductor devices.

④ STATUS BEFORE INITIALIZATION

Power-on does not necessarily define the initial status of a MOS device. Immediately after the power source is turned ON, devices with reset functions have not yet been initialized. Hence, power-on does not guarantee output pin levels, I/O settings or contents of registers. A device is not initialized until the reset signal is received. A reset operation must be executed immediately after power-on for devices with reset functions.

⑤ POWER ON/OFF SEQUENCE

In the case of a device that uses different power supplies for the internal operation and external interface, as a rule, switch on the external power supply after switching on the internal power supply. When switching the power supply off, as a rule, switch off the external power supply and then the internal power supply. Use of the reverse power on/off sequences may result in the application of an overvoltage to the internal elements of the device, causing malfunction and degradation of internal elements due to the passage of an abnormal current.

The correct power on/off sequence must be judged separately for each device and according to related specifications governing the device.

⑥ INPUT OF SIGNAL DURING POWER OFF STATE

Do not input signals or an I/O pull-up power supply while the device is not powered. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements.

Input of signals during the power off state must be judged separately for each device and according to related specifications governing the device.

SALES OFFICES Renesas Electronics Corporation http://www.renesas.com

Refer to "http://www.renesas.com/" for the latest and detailed information.

Renesas Electronics America Inc.
2801 Scott Boulevard Santa Clara, CA 95050-2549, U.S.A.
Tel: +1-408-588-6000, Fax: +1-408-588-6130

Renesas Electronics Canada Limited
9251 Yonge Street, Suite 8309 Richmond Hill, Ontario Canada L4C 9T3
Tel: +1-905-237-2004

Renesas Electronics Europe Limited
Dukes Meadow, Millboard Road, Bourne End, Buckinghamshire, SL8 5FH, U.K
Tel: +44-1628-585-100, Fax: +44-1628-585-900

Renesas Electronics Europe GmbH
Arcadiastrasse 10, 40472 Düsseldorf, Germany
Tel: +49-211-6503-0, Fax: +49-211-6503-1327

Renesas Electronics (China) Co., Ltd.
Room 1709, Quantum Plaza, No.27 ZhiChunLu Haidian District, Beijing 100191, P.R.China
Tel: +86-10-8235-1155, Fax: +86-10-8235-7679

Renesas Electronics (Shanghai) Co., Ltd.
Unit 301, Tower A, Central Towers, 555 Langao Road, Putuo District, Shanghai, P. R. China 200333
Tel: +86-21-2226-0888, Fax: +86-21-2226-0999

Renesas Electronics Hong Kong Limited
Unit 1601-1611, 16/F., Tower 2, Grand Century Place, 193 Prince Edward Road West, Mongkok, Kowloon, Hong Kong
Tel: +852-2265-6688, Fax: +852 2886-9022

Renesas Electronics Taiwan Co., Ltd.
13F, No. 363, Fu Shing North Road, Taipei 10543, Taiwan
Tel: +886-2-8175-9600, Fax: +886 2-8175-9670

Renesas Electronics Singapore Pte. Ltd.
80 Bendemeer Road, Unit #06-02 Hyflux Innovation Centre, Singapore 339949
Tel: +65-6213-0200, Fax: +65-6213-0300

Renesas Electronics Malaysia Sdn.Bhd.
Unit 1207, Block B, Menara Amcorp, Amcorp Trade Centre, No. 18, Jln Persiaran Barat, 46050 Petaling Jaya, Selangor Darul Ehsan, Malaysia
Tel: +60-3-7955-9390, Fax: +60-3-7955-9510

Renesas Electronics India Pvt. Ltd.
No.777C, 100 Feet Road, HALII Stage, Indiranagar, Bangalore, India
Tel: +91-80-67208700, Fax: +91-80-67208777

Renesas Electronics Korea Co., Ltd.
12F., 234 Teheran-ro, Gangnam-Gu, Seoul, 135-080, Korea
Tel: +82-2-558-3737, Fax: +82-2-558-5141

Colophon 5.0