R9A02G020

ASSP EASY for motor control based on RISC-V

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Rev.1.10
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Ultra low power 32 MHz RISC-V Andes N22 core, 48-KB code flash memory, 16 KB SRAM, 12-bit A/D Converter, and Safety features.

Features

■ RISC-V Andes N22 Core

- RISC-V instruction-set architecture (RV32I)
- Maximum operating frequency: 32 MHz
- Andes Physical Memory Protection unit (Andes PMP)
- Debug and Trace: RISC-V External Debug Support
- Debug Port: JTAG

■ Memory

- 48-KB code flash memory
- 16 KB SRAM
- Memory protection units
- 128-bit unique ID

■ Connectivity

- Serial Communications Interface (SCI) × 1
  - Asynchronous interfaces
  - 8-bit clock synchronous interface
  - Simple IIC
  - Simple SPI
  - Smart card interface

■ Analog

- 12-bit A/D Converter (ADC12) with 3 sample-and-hold-circuits (S/H)
- Programmable Gain Amplifier (PGA) × 3
- High-Speed Analog Comparator (ACMPHS) × 2
- 8-bit D/A Converter (DAC8) × 2
- Temperature Sensor (TSN)

■ Timers

- General PWM Timer 16-bit (GPT) × 6
- Watchdog Timer (WDT)

■ Safety

- SRAM parity and ECC error check
- Flash area protection
- ADC self-diagnosis function
- Clock Frequency Accuracy Measurement Circuit (CAC)
- Cyclic Redundancy Check (CRC) calculator
- Data Operation Circuit (DOC)
- Port Output Enable for GPT (POEG)
- Independent Watchdog Timer (IWDT)
- GPIO readback level detection
- Register write protection
- Illegal memory access detection

■ System and Power Management

- Low power modes
- Data Transfer Controller (DTC)
- Power-on reset
- Low Voltage Detection (LVD) with voltage settings

■ Multiple Clock Sources

- High-speed on-chip oscillator (HOCO) (24/32/48/64 MHz)
- Middle-speed on-chip oscillator (MOCO) (8 MHz)
- Low-speed on-chip oscillator (LOCO) (32.768 kHz)
- Clock trim function for HOCO
- IWDT-dedicated on-chip oscillator (15 kHz)
- Clock out support

■ Up to 28 pins for general I/O ports

- Open drain, input pull-up

■ Operating Voltage

- VCC: 2.7 to 5.5 V

■ Operating Temperature and Packages

- Ta = -40°C to +125°C
  - 32-pin HWQFN (5 mm × 5 mm, 0.5 mm pitch)
  - 24-pin HWQFN (4 mm × 4 mm, 0.5 mm pitch)

1. Overview

The MCU in this series incorporates an energy-efficient Andes AndesCore™ N22 32-bit core, that is particularly well suited for cost-sensitive and low-power applications, with the following features:

- 48-KB code flash memory
- 16 KB SRAM
- 12-bit A/D Converter (ADC12)
- Analog peripherals

1.1 Function Outline

Table 1.1 RISC-V Andes core

Feature	Functional description
Andes AndesCore N22	• Maximum operating frequency: up to 32 MHz • Andes AndesCore N22: – Revision: 1.4.1 – RISC-V instruction-set architecture (ISA) • RISC-V RV32I base integer instruction set • RISC-V RVC standard extension for compressed instructions • RISC-V RVM standard extension for integer multiplication and division • Andes Performance extension (AndeStar V5 ISA) • Andes CoDense extension (AndeStar V5 ISA) – Physical Memory Protection (PMP), 8 regions – Performance monitors, cycle and instruction count CSRs – Andes StackSafe™ hardware stack protection – Power Brake Extension – Recoverable NMI and Extension – RISC-V external debug support – Debug Port: JTAG • Machine timer: – Driven by MTCLK (LOCO) or ICLK

Table 1.2 Memory

Feature	Functional description
Code flash memory	48-KB of code flash memory.
Option-setting memory	The option-setting memory determines the state of the MCU after a reset.
SRAM	On-chip high-speed SRAM with either parity bit or Error Correction Code (ECC).

Table 1.3 System (1 of 2)

Feature	Functional description
Operating modes	Two operating modes: • Single-chip mode • SCI boot mode
Resets	The MCU provides 12 resets (RES pin reset, power-on reset, independent watchdog timer reset, watchdog timer reset, voltage monitor 0/1/2 resets, SRAM parity error reset, SRAM ECC error reset, bus master MPU error resets, debug reset, software reset).
Low Voltage Detection (LVD)	The Low Voltage Detection (LVD) module monitors the voltage level input to the VCC pin. The detection level can be selected by register settings. The LVD module consists of three separate voltage level detectors (LVD0, LVD1, LVD2). LVD0, LVD1, and LVD2 measure the voltage level input to the VCC pin. LVD registers allow your application to configure detection of VCC changes at various voltage thresholds.
Clocks	• High-speed on-chip oscillator (HOCO) • Middle-speed on-chip oscillator (MOCO) • Low-speed on-chip oscillator (LOCO) • IWDT-dedicated on-chip oscillator • Clock out support

Table 1.3 System (2 of 2)

Feature	Functional description
Clock Frequency Accuracy Measurement Circuit (CAC)	The Clock Frequency Accuracy Measurement Circuit (CAC) counts pulses of the clock to be measured (measurement target clock) within the time generated by the clock selected as the measurement reference (measurement reference clock), and determines the accuracy depending on whether the number of pulses is within the allowable range.When measurement is complete or the number of pulses within the time generated by the measurement reference clock is not within the allowable range, an interrupt request is generated.
Interrupt Controller Unit (ICU)	The Interrupt Controller Unit (ICU) controls which event signals are linked to the Core-Local Interrupt Controller (CLIC), and the Data Transfer Controller (DTC) modules. The ICU also controls non-maskable interrupts.
Low power modes	Power consumption can be reduced in multiple ways, including setting clock dividers, stopping modules, selecting power control mode in normal operation, and transitioning to low power modes.
Register write protection	The register write protection function protects important registers from being overwritten due to software errors. The registers to be protected are set with the Protect Register (PRCR).
Memory Protection Unit (MPU)	The MCU has two memory protection units.
Watchdog Timer (WDT)	The Watchdog Timer (WDT) is a 14-bit down counter that can be used to reset the MCU when the counter underflows because the system has run out of control and is unable to refresh the WDT. In addition, the WDT can be used to generate a non-maskable interrupt or an underflow interrupt.
Independent Watchdog Timer (IWDT)	The Independent Watchdog Timer (IWDT) consists of a 14-bit down counter that must be serviced periodically to prevent counter underflow. The IWDT provides functionality to reset the MCU or to generate a non-maskable interrupt or an underflow interrupt. Because the timer operates with an independent, dedicated clock source, it is particularly useful in returning the MCU to a known state as a fail-safe mechanism when the system runs out of control. The IWDT can be triggered automatically by a reset, underflow, refresh error, or a refresh of the count value in the registers.

Table 1.4 Direct memory access

Feature	Functional description
Data Transfer Controller (DTC)	A Data Transfer Controller (DTC) module is provided for transferring data when activated by an interrupt request.

Table 1.5 Timers

Feature	Functional description
General PWM Timer (GPT)	The General PWM Timer (GPT) is a 16-bit timer with GPT16 × 6 channels.
Port Output Enable for GPT (POEG)	The POEG issues requests to stop output from output pins of the general PWM timer (GPT). The combination of output pins of the POEG to be disabled can be specified from any channel of the GPT.

Table 1.6 Communication interfaces

Feature	Functional description
Serial Communications Interface (SCI)	The Serial Communications Interface (SCI) × 1 channel has asynchronous and synchronous serial interface: ● Asynchronous interfaces (UART and Asynchronous Communications Interface Adapter (ACIA)) ● 8-bit clock synchronous interface ● Simple IIC (master-only) ● Simple SPI ● Smart card interface The smart card interface complies with the ISO/IEC 7816-3 standard for electronic signals and transmission protocol. The data transfer speed can be configured independently using an on-chip baud rate generator.

Table 1.7 Analog

Feature	Functional description
12-bit A/D Converter (ADC12)	A 12-bit successive approximation A/D converter is provided. Up to 10 analog input channels are selectable. Three units of sample-and-hold circuit (S/H) are included, and sampling time can be set for each channel. Input signals can be amplified by 3 channels of the programmable gain amplifier (PGA). Temperature sensor output and internal reference voltage are selectable for conversion.
High-Speed Analog Comparator (ACMPHS)	The High-Speed Analog Comparator (ACMPHS) compares a test voltage with a reference voltage and provides a digital output based on the conversion result. The test voltages can be provided to the comparator from an external source with or without an internal PGA. The reference voltages can be provided to the comparator from internal DAC8 output and an external source. Such flexibility is useful in applications that require go/no-go comparisons to be performed between analog signals without necessarily requiring A/D conversion.
8-bit D/A Converter (DAC8)	Two channels of 8-bit D/A Converter (DAC8) can be used as comparator reference voltage and can be output externally.
Temperature Sensor (TSN)	The on-chip Temperature Sensor (TSN) determines and monitors the die temperature for reliable operation of the device. The sensor outputs a voltage directly proportional to the die temperature, and the relationship between the die temperature and the output voltage is fairly linear. The output voltage is provided to the ADC12 for conversion and can be further used by the end application.

Table 1.8 Data processing

Feature	Functional description
Cyclic Redundancy Check (CRC) calculator	The Cyclic Redundancy Check (CRC) generates CRC codes to detect errors in the data. The bit order of CRC calculation results can be switched for LSB-first or MSB-first communication. Additionally, various CRC-generation polynomials are available. The snoop function allows to monitor the access to specific addresses. This function is useful in applications that require CRC code to be generated automatically in certain events, such as monitoring writes to the serial transmit buffer and reads from the serial receive buffer.
Data Operation Circuit (DOC)	The Data Operation Circuit (DOC) compares, adds, and subtracts 16-bit data. When a selected condition applies, 16-bit data is compared and an interrupt can be generated.

1.2 Block Diagram

Figure 1.1 shows a block diagram of the MCU superset. Some individual devices within the group have a subset of the features.

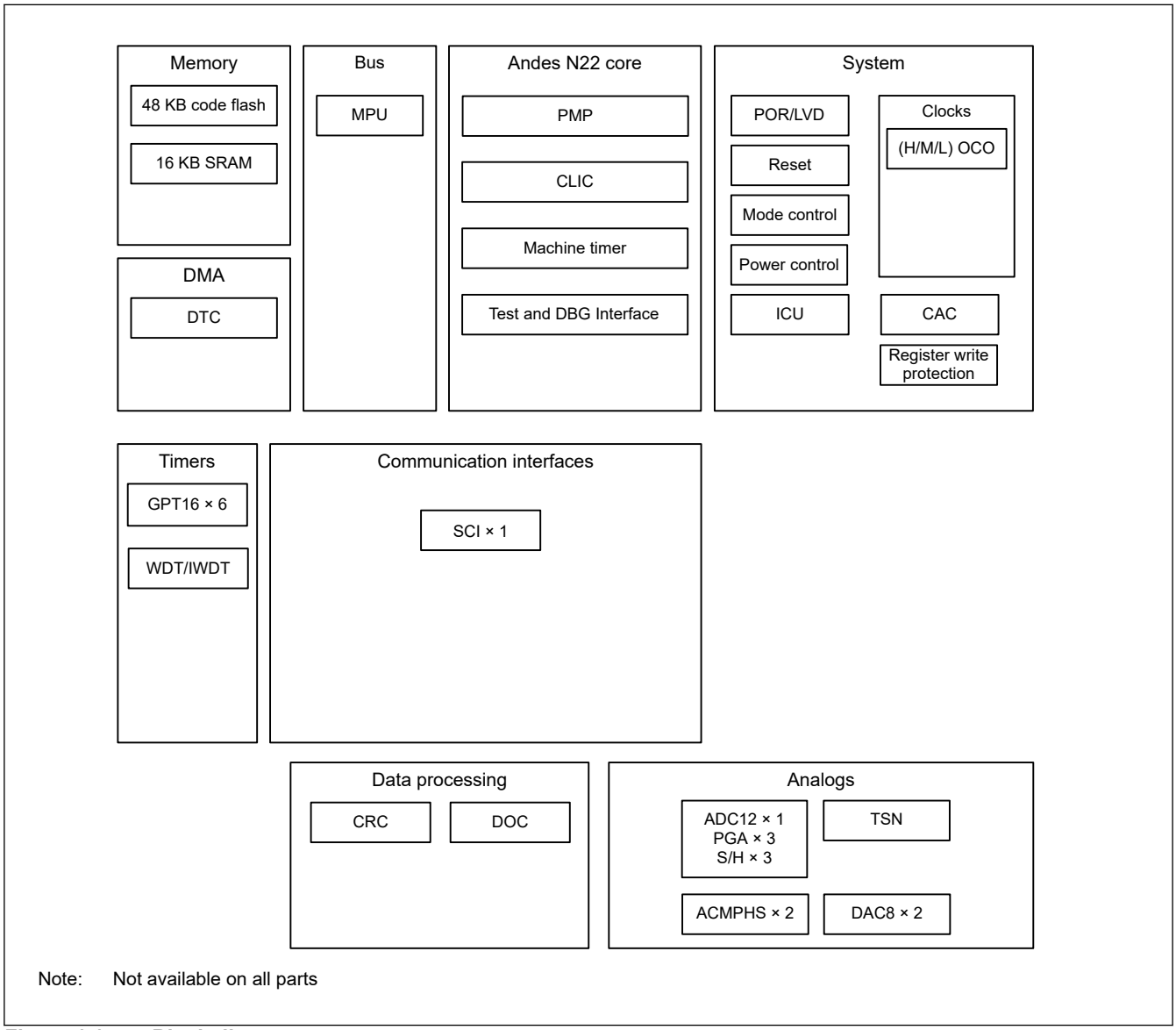


Figure 1.1 Block diagram

1.3 Part Numbering

Figure 1.2 shows the product part number information, including memory capacity and package type. Table 1.9 shows a list of products.

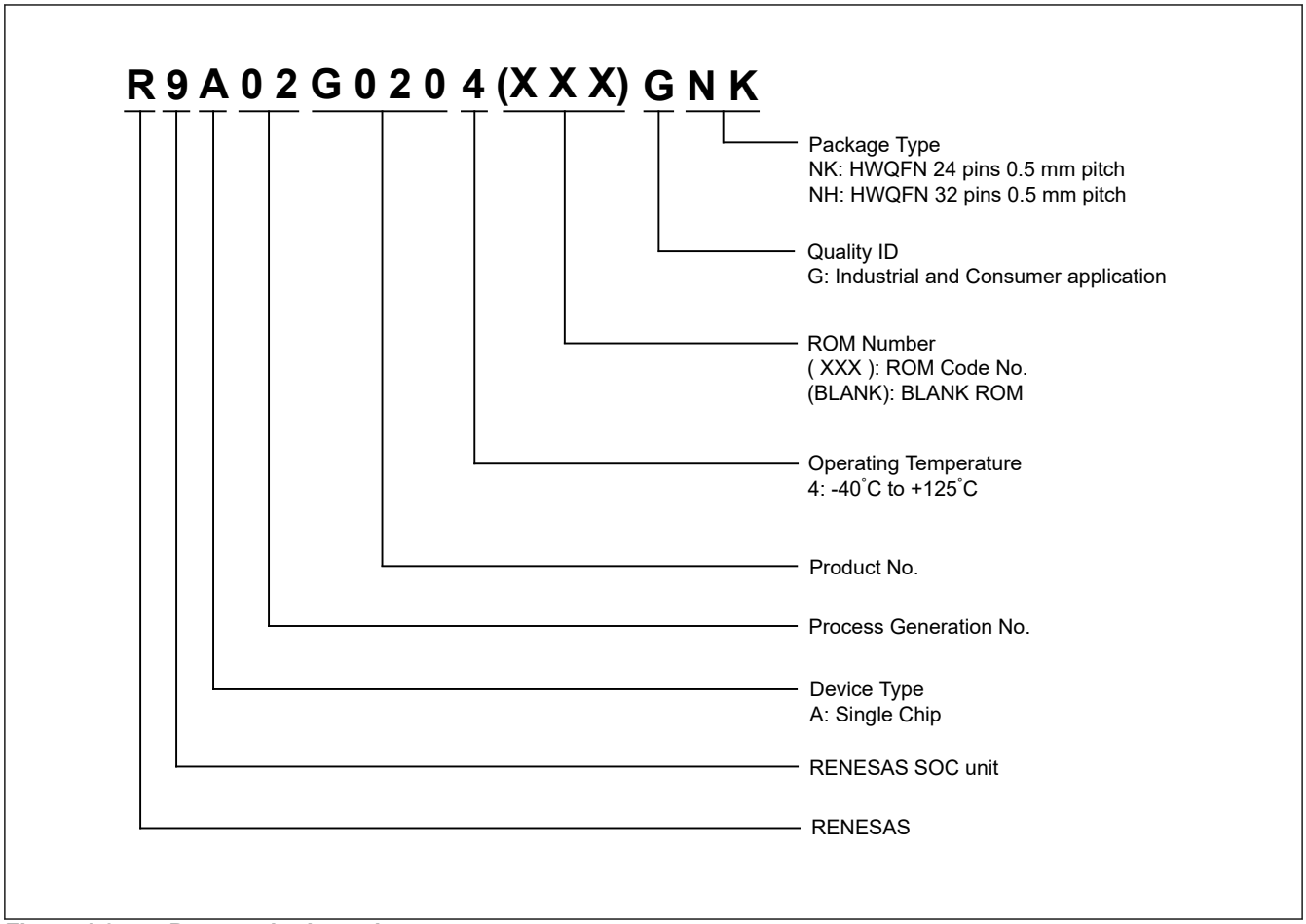


Figure 1.2 Part numbering scheme

Table 1.9 Product list

Product part number	Package code	Code flash	SRAM	Operating temperature
R9A02G0204GNH	PWQN0032KE-A	48	16	-40 to +125°C
R9A02G0204GNK	PWQN0024KG-A			

1.4 Function Comparison

Table 1.10 Function comparison

Part number		R9A02G0204GNH	R9A02G0204GNK
Pin count		32	24
Package		HWQFN	HWQFN
Code flash memory		48 KB	48 KB
SRAM(Parity)		12 KB	12 KB
SRAM (ECC)		4 KB	4 KB
System	CPU clock	32 MHz	32 MHz
	ICU	Yes	Yes
DMA	DTC	Yes	Yes
Timers	GPT16	6 (PWM outputs: 12)	6 (PWM outputs: 12)
	WDT/IWDT	Yes	Yes
Communication	SCI	1	1
Analog	ADC12	10	8
	S/H	3	3
	PGA	3	3
	ACMPHS	2	2
	DAC8	2	2
	TSN	Yes	Yes
Data processing	CRC	Yes	Yes
	DOC	Yes	Yes

1.5 Pin Functions

Table 1.11 Pin functions (1 of 2)

Function	Signal	I/O	Description
Power supply	VCC	Input	Power supply pin. Connect it to the system power supply. Connect this pin to VSS by a 0.1-μF capacitor. Place the capacitor close to the pin.
	VCL	I/O	Connect this pin to the VSS pin by the smoothing capacitor used to stabilize the internal power supply. Place the capacitor close to the pin.
	VSS	Input	Ground pin. Connect it to the system power supply (0 V).
Clock	CLKOUT	Output	Clock output pin
Operating mode control	MD	Input	Pin for setting the operating mode. The signal level on this pin must not be changed during operation mode transition on release from the reset state.
System control	RES	Input	Reset signal input pin. The MCU enters the reset state when this signal goes low.
CAC	CACREF	Input	Measurement reference clock input pin
On-chip debug	TDI	Input	JTAG debug data input pin
	TDO	Output	JTAG debug data output pin
	TMS	Input	JTAG control pin
	TCK	Input	JTAG clock pin
Interrupt	NMI	Input	Non-maskable interrupt request pin
	IRQ0 to IRQ7	Input	Maskable interrupt request pins
GPT	GTETRGA, GTETRGB, GTETRGC, GTETRGD	Input	External trigger input pins
	GTIOCnA (n = 4 to 9), GTIOCnB (n = 4 to 9)	I/O	Input capture, output compare, or PWM output pins
	GTIU	Input	Hall sensor input pin U
	GTIV	Input	Hall sensor input pin V
	GTIW	Input	Hall sensor input pin W
	GTOUUP	Output	3-phase PWM output for BLDC motor control (positive U phase)
	GTOULO	Output	3-phase PWM output for BLDC motor control (negative U phase)
	GTOVUP	Output	3-phase PWM output for BLDC motor control (positive V phase)
	GTOVLO	Output	3-phase PWM output for BLDC motor control (negative V phase)
	GTOWUP	Output	3-phase PWM output for BLDC motor control (positive W phase)
	GTOWLO	Output	3-phase PWM output for BLDC motor control (negative W phase)

Table 1.11 Pin functions (2 of 2)

Function	Signal	I/O	Description
SCI	SCKn (n = 9)	I/O	Input/output pins for the clock (clock synchronous mode)
	RXDn (n = 9)	Input	Input pins for received data (asynchronous mode/clock synchronous mode)
	TXDn (n = 9)	Output	Output pins for transmitted data (asynchronous mode/clock synchronous mode)
	CTSn_RTSn (n = 9)	I/O	Input/output pins for controlling the start of transmission and reception (asynchronous mode/clock synchronous mode), active-low.
	SCLn (n = 9)	I/O	Input/output pins for the IIC clock (simple IIC mode)
	SDAn (n = 9)	I/O	Input/output pins for the IIC data (simple IIC mode)
	SCKn (n = 9)	I/O	Input/output pins for the clock (simple SPI mode)
	MISOn (n = 9)	I/O	Input/output pins for slave transmission of data (simple SPI mode)
	MOSIn (n = 9)	I/O	Input/output pins for master transmission of data (simple SPI mode)
	SSn (n = 9)	Input	Chip-select input pins (simple SPI mode), active-low
Analog power supply	VREFH0	Input	Analog reference voltage supply pin for the ADC12. Connect this pin to VCC when not using the ADC12.
	VREFL0	Input	Analog reference ground pin for the ADC12. Connect this pin to VSS when not using the ADC12.
ADC12	AN000 to AN007, AN016, AN017	Input	Input pins for the analog signals to be processed by the ADC12.
	ADST0	Output	Output pin for A/D conversion status.
	ADTRG0	Input	Input pin for the external trigger signals that start the A/D conversion, active-low.
ACMPHS	CMPREF0, CMPREF1	Input	Reference voltage input pins for comparator
	CMPIN0, CMPIN1	Input	Analog voltage input pins for comparator
	CMPOUT0, CMPOUT1	Output	Comparator detection result output pins.
DAC8	DACOUT0, DACOUT1	Output	Output pins for the analog signals to be processed by the DAC8.
I/O ports	P000 to P007	I/O	General-purpose input/output pins
	P100 to P111	I/O	General-purpose input/output pins
	P200	Input	General-purpose input pin
	P201 to P203	I/O	General-purpose input/output pins
	P300 to P303	I/O	General-purpose input/output pins

1.6 Pin Assignments

Figure 1.3 to Figure 1.4 show the pin assignments from the top view.

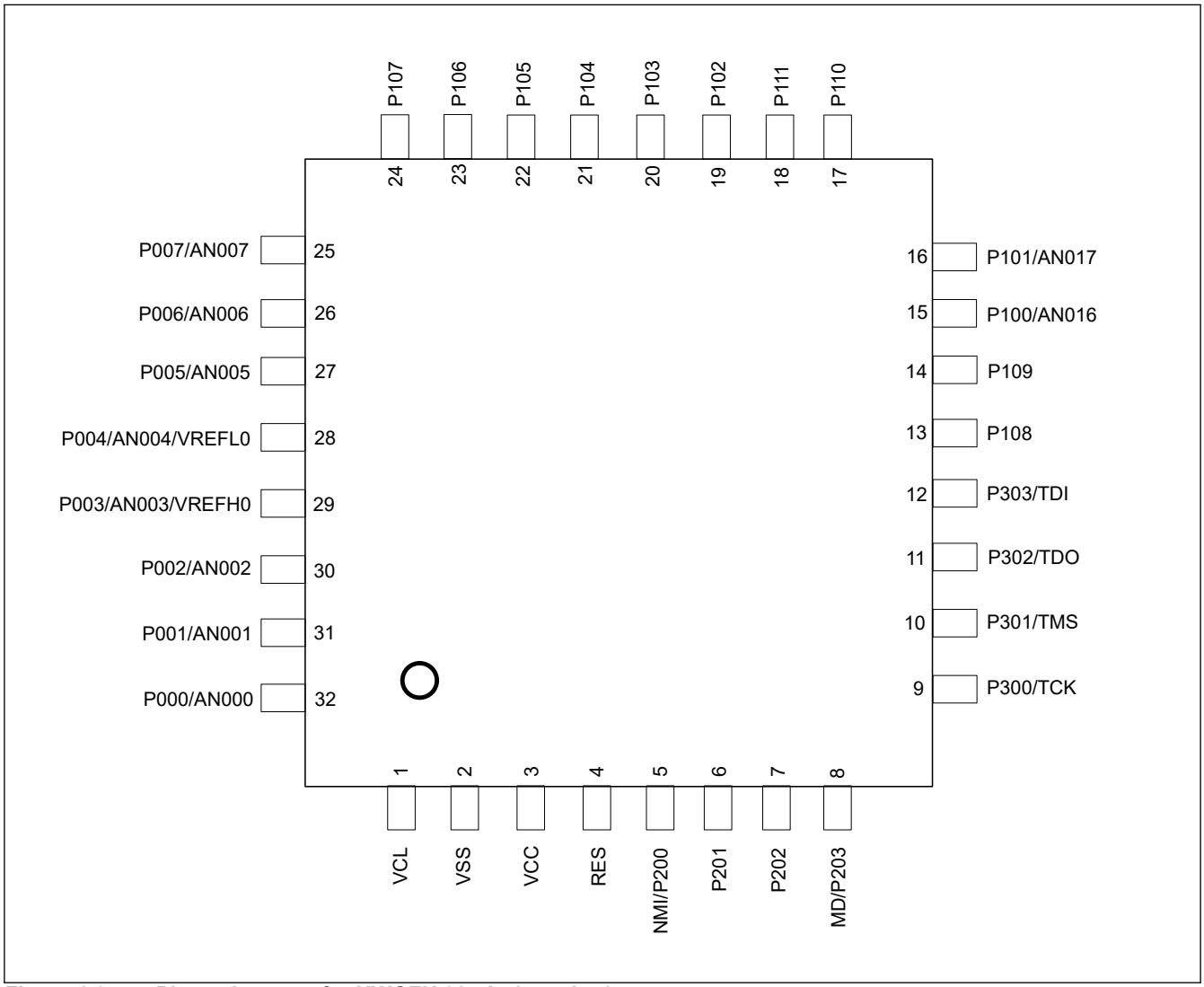


Figure 1.3 Pin assignment for HWQFN 32-pin (top view)

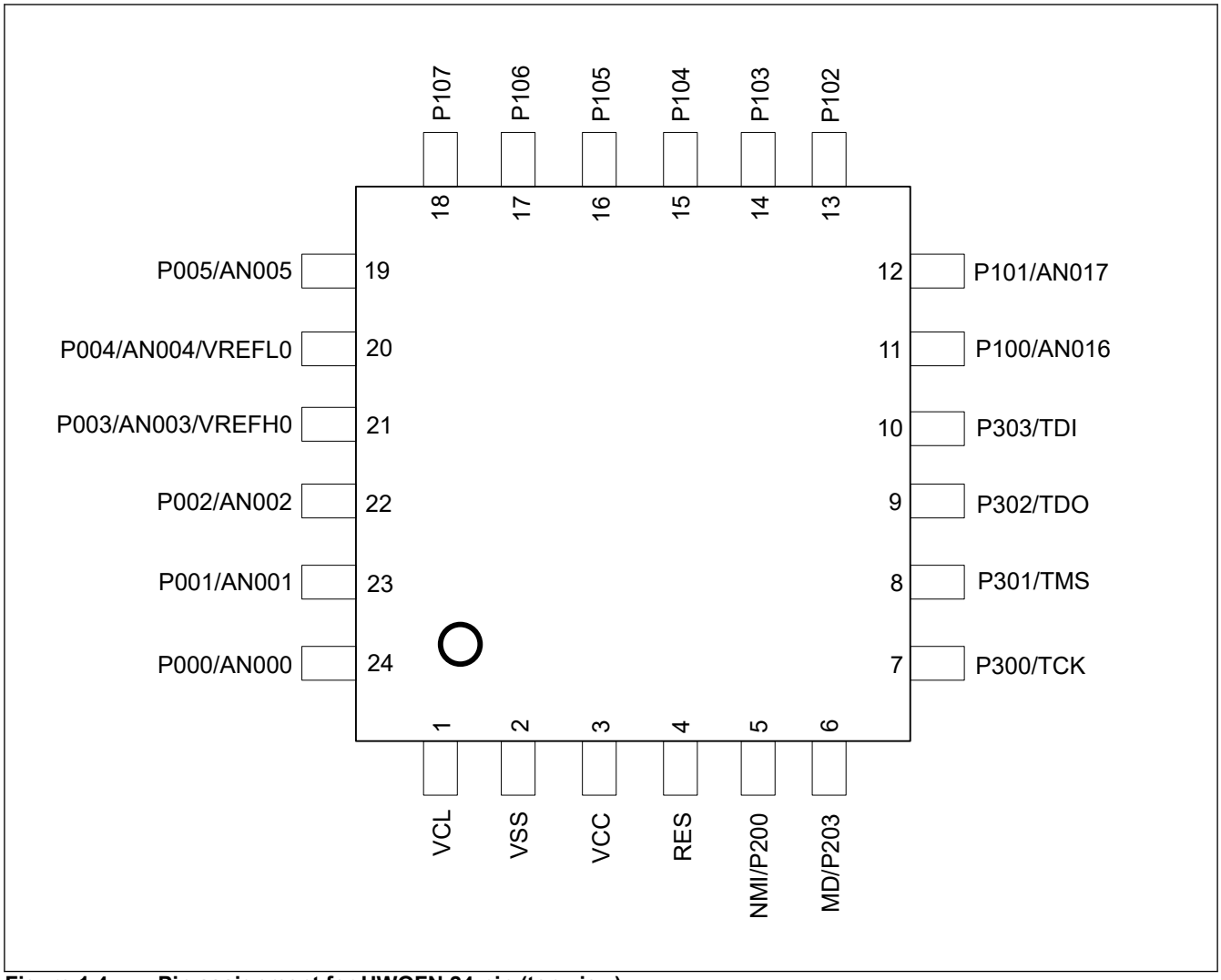


Figure 1.4 Pin assignment for HWQFN 24-pin (top view)

1.7 Pin Lists

Table 1.12 Pin list

Pin number				Timers		Communication interfaces	Analogs			HMI
HWQFN 32-pin	HWQFN 24-pin	Power, System, Clock, Debug, CAC	I/O ports	GPT_OPS, POEG	GPT	SCI9	ADC	CMP	DAC	Interrupt
1	1	VCL	—	—	—	—	—	—	—	—
2	2	VSS/AVSS	—	—	—	—	—	—	—	—
3	3	VCC/AVCC	—	—	—	—	—	—	—	—
4	4	RES#	—	—	—	—	—	—	—	—
5	5	—	P200	GTETRGA_A	—	—	ADTRG_A	—	—	NMI
6	—	—	P201	GTETRGB_C	GTIOC9A_B	RXD9_D	—	CMPOUT1_C	—	IRQ3_C
7	—	CLKOUT_B	P202	GTETRGB_B	GTIOC9B_B	TXD9_D	ADTRG_C	—	—	IRQ2_C
8	6	MD	P203	—	—	—	—	—	—	—
9	7	TCK	P300	GTETRGA_C	GTIOC8A_C	SCK9_A	—	CMPOUT0_C	—	IRQ0_A
10	8	TMS	P301	GTETRGB_A	GTIOC8B_C	RTS_CTS9_A	—	—	—	IRQ1_A
11	9	TDO	P302	—	GTIOC5B_B, GTIOC7B_A	TXD9_A	—	—	—	IRQ3_B
12	10	TDI, CLKOUT_A	P303	—	GTIOC5A_B, GTIOC7A_A	RXD9_A	—	—	—	IRQ2_B
13	—	—	P108	GTETRGA_D	GTIOC7A_B	SCK9_D, CTS9_F	—	CMPOUT0_D	—	IRQ4_B
14	—	—	P109	GTETRGB_D	GTIOC7B_B	RTS_CTS9_D, SCK9_F	—	CMPOUT1_D	—	IRQ5_B
15	11	—	P100	GTETRGA_B	GTIOC9A_A	RXD9_B	AN016, ADTRG_B	CMPOUT1_A	DACOUT0	IRQ6_C
16	12	—	P101	GTIU	GTIOC9B_A	TXD9_B	AN017, ADST_A	CMPOUT0_A	DACOUT1	IRQ7_C
17	—	—	P110	GTIV	GTIOC8B_A	RXD9_F	—	—	—	IRQ7_B
18	—	—	P111	GTIW	GTIOC8A_A	TXD9_F	ADST_C	—	—	IRQ6_B
19	13	—	P102	GTOUUP	GTIOC4B_A	SCK9_B	—	CMPOUT0_B	—	IRQ2_A
20	14	—	P103	GTOULO	GTIOC4A_A	RTS_CTS9_B	—	CMPOUT1_B	—	IRQ3_A
21	15	—	P104	GTOVUP	GTIOC5B_A	SCK9_C, CTS9_E	ADST_B	—	—	IRQ4_A
22	16	—	P105	GTOVLO	GTIOC5A_A	RTS_CTS9_C, SCK9_E	—	—	—	IRQ5_A
23	17	—	P106	GTOWUP	GTIOC6B_A	TXD9_C, RXD9_E	—	—	—	IRQ6_A
24	18	CACREF	P107	GTOWLO	GTIOC6A_A	RXD9_C, TXD9_E	—	—	—	IRQ7_A
25	—	—	P007	—	—	—	AN007	—	—	—
26	—	—	P006	—	—	—	AN006	—	—	—
27	19	—	P005	—	—	—	AN005	CMPIN0_B, CMPIN1_D, CMPREF0, CMPREF1_B	—	—
28	20	VREFL0	P004	—	—	—	AN004	CMPIN1_C, CMPREF1_A	—	—
29	21	VREFH0	P003	—	—	—	AN003	—	—	—
30	22	—	P002	—	—	—	AN002	CMPIN1_B	—	—
31	23	—	P001	—	—	—	AN001	CMPIN1_A	—	—
32	24	—	P000	—	—	—	AN000	CMPIN0_A	—	—

Note: Several pin names have the added suffix of _A, _B, _C, _D, _E, and _F. The suffix can be ignored when assigning functionality.

2. Electrical Characteristics

Unless otherwise specified, the electrical characteristics of the MCU are defined under the following conditions:

VCC[*1] = 2.7 to 5.5 V, VREFH0 = 2.7 V to VCC

VSS = VREFL0 = 0 V, Ta = T_{opr}

Note 1. The typical condition is set to VCC = 3.3 V.

Figure 2.1 shows the timing conditions.

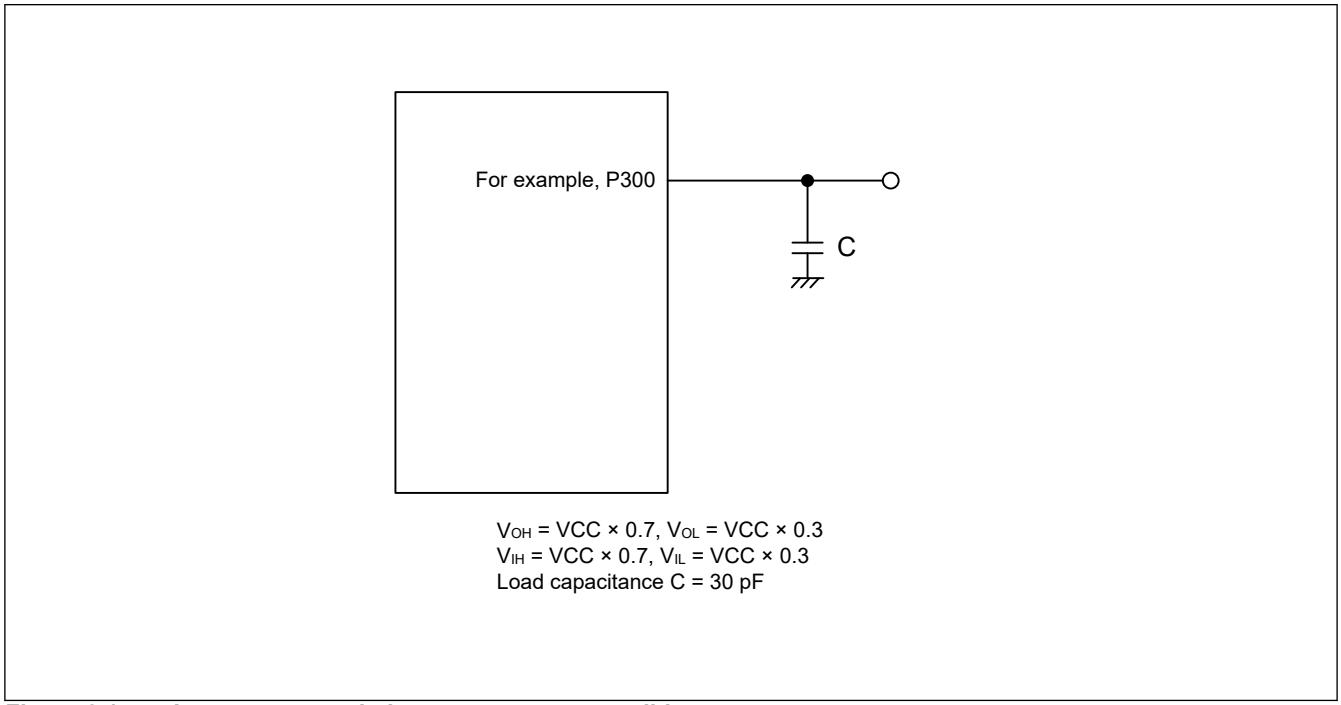


Figure 2.1 Input or output timing measurement conditions

The measurement conditions of the timing specifications for each peripheral are recommended for the best peripheral operation. However, make sure to adjust driving abilities for each pin to meet the conditions of your system.

Each function pin used for the same function must select the same drive ability. If the I/O drive ability of each function pin is mixed, the AC characteristics of each function are not guaranteed.

2.1 Absolute Maximum Ratings

Table 2.1 Absolute maximum ratings

Parameter	Symbol	Value	Unit
Power supply voltage	VCC	-0.5 to +6.5	V
Input voltage	V_{in}	-0.3 to VCC + 0.3	V
Reference power supply voltage	VREFH0	-0.3 to VCC + 0.3	V
Analog input voltage	V_{AN}	-0.3 to VCC + 0.3	V
Operating temperature[*1]	T_{opr}	-40 to +125	°C
Storage temperature	T_{stg}	-55 to +140	°C

Note 1. See section 2.2.1. Tj/Ta Definition.
Note 2.

Caution: Permanent damage to the MCU may result if absolute maximum ratings are exceeded.

To preclude any malfunctions due to noise interference, insert capacitors with high frequency characteristics between the VCC and VSS pins, and between the VREFH0 and VREFL0 pins when VREFH0

is selected as the high potential reference voltage for the ADC12. Place capacitors of the following value as close as possible to every power supply pin and use the shortest and heaviest possible traces:

- **VCC and VSS: about 0.1 µF**
- **VREFH0 and VREFL0: about 0.1 µF**

Also, connect capacitors as stabilization capacitance.

Connect the VCL pin to a VSS pin by a 4.7 µF capacitor. Each capacitor must be placed close to the pin.

Table 2.2 Recommended operating conditions

Parameter	Symbol		Min	Typ	Max	Unit
Power supply voltages	VCC		2.7	—	5.5	V
	VSS		—	0	—	V
Analog power supply voltages	VREFH0	When used as ADC12 Reference	2.7	—	VCC	V
	VREFL0		—	0	—	V

2.2 DC Characteristics

2.2.1 Tj/Ta Definition

Table 2.3 DC characteristics

Conditions: Products with operating temperature (Ta) -40 to +105°C

Parameter	Symbol	Typ	Max	Unit	Test conditions
Permissible junction temperature	Tj	—	140	°C	High-speed mode Middle-speed mode Low-speed mode

Note: Make sure that Tj = T_a + θja × total power consumption (W), where total power consumption = (VCC - V_{OH}) × ΣI_{OH} + V_{OL} × ΣI_{OL} + I_{CC}max × VCC.

2.2.2 I/O V_{IH}, V_{IL}

Table 2.4 I/O V_{IH}, V_{IL}

Conditions: VCC = 2.7 to 5.5 V

Parameter		Symbol	Min	Typ	Max	Unit	Test Conditions
Schmitt trigger input voltage	RES, NMI All peripheral input pins	V_{IH}	VCC × 0.8	—	—	V	—
		V_{IL}	—	—	VCC × 0.2		
Input voltage (except for Schmitt trigger input pin)	Input ports pins	V_{IH}	VCC × 0.8	—	—		—
		V_{IL}	—	—	VCC × 0.2		

2.2.3 I/O I_{OH}, I_{OL}

Table 2.5 I/O I_{OH}, I_{OL} (1 of 2)

Conditions: VCC = 2.7 to 5.5 V

Parameter		Symbol	Min	Typ	Max	Unit	Test conditions
Permissible output current (average value per pin)	Ports P000 to P007	I_{OH}	—	—	-4.0	mA	
		I_{OL}	—	—	8.0	mA	
	Other output pins*1	I_{OH}	—	—	-4.0	mA	
		I_{OL}	—	—	20.0	mA	

Table 2.5 I/O I_{OH}, I_{OL} (2 of 2)

Conditions: VCC = 2.7 to 5.5 V

Parameter		Symbol	Min	Typ	Max	Unit	Test conditions
Permissible output current (max value total pins)*1	Total of ports P000 to P007	$\Sigma I_{OH\ (max)}$	—	—	-24.0	mA	VCC = 2.7 to 5.5 V
		$\Sigma I_{OL\ (max)}$	—	—	48.0	mA	VCC = 2.7 to 5.5 V
	Total of other output ports	$\Sigma I_{OH\ (max)}$	—	—	-30.0	mA	VCC = 2.7 to 5.5 V
		$\Sigma I_{OL\ (max)}$	—	—	50.0	mA	VCC = 2.7 to 5.5 V
	Total of all output pin	$\Sigma I_{OH\ (max)}$	—	—	-50.0	mA	—
		$\Sigma I_{OL\ (max)}$	—	—	95.0	mA	—

Note 1. Specification under conditions where the duty factor ≤ 70%.
The output current value that has changed to the duty factor > 70% the duty ratio can be calculated with the following expression (when changing the duty factor from 70% to n%).
Total output current of pins = (I_{OH} × 0.7)/(n × 0.01)
<Example> Where n = 80% and I_{OH} = −30.0 mA
Total output current of pins = (−30.0 × 0.7)/(80 × 0.01) ≅ −26.2 mA
However, the current that is allowed to flow into one pin does not vary depending on the duty factor.

Caution: To protect the reliability of the MCU, the output current values should not exceed the values in Table 2.5.

2.2.4 I/O V_{OH}, V_{OL}, and Other Characteristics

Table 2.6 I/O V_{OH}, V_{OL} (1)

Conditions: VCC = 4.0 to 5.5 V

Parameter		Symbol	Min	Typ	Max	Unit	Test conditions
Output voltage	Output pins*1	V_{OH}	VCC - 0.8	—	—	V	I_{OH} = -4.0 mA
	P000 to P007	V_{OL}	—	—	0.8		I_{OL} = 8.0 mA
	Output pins except for P000 to P007*1	V_{OL}	—	—	1.2		I_{OL} = 20.0 mA

Note 1. Except for Port P200, which is input port.

Table 2.7 I/O V_{OH}, V_{OL} (2)

Conditions: VCC = 2.7 to 4.0 V

Parameter		Symbol	Min	Typ	Max	Unit	Test conditions
Output voltage	Output pins*1	V_{OH}	VCC - 0.8	—	—	V	I_{OH} = -4.0 mA
	Output pins*1	V_{OL}	—	—	0.8		I_{OL} = 8.0 mA

Note 1. Except for Port P200, which is input port.

Table 2.8 I/O other characteristics

Conditions: VCC = 2.7 to 5.5 V

Parameter		Symbol	Min	Typ	Max	Unit	Test conditions
Input leakage current	RES, P200	$\lvert I_{in} \rvert$	—	—	1.0	µA	V_{in} = 0 V V_{in} = VCC
Three-state leakage current (off state)	All ports (except for P200)	$\lvert I_{TSI} \rvert$	—	—	1.0	µA	V_{in} = 0 V V_{in} = VCC
Input pull-up resistor	All ports (except for P200)	R_U	10	20	100	kΩ	V_{in} = 0 V
Input capacitance	P200	C_{in}	—	—	30	pF	V_{in} = 0 V f = 1 MHz T_a = 25°C
	Other input pins		—	—	15		

2.2.5 Operating and Standby Current

Table 2.9 Operating and standby current (1)

Conditions: VCC = 2.7 to 5.5 V

Parameter					Symbol	Typ*8	Max	Unit	Test Conditions
Supply current*1	High-speed mode*2	Normal mode	All peripheral clocks disabled, CoreMark code executing from flash*5	ICLK = 32 MHz	I_{CC}	3.46	—	mA	*5 *9
				ICLK = 16 MHz		2.20	—		
				ICLK = 8 MHz		1.50	—		
			All peripheral clocks enabled, code executing from flash	ICLK = 32 MHz		—	11.82		*7 *9
		Sleep mode	All peripheral clocks disabled	ICLK = 32 MHz		0.89	—		*5
				ICLK = 16 MHz		0.71	—		
				ICLK = 8 MHz		0.62	—		
			All peripheral clocks enabled	ICLK = 32 MHz		2.20	—		*6
				ICLK = 16 MHz		1.34	—		
				ICLK = 8 MHz		0.89	—		
	Middle-speed mode*2	Normal mode	All peripheral clocks disabled, CoreMark code executing from flash	ICLK = 24 MHz	I_{CC}	2.65	—	mA	*5 *9
				ICLK = 4 MHz		0.81	—		
			All peripheral clocks enabled, code executing from flash	ICLK = 24 MHz		—	8.76		*6 *9
		Sleep mode	All peripheral clocks disabled	ICLK = 24 MHz		0.73	—		*5
				ICLK = 4 MHz		0.57	—		
			All peripheral clocks enabled	ICLK = 24 MHz		1.71	—		*6
				ICLK = 4 MHz		0.67	—		
	Low-speed mode*3	Normal mode	All peripheral clocks disabled, CoreMark code executing from flash	ICLK = 1 MHz	I_{CC}	0.20	—	mA	*5 *9
			All peripheral clocks enabled, code executing from flash	ICLK = 1 MHz		—	5.13		*6 *9
		Sleep mode	All peripheral clocks disabled	ICLK = 1 MHz		0.13	—		*5
			All peripheral clocks enabled	ICLK = 1 MHz		0.15	—		*6

Note 1. Supply current is the total current flowing into VCC. Supply current values apply when internal pull-up MOSs are in the off state and these values do not include output charge/discharge current from any of the pins.
Note 2. The clock source is HOCO.
Note 3. The clock source is MOCO.
Note 4. The clock source is LOCO.
Note 5. PCLKB and PCLKD are set to divided by 64.
Note 6. PCLKB and PCLKD are the same frequency as that of ICLK.
Note 7. PCLKB are set to be divided by 2 and PCLKD is the same frequency as that of ICLK.
Note 8. VCC = 3.3 V.
Note 9. The prefetch is operating.

Table 2.10 Operating and standby current (2)

Conditions: VCC = 2.7 to 5.5 V

Parameter					Symbol	Typ*3	Max	Unit	Test conditions
Supply current *1	Software Standby mode*2	Peripheral modules stop	All SRAM (0x2000_0000 to 0x2000_0FFF and 0x2000_4000 to 0x2000_6FFF) is on	T_a = 25°C	I_{CC}	0.25	1.30	µA	—
				T_a = 55°C		0.40	4.90		
				T_a = 85°C		1.07	18.53		
				T_a = 105°C		2.42	39.03		
				T_a = 125°C		5.30	84.62		
			8KB SRAM (0x2000_0000 to 0x2000_0FFF and 0x2000_4000 to 0x2000_4FFF) is on	T_a = 25°C		0.25	1.30		
				T_a = 55°C		0.40	4.74		
				T_a = 85°C		1.07	17.73		
				T_a = 105°C		2.42	37.57		
				T_a = 125°C		5.30	82.09		

Note 1. Supply current is the total current flowing into VCC. Supply current values apply when internal pull-up MOSs are in the off state and these values do not include output charge/discharge current from any of the pins.
Note 2. The IWDT and LVD are not operating.
Note 3. VCC = 3.3 V.

Table 2.11 Operating and standby current (3)

Conditions: VCC = 2.7 to 5.5 V

Parameter		Symbol	Min	Typ	Max	Unit	Test conditions
Analog power supply current	During 12-bit A/D conversion (at high-speed conversion)	I_{VCCAD}	—	—	1.44	mA	—
	During 12-bit A/D conversion (at low-power conversion)		—	—	0.78	mA	—
	Waiting for 12-bit A/D conversion (all units)*1		—	—	1.00	µA	—
	PGA enabled (per channel)	I_{VCCPGA}	—	—	0.80	mA	—
	S/H enabled (per channel)	I_{VCCSH}	—	—	1.50	mA	—
	ACMPHS enabled (per channel)	I_{VCCCMP}	—	—	0.15	mA	—
	DAC8 enabled (per channel)	I_{VCCCMP}	—	—	0.50	mA	—
Reference power supply current	During 12-bit A/D conversion	I_{REFH0}	—	—	120	µA	—
	Waiting for 12-bit A/D conversion		—	—	0.3	µA	—
Temperature Sensor (TSN) operating current		I_{TNS}	—	95	—	µA	—

Note 1. When the MCU is in Software Standby mode or the MSTPCRD.MSTPD16 (ADC12 module-stop bit) is in the module-stop state.

2.2.6 VCC Rise and Fall Gradient and Ripple Frequency

Table 2.12 Rise and fall gradient characteristics

Conditions: VCC = 0 to 5.5 V

Parameter		Symbol	Min	Typ	Max	Unit	Test conditions
Power-on VCC rising gradient	Voltage monitor 0 reset disabled at startup	SrVCC	0.02	—	2	ms/V	—
	Voltage monitor 0 reset enabled at startup*1 *2				—		
	SCI boot mode*2				2		

Note 1. When OFS1.LVDAS = 0.
Note 2. At boot mode, the reset from voltage monitor 0 is disabled regardless of the value of OFS1.LVDAS bit.

Table 2.13 Rising and falling gradient and ripple frequency characteristics

Conditions: VCC = 2.7 to 5.5 V
The ripple voltage must meet the allowable ripple frequency $f_{r(VCC)}$ within the range between the VCC upper limit (5.5 V) and lower limit (2.7 V).
When the VCC change exceeds VCC ± 10%, the allowable voltage change rising and falling gradient dt/dVCC must be met.

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
Allowable ripple frequency	$f_{r(VCC)}$	—	—	10	kHz	Figure 2.2 $V_{r\ (VCC)} \leq VCC \times 0.2$
		—	—	1	MHz	Figure 2.2 $V_{r\ (VCC)} \leq VCC \times 0.08$
		—	—	10	MHz	Figure 2.2 $V_{r\ (VCC)} \leq VCC \times 0.06$
Allowable voltage change rising and falling gradient	dt/dVCC	1.0	—	—	ms/V	When VCC change exceeds VCC ± 10%

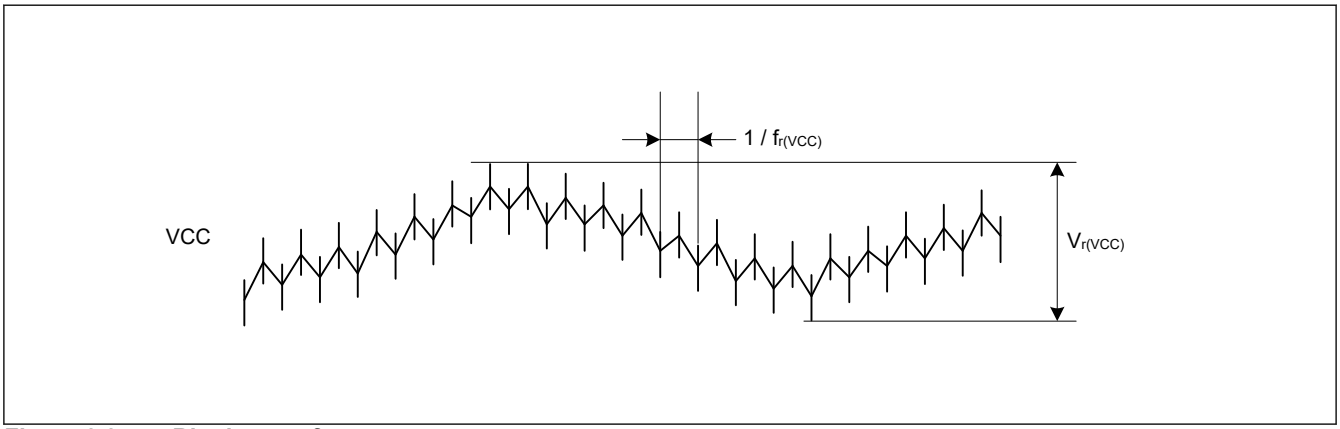


Figure 2.2 Ripple waveform

2.3 AC Characteristics

2.3.1 Frequency

Table 2.14 Operation frequency in high-speed operating mode

Conditions: VCC = 2.7 to 5.5 V

Parameter			Symbol	Min	Typ	Max*4	Unit
Operation frequency	System clock (ICLK)*1*2	2.7 to 5.5 V	f	0.032768	—	32	MHz
	Peripheral module clock (PCLKB)	2.7 to 5.5 V		—	—	32	
	Peripheral module clock (PCLKD)*3	2.7 to 5.5 V		—	—	64	

Note 1. The lower-limit frequency of ICLK is 1 MHz while programming or erasing the flash memory. When using ICLK for programming or erasing the flash memory at below 4 MHz, the frequency can be set to 1 MHz, 2 MHz, or 3 MHz. A non-integer frequency such as 1.5 MHz cannot be set.

Note 2. The frequency accuracy of ICLK must be ± 1.5% during programming or erasing the flash memory. Confirm the frequency accuracy of the clock source.
Note 3. The lower-limit frequency of PCLKD is 1 MHz when the ADC12 is in use.
Note 4. The maximum value of operation frequency does not include internal oscillator errors. For details on the range for guaranteed operation, see Table 2.17.

Table 2.15 Operation frequency in middle-speed mode

Conditions: VCC = 2.7 to 5.5 V

Parameter			Symbol	Min	Typ	Max*4	Unit
Operation frequency	System clock (ICLK)*1*2	2.7 to 5.5 V	f	0.032768	—	24	MHz
	Peripheral module clock (PCLKB)	2.7 to 5.5 V		—	—	24	
	Peripheral module clock (PCLKD)*3	2.7 to 5.5 V		—	—	24	

Note 1. The lower-limit frequency of ICLK is 1 MHz while programming or erasing the flash memory. When using ICLK for programming or erasing the flash memory at below 4 MHz, the frequency can be set to 1 MHz, 2 MHz, or 3 MHz. A non-integer frequency such as 1.5 MHz cannot be set.
Note 2. The frequency accuracy of ICLK must be ± 1.5% while programming or erasing the flash memory. Confirm the frequency accuracy of the clock source.
Note 3. The lower-limit frequency of PCLKD is 1 MHz when the ADC12 is in use.
Note 4. The maximum value of operation frequency does not include internal oscillator errors. For details on the range for guaranteed operation, see Table 2.17.

Table 2.16 Operation frequency in low-speed mode

Conditions: VCC = 2.7 to 5.5 V

Parameter			Symbol	Min	Typ	Max*4	Unit
Operation frequency	System clock (ICLK)*1*2	2.7 to 5.5 V	f	0.032768	—	1	MHz
	Peripheral module clock (PCLKB)	2.7 to 5.5 V		—	—	1	
	Peripheral module clock (PCLKD)*3	2.7 to 5.5 V		—	—	1	

Note 1. The lower-limit frequency of ICLK is 1 MHz while programming or erasing the flash memory.
Note 2. The frequency accuracy of ICLK must be ± 1.5% while programming or erasing the flash memory. Confirm the frequency accuracy of the clock source.
Note 3. The lower-limit frequency of PCLKD is 1 MHz when the ADC12 is in use.
Note 4. The maximum value of operation frequency does not include internal oscillator errors. For details on the range for guaranteed operation, see Table 2.17.

2.3.2 Clock Timing

Table 2.17 Clock timing

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
LOCO clock oscillation frequency	f_{LOCO}	27.8528	32.768	37.6832	kHz	—
LOCO clock oscillation stabilization time	t_{LOCO}	—	—	100	µs	Figure 2.3
IWDT-dedicated clock oscillation frequency	f_{ILOCO}	12.75	15	17.25	kHz	—
MOCO clock oscillation frequency	f_{MOCO}	6.8	8	9.2	MHz	—
MOCO clock oscillation stabilization time	t_{MOCO}	—	—	1	µs	—
HOCO clock oscillation frequency*3	f_{HOCO24}	23.64	24	24.36	MHz	Ta = -40 to 125°C 2.7 ≤ VCC ≤ 5.5
	f_{HOCO32}	31.52	32	32.48		Ta = -40 to 125°C 2.7 ≤ VCC ≤ 5.5
	f_{HOCO48}	47.28	48	48.72		Ta = -40 to 125°C 2.7 ≤ VCC ≤ 5.5
	f_{HOCO64}	63.04	64	64.96		Ta = -40 to 125°C 2.7 ≤ VCC ≤ 5.5
HOCO clock oscillation stabilization time*1 *2	t_{HOCO24} t_{HOCO32} t_{HOCO48} t_{HOCO64}	—	6.7	7.7	µs	Figure 2.4

Note 1. This is a characteristic when the HOCOCR.HCSTP bit is set to 0 (oscillation) in the MOCO stop state. When the HOCOCR.HCSTP bit is set to 0 (oscillation) during MOCO oscillation, this specification is shortened by 1 µs.
Note 2. Check OSCSF.HOCOSF to confirm whether stabilization time has elapsed.
Note 3. Accuracy at production test.

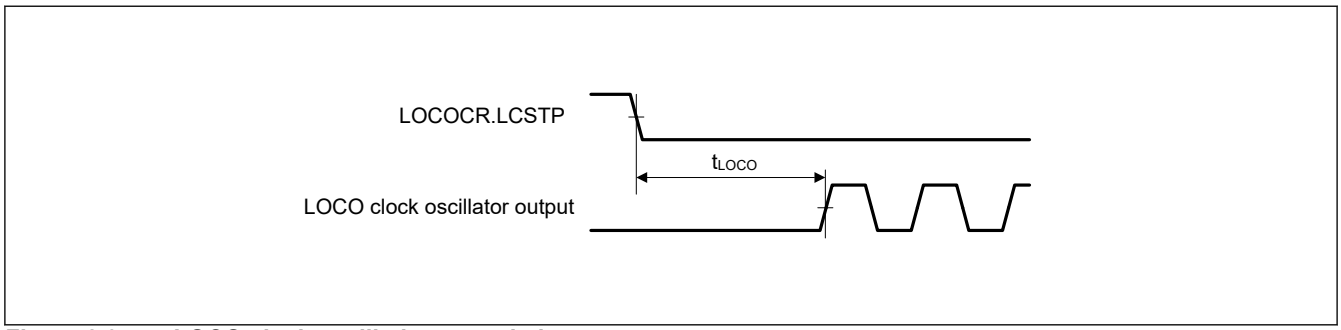


Figure 2.3 LOCO clock oscillation start timing

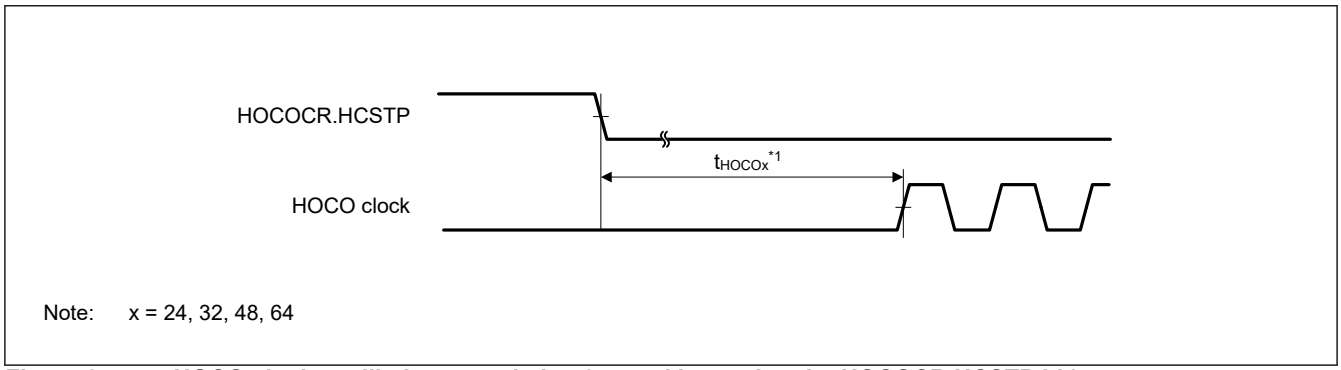


Figure 2.4 HOCO clock oscillation start timing (started by setting the HOCOCR.HCSTP bit)

2.3.3 Reset Timing

Table 2.18 Reset timing

Parameter		Symbol	Min	Typ	Max	Unit	Test conditions
RES pulse width	At power-on	t_{RESWP}	10	—	—	ms	Figure 2.5
	Not at power-on	t_{RESW}	30	—	—	µs	Figure 2.6
Wait time after RES cancellation (at power-on)	LVD0 enabled*1	t_{RESWT}	—	0.9	—	ms	Figure 2.5
	LVD0 disabled*2		—	0.2	—		
Wait time after RES cancellation (during powered-on state)	LVD0 enabled*1	t_{RESWT2}	—	0.9	—	ms	Figure 2.6
	LVD0 disabled*2		—	0.2	—		
Wait time after internal reset cancellation (Watchdog timer reset, SRAM parity error reset, SRAM ECC error reset, bus master MPU error reset, debug reset, software reset)	LVD0 enabled*1	t_{RESWT3}	—	0.9	—	ms	Figure 2.7
	LVD0 disabled*2		—	0.2	—		

Note 1. When OFS1.LVDAS = 0.
Note 2. When OFS1.LVDAS = 1.

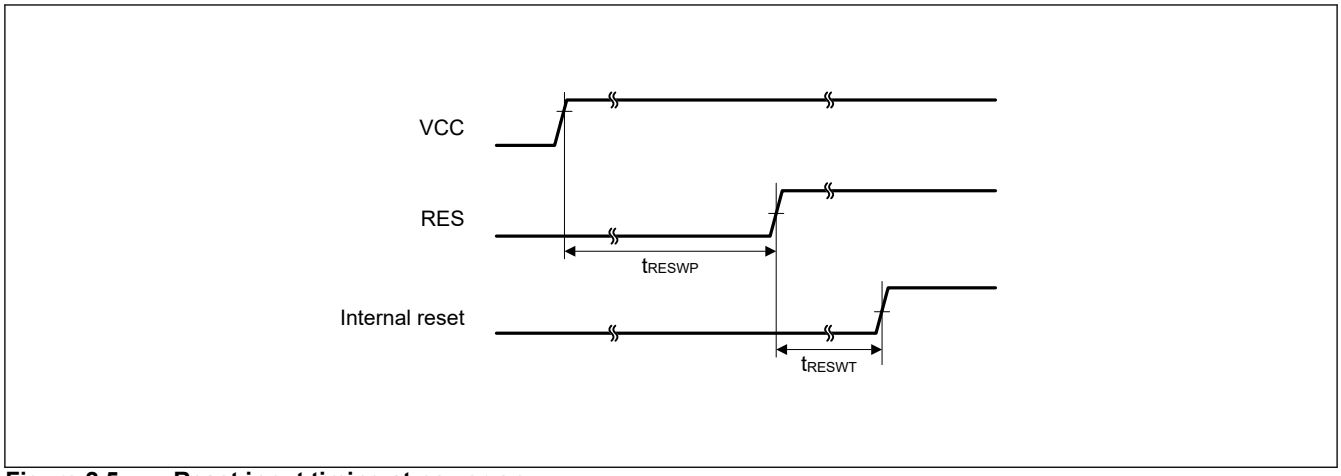


Figure 2.5 Reset input timing at power-on

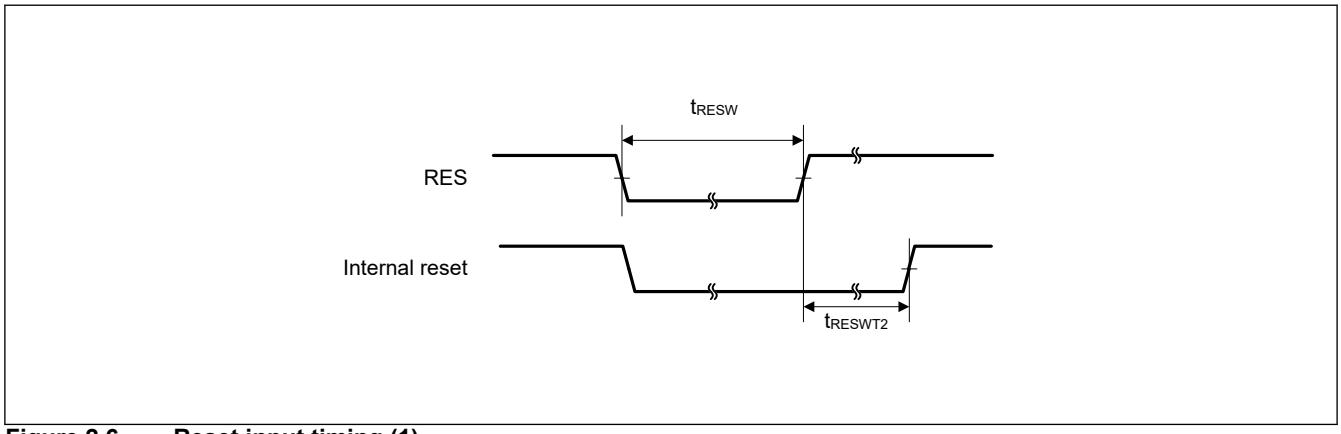


Figure 2.6 Reset input timing (1)

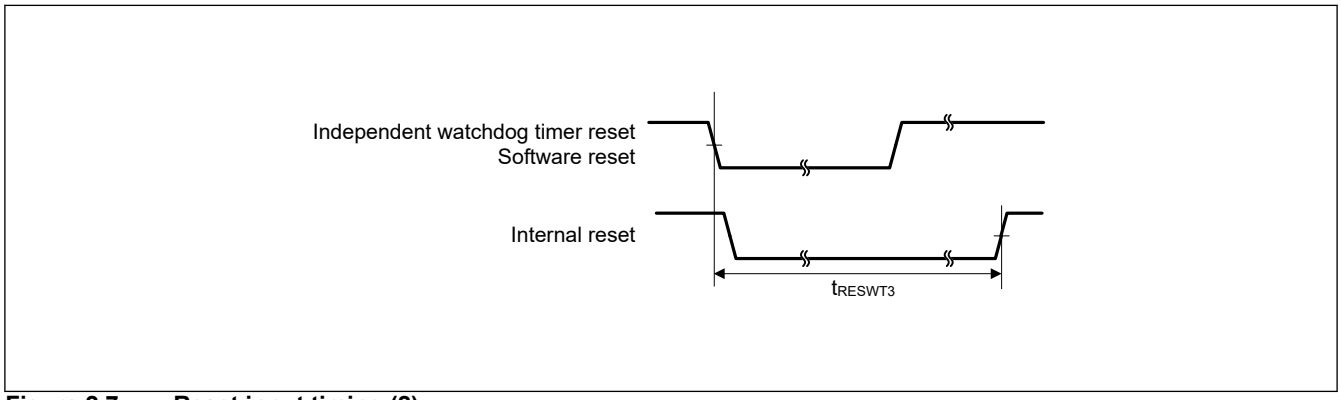


Figure 2.7 Reset input timing (2)

2.3.4 Wakeup Time

Table 2.19 Timing of recovery from low power modes (1)

Parameter			Symbol	Min	Typ	Max	Unit	Test conditions
Recovery time from Software Standby mode*1	High-speed mode	System clock source is HOCO (HOCO clock is 32 MHz)*2	t_{SBYHO}	—	7.9	10.0	µs	Figure 2.8
		System clock source is HOCO (HOCO clock is 48 MHz)*3	t_{SBYHO}	—	8.2	10.3	µs	
		System clock source is HOCO (HOCO clock is 64 MHz)*2	t_{SBYHO}	—	7.9	10.0	µs	
		System clock source is MOCO (8 MHz)	t_{SBYMO}	—	3.8	5.8	µs	

Note 1. The division ratio of ICLK and PCLKx is the minimum division ratio within the allowable frequency range. The recovery time is determined by the system clock source.
Note 2. The system clock is 32 MHz.
Note 3. The system clock is 24 MHz.

Table 2.20 Timing of recovery from low power modes (2)

Parameter				Symbol	Min	Typ	Max	Unit	Test conditions
Recovery time from Software Standby mode*1	Middle-speed mode	System clock source is HOCO*2	VCC = 2.7 V to 5.5 V	t_{SBYHO}	—	8.2	10.3	µs	Figure 2.8
		System clock source is MOCO (8 MHz)	VCC = 2.7 V to 5.5 V	t_{SBYMO}	—	3.8	5.8	µs	

Note 1. The division ratio of ICLK and PCLKx is the minimum division ratio within the allowable frequency range. The recovery time is determined by the system clock source.
Note 2. The system clock is 24 MHz.

Table 2.21 Timing of recovery from low power modes (3)

Parameter			Symbol	Min	Typ	Max	Unit	Test conditions
Recovery time from Software Standby mode*1	Low-speed mode	System clock source is MOCO (1 MHz)	t_{SBYMO}	—	29	40	µs	—

Note 1. The division ratio of ICLK and PCLKx is the minimum division ratio within the allowable frequency range. The recovery time is determined by the system clock source.

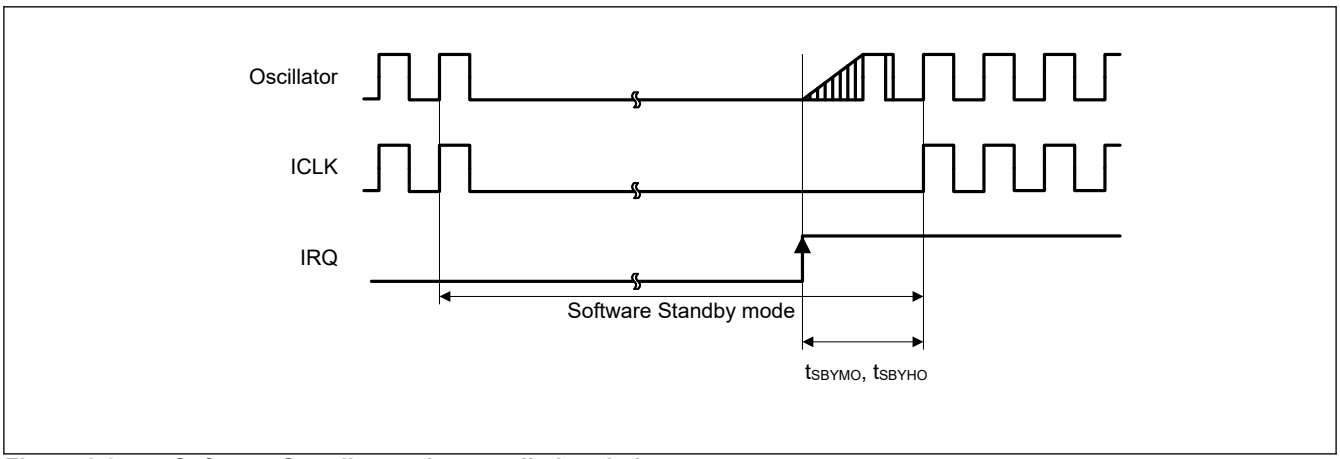


Figure 2.8 Software Standby mode cancellation timing

2.3.5 NMI and IRQ Noise Filter

Table 2.22 NMI and IRQ noise filter

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions	
NMI pulse width	t_{NMIW}	200	—	—	ns	NMI digital filter disabled	$t_{Pcyc} \times 2 \leq 200$ ns
		$t_{Pcyc} \times 2$*1	—	—			$t_{Pcyc} \times 2 > 200$ ns
		200	—	—		NMI digital filter enabled	$t_{NMICK} \times 3 \leq 200$ ns
		$t_{NMICK} \times 3.5$*2	—	—			$t_{NMICK} \times 3 > 200$ ns
IRQ pulse width	t_{IRQW}	200	—	—	ns	IRQ digital filter disabled	$t_{Pcyc} \times 2 \leq 200$ ns
		$t_{Pcyc} \times 2$*1	—	—			$t_{Pcyc} \times 2 > 200$ ns
		200	—	—		IRQ digital filter enabled	$t_{IRQCK} \times 3 \leq 200$ ns
		$t_{IRQCK} \times 3.5$*3	—	—			$t_{IRQCK} \times 3 > 200$ ns

Note: 200 ns minimum in Software Standby mode.
Note: If the clock source is being switched it is needed to add 4 clock cycle of switched source.
Note 1. t_{Pcyc} indicates the PCLKB cycle.
Note 2. t_{NMICK} indicates the cycle of the NMI digital filter sampling clock.
Note 3. t_{IRQCK} indicates the cycle of the IRQi digital filter sampling clock (i = 0 to 7).

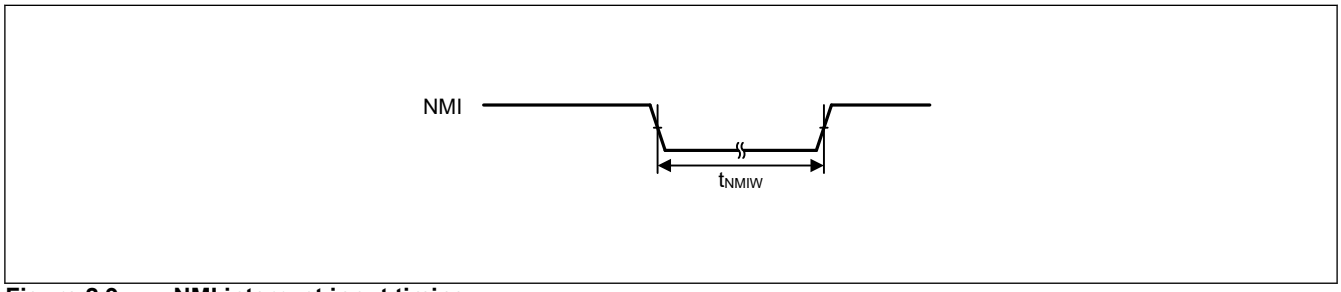


Figure 2.9 NMI interrupt input timing

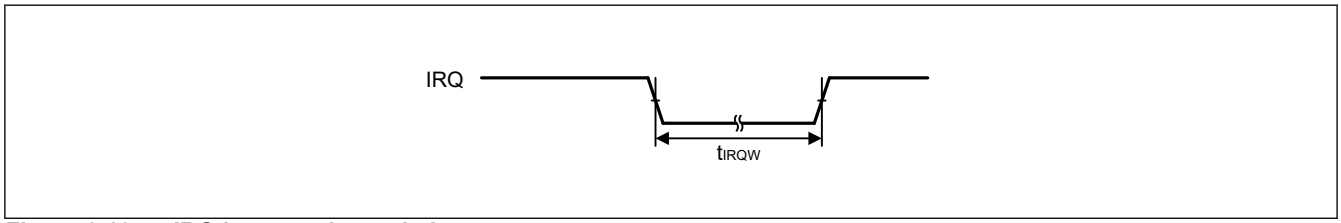


Figure 2.10 IRQ interrupt input timing

2.3.6 I/O Ports, POEG, GPT, and ADC12 Trigger Timing

Table 2.23 I/O Ports, POEG, GPT, and ADC12 trigger timing

Parameter			Symbol	Min	Max	Unit*1	Test conditions
I/O Ports	Input data pulse width	2.7 V ≤ VCC ≤ 5.5 V	t_{PRW}	2	—	t_{Pcyc}	Figure 2.11
POEG	POEG input trigger pulse width		t_{POEW}	3	—	t_{Pcyc}	Figure 2.12
GPT	Input capture pulse width	Single edge	t_{GTICW}	1.5	—	t_{PDcyc}	Figure 2.13
		Dual edge		2.5	—		
ADC12	12-bit A/D converter trigger input pulse width		t_{TRGW}	1.5	—	t_{Pcyc}	Figure 2.14

Note: If the clock source is being switched, add 4 clock cycles to the switched source.
Note 1. t_{Pcyc}: PCLKB cycle
t_{PDcyc}: PCLKD cycle

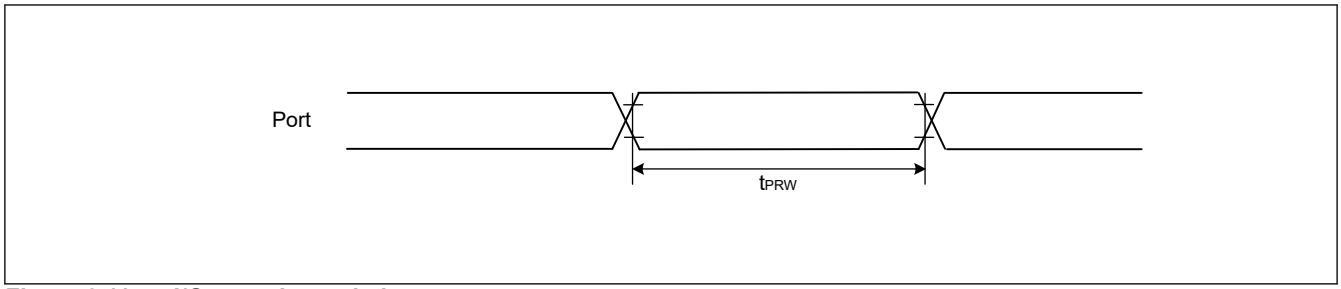


Figure 2.11 I/O ports input timing

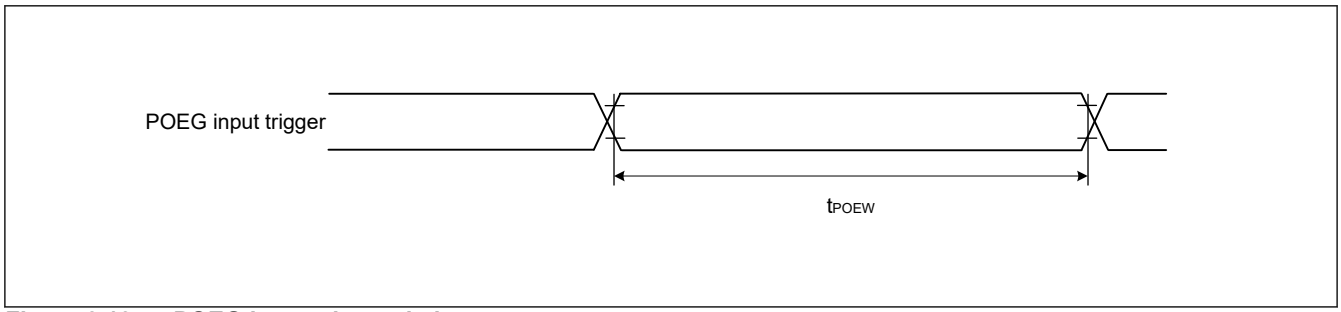


Figure 2.12 POEG input trigger timing

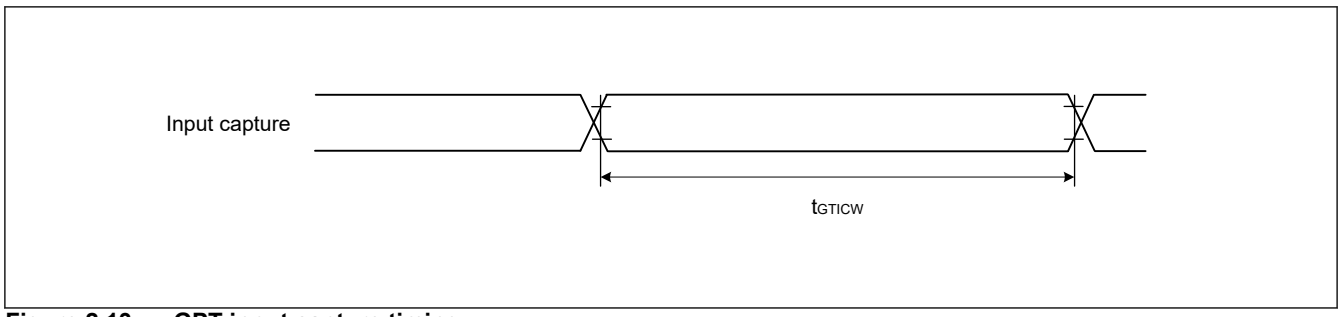


Figure 2.13 GPT input capture timing

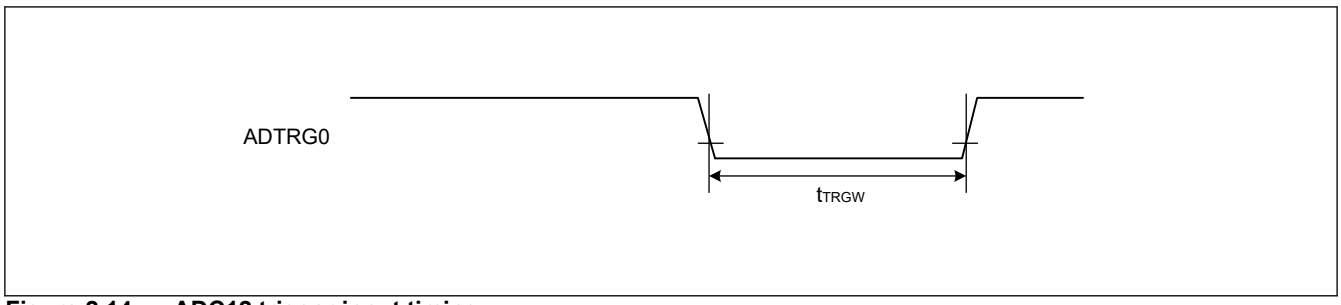


Figure 2.14 ADC12 trigger input timing

2.3.7 CAC Timing

Table 2.24 CAC timing

Conditions: VCC = 2.7 to 5.5 V

Parameter			Symbol	Min	Typ	Max	Unit	Test conditions
CAC	CACREF input pulse width	t_{Pcyc}*1 ≤ t_{CAC}*2	t_{CACREF}	4.5 × t_{CAC} + 3 × t_{Pcyc}	—	—	ns	—
		t_{Pcyc}*1 > t_{CAC}*2		5 × t_{CAC} + 6.5 × t_{Pcyc}	—	—	ns	

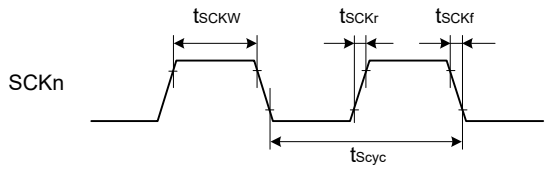
Note 1. t_{Pcyc}: PCLKB cycle.
Note 2. t_{CAC}: CAC count clock source cycle.

2.3.8 SCI Timing

Table 2.25 SCI timing (1)

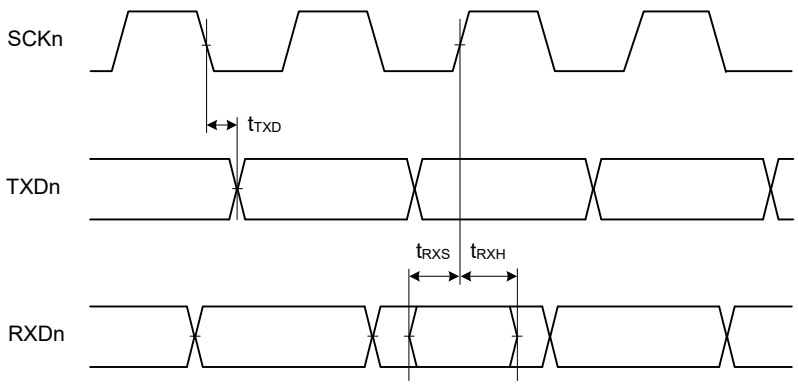
Conditions: VCC = 2.7 to 5.5 V

Parameter				Symbol	Min	Max	Unit	Test conditions
SCI	Input clock cycle	Asynchronous	2.7 V ≤ VCC ≤ 5.5 V	t_{Scyc}	125	—	ns	Figure 2.15
		Clock synchronous	2.7 V ≤ VCC ≤ 5.5 V		187.5	—		
	Input clock pulse width			t_{SCKW}	0.4	0.6	t_{Scyc}	
	Input clock rise time			t_{SCKr}	—	20	ns	
	Input clock fall time			t_{SCKf}	—	20	ns	
	Output clock cycle	Asynchronous	2.7 V ≤ VCC ≤ 5.5 V	t_{Scyc}	187.5	—	ns	
		Clock synchronous	2.7 V ≤ VCC ≤ 5.5 V		125	—		
	Output clock pulse width			t_{SCKW}	0.4	0.6	t_{Scyc}	
	Output clock rise time		2.7 V ≤ VCC ≤ 5.5 V	t_{SCKr}	—	20	ns	
	Output clock fall time		2.7 V ≤ VCC ≤ 5.5 V	t_{SCKf}	—	20	ns	
	Transmit data delay time (master)	Clock synchronous	2.7 V ≤ VCC ≤ 5.5 V	t_{TXD}	—	40	ns	Figure 2.16
	Transmit data delay time (slave)	Clock synchronous	2.7 V ≤ VCC ≤ 5.5 V		—	55	ns	
	Receive data setup time (master)	Clock synchronous	2.7 V ≤ VCC ≤ 5.5 V	t_{RXS}	45	—	ns	
	Receive data setup time (slave)	Clock synchronous	2.7 V ≤ VCC ≤ 5.5 V		40	—	ns	
	Receive data hold time (master)	Clock synchronous		t_{RXH}	5	—	ns	
	Receive data hold time (slave)	Clock synchronous		t_{RXH}	40	—	ns	



Note: n = 9

Figure 2.15 SCK clock input timing



Note: n = 9

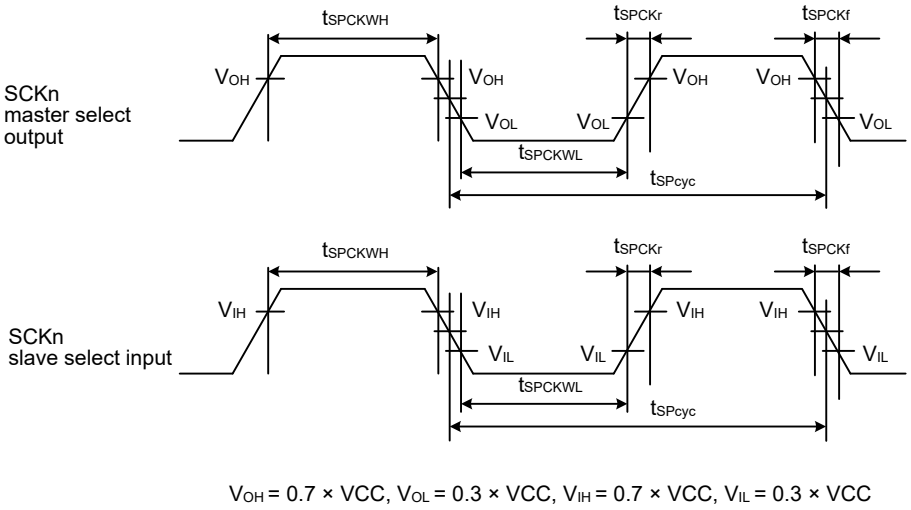
Figure 2.16 SCI input/output timing in clock synchronous mode

Table 2.26 SCI timing (2)

Conditions: VCC = 2.7 to 5.5 V

Parameter				Symbol	Min	Max	Unit*1	Test conditions
Simple SPI	SCK clock cycle output (master)		2.7 V ≤ VCC ≤ 5.5 V	t_{SPcyc}	125	—	ns	Figure 2.17
	SCK clock cycle input (slave)		2.7 V ≤ VCC ≤ 5.5 V		187.5	—		
	SCK clock high pulse width			t_{SPCKWH}	0.4	0.6	t_{SPcyc}	
	SCK clock low pulse width			t_{SPCKWL}	0.4	0.6	t_{SPcyc}	
	SCK clock rise and fall time		2.7 V ≤ VCC ≤ 5.5 V	t_{SPCKr}, t_{SPCKf}	—	20	ns	
	Data input setup time	Master	2.7 V ≤ VCC ≤ 5.5 V	t_{SU}	45	—	ns	Figure 2.18 to Figure 2.21
		Slave	2.7 V ≤ VCC ≤ 5.5 V		40	—		
	Data input hold time	Master		t_H	33.3	—	ns	
		Slave			40	—		
	SS input setup time			t_{LEAD}	1	—	t_{SPcyc}	
	SS input hold time			t_{LAG}	1	—	t_{SPcyc}	
	Data output delay time	Master	2.7 V ≤ VCC ≤ 5.5 V	t_{OD}	—	40	ns	
		Slave	2.7 V ≤ VCC ≤ 5.5 V		—	65		
	Data output hold time	Master	2.7 V ≤ VCC ≤ 5.5 V	t_{OH}	-10	—	ns	
		Slave			-10	—		
	Data rise and fall time	Master	2.7 V ≤ VCC ≤ 5.5 V	t_{Dr}, t_{Df}	—	20	ns	
		Slave	2.7 V ≤ VCC ≤ 5.5 V		—	20		
	Slave access time		2.7 V ≤ VCC ≤ 5.5 V	t_{SA}	—	6	t_{Pcyc}	Figure 2.21
	Slave output release time		2.7 V ≤ VCC ≤ 5.5 V	t_{REL}	—	6	t_{Pcyc}	

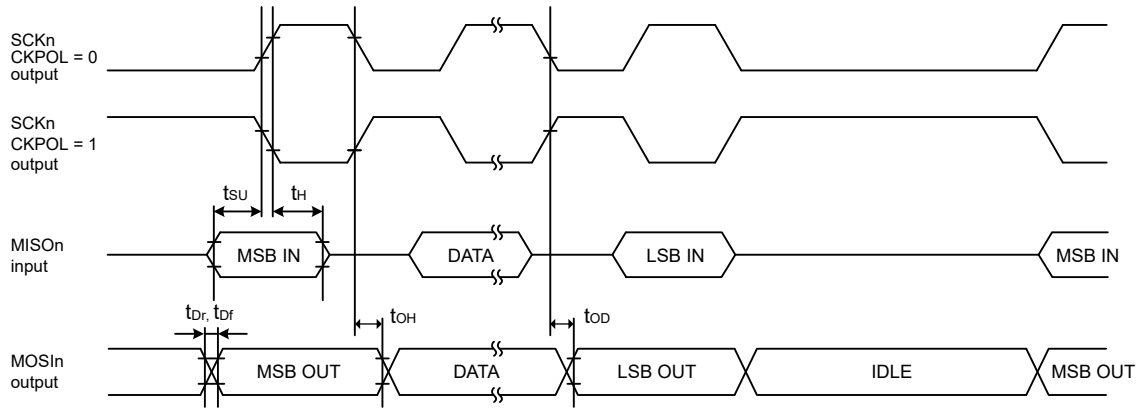
Note 1. t_{Pcyc}: PCLKB cycle.



V_{OH} = 0.7 × VCC, V_{OL} = 0.3 × VCC, V_{IH} = 0.7 × VCC, V_{IL} = 0.3 × VCC

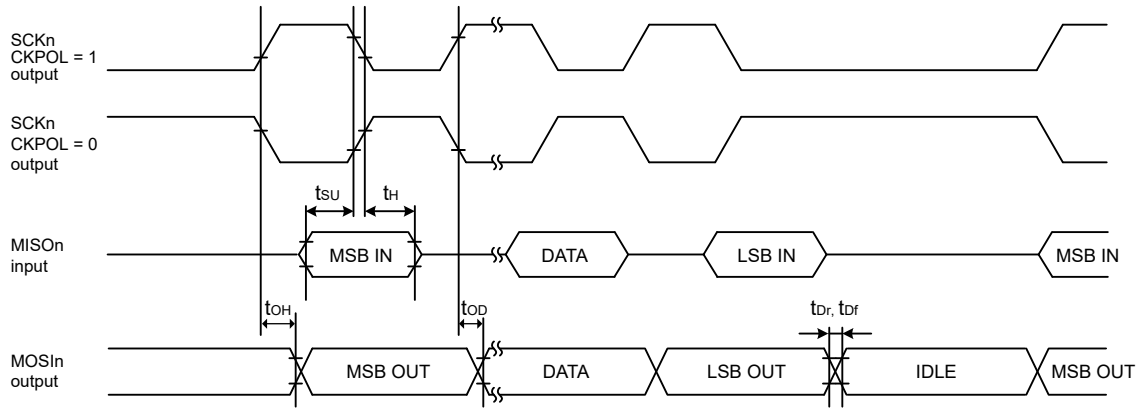
Note: n = 9

Figure 2.17 SCI simple SPI mode clock timing



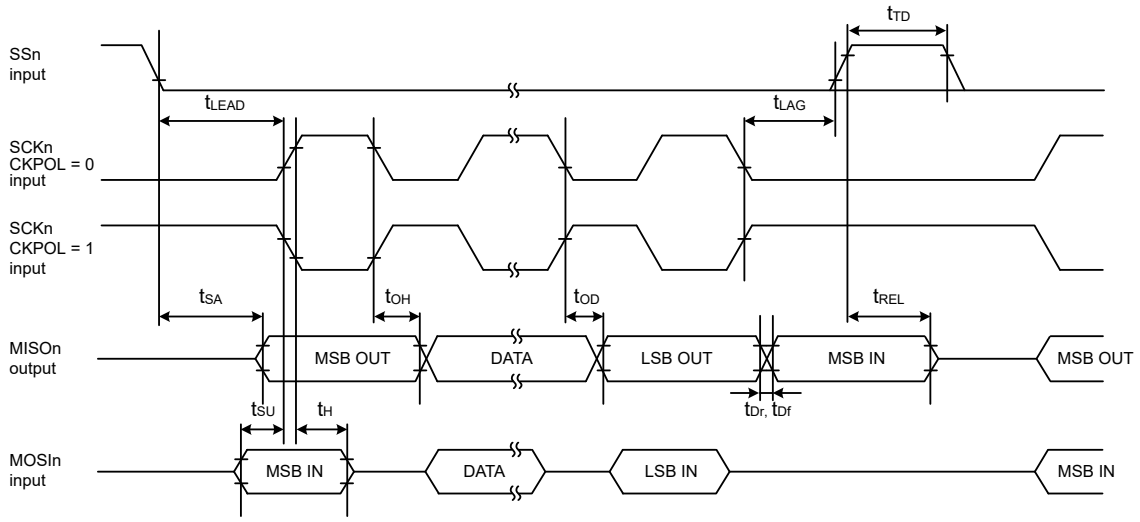
Note: n = 9

Figure 2.18 SCI simple SPI mode timing (master, CKPH = 1)



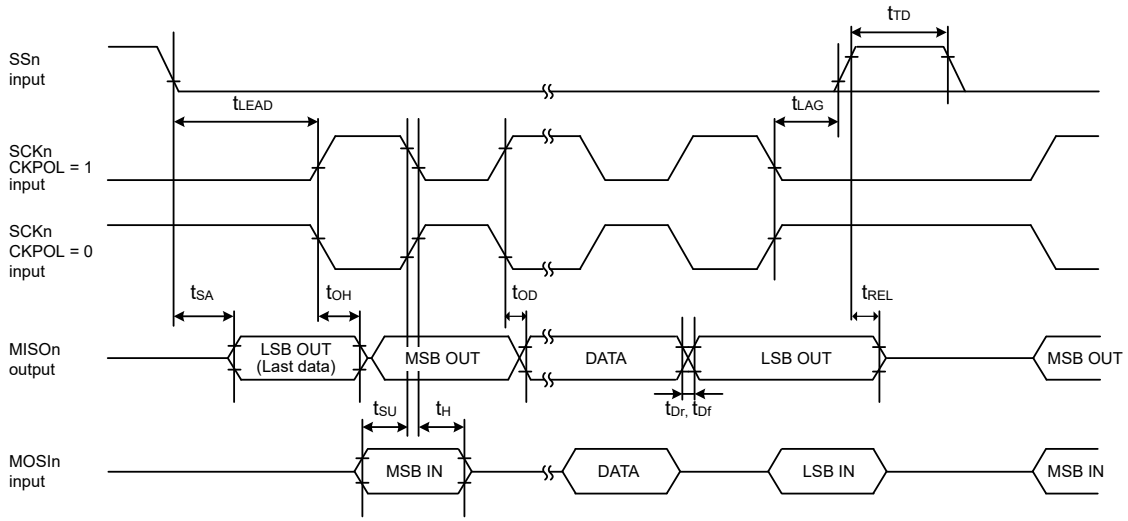
Note: n = 9

Figure 2.19 SCI simple SPI mode timing (master, CKPH = 0)



Note: n = 9

Figure 2.20 SCI simple SPI mode timing (slave, CKPH = 1)



Note: n = 9

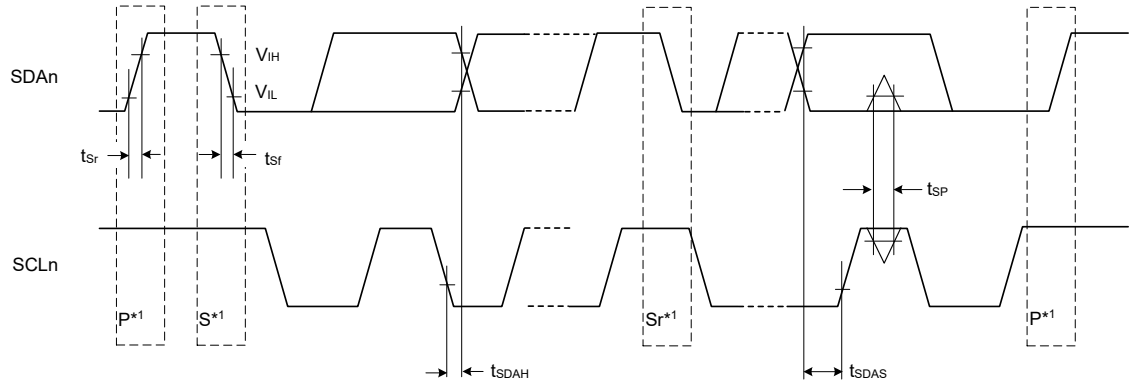
Figure 2.21 SCI simple SPI mode timing (slave, CKPH = 0)

Table 2.27 SCI timing (3)

Conditions: VCC = 2.7 to 5.5 V

Parameter		Symbol	Min	Max	Unit	Test conditions
Simple IIC (Standard mode)	SDA input rise time	t_{Sr}	—	1000	ns	Figure 2.22
	SDA input fall time	t_{Sf}	—	300	ns	
	SDA input spike pulse removal time	t_{SP}	0	4 × t_{IICcyc} *1	ns	
	Data input setup time	t_{SDAS}	250	—	ns	
	Data input hold time	t_{SDAH}	0	—	ns	
	SCL, SDA capacitive load	C_b *2	—	400	pF	
Simple IIC (Fast mode)	SDA input rise time	t_{Sr}	—	300	ns	Figure 2.22
	SDA input fall time	t_{Sf}	—	300	ns	
	SDA input spike pulse removal time	t_{SP}	0	4 × t_{IICcyc} *1	ns	
	Data input setup time	t_{SDAS}	100	—	ns	
	Data input hold time	t_{SDAH}	0	—	ns	
	SCL, SDA capacitive load	C_b *2	—	400	pF	

Note 1. t_{IICcyc}: Clock cycle selected by the SMR.CKS[1:0] bits.
Note 2. C_b indicates the total capacity of the bus line.



Test conditions:
V_{IH} = VCC × 0.7, V_{IL} = VCC × 0.3
V_{OL} = 0.6 V, I_{OL} = 6 mA

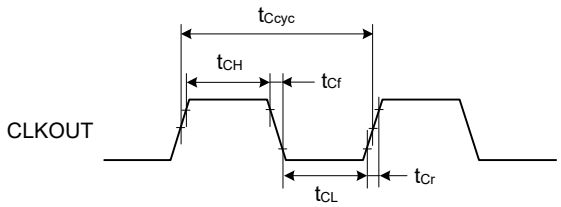
Note: n = 9
Note 1. S, P, and Sr indicate the following conditions:
S: Start condition
P: Stop condition
Sr: Restart condition

Figure 2.22 SCI simple IIC mode timing

2.3.9 CLKOUT Timing

Table 2.28 CLKOUT timing

Parameter			Symbol	Min	Max	Unit	Test conditions
CLKOUT	CLKOUT pin output cycle	2.7 V ≤ VCC ≤ 5.5 V	t_{Ccyc}	62.5	—	ns	Figure 2.23
	CLKOUT pin high pulse width	2.7 V ≤ VCC ≤ 5.5 V	t_{CH}	15	—	ns	
	CLKOUT pin low pulse width	2.7 V ≤ VCC ≤ 5.5 V	t_{CL}	15	—	ns	
	CLKOUT pin output rise time	2.7 V ≤ VCC ≤ 5.5 V	t_{Cr}	—	12	ns	
	CLKOUT pin output fall time	2.7 V ≤ VCC ≤ 5.5 V	t_{Cf}	—	12	ns	



Test conditions: V_{OH} = VCC × 0.7, V_{OL} = VCC × 0.3, I_{OH} = -1.0 mA, I_{OL} = 1.0 mA, C = 30 pF

Figure 2.23 CLKOUT output timing

2.4 ADC12 Characteristics

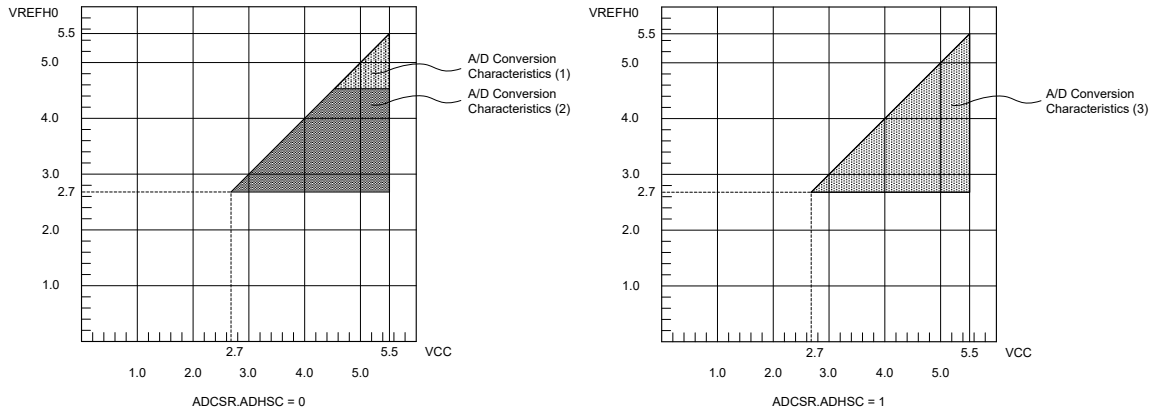


Figure 2.24 VCC to VREFH0 voltage range

Table 2.29 A/D conversion characteristics (1) in high-speed A/D conversion mode (1 of 2)

Conditions: VCC = VREFH0 = 4.5 to 5.5 V*5, VSS = VREFL0 = 0 V
Reference voltage range applied to the VREFH0 and VREFL0.

Parameter		Min	Typ	Max	Unit	Test conditions
PCLKD (ADCLK) frequency		1	—	64	MHz	ADACSR.ADSAC = 0
				48	MHz	ADACSR.ADSAC = 1
Analog input capacitance*2	Cs	—	—	9*3	pF	High-precision channel
		—	—	10*3	pF	Normal-precision channel
Analog input resistance	Rs	—	—	1.3*3	kΩ	High-precision channel
		—	—	5.0*3	kΩ	Normal-precision channel
Analog input voltage range	Ain	0	—	VREFH0	V	—
Resolution		—	—	12	Bit	—
Conversion time*1 (Operation at PCLKD = 64 MHz)	Permissible signal source impedance Max. = 0.3 kΩ	0.70 (0.211)*4	—	—	µs	High-precision channel ADCSR.ADHSC = 0 ADSSTRn.SST[7:0] = 0x0D ADACSR.ADSAC = 0
		1.34 (0.852)*4	—	—	µs	Normal-precision channel ADCSR.ADHSC = 0 ADSSTRn.SST[7:0] = 0x36 ADACSR.ADSAC = 0
	Permissible signal source impedance Max. = 0.3 kΩ when using Sample-and-hold circuit	1.31 (0.406)*4	—	—	µs	S/H channel ADCSR.ADHSC = 0 ADSSTRn.SST[7:0] = 0x0D ADSHCR.SSTSH[7:0]= 0x1A ADACSR.ADSAC = 0 AN000 to AN002 = 0.25 V to (VCC - 0.25 V)

Table 2.29 A/D conversion characteristics (1) in high-speed A/D conversion mode (2 of 2)

Conditions: VCC = VREFH0 = 4.5 to 5.5 V*5, VSS = VREFL0 = 0 V
Reference voltage range applied to the VREFH0 and VREFL0.

Parameter		Min	Typ	Max	Unit	Test conditions
Conversion time*1 (Operation at PCLKD = 48 MHz)	Permissible signal source impedance Max. = 0.3 kΩ	0.67 (0.219)*4	—	—	μs	High-precision channel ADCSR.ADHSC = 0 ADSSTRn.SST[7:0] = 0x0A ADACSR.ADSAC = 1
		1.29 (0.844)*4	—	—	μs	Normal-precision channel ADCSR.ADHSC = 0 ADSSTRn.SST[7:0] = 0x28 ADACSR.ADSAC = 1
	Permissible signal source impedance Max. = 0.3 kΩ when using Sample-and-hold circuit	1.48 (0.542)*4	—	—	μs	S/H channel ADCSR.ADHSC = 0 ADSSTRn.SST[7:0] = 0x0A ADSHCR.SSTSH[7:0]= 0x1A ADACSR.ADSAC = 1 AN000 to AN002 = 0.25 V to (VCC - 0.25 V)
Offset error		—	±1.0	±5.0	LSB	High-precision channel
				±6.0	LSB	Normal-precision channel
Full-scale error		—	±1.0	±5.0	LSB	High-precision channel
				±6.0	LSB	Normal-precision channel
Quantization error		—	±0.5	—	LSB	—
Absolute accuracy	When using Sample-and-hold circuits	—	—	±8.0	LSB	S/H channel AN000 to AN002 = 0.25 V to (VCC - 0.25 V)
	When Sample-and-hold circuits are not used			±6.0	LSB	High-precision channel
				±9.0	LSB	Normal-precision channel
DNL differential nonlinearity error		—	±1.0	—	LSB	—
INL integral nonlinearity error		—	±1.5	±3.0	LSB	—

Note: The characteristics apply when no pin functions other than 12-bit A/D converter input are used. Absolute accuracy does not include quantization errors. Offset error, full-scale error, DNL differential nonlinearity error, and INL integral nonlinearity error do not include quantization errors.
Note 1. The conversion time is the sum of the sampling time and the comparison time. The number of sampling states is indicated for the test conditions.
Note 2. Except for I/O input capacitance (Cin), see section 2.2.4. I/O VOH, VOL, and Other Characteristics.
Note 3. Reference data.
Note 4. ( ) lists sampling time.
Note 5. When VREFH0 < VCC, the MAX. values are as follows.
Absolute accuracy/Offset error/Full-scale error:
For voltage difference between VCC and VREFH0, it should be added ±0.5 LSB/V to the Max spec.
INL integral non-linearity error:
For voltage difference between VCC and VREFH0, it should be added ±0.2 LSB/V to the Max spec.

Table 2.30 A/D conversion characteristics (2) in high-speed A/D conversion mode (1 of 2)

Conditions: VCC = VREFH0 = 2.7 to 5.5 V*5, VSS = VREFL0 = 0 V
Reference voltage range applied to the VREFH0 and VREFL0.

Parameter		Min	Typ	Max	Unit	Test conditions
PCLKD (ADCLK) frequency		1	—	48	MHz	—
Analog input capacitance*2	Cs	—	—	9*3	pF	High-precision channel
		—	—	10*3	pF	Normal-precision channel
Analog input resistance	Rs	—	—	1.9*3	kΩ	High-precision channel
		—	—	6.0*3	kΩ	Normal-precision channel

Table 2.30 A/D conversion characteristics (2) in high-speed A/D conversion mode (2 of 2)

Conditions: VCC = VREFH0 = 2.7 to 5.5 V[*5], VSS = VREFL0 = 0 V
Reference voltage range applied to the VREFH0 and VREFL0.

Parameter		Min	Typ	Max	Unit	Test conditions
Analog input voltage range	Ain	0	—	VREFH0	V	—
Resolution		—	—	12	Bit	—
Conversion time[*1] (Operation at PCLKD = 48 MHz)	Permissible signal source impedance Max. = 0.3 kΩ	0.67 (0.219)[*4]	—	—	µs	High-precision channel ADCSR.ADHSC = 0 ADSSTRn.SST[7:0] = 0x0A ADACSR.ADSAC = 1
		1.29 (0.844)[*4]	—	—	µs	Normal-precision channel ADCSR.ADHSC = 0 ADSSTRn.SST[7:0] = 0x28 ADACSR.ADSAC = 1
	Permissible signal source impedance Max. = 0.3 kΩ when using Sample-and-hold circuit	1.48 (0.542)[*4]	—	—	µs	S/H channel ADCSR.ADHSC = 0 ADSSTRn.SST[7:0] = 0x0A ADSHCR.SSTSH[7:0]= 0x1A ADACSR.ADSAC = 1 AN000 to AN002 = 0.25 V to (VCC - 0.25 V)
Offset error		—	±1.0	±6.5	LSB	High-precision channel
				±8.0	LSB	Normal-precision channel
Full-scale error		—	±1.0	±6.5	LSB	High-precision channel
				±8.0	LSB	Normal-precision channel
Quantization error		—	±0.5	—	LSB	—
Absolute accuracy	When using Sample-and-hold circuits	—	—	±9.0	LSB	S/H channel AN000 to AN002 = 0.25 V to (VCC - 0.25 V)
	When Sample-and-hold circuits are not used			±7.5	LSB	High-precision channel
				±10.5	LSB	Normal-precision channel
DNL differential nonlinearity error		—	±1.0	—	LSB	—
INL integral nonlinearity error		—	±1.5	±3.0	LSB	—

Note: The characteristics apply when no pin functions other than 12-bit A/D converter input are used. Absolute accuracy does not include quantization errors. Offset error, full-scale error, DNL differential nonlinearity error, and INL integral nonlinearity error do not include quantization errors.
Note 1. The conversion time is the sum of the sampling time and the comparison time. The number of sampling states is indicated for the test conditions.
Note 2. Except for I/O input capacitance (Cin), see section 2.2.4. I/O VOH, VOL, and Other Characteristics.
Note 3. Reference data.
Note 4. ( ) lists sampling time.
Note 5. When VREFH0 < VCC, the MAX. values are as follows.
Absolute accuracy/Offset error/Full-scale error:
For voltage difference between VCC and VREFH0, it should be added ±0.5 LSB/V to the Max spec.
INL integral non-linearity error:
For voltage difference between VCC and VREFH0, it should be added ±0.2 LSB/V to the Max spec.

Table 2.31 A/D conversion characteristics (3) in low-power A/D conversion mode (1 of 2)

Conditions: VCC = VREFH0 = 2.7 to 5.5 V[*5], VSS = VREFL0 = 0 V
Reference voltage range applied to the VREFH0 and VREFL0.

Parameter		Min	Typ	Max	Unit	Test conditions
PCLKD (ADCLK) frequency		1	—	24	MHz	—
Analog input capacitance[*2]	Cs	—	—	9[*3]	pF	High-precision channel
		—	—	10[*3]	pF	Normal-precision channel

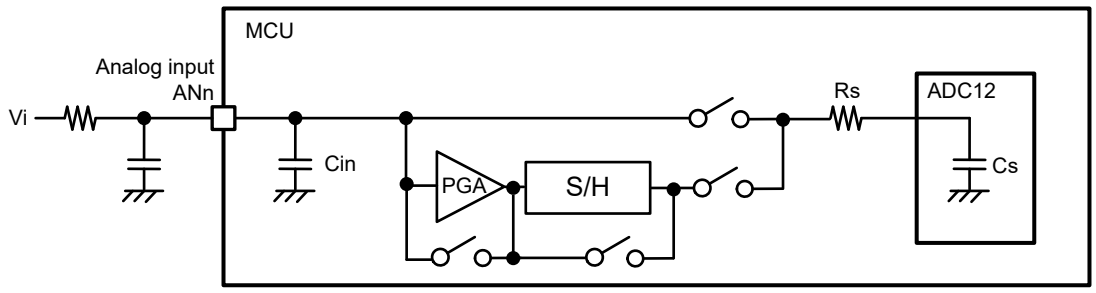
Table 2.31 A/D conversion characteristics (3) in low-power A/D conversion mode (2 of 2)

Conditions: VCC = VREFH0 = 2.7 to 5.5 V[*5], VSS = VREFL0 = 0 V
Reference voltage range applied to the VREFH0 and VREFL0.

Parameter		Min	Typ	Max	Unit	Test conditions
Analog input resistance	Rs	—	—	1.9[*3]	kΩ	High-precision channel
		—	—	6.0[*3]	kΩ	Normal-precision channel
Analog input voltage range	Ain	0	—	VREFH0	V	—
Resolution		—	—	12	Bit	—
Conversion time[*1] (Operation at PCLKD = 24 MHz)	Permissible signal source impedance Max. = 0.3 kΩ	1.58 (0.438)[*4]	—	—	µs	High-precision channel ADCSR.ADHSC = 1 ADSSTRn.SST[7:0] = 0x0A ADACSR.ADSAC = 1
		2.0 (0.854)[*4]	—	—	µs	Normal-precision channel ADCSR.ADHSC = 1 ADSSTRn.SST[7:0] = 0x14 ADACSR.ADSAC = 1
	Permissible signal source impedance Max. = 0.3 kΩ when using Sample-and-hold circuit	3.21 (1.083)[*4]	—	—	µs	S/H channel ADCSR.ADHSC = 0 ADSSTRn.SST[7:0] = 0x0A ADSHCR.SSTSH[7:0]= 0x1A ADACSR.ADSAC = 1 AN000 to AN002 = 0.25 V to (VCC - 0.25 V)
Offset error		—	±1.0	±6.5	LSB	High-precision channel
				±8.0	LSB	Normal-precision channel
Full-scale error		—	±1.0	±6.5	LSB	High-precision channel
				±8.0	LSB	Normal-precision channel
Quantization error		—	±0.5	—	LSB	—
Absolute accuracy	When using Sample-and-hold circuits	—	—	±9.0	LSB	S/H channel AN000 to AN002 = 0.25 V to (VCC - 0.25 V)
	When Sample-and-hold circuits are not used			±7.5	LSB	High-precision channel
				±10.5	LSB	Normal-precision channel
DNL differential nonlinearity error		—	±1.0	—	LSB	—
INL integral nonlinearity error		—	±1.5	±3.0	LSB	—

Note: The characteristics apply when no pin functions other than 12-bit A/D converter input are used. Absolute accuracy does not include quantization errors. Offset error, full-scale error, DNL differential nonlinearity error, and INL integral nonlinearity error do not include quantization errors.
Note 1. The conversion time is the sum of the sampling time and the comparison time. The number of sampling states is indicated for the test conditions.
Note 2. Except for I/O input capacitance (Cin), see section 2.2.4. I/O VOH, VOL, and Other Characteristics.
Note 3. Reference data.
Note 4. ( ) lists sampling time.
Note 5. When VREFH0 < VCC, the MAX. values are as follows.
Absolute accuracy/Offset error/Full-scale error:
For voltage difference between VCC and VREFH0, it should be added ±0.5 LSB/V to the Max spec.
INL integral non-linearity error:
For voltage difference between VCC and VREFH0, it should be added ±0.2 LSB/V to the Max spec.

Figure 2.25 shows the equivalent circuit for analog input.



Note: Terminal leakage current is not shown in this figure.

Figure 2.25 Equivalent circuit for analog input

Table 2.32 12-bit A/D converter channel classification

Classification	Channel	Conditions	Remarks
High-precision channel (w/o PGA and S/H)	AN000 to AN007	VCC = 2.7 to 5.5 V	Pins AN000 to AN007 cannot be used as general I/O, TS transmission, when the A/D converter is in use.
Normal-precision channel	AN016 to AN017		
S/H channel (w/ S/H)	AN000 to AN002		
PGA channel (w/ PGA or PGA+S/H)	AN000 to AN002		
Internal reference voltage input channel	Internal reference voltage	VCC = 2.7 to 5.5 V	—
Temperature sensor input channel	Temperature sensor output	VCC = 2.7 to 5.5 V	—

Table 2.33 A/D internal reference voltage characteristics

Conditions: VCC = VREFH0 = 2.7 to 5.5 V

Parameter	Min	Typ	Max	Unit	Test conditions
Internal reference voltage input channel[*1]	1.40	1.47	1.54	V	—
Sampling time[*2]	5.0	—	—	µs	—

Note 1. The 12-bit A/D internal reference voltage indicates the voltage when the internal reference voltage is input to the 12-bit A/D converter.
Note 2. When the internal reference voltage is converted.

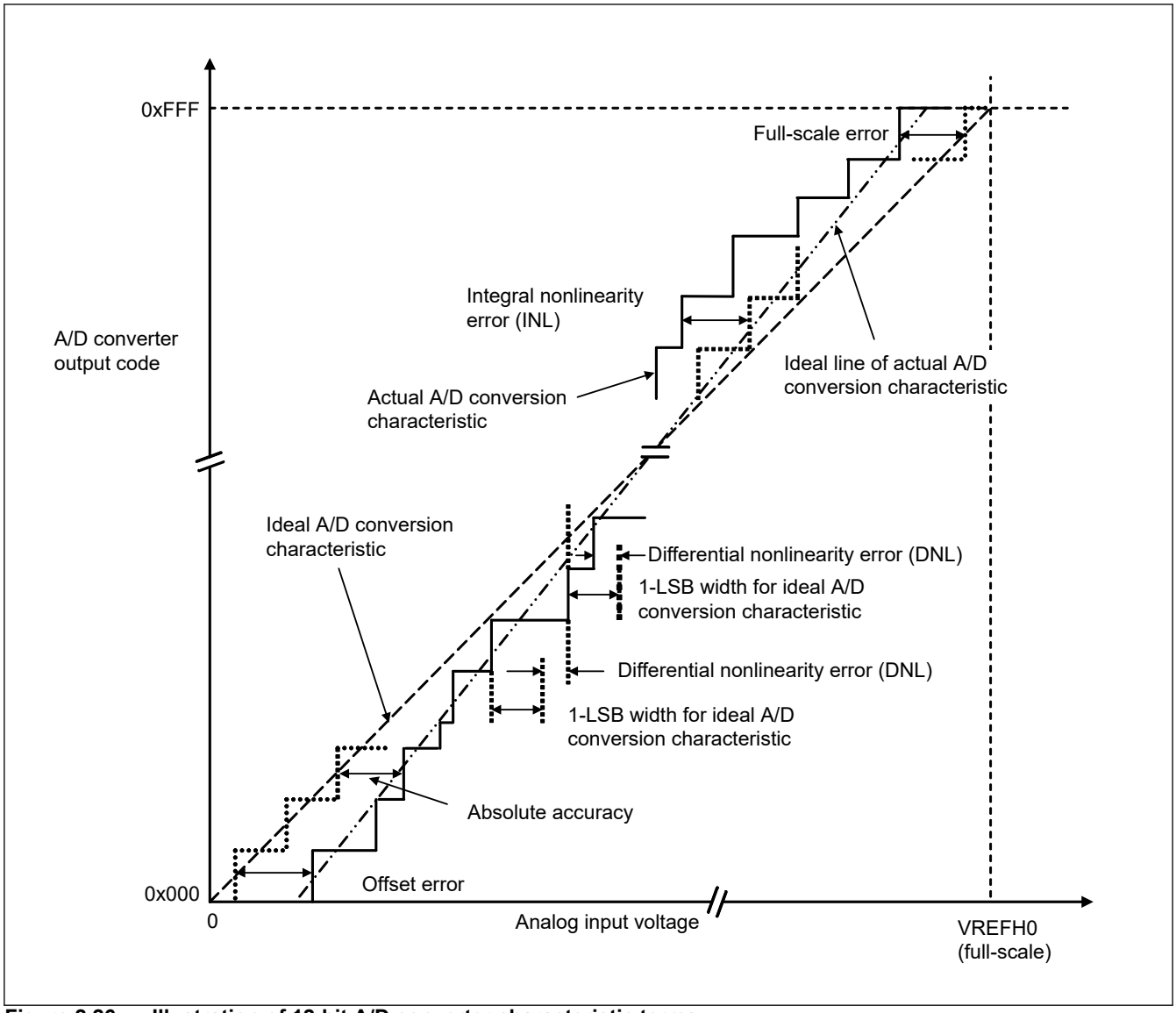


Figure 2.26 Illustration of 12-bit A/D converter characteristic terms

Absolute accuracy

Absolute accuracy is the difference between output code based on the theoretical A/D conversion characteristics, and the actual A/D conversion result. When measuring absolute accuracy, the voltage at the midpoint of the width of the analog input voltage (1-LSB width), which can meet the expectation of outputting an equal code based on the theoretical A/D conversion characteristics, is used as the analog input voltage. For example, if 12-bit resolution is used and the reference voltage VREFH0 = 3.072 V, then 1-LSB width becomes 0.75 mV, and 0 mV, 0.75 mV, and 1.5 mV are used as the analog input voltages. If analog input voltage is 6 mV, an absolute accuracy of ±5 LSB means that the actual A/D conversion result is in the range of 0x003 to 0x00D, though an output code of 0x008 can be expected from the theoretical A/D conversion characteristics.

Integral nonlinearity error (INL)

Integral nonlinearity error is the maximum deviation between the ideal line when the measured offset and full-scale errors are zeroed, and the actual output code.

Differential nonlinearity error (DNL)

Differential nonlinearity error is the difference between 1-LSB width based on the ideal A/D conversion characteristics and the width of the actual output code.

Offset error

Offset error is the difference between the transition point of the ideal first output code and the actual first output code.

Full-scale error

Full-scale error is the difference between the transition point of the ideal last output code and the actual last output code.

2.5 Programmable Gain Amplifier Characteristics

Table 2.34 Programmable gain amplifier characteristics

Conditions: VCC = 2.7 to 5.5 V, VSS = 0 V

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
Input offset voltage	V_{IOPGA}	—	—	±10	mV	—
Input voltage range	V_{IPGA}	V_{IOLPGA}/G	—	V_{IOHPGA}/G	V	—
Output voltage range	V_{IOHPGA}	0.93 × VCC	—	—	V	—
	V_{IOLPGA}	—	—	0.07 × VCC		—
Gain	G	4	—	8	Times	G = 4, 5.33, 6.4, 8
Gain error	G_{ERR}	—	—	1.5	%	—
Slew rate (Rise)	SR_{RPGA}	3.5	—	—	V/us	VCC = 4.0 to 5.5V
		1.5	—	—		VCC = 3.6 to 4.0V
		0.5	—	—		VCC = 2.7 to 4.0V
Slew rate (Fall)	SR_{FPGA}	3.5	—	—	V/us	VCC = 4.0 to 5.5V
		1.5	—	—		VCC = 3.6 to 4.0V
		0.5	—	—		VCC = 2.7 to 4.0V
Operation stabilization Wait time	t_{PGA}	—	—	5	us	—

2.6 ACMPHS Characteristics

Table 2.35 ACMPHS characteristics

Conditions: VCC = 2.7 to 5.5 V, VSS = 0 V

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
Input offset voltage	V_{IOCMP}	—	±5	±40	mV	—
Input voltage range	V_{ICMP}	0	—	VCC	V	—
Response time	t_{CR}	—	70	150	ns	Input amplitude=±100mV CMPCTL.CDFS=00
	t_{CF}	—	70	150		
Input channel switching stabilization time	t_{WAIT}	—	—	300	ns	Input amplitude=±100mV CMPCTL.CDFS=00
Operation stabilization time	t_{VR}	—	_	1	µs	VCC = 3.3V to 5.5V
		—	—	3		VCC = 2.7V to 3.3V

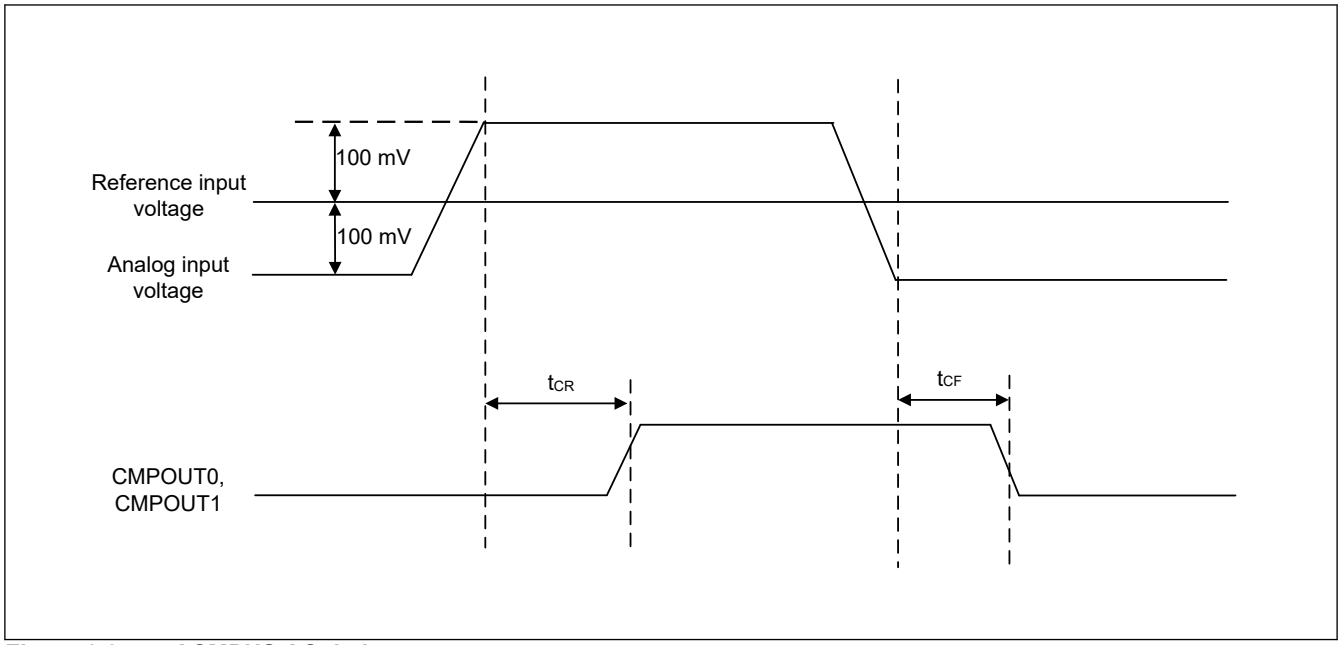


Figure 2.27 ACMPHS AC timing

2.7 DAC8 Characteristics

Table 2.36 D/A conversion characteristics

Conditions: VCC = 2.7 to 5.5 V, VSS = 0 V

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
Resolution	—	—	—	8	bit	—
Conversion time	t_{DCONV}	—	—	3.0	µs	—
Absolute accuracy	—	—	—	±3	LSB	—
Output load resistance	—	2	—	—	MΩ	—
Output load capacitance	—	—	—	35	pF	—
Output resistance	—	—	9.0	—	kΩ	—

2.8 TSN Characteristics

Table 2.37 TSN characteristics

Conditions: VCC = 2.7 to 5.5 V

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
Relative accuracy	—	—	±1.5	—	°C	—
Temperature slope	—	—	-3.3	—	mV/°C	—
Output voltage (at 25°C)	—	—	1.05	—	V	VCC = 3.3 V
Temperature sensor start time	t_{START}	—	—	5	µs	—
Sampling time	—	5	—	—	µs	

2.9 POR and LVD Characteristics

Table 2.38 Power-on reset circuit and voltage detection circuit characteristics (1)

Parameter			Symbol	Min	Typ	Max	Unit	Test Conditions
Voltage detection level*1	Power-on reset (POR)	When power supply rise	V_{POR}	1.47	1.51	1.6	V	Figure 2.28
		When power supply fall	V_{PDR}	1.46	1.50	1.59		Figure 2.29
	Voltage detection circuit (LVD0)*2	When power supply rise	V_{det0_0}	3.74	3.91	4.06	V	Figure 2.30 At falling edge VCC
		When power supply fall		3.68	3.85	4.00		
		When power supply rise	V_{det0_1}	2.73	2.9	3.01		
		When power supply fall		2.68	2.85	2.96		
		When power supply rise	V_{det0_2}	2.44	2.59	2.70		
		When power supply fall		2.38	2.53	2.64		
Voltage detection level*1	Voltage detection circuit (LVD1)*3	When power supply rise	V_{det1_0}	4.23	4.39	4.55	V	Figure 2.31 At falling edge VCC
		When power supply fall		4.13	4.29	4.45		
		When power supply rise	V_{det1_1}	4.07	4.25	4.39		
		When power supply fall		3.98	4.16	4.30		
		When power supply rise	V_{det1_2}	3.97	4.14	4.29		
		When power supply fall		3.86	4.03	4.18		
		When power supply rise	V_{det1_3}	3.74	3.92	4.06		
		When power supply fall		3.68	3.86	4.00		
		When power supply rise	V_{det1_4}	3.05	3.17	3.29		
		When power supply fall		2.98	3.10	3.22		
		When power supply rise	V_{det1_5}	2.95	3.06	3.17		
		When power supply fall		2.89	3.00	3.11		
		When power supply rise	V_{det1_6}	2.86	2.97	3.08		
		When power supply fall		2.79	2.90	3.01		
		When power supply rise	V_{det1_7}	2.74	2.85	2.96		
		When power supply fall		2.68	2.79	2.90		
		When power supply rise	V_{det1_8}	2.63	2.75	2.85		
		When power supply fall		2.58	2.68	2.78		
Voltage detection level*1	Voltage detection circuit (LVD2)*4	When power supply rise	V_{det2_0}	4.20	4.40	4.57	V	Figure 2.32 At falling edge VCC
		When power supply fall		4.11	4.31	4.48		
		When power supply rise	V_{det2_1}	4.05	4.25	4.42		
		When power supply fall		3.97	4.17	4.34		
		When power supply rise	V_{det2_2}	3.91	4.11	4.28		
		When power supply fall		3.83	4.03	4.20		
		When power supply rise	V_{det2_3}	3.71	3.91	4.08		
		When power supply fall		3.64	3.84	4.01		

Note 1. These characteristics apply when noise is not superimposed on the power supply. When a setting causes this voltage detection level to overlap with that of the voltage detection circuit, it cannot be specified whether LVD1 or LVD2 is used for voltage detection.
Note 2. # in the symbol $V_{det0\_\#}$ denotes the value of the OFS1.VDSEL1[2:0] bits.
Note 3. # in the symbol $V_{det1\_\#}$ denotes the value of the LVDLVLR.LVD1LVL[4:0] bits.
Note 4. # in the symbol $V_{det2\_\#}$ denotes the value of the LVDLVLR.LVD2LVL[2:0] bits.

Table 2.39 Power-on reset circuit and voltage detection circuit characteristics (2)

Parameter		Symbol	Min	Typ	Max	Unit	Test Conditions
Wait time after power-on reset cancellation	LVD0: enable	t_{POR}	—	4.3	—	ms	—
	LVD0: disable	t_{POR}	—	3.7	—	ms	—
Wait time after voltage monitor 0, 1, 2 reset cancellation	LVD0: enable*1	$t_{LVD0,1,2}$	—	1.4	—	ms	—
	LVD0: disable*2	$t_{LVD1,2}$	—	0.7	—	ms	—
Power-on reset response delay time*3		t_{det}	—	—	500	µs	Figure 2.28, Figure 2.29
LVD0 response delay time*3		t_{det}	—	—	500	µs	Figure 2.30
LVD1 response delay time*3		t_{det}	—	—	350	µs	Figure 2.31
LVD2 response delay time*3		t_{det}	—	—	600	µs	Figure 2.32
Minimum VCC down time		t_{VOFF}	500	—	—	µs	Figure 2.28, VCC = 1.0 V or above
Power-on reset enable time		$t_{W\ (POR)}$	1	—	—	ms	Figure 2.29, VCC = below 1.0 V
LVD1 operation stabilization time (after LVD1 is enabled)		$T_{d\ (E-A)}$	—	—	300	µs	Figure 2.31
LVD2 operation stabilization time (after LVD2 is enabled)		$T_{d\ (E-A)}$	—	—	1200	µs	Figure 2.32
Hysteresis width (POR)		V_{PORH}	—	10	—	mV	—
Hysteresis width (LVD0, LVD1 and LVD2)		V_{LVH}	—	60	—	mV	LVD0 selected
			—	110	—		V_{det1_0} to V_{det1_2} selected
			—	70	—		V_{det1_3} to V_{det1_8} selected
			—	90	—		LVD2 selected

Note 1. When OFS1.LVDAS = 0.
Note 2. When OFS1.LVDAS = 1.
Note 3. The minimum VCC down time indicates the time when VCC is below the minimum value of voltage detection levels V_{POR}, V_{det0}, V_{det1}, and V_{det2} for the POR/LVD.

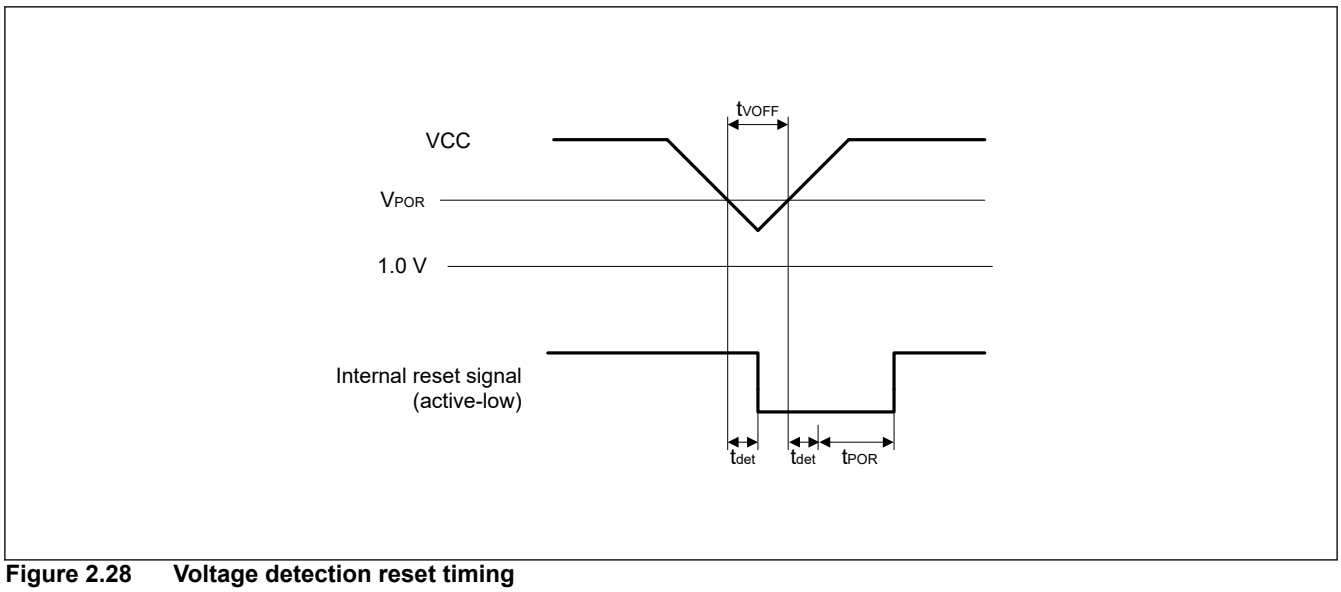
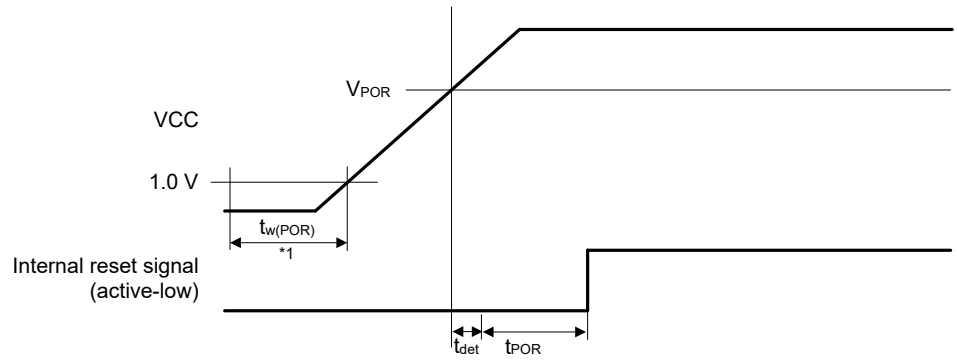


Figure 2.28 Voltage detection reset timing



Note 1. $t_{w(POR)}$ is the time required for a power-on reset to be enabled while the external power VCC is being held below the valid voltage (1.0 V).
When VCC turns on, maintain $t_{w(POR)}$ for 1.0 ms or more.

Figure 2.29 Power-on reset timing

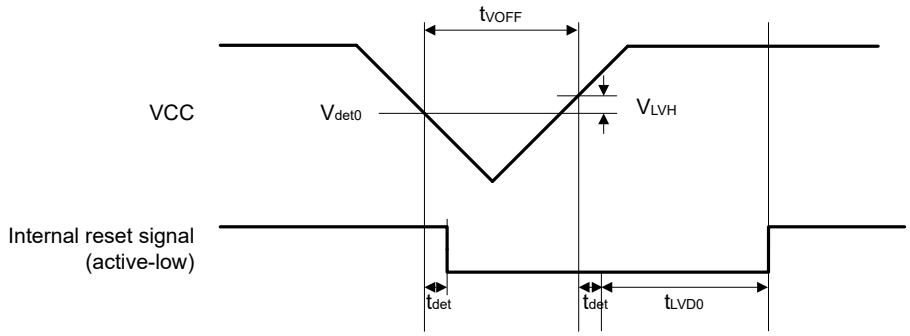


Figure 2.30 Voltage detection circuit timing (V_{det0})

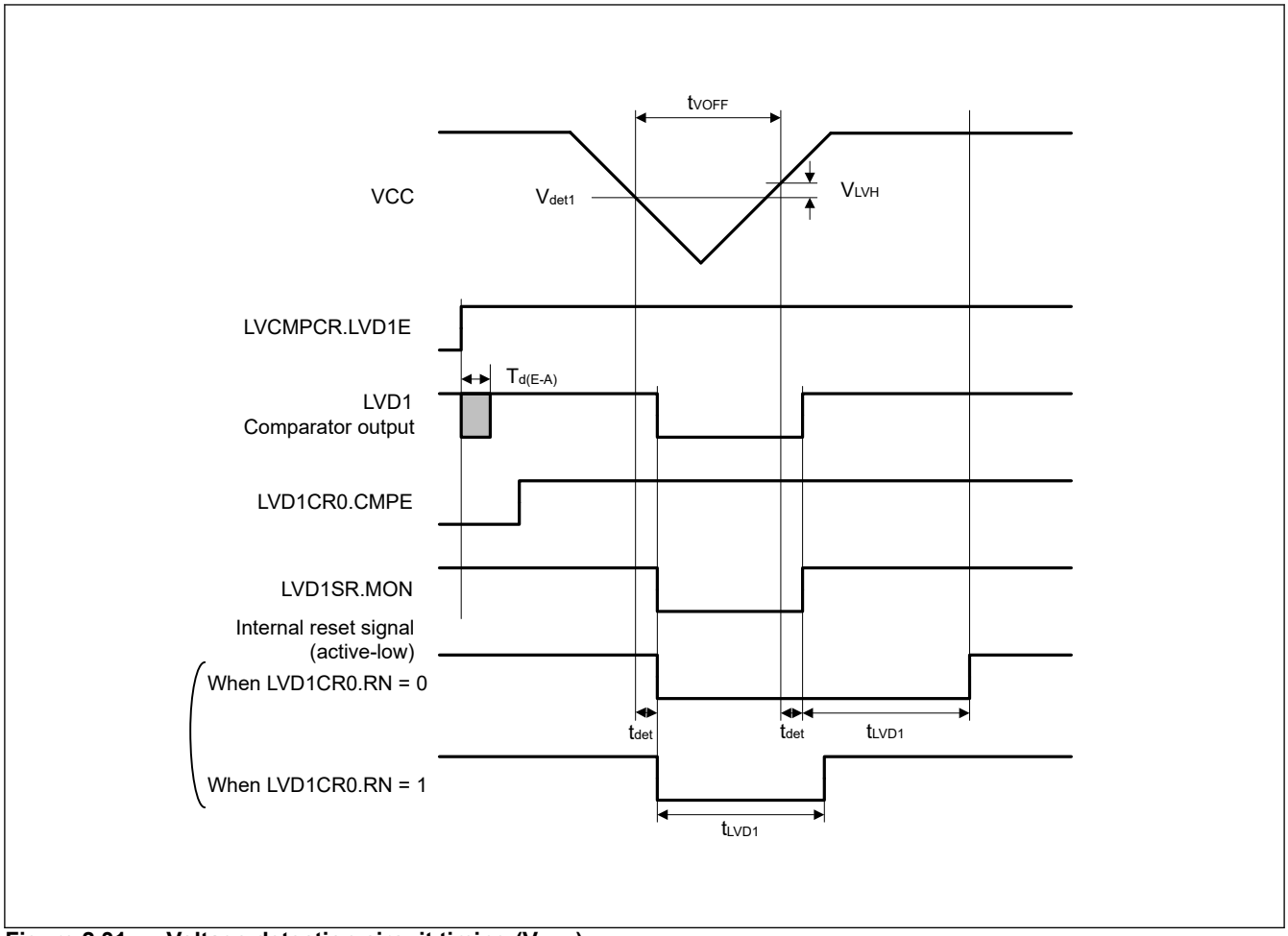


Figure 2.31 Voltage detection circuit timing (V_{det1})

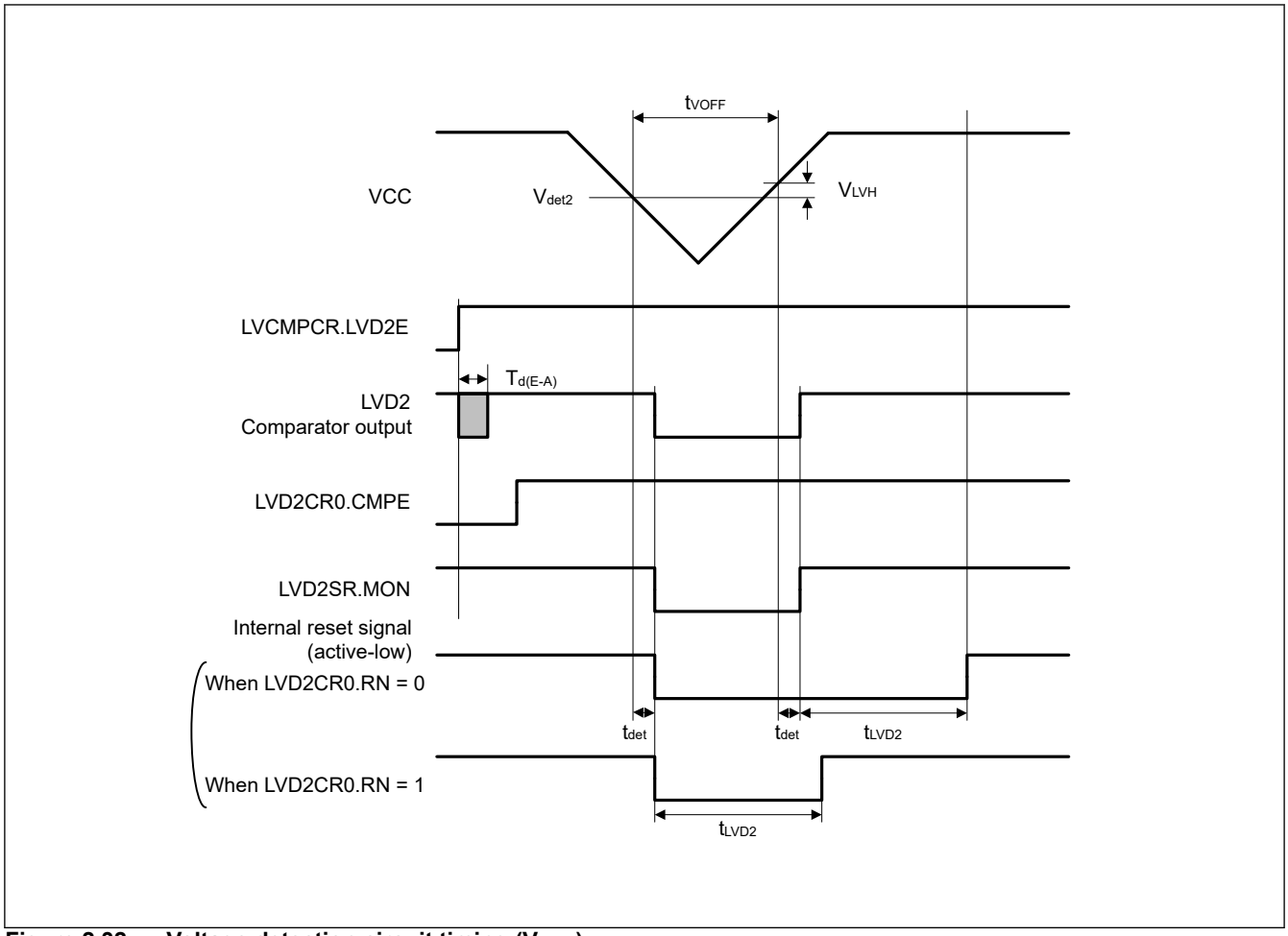


Figure 2.32 Voltage detection circuit timing (V_{det2})

2.10 Flash Memory Characteristics

2.10.1 Code Flash Memory Characteristics

Table 2.40 Code flash characteristics (1)

Parameter		Symbol	Min	Typ	Max	Unit	Conditions
Reprogramming/erasure cycle*1		N_{PEC}	1000	—	—	Times	T_a = ±0°C to +60°C
Data hold time	After 1000 times N_{PEC}	t_{DRP}	20*2 *3	—	—	Year	T_a = +105°C
			10	—	—		T_a = +125°C

Note 1. The reprogram/erase cycle is the number of erasures for each block. When the reprogram/erase cycle is n times (n = 1,000), erasing can be performed n times for each block. For instance, when 8-byte programming is performed 256 times for different addresses in 2-KB blocks, and then the entire block is erased, the reprogram/erase cycle is counted as one. However, programming the same address for several times as one erasure is not enabled (overwriting is prohibited).
Note 2. Characteristic when using the flash memory programmer and the self-programming library provided by Renesas Electronics.
Note 3. This result is target spec, may changed after reliability testing.

Table 2.41 Code flash characteristics (2) (1 of 2)

High-speed operating mode
Conditions: VCC = 2.7 to 5.5 V, T_a = ±0℃ to +60℃

Parameter		Symbol	ICLK = 1 MHz			ICLK = 32 MHz			Unit
			Min	Typ	Max	Min	Typ	Max	
Programming time	8 bytse	t_{P8}	—	97.3	842.3	—	47	448.2	µs
Erasure time	2 KB	t_{E2K}	—	8.63	281.7	—	5.62	220	ms

Table 2.41 Code flash characteristics (2) (2 of 2)

High-speed operating mode
Conditions: VCC = 2.7 to 5.5 V, T_a = ±0℃ to +60℃

Parameter		Symbol	ICLK = 1 MHz			ICLK = 32 MHz			Unit
			Min	Typ	Max	Min	Typ	Max	
Blank check time	8 bytes	t_{BC8}	—	—	44.5	—	—	8.9	µs
	2 KB	t_{BC2K}	—	—	1629	—	—	124.4	µs
Erase suspended time		t_{SED}	—	—	21.3	—	—	10.12	µs
Access window information program and security setting time		t_{AWSSAS}	—	28.3	514	—	12.2	437.5	ms
Flash memory mode transition wait time 1		t_{DIS}	2	—	—	2	—	—	µs
Flash memory mode transition wait time 2		t_{MS}	15	—	—	15	—	—	µs

Note: Does not include the time until each operation of the flash memory is started after instructions are executed by software.
Note: The lower-limit frequency of ICLK is 1 MHz during programming or erasing the flash memory. When using ICLK at below 4 MHz, the frequency can be set to 1 MHz, 2 MHz, or 3 MHz. A non-integer frequency such as 1.5 MHz cannot be set.
Note: The frequency accuracy of ICLK must be ± 1.5% during programming or erasing the flash memory. Confirm the frequency accuracy of the clock source.

Table 2.42 Code flash characteristics (3)

Middle-speed operating mode
Conditions: VCC = 2.7 to 5.5 V, T_a = ±0℃ to +60℃

Parameter		Symbol	ICLK = 1 MHz			ICLK = 24 MHz			Unit
			Min	Typ	Max	Min	Typ	Max	
Programming time	8 bytes	t_{P8}	—	97.3	842.3	—	47.4	450.2	µs
Erasure time	2 KB	t_{E2K}	—	8.63	281.7	—	5.62	220	ms
Blank check time	8 bytes	t_{BC8}	—	—	44.5	—	—	9.1	µs
	2 KB	t_{BC2K}	—	—	1629	—	—	119	µs
Erase suspended time		t_{SED}	—	—	21.3	—	—	10.3	µs
Access window information program and security setting time		t_{AWSSAS}	—	28.3	514	—	12.2	437.3	ms
Flash memory mode transition wait time 1		t_{DIS}	2	—	—	2	—	—	µs
Flash memory mode transition wait time 2		t_{MS}	15	—	—	15	—	—	µs

Note: Does not include the time until each operation of the flash memory is started after instructions are executed by software.
Note: The lower-limit frequency of ICLK is 1 MHz during programming or erasing the flash memory. When using ICLK at below 4 MHz, the frequency can be set to 1 MHz, 2 MHz, or 3 MHz. A non-integer frequency such as 1.5 MHz cannot be set.
Note: The frequency accuracy of ICLK must be ± 1.5% during programming or erasing the flash memory. Confirm the frequency accuracy of the clock source.

Table 2.43 Code flash characteristics (4) (1 of 2)

Low-speed operating mode
Conditions: VCC = 2.7 to 5.5 V, T_a = ±0℃ to +60℃

Parameter		Symbol	ICLK = 1 MHz			Unit
			Min	Typ	Max	
Programming time	8 bytes	t_{P8}	—	97.3	842.3	µs
Erasure time	2 KB	t_{E2K}	—	8.63	281.7	ms
Blank check time	8 bytes	t_{BC8}	—	—	44.5	µs
	2 KB	t_{BC2K}	—	—	1629	µs
Erase suspended time		t_{SED}	—	—	21.3	µs

Table 2.43 Code flash characteristics (4) (2 of 2)

Low-speed operating mode
Conditions: VCC = 2.7 to 5.5 V, T_a = ±0°C to +60°C

Parameter	Symbol	ICLK = 1 MHz			Unit
		Min	Typ	Max	
Access window information program and security setting time	t_{AWSSAS}	—	28.3	514	ms
Flash memory mode transition wait time 1	t_{DIS}	2	—	—	µs
Flash memory mode transition wait time 2	t_{MS}	15	—	—	µs

Note: Does not include the time until each operation of the flash memory is started after instructions are executed by software.
Note: The lower-limit frequency of ICLK is 1 MHz during programming or erasing the flash memory. When using ICLK at below 4 MHz, the frequency can be set to 1 MHz or 2 MHz. A non-integer frequency such as 1.5 MHz cannot be set.
Note: The frequency accuracy of ICLK must be ± 1.5% during programming or erasing the flash memory. Confirm the frequency accuracy of the clock source.

2.11 Joint Test Action Group (JTAG)

Table 2.44 JTAG characteristics

Conditions: VCC = 2.7 to 5.5 V

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
TCK clock cycle time	t_{TCKcyc}	80	—	—	ns	Figure 2.33
TCK clock high pulse width	t_{TCKH}	35	—	—	ns	
TCK clock low pulse width	t_{TCKL}	35	—	—	ns	
TCK clock rise time	t_{TCKr}	—	—	5	ns	
TCK clock fall time	t_{TCKf}	—	—	5	ns	
TMS setup time	t_{TMSS}	16	—	—	ns	Figure 2.34
TMS hold time	t_{TMSH}	16	—	—	ns	
TDI setup time	t_{TDIS}	16	—	—	ns	
TDI hold time	t_{TDIH}	16	—	—	ns	
TDO data delay time	t_{TDOD}	—	—	70	ns	

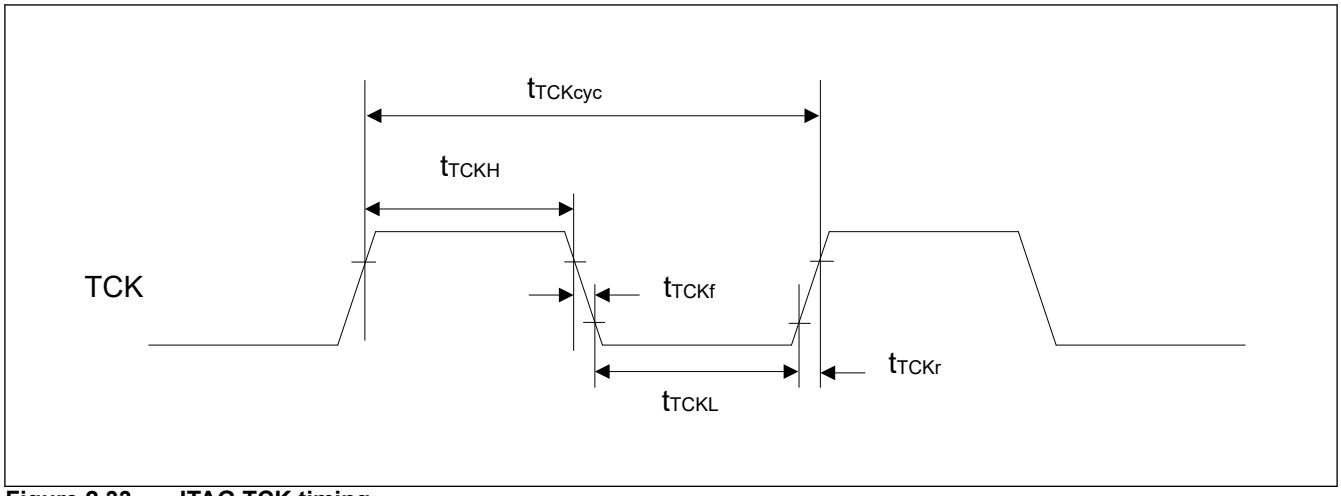


Figure 2.33 JTAG TCK timing

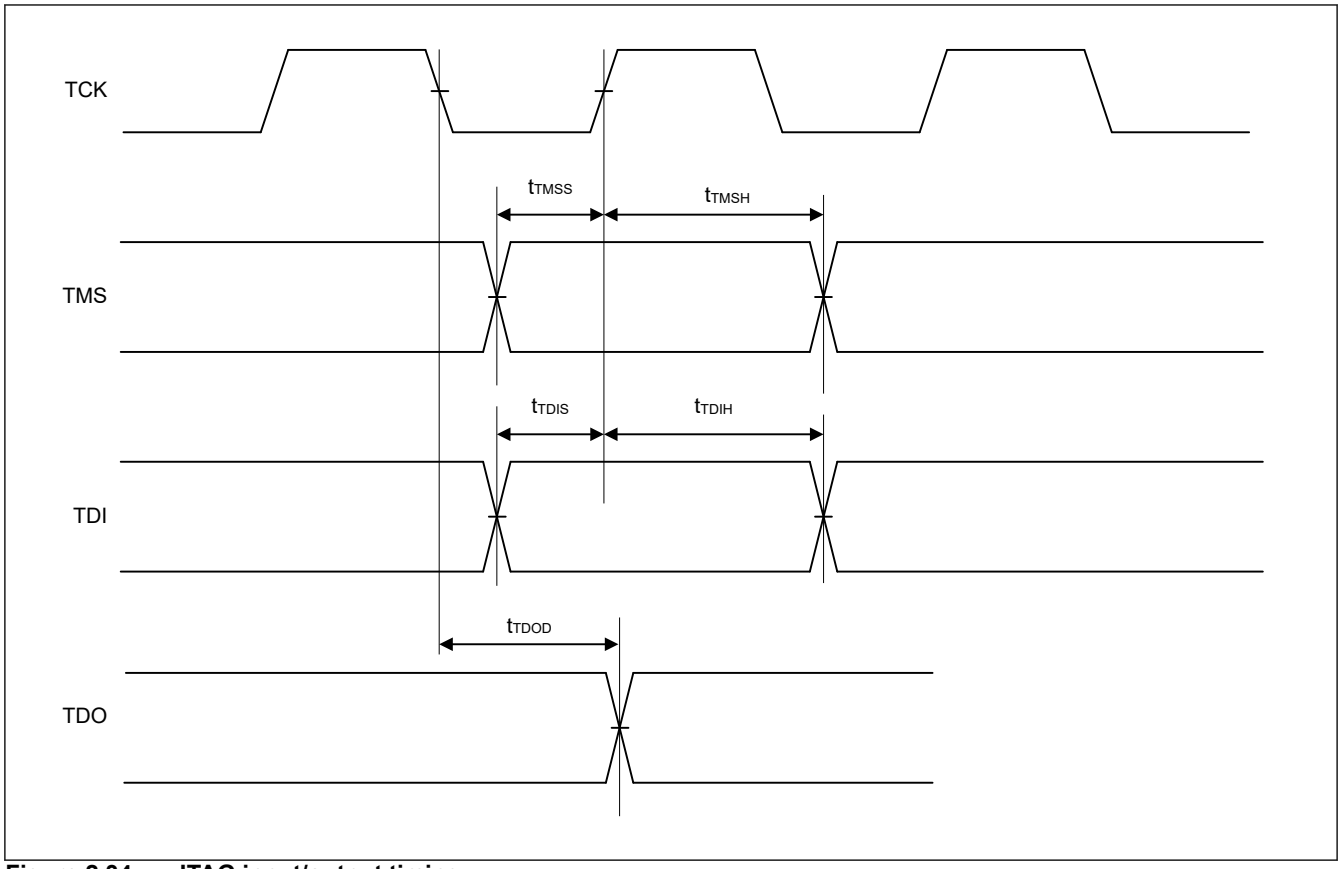


Figure 2.34 JTAG input/output timing

Appendix 1. Port States in Each Processing Mode

Table 1.1 Port states in each processing mode

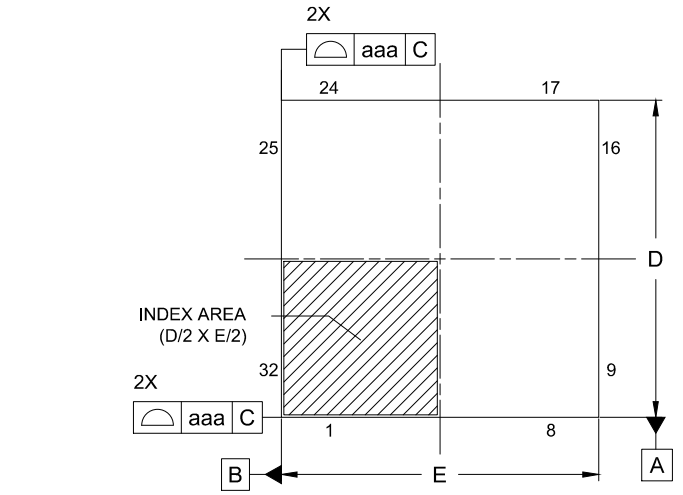
Port name	Reset	Software Standby Mode
P000/AN000/CMPIN0_A	Hi-Z	Keep-O
P001/AN001/CMPIN1_A	Hi-Z	Keep-O
P002/AN002/CMPIN1_B	Hi-Z	Keep-O
P003/AN003	Hi-Z	Keep-O
P004/AN004/CMPIN1_C/CMPREF1_A	Hi-Z	Keep-O
P005/AN005/CMPIN0_B/CMPIN1_D/CMPREF0/CMPREF1_B	Hi-Z	Keep-O
P006/AN006	Hi-Z	Keep-O
P007/AN007	Hi-Z	Keep-O
P100/GTETRGA_B/GTIOC9A_A/RXD9_B/AN016/DACOUT0/IRQ6_C/ADTRG_B/ CMPOUT1_A	Hi-Z	Keep-O*1
P101/GTIU/GTIOC9B_A/TXD9_B/AN017/DACOUT1/IRQ7_C/ADST_A/CMPOUT0_A	Hi-Z	Keep-O*1
P102/GTOUUP/GTIOC4B_A/SCK9_B/IRQ2_A/CMPOUT0_B	Hi-Z	Keep-O*1
P103/GTOULO/GTIOC4A_A/RTS_CTS9_B/IRQ3_A/CMPOUT1_B	Hi-Z	Keep-O*1
P104/GTOVUP/GTIOC5B_A/CTS9_E/SCK9_C/IRQ4_A/ADST_B	Hi-Z	Keep-O*1
P105/GTOVLO/GTIOC5A_A/SCK9_E/RTS_CTS9_C/IRQ5_A	Hi-Z	Keep-O*1
P106/GTOWUP/GTIOC6B_A/RXD9_E/TXD9_C/IRQ6_A	Hi-Z	Keep-O*1
P107/GTOWLO/GTIOC6A_A/TXD9_E/RXD9_C/IRQ7_A/CACREF	Hi-Z	Keep-O*1
P108/GTETRGA_D/GTIOC7A_B/CTS9_F/SCK9_D/IRQ4_B/CMPOUT0_D	Hi-Z	Keep-O*1
P109/GTETRGB_D/GTIOC7B_B/SCK9_F/RTS_CTS9_D/IRQ5_B/CMPOUT1_D	Hi-Z	Keep-O*1
P110/GTIV/GTIOC8B_A/RXD9_F/IRQ7_B	Hi-Z	Keep-O*1
P111/GTIW/GTIOC8A_A/TXD9_F/IRQ6_B/ADST_C	Hi-Z	Keep-O*1
P200/NMI/GTETRGA_A/ADTRG_A	Hi-Z	Hi-Z*2
P201/GTETRGB_C/GTIOC9A_B/RXD9_D/IRQ3_C/CMPOUT1_C	Hi-Z	Keep-O*1
P202/GTETRGB_B/GTIOC9B_B/TXD9_D/IRQ2_C/ADTRG_C/CLKOUT_B	Hi-Z	[CLKOUT selected] CLKOUT output [Other than the above] Keep-O*1
P203/MD	Pull-up	Keep-O*1
P300/TCK/GTETRGA_C/GTIOC8A_C/SCK9_A/IRQ0_A/CMPOUT0_C	Pull-up	Keep-O*1
P301/TMS/GTETRGB_A/GTIOC8B_C/RTS_CTS9_A/IRQ1_A	Pull-up	Keep-O*1
P302/TDO/GTIOC7B_A/GTIOC5B_B/TXD9_A/IRQ3_B	Hi-Z	Keep-O*1
P303/TDI/GTIOC7A_A/GTIOC5A_B/RXD9_A/IRQ2_B/CLKOUT_A	Pull-up	[CLKOUT selected] CLKOUT output [Other than the above] Keep-O*1

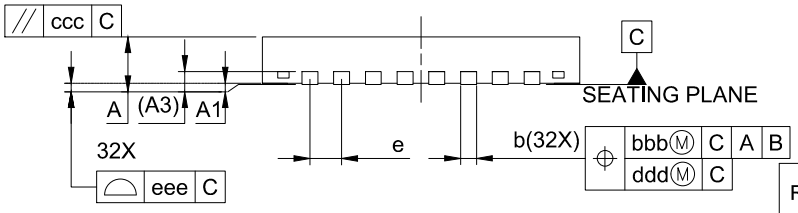
Note: Hi-Z: High-impedance
Keep-O: Output pins retain their previous values. Input pins become high-impedance.
Note 1. Input is enabled if the pin is specified as the software standby canceling source while it is used as an external interrupt pin.
Note 2. Input is enabled.

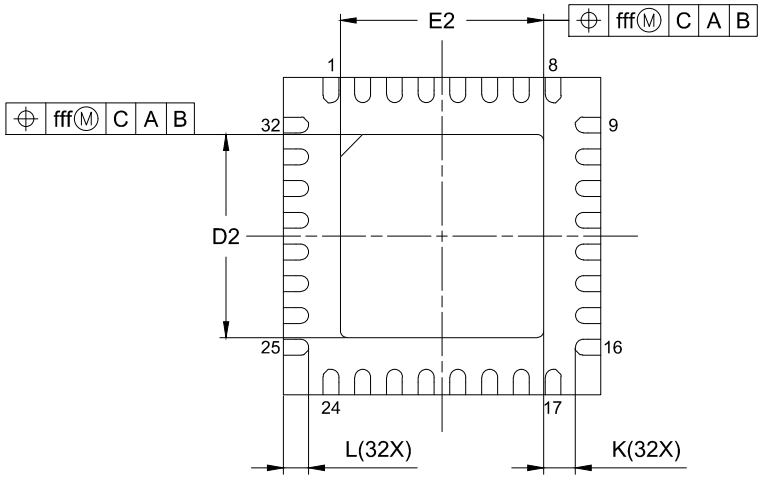
Appendix 2. Package Dimensions

Information on the latest version of the package dimensions or mountings is displayed in packages on the Renesas Electronics Corporation website.

JEITA Package code	RENESAS code	MASS(TYP.)[g]
P-HWQFN032-5x5-0.50	PWQN0032KE-A	0.06



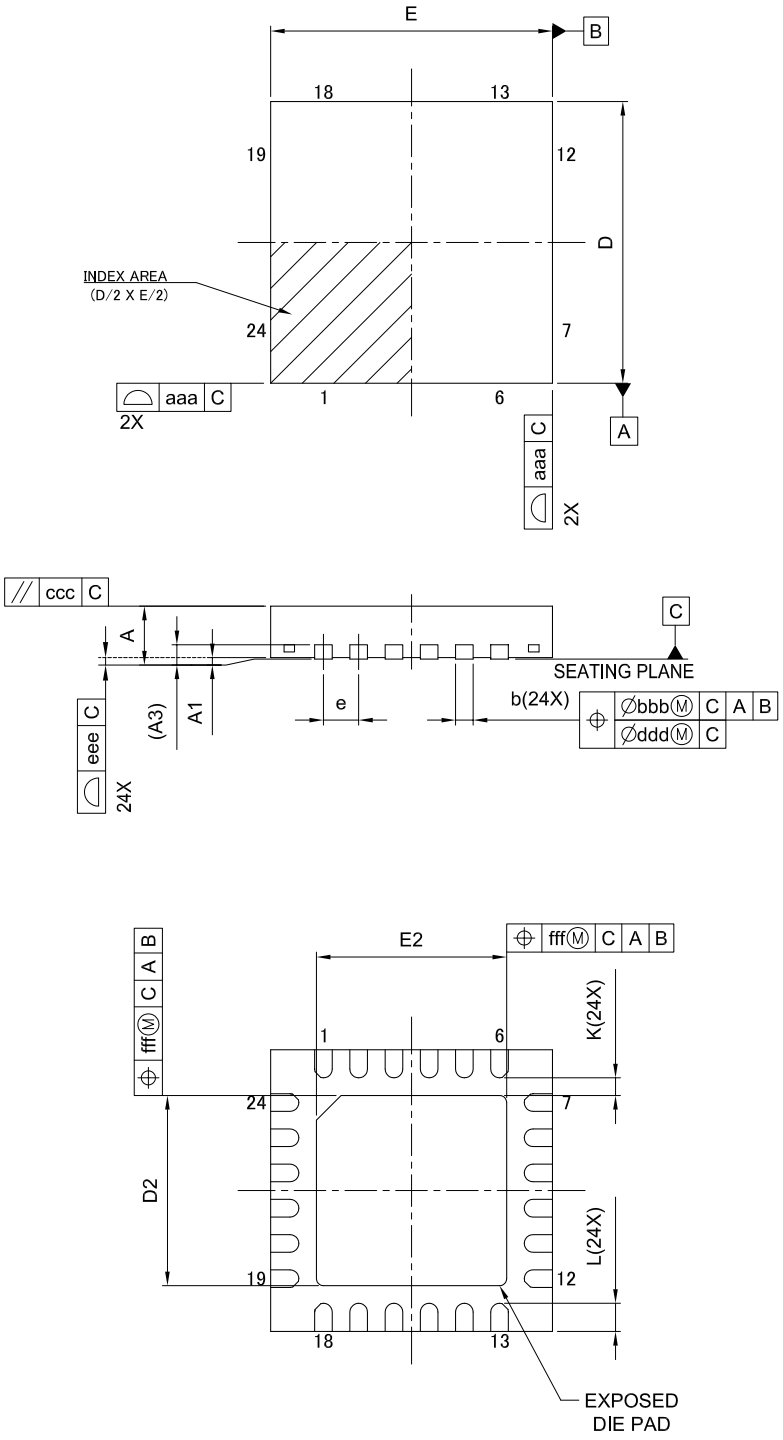




Reference Symbol	Dimension in Millimeters		
	Min.	Nom.	Max.
A	—	—	0.80
A_1	0.00	0.02	0.05
A_3		0.203 REF.	
b	0.18	0.25	0.30
D		5.00 BSC	
E		5.00 BSC	
e		0.50 BSC	
L	0.35	0.40	0.45
K	0.20	—	—
D_2	3.15	3.20	3.25
E_2	3.15	3.20	3.25
aaa		0.15	
bbb		0.10	
ccc		0.10	
ddd		0.05	
eee		0.08	
fff		0.10	

Figure 2.1 HWQFN 32-pin

JEITA Package Code	RENESAS Code	MASS(Typ.)[g]
P-HWFQFN24-4×4-0.50	PWQN0024KG-A	0.04



Reference Symbol	Dimension in Millimeters		
	Min.	Nom.	Max.
A	—	—	0.80
A_1	0.00	0.02	0.05
A_3		0.203 REF.	
b	0.18	0.25	0.30
D		4.00 BSC	
E		4.00 BSC	
e		0.50 BSC	
L	0.35	0.40	0.45
K	0.20	—	—
D_2	2.65	2.70	2.75
E_2	2.65	2.70	2.75
aaa		0.15	
bbb		0.10	
ccc		0.10	
ddd		0.05	
eee		0.08	
fff		0.10	

Figure 2.2 HWQFN 24-pin

Appendix 3. I/O Registers

This appendix describes I/O register addresses, access cycles, and reset values by function.

3.1 Peripheral Base Addresses

This section provides the base addresses for peripherals described in this manual.

Table 3.1 shows the name, description, and the base address of each peripheral.

Table 3.1 Peripheral base address (1 of 2)

Name	Description	Base address
RMPU	Memory Protection Unit	0x4000_0000
SRAM	SRAM Control	0x4000_2000
BUS	BUS Control	0x4000_3000
DTC	Data Transfer Controller	0x4000_5400
ICU	Interrupt Controller	0x4000_6000
CPU_AUX	CPU Auxiliary Registers	0x4001_A000
CPU_DBG	Debug Function	0x4001_B000
SYSC	System Control	0x4001_E000
PORT0	Port 0 Control Registers	0x4004_0000
PORT1	Port 1 Control Registers	0x4004_0020
PORT2	Port 2 Control Registers	0x4004_0040
PORT3	Port 3 Control Registers	0x4004_0060
PFS	Pmn Pin Function Control Register	0x4004_0800
POEG	Port Output Enable Module for GPT	0x4004_2000
WDT	Watchdog Timer	0x4004_4200
IWDT	Independent Watchdog Timer	0x4004_4400
CAC	Clock Frequency Accuracy Measurement Circuit	0x4004_4600
MSTP	Module Stop Control B, C, D	0x4004_7000
DOC	Data Operation Circuit	0x4005_4100
ADC120	12-bit A/D Converter	0x4005_C000
DAC8	8-bit D/A Converter	0x4005_E000
SCI9	Serial Communication Interface 9	0x4007_0240
CRC	CRC Calculator	0x4007_4000
GPT4	General PWM Timer 4 (16-bit)	0x4007_8400
GPT5	General PWM Timer 5 (16-bit)	0x4007_8500
GPT6	General PWM Timer 6 (16-bit)	0x4007_8600
GPT7	General PWM Timer 7 (16-bit)	0x4007_8700
GPT8	General PWM Timer 8 (16-bit)	0x4007_8800
GPT9	General PWM Timer 9 (16-bit)	0x4007_8900
GPT_OPS	Output Phase Switching Controller	0x4007_8FF0
ACMPHS0	Analog Comparator Unit 0	0x4008_5000
ACMPHS1	Analog Comparator Unit 1	0x4008_5100
FLCN	Flash I/O Registers	0x407E_C000
CLIC	Core-Local Interrupt Controller	0xE200_0000
IMT	Machine Timer	0xE600_0000

Table 3.1 Peripheral base address (2 of 2)

Name	Description	Base address
DBG	Debug Module	0xE680_0000

Note: Name = Peripheral name
Description = Peripheral functionality
Base address = Lowest reserved address or address used by the peripheral

3.2 Access Cycles

This section provides access cycle information for the I/O registers described in this manual.

The following information applies to Table 3.2:

- Registers are grouped by associated module.
- The number of access cycles indicates the number of cycles based on the specified reference clock.
- In the internal I/O area, reserved addresses that are not allocated to registers must not be accessed, otherwise operations cannot be guaranteed.
- The number of I/O access cycles depends on bus cycles of the internal peripheral bus, divided clock synchronization cycles, and wait cycles of each module. Divided clock synchronization cycles differ depending on the frequency ratio between ICLK and PCLK.
- When the frequency of ICLK is equal to that of PCLK, the number of divided clock synchronization cycles is always constant.
- When the frequency of ICLK is greater than that of PCLK, at least 1 PCLK cycle is added to the number of divided clock synchronization cycles.

Note: This applies to the number of cycles when access from the CPU does not conflict with the instruction fetching to the external memory or bus access from other bus master such as DTC.

Table 3.2 shows the register access cycles for non-GPT modules.

Table 3.2 Access cycles for non-GPT modules (1 of 2)

Peripherals	Address		Number of access cycles				Cycle unit	Related function
			ICLK = PCLK		ICLK > PCLK*1			
	From	To	Read	Write	Read	Write		
RMPU, RAM, BUS, DTC, ICU, CPU_AUX, CPU_DBG	0x4000_0000	0x4001_BFFF	3				ICLK	Memory Protection Unit, SRAM, Buses, Data Transfer Controller, Interrupt Controller, CPU
SYSC*2	0x4001_E000	0x4001_EFFF	4				ICLK	Low Power Modes, Resets, Low Voltage Detection, Clock Generation Circuit, Register Write Protection
PORT, PFS	0x4004_0000	0x4004_1FFF	3*3	3	2 to 3*3	2 to 3	PCLKB	I/O Ports
POEG, WDT, IWDT, CAC, MSTP, DOC, AC120, DAC8	0x4004_2000	0x4005_FFFF	3		2 to 3		PCLKB	Port Output Enable for GPT, Watchdog Timer, Independent Watchdog Timer, Clock Frequency Accuracy Measurement Circuit, Module Stop Control, Data Operation Circuit, 12-bit A/D Converter, 8-bit D/A Converter
SCIn (n = 9)	0x4007_0240	0x4007_027F	3*4		2 to 3*4		PCLKB	Serial Communications Interface
CRC	0x4007_4000	0x4007_40FF	3		2 to 3		PCLKB	CRC Calculator
GPTn (n = 4 to 9), GPT_OPS	0x4007_8400	0x4007_8FFF	See Table 3.3.				PCLKB	General PWM Timer
ACMPHSn (n = 0, 1)	0x4008_5000	0x4008_51FF	3		2 to 3		PCLKB	Analog Comparator

Table 3.2 Access cycles for non-GPT modules (2 of 2)

Peripherals	Address		Number of access cycles				Cycle unit	Related function
			ICLK = PCLK		ICLK > PCLK*1			
	From	To	Read	Write	Read	Write		
FLCN	0x407E_0000	0x407F_FFFF	3				ICLK	Temperature Sensor, Flash Control
CLIC, IMT, DBG	0xE200_0000	0xE680_0FFF	2				ICLK	CPU

Note 1. If the number of PCLK cycles is non-integer (for example 1.5), the minimum value is without the decimal point, and the maximum value is rounded up to the decimal point. For example, 1.5 to 2.5 is 1 to 3.
Note 2. These values indicate the minimum numbers of cycles for access by the CPU. They do not include the cycles required for changes in the source of the ICLK clock and frequency after changes to the SCKSCR and SCKDIVCR registers.
Note 3. When reading the PCNTR2, PIDR, and PmnPFS* registers, access is (setting value of the PRWCNTR register) cycles more than this value.
Note 4. When accessing the 16-bit register (RDRHL, TDRHL, and CDR), access is 2 cycles more than the value in Table 3.2.

Table 3.3 shows register access cycles for GPT modules.

Table 3.3 Access cycles for GPT modules

Frequency ratio between ICLK and PCLK	Number of access cycles		Cycle unit
	Read	Write	
ICLK > PCLKD = PCLKB	5 to 6	3 to 4	PCLKB
ICLK > PCLKD > PCLKB	3 to 4	2 to 3	PCLKB
PCLKD = ICLK = PCLKB	6	4	PCLKB
PCLKD = ICLK > PCLKB	2 to 3	1 to 2	PCLKB
PCLKD > ICLK = PCLKB	4	3	PCLKB
PCLKD > ICLK > PCLKB	2 to 3	1 to 2	PCLKB

3.3 Register Descriptions

This section provides information associated with registers described in this manual.

Table 3.4 shows a list of registers including address offsets, address sizes, access rights, and reset values.

Table 3.4 Register description (1 of 9)

Peripheral name	Dim	Dim inc.	Dim index	Register name	Description	Address offset	Size	R/W	Reset value	Reset mask
RMPU	-	-	-	MMPUCTLA	Bus Master MPU Control Register	0x000	16	R/W	0x0000	0xFFFF
RMPU	-	-	-	MMPUPTA	Group A Protection of Register	0x102	16	R/W	0x0000	0xFFFF
RMPU	4	0x010	0-3	MMPUACA%s	Group A Region %s access control register	0x200	16	R/W	0x0000	0xFFFF
RMPU	4	0x010	0-3	MMPUSA%s	Group A Region %s Start Address Register	0x204	32	R/W	0x00000000	0x00000003
RMPU	4	0x010	0-3	MMPUEA%s	Group A Region %s End Address Register	0x208	32	R/W	0x00000003	0x00000003
SRAM	-	-	-	PARIOAD	SRAM Parity Error Operation After Detection Register	0x00	8	R/W	0x00	0xFF
SRAM	-	-	-	SRAMPRCR	SRAM Protection Register	0x04	8	R/W	0x00	0xFF
SRAM	-	-	-	ECCMODE	ECC Operating Mode Control Register	0xC0	8	R/W	0x00	0xFF
SRAM	-	-	-	ECC2STS	ECC 2-Bit Error Status Register	0xC1	8	R/W	0x00	0xFF
SRAM	-	-	-	ECC1STSEN	ECC 1-Bit Error Information Update Enable Register	0xC2	8	R/W	0x00	0xFF
SRAM	-	-	-	ECC1STS	ECC 1-Bit Error Status Register	0xC3	8	R/W	0x00	0xFF
SRAM	-	-	-	ECCPRCR	ECC Protection Register	0xC4	8	R/W	0x00	0xFF
SRAM	-	-	-	ECCPRCR2	ECC Protection Register 2	0xD0	8	R/W	0x00	0xFF
SRAM	-	-	-	ECCETST	ECC Test Control Register	0xD4	8	R/W	0x00	0xFF

Table 3.4 Register description (2 of 9)

Peripheral name	Dim	Dim inc.	Dim index	Register name	Description	Address offset	Size	R/W	Reset value	Reset mask
SRAM	-	-	-	ECCOAD	SRAM ECC Error Operation After Detection Register	0xD8	8	R/W	0x00	0xFF
BUS	-	-	-	BUSMCNTSYS	Master Bus Control Register SYS	0x1008	16	R/W	0x0000	0xFFFF
BUS	-	-	-	BUSMCNTDMA	Master Bus Control Register DMA	0x100C	16	R/W	0x0000	0xFFFF
BUS	-	-	-	BUS3ERRADD	Bus Error Address Register 3	0x1820	32	R	0x00000000	0x00000000
BUS	-	-	-	BUS3ERRSTAT	BUS Error Status Register 3	0x1824	8	R	0x00	0xFE
BUS	-	-	-	BUS4ERRADD	Bus Error Address Register 4	0x1830	32	R	0x00000000	0x00000000
BUS	-	-	-	BUS4ERRSTAT	BUS Error Status Register 4	0x1834	8	R	0x00	0xFE
DTC	-	-	-	DTCCR	DTC Control Register	0x00	8	R/W	0x08	0xFF
DTC	-	-	-	DTCVBR	DTC Vector Base Register	0x04	32	R/W	0x00000000	0xFFFFFFFF
DTC	-	-	-	DTCST	DTC Module Start Register	0x0C	8	R/W	0x00	0xFF
DTC	-	-	-	DTCSTS	DTC Status Register	0x0E	16	R	0x0000	0xFFFF
ICU	8	0x1	0-7	IRQCR%s	IRQ Control Register	0x000	8	R/W	0x00	0xFF
ICU	-	-	-	NMICR	NMI Pin Interrupt Control Register	0x100	8	R/W	0x00	0xFF
ICU	-	-	-	NMIER	Non-Maskable Interrupt Enable Register	0x120	16	R/W	0x0000	0xFFFF
ICU	-	-	-	NMICLR	Non-Maskable Interrupt Status Clear Register	0x130	16	R/W	0x0000	0xFFFF
ICU	-	-	-	NMISR	Non-Maskable Interrupt Status Register	0x140	16	R	0x0000	0xFFFF
ICU	-	-	-	WUPEN	Wake Up Interrupt Enable Register	0x1A0	32	R/W	0x00000000	0xFFFFFFFF
ICU	-	-	-	IELEN	ICU event Enable Register	0x1C0	8	R/W	0x00	0xFF
ICU	32	0x4	0-31	IELSR%s	ICU Event Link Setting Register %s	0x300	32	R/W	0x00000000	0xFFFFFFFF
CPU_AUX	-	-	-	MACTCR	Machine Timer Control Register	0x000	32	R/W	0x00000000	0xFFFFFFFF
CPU_AUX	-	-	-	N22RCR	Reset Control Register	0x100	32	R/W	0x00000000	0xFFFFFFFF
CPU_DBG	-	-	-	DBGSTR	Debug Status Register	0x00	32	R	0x00000000	0xFFFFFFFF
CPU_DBG	-	-	-	DBGSTOPCR	Debug Stop Control Register	0x10	32	R/W	0x00000003	0xFFFFFFFF
SYSC	-	-	-	SBYCR	Standby Control Register	0x00C	16	R/W	0x0000	0xFFFF
SYSC	-	-	-	MSTPCRA	Module Stop Control Register A	0x01C	32	R/W	0xFFBFFFFF	0xFFFFFFFF
SYSC	-	-	-	SCKDIVCR	System Clock Division Control Register	0x020	32	R/W	0x04000404	0xFFFFFFFF
SYSC	-	-	-	SCKSCR	System Clock Source Control Register	0x026	8	R/W	0x01	0xFF
SYSC	-	-	-	HOCOCR	High-Speed On-Chip Oscillator Control Register	0x036	8	R/W	0x00	0xFE
SYSC	-	-	-	MOCOCR	Middle-Speed On-Chip Oscillator Control Register	0x038	8	R/W	0x00	0xFF
SYSC	-	-	-	OSCSF	Oscillation Stabilization Flag Register	0x03C	8	R	0x00	0xFE
SYSC	-	-	-	CKOCR	Clock Out Control Register	0x03E	8	R/W	0x00	0xFF
SYSC	-	-	-	LPOPT	Lower Power Operation Control Register	0x04C	8	R/W	0x00	0xFF
SYSC	-	-	-	HOCOUTCR	HOCO User Trimming Control Register	0x062	8	R/W	0x00	0xFF
SYSC	-	-	-	PSMCR	Power Save Memory Control Register	0x09F	8	R/W	0x00	0xFF
SYSC	-	-	-	OPCCR	Operating Power Control Register	0x0A0	8	R/W	0x01	0xFF
SYSC	-	-	-	RSTSR1	Reset Status Register 1	0x0C0	16	R/W	0x0000	0xF4F8
SYSC	-	-	-	LVD1CR1	Voltage Monitor 1 Circuit Control Register	0x0E0	8	R/W	0x01	0xFF
SYSC	-	-	-	LVD1SR	Voltage Monitor 1 Circuit Status Register	0x0E1	8	R/W	0x02	0xFF
SYSC	-	-	-	LVD2CR1	Voltage Monitor 2 Circuit Control Register 1	0x0E2	8	R/W	0x01	0xFF
SYSC	-	-	-	LVD2SR	Voltage Monitor 2 Circuit Status Register	0x0E3	8	R/W	0x02	0xFF
SYSC	-	-	-	PRCR	Protect Register	0x3FE	16	R/W	0x0000	0xFFFF
SYSC	-	-	-	SYOCDCR	System Control OCD Control Register	0x040E	8	R/W	0x00	0xFF
SYSC	-	-	-	RSTSR0	Reset Status Register 0	0x410	8	R/W	0x00	0xF0

Table 3.4 Register description (3 of 9)

Peripheral name	Dim	Dim inc.	Dim index	Register name	Description	Address offset	Size	R/W	Reset value	Reset mask
SYSC	-	-	-	RSTSR2	Reset Status Register 2	0x411	8	R/W	0x00	0xFE
SYSC	-	-	-	LVCMPCR	Voltage Monitor Circuit Control Register	0x417	8	R/W	0x00	0xFF
SYSC	-	-	-	LVDLVLR	Voltage Detection Level Select Register	0x418	8	R/W	0x07	0xFF
SYSC	-	-	-	LVD1CR0	Voltage Monitor 1 Circuit Control Register 0	0x41A	8	R/W	0x80	0xF7
SYSC	-	-	-	LVD2CR0	Voltage Monitor 2 Circuit Control Register 0	0x41B	8	R/W	0x80	0xF7
SYSC	-	-	-	LOCOCR	Low-Speed On-Chip Oscillator Control Register	0x490	8	R/W	0x00	0xFF
PORT0-3	-	-	-	PCNTR1	Port Control Register 1	0x000	32	R/W	0x00000000	0xFFFFFFFF
PORT0-3	-	-	-	PODR	Port Control Register 1	0x000	16	R/W	0x0000	0xFFFF
PORT0-3	-	-	-	PDR	Port Control Register 1	0x002	16	R/W	0x0000	0xFFFF
PORT0-3	-	-	-	PCNTR2	Port Control Register 2	0x004	32	R	0x00000000	0xFFFF0000
PORT0-3	-	-	-	PIDR	Port Control Register 2	0x006	16	R	0x0000	0x0000
PORT0-3	-	-	-	PCNTR3	Port Control Register 3	0x008	32	W	0x00000000	0xFFFFFFFF
PORT0-3	-	-	-	PORR	Port Control Register 3	0x008	16	W	0x0000	0xFFFF
PORT0-3	-	-	-	POSR	Port Control Register 3	0x00A	16	W	0x0000	0xFFFF
PFS	8	0x4	0-7	P0%sPFS	Port 0%s Pin Function Select Register	0x000	32	R/W	0x00000000	0xFFFFFFFD
PFS	8	0x4	0-7	P0%sPFS_HA	Port 0%s Pin Function Select Register	0x002	16	R/W	0x0000	0xFFFD
PFS	8	0x4	0-7	P0%sPFS_BY	Port 0%s Pin Function Select Register	0x003	8	R/W	0x00	0xFD
PFS	10	0x4	0-9	P10%sPFS	Port 10%s Pin Function Select Register	0x040	32	R/W	0x00000000	0xFFFFFFFD
PFS	10	0x4	0-9	P10%sPFS_HA	Port 10%s Pin Function Select Register	0x042	16	R/W	0x0000	0xFFFD
PFS	10	0x4	0-9	P10%sPFS_BY	Port 10%s Pin Function Select Register	0x043	8	R/W	0x00	0xFD
PFS	-	-	-	P110PFS	Port 110 Pin Function Select Register	0x068	32	R/W	0x00000000	0xFFFFFFFD
PFS	-	-	-	P110PFS_HA	Port 110 Pin Function Select Register	0x06A	16	R/W	0x0000	0xFFFD
PFS	-	-	-	P110PFS_BY	Port 110 Pin Function Select Register	0x06B	8	R/W	0x00	0xFD
PFS	-	-	-	P111PFS	Port 111 Pin Function Select Register	0x06C	32	R/W	0x00000000	0xFFFFFFFD
PFS	-	-	-	P111PFS_HA	Port 111 Pin Function Select Register	0x06E	16	R/W	0x0000	0xFFFD
PFS	-	-	-	P111PFS_BY	Port 111 Pin Function Select Register	0x06F	8	R/W	0x00	0xFD
PFS	4	0x4	0-3	P20%sPFS	Port 20%s Pin Function Select Register	0x080	32	R/W	0x00000000	0xFFFFFFFD
PFS	4	0x4	0-3	P20%sPFS_HA	Port 20%s Pin Function Select Register	0x082	16	R/W	0x0000	0xFFFD
PFS	4	0x4	0-3	P20%sPFS_BY	Port 20%s Pin Function Select Register	0x083	8	R/W	0x00	0xFD
PFS	4	0x4	0-3	P30%sPFS	Port 30%s Pin Function Select Register	0x0C0	32	R/W	0x00000000	0xFFFFFFFD
PFS	4	0x4	0-3	P30%sPFS_HA	Port 30%s Pin Function Select Register	0x0C2	16	R/W	0x0000	0xFFFD
PFS	4	0x4	0-3	P30%sPFS_BY	Port 30%s Pin Function Select Register	0x0C3	8	R/W	0x00	0xFD
POEG	-	-	-	POEGGA	POEG Group A Setting Register	0x000	32	R/W	0x00000000	0xFFFFFFFF
POEG	-	-	-	GTONCWPA	GPTW Output Stopping Control Group A Write Protection Register	0x040	16	R/W	0x0000	0xFFFF
POEG	-	-	-	GTONCCRA	GPTW Output Stopping Control Group A Controlling Register	0x044	16	R/W	0x0000	0xFFFF
POEG	-	-	-	POEGGB	POEG Group B Setting Register	0x100	32	R/W	0x00000000	0xFFFFFFFF
POEG	-	-	-	GTONCWPB	GPTW Output Stopping Control Group B Write Protection Register	0x140	16	R/W	0x0000	0xFFFF
POEG	-	-	-	GTONCCRB	GPTW Output Stopping Control Group B Controlling Register	0x144	16	R/W	0x0000	0xFFFF
WDT	-	-	-	WDTRR	WDT Refresh Register	0x00	8	R/W	0xFF	0xFF
WDT	-	-	-	WDTCR	WDT Control Register	0x02	16	R/W	0x33F3	0xFFFF
WDT	-	-	-	WDTSR	WDT Status Register	0x04	16	R/W	0x0000	0xFFFF

Table 3.4 Register description (4 of 9)

Peripheral name	Dim	Dim inc.	Dim index	Register name	Description	Address offset	Size	R/W	Reset value	Reset mask
WDT	-	-	-	WDTRCR	WDT Reset Control Register	0x06	8	R/W	0x80	0xFF
WDT	-	-	-	WDTCSTPR	WDT Count Stop Control Register	0x08	8	R/W	0x80	0xFF
IWDT	-	-	-	IWDTRR	IWDT Refresh Register	0x00	8	R/W	0xFF	0xFF
IWDT	-	-	-	IWDTSR	IWDT Status Register	0x04	16	R/W	0x0000	0xFFFF
CAC	-	-	-	CACR0	CAC Control Register 0	0x00	8	R/W	0x00	0xFF
CAC	-	-	-	CACR1	CAC Control Register 1	0x01	8	R/W	0x00	0xFF
CAC	-	-	-	CACR2	CAC Control Register 2	0x02	8	R/W	0x00	0xFF
CAC	-	-	-	CAICR	CAC Interrupt Control Register	0x03	8	R/W	0x00	0xFF
CAC	-	-	-	CASTR	CAC Status Register	0x04	8	R	0x00	0xFF
CAC	-	-	-	CAULVR	CAC Upper-Limit Value Setting Register	0x06	16	R/W	0x0000	0xFFFF
CAC	-	-	-	CALLVR	CAC Lower-Limit Value Setting Register	0x08	16	R/W	0x0000	0xFFFF
CAC	-	-	-	CACNTBR	CAC Counter Buffer Register	0x0A	16	R	0x0000	0xFFFF
MSTP	-	-	-	MSTPCRB	Module Stop Control Register B	0x000	32	R/W	0xFFFFFFFF	0xFFFFFFFF
MSTP	-	-	-	MSTPCRC	Module Stop Control Register C	0x004	32	R/W	0xFFFFFFFF	0xFFFFFFFF
MSTP	-	-	-	MSTPCRD	Module Stop Control Register D	0x008	32	R/W	0xFFFFFFFF	0xFFFFFFFF
MSTP	-	-	-	LSMRWDIS	Low Speed Module R/W Disable Control Register	0x00C	16	R/W	0x0000	0xFFFF
DOC	-	-	-	DOCR	DOC Control Register	0x00	8	R/W	0x00	0xFF
DOC	-	-	-	DODIR	DOC Data Input Register	0x02	16	R/W	0x0000	0xFFFF
DOC	-	-	-	DODSR	DOC Data Setting Register	0x04	16	R/W	0x0000	0xFFFF
ADC120	-	-	-	ADCSR	A/D Control Register	0x000	16	R/W	0x0000	0xFFFF
ADC120	-	-	-	ADANSA0	A/D Channel Select Register A0	0x004	16	R/W	0x0000	0xFFFF
ADC120	-	-	-	ADANSA1	A/D Channel Select Register A1	0x006	16	R/W	0x0000	0xFFFF
ADC120	-	-	-	ADADS0	A/D-Converted Value Addition/Average Channel Select Register 0	0x008	16	R/W	0x0000	0xFFFF
ADC120	-	-	-	ADADS1	A/D-Converted Value Addition/Average Channel Select Register 1	0x00A	16	R/W	0x0000	0xFFFF
ADC120	-	-	-	ADADC	A/D-Converted Value Addition/Average Count Select Register	0x00C	8	R/W	0x00	0xFF
ADC120	-	-	-	ADCER	A/D Control Extended Register	0x00E	16	R/W	0x0000	0xFFFF
ADC120	-	-	-	ADSTRGR	A/D Conversion Start Trigger Select Register	0x010	16	R/W	0x0000	0xFFFF
ADC120	-	-	-	ADEXICR	A/D Conversion Extended Input Control Registers	0x012	16	R/W	0x0000	0xFFFF
ADC120	-	-	-	ADANSB0	A/D Channel Select Register B0	0x014	16	R/W	0x0000	0xFFFF
ADC120	-	-	-	ADANSB1	A/D Channel Select Register B1	0x016	16	R/W	0x0000	0xFFFF
ADC120	-	-	-	ADDBLDR	A/D Data Duplexing Register	0x018	16	R	0x0000	0xFFFF
ADC120	-	-	-	ADTSDR	A/D Temperature Sensor Data Register	0x01A	16	R	0x0000	0xFFFF
ADC120	-	-	-	ADOCDR	A/D Internal Reference Voltage Data Register	0x01C	16	R	0x0000	0xFFFF
ADC120	-	-	-	ADRD	A/D Self-Diagnosis Data Register	0x01E	16	R	0x0000	0xFFFF
ADC120	8	0x2	0-7	ADDR%s	A/D Data Registers %s	0x020	16	R	0x0000	0xFFFF
ADC120	2	0x2	16-17	ADDR%s	A/D Data Registers %s	0x040	16	R	0x0000	0xFFFF
ADC120	-	-	-	ADSHCR	A/D S&H Circuit Control Register	0x066	16	R/W	0x001A	0xFFFF
ADC120	-	-	-	ADDISCR	A/D Disconnection Detection Control Register	0x07A	8	R/W	0x00	0xFF
ADC120	-	-	-	ADACSR	A/D Conversion Operation Mode Select Register	0x07E	8	R/W	0x00	0xFF
ADC120	-	-	-	ADGSPCR	A/D Group Scan Priority Control Register	0x080	16	R/W	0x0000	0xFFFF

Table 3.4 Register description (5 of 9)

Peripheral name	Dim	Dim inc.	Dim index	Register name	Description	Address offset	Size	R/W	Reset value	Reset mask
ADC120	-	-	-	ADDBLDRA	A/D Data Duplexing Register A	0x084	16	R	0x0000	0xFFFF
ADC120	-	-	-	ADDBLDRB	A/D Data Duplexing Register B	0x086	16	R	0x0000	0xFFFF
ADC120	-	-	-	ADHVREFCNT	A/D High-Potential/Low-Potential Reference Voltage Control Register	0x08A	8	R/W	0x00	0xFF
ADC120	-	-	-	ADWINMON	A/D Compare Function Window A/B Status Monitor Register	0x08C	8	R	0x00	0xFF
ADC120	-	-	-	ADCMPCR	A/D Compare Function Control Register	0x090	16	R/W	0x0000	0xFFFF
ADC120	-	-	-	ADCMPANSER	A/D Compare Function Window A Extended Input Select Register	0x092	8	R/W	0x00	0xFF
ADC120	-	-	-	ADCMPLER	A/D Compare Function Window A Extended Input Comparison Condition Setting Register	0x093	8	R/W	0x00	0xFF
ADC120	-	-	-	ADCMPANSR0	A/D Compare Function Window A Channel Select Register 0	0x094	16	R/W	0x0000	0xFFFF
ADC120	-	-	-	ADCMPANSR1	A/D Compare Function Window A Channel Select Register 1	0x096	16	R/W	0x0000	0xFFFF
ADC120	-	-	-	ADCMPLR0	A/D Compare Function Window A Comparison Condition Setting Register 0	0x098	16	R/W	0x0000	0xFFFF
ADC120	-	-	-	ADCMPLR1	A/D Compare Function Window A Comparison Condition Setting Register 1	0x09A	16	R/W	0x0000	0xFFFF
ADC120	2	0x2	0-1	ADCMPDR%s	A/D Compare Function Window A Lower-Side/Upper-Side Level Setting Register	0x09C	16	R/W	0x0000	0xFFFF
ADC120	-	-	-	ADCMPSR0	A/D Compare Function Window A Channel Status Register 0	0x0A0	16	R/W	0x0000	0xFFFF
ADC120	-	-	-	ADCMPSR1	A/D Compare Function Window A Channel Status Register1	0x0A2	16	R/W	0x0000	0xFFFF
ADC120	-	-	-	ADCMPSER	A/D Compare Function Window A Extended Input Channel Status Register	0x0A4	8	R/W	0x00	0xFF
ADC120	-	-	-	ADCMPBNSR	A/D Compare Function Window B Channel Select Register	0x0A6	8	R/W	0x00	0xFF
ADC120	-	-	-	ADWINLLB	A/D Compare Function Window B Lower-Side Level Setting Register	0x0A8	16	R/W	0x0000	0xFFFF
ADC120	-	-	-	ADWINULB	A/D Compare Function Window B Upper-Side Level Setting Register	0x0AA	16	R/W	0x0000	0xFFFF
ADC120	-	-	-	ADCMPBSR	A/D Compare Function Window B Status Register	0x0AC	8	R/W	0x00	0xFF
ADC120	-	-	-	ADANSC0	A/D Channel Select Register C0	0x0D4	16	R/W	0x0000	0xFFFF
ADC120	-	-	-	ADANSC1	A/D Channel Select Register C1	0x0D6	16	R/W	0x0000	0xFFFF
ADC120	-	-	-	ADGCTRGR	A/D Group C Trigger Select Register	0x0D9	8	R/W	0x00	0xFF
ADC120	-	-	-	ADSSTRL	A/D Sampling State Register L	0x0DD	8	R/W	0x00	0xFF
ADC120	-	-	-	ADSSTRT	A/D Sampling State Register T	0x0DE	8	R/W	0x00	0xFF
ADC120	-	-	-	ADSSTRO	A/D Sampling State Register O	0x0DF	8	R/W	0x00	0xFF
ADC120	8	0x1	0-7	ADSSTR%s	A/D Sampling State Register	0x0E0	8	R/W	0x0D	0xFF
ADC120	-	-	-	ADPGACR	A/D Programmable Gain Amplifier Control Register	0x1A0	16	R/W	0x0000	0xFFFF
ADC120	-	-	-	ADPGAGS0	A/D Programmable Gain Amplifier Gain Setting Register 0	0x1A2	16	R/W	0x0000	0xFFFF
DAC8	2	0x2	0-1	DADR%s	D/A Data Register	0x000	16	R/W	0x0000	0xFFFF
DAC8	-	-	-	DACR	D/A Control Register	0x004	8	R/W	0x1F	0xFF
DAC8	-	-	-	DADPR	Data Register Format Select Register	0x005	8	R/W	0x00	0xFF
DAC8	-	-	-	DAADSCR	D/A A/D Synchronous Start Control Register	0x006	8	R/W	0x00	0xFF
DAC8	-	-	-	DAEXOUT	D/A External Output Enable Register	0x700	16	R/W	0x0000	0xFFFF

Table 3.4 Register description (6 of 9)

Peripheral name	Dim	Dim inc.	Dim index	Register name	Description	Address offset	Size	R/W	Reset value	Reset mask
SCI9	-	-	-	SMR	Serial Mode Register for Non-Smart Card Interface Mode (SCMR.SMIF = 0)	0x00	8	R/W	0x00	0xFF
SCI9	-	-	-	SMR_SMCI	Serial Mode Register for Smart Card Interface Mode (SCMR.SMIF = 1)	0x00	8	R/W	0x00	0xFF
SCI9	-	-	-	BRR	Bit Rate Register	0x01	8	R/W	0xFF	0xFF
SCI9	-	-	-	SCR	Serial Control Register for Non-Smart Card Interface Mode (SCMR.SMIF = 0)	0x02	8	R/W	0x00	0xFF
SCI9	-	-	-	SCR_SMCI	Serial Control Register for Smart Card Interface Mode (SCMR.SMIF = 1)	0x02	8	R/W	0x00	0xFF
SCI9	-	-	-	TDR	Transmit Data Register	0x03	8	R/W	0xFF	0xFF
SCI9	-	-	-	SSR	Serial Status Register for Non-Smart Card Interface and Non-FIFO Mode (SCMR.SMIF = 0 and FCR.FM = 0)	0x04	8	R/W	0x84	0xFF
SCI9	-	-	-	SSR_SMCI	Serial Status Register for Smart Card Interface Mode (SCMR.SMIF = 1)	0x04	8	R/W	0x84	0xFF
SCI9	-	-	-	RDR	Receive Data Register	0x05	8	R/W	0x00	0xFF
SCI9	-	-	-	SCMR	Smart Card Mode Register	0x06	8	R/W	0xF2	0xFF
SCI9	-	-	-	SEMR	Serial Extended Mode Register	0x07	8	R/W	0x00	0xFF
SCI9	-	-	-	SNFR	Noise Filter Setting Register	0x08	8	R/W	0x00	0xFF
SCI9	-	-	-	SIMR1	IIC Mode Register 1	0x09	8	R/W	0x00	0xFF
SCI9	-	-	-	SIMR2	IIC Mode Register 2	0x0A	8	R/W	0x00	0xFF
SCI9	-	-	-	SIMR3	IIC Mode Register 3	0x0B	8	R/W	0x00	0xFF
SCI9	-	-	-	SISR	IIC Status Register	0x0C	8	R	0x00	0xCB
SCI9	-	-	-	SPMR	SPI Mode Register	0x0D	8	R/W	0x00	0xFF
SCI9	-	-	-	TDRHL	Transmit Data Register	0x0E	16	R/W	0xFFFF	0xFFFF
SCI9	-	-	-	RDRHL	Receive Data Register	0x10	16	R	0x0000	0xFFFF
SCI9	-	-	-	MDDR	Modulation Duty Register	0x12	8	R/W	0xFF	0xFF
SCI9	-	-	-	DCCR	Data Compare Match Control Register	0x13	8	R/W	0x40	0xFF
SCI9	-	-	-	CDR	Compare Match Data Register	0x1A	16	R/W	0x0000	0xFFFF
SCI9	-	-	-	SPTR	Serial Port Register	0x1C	8	R/W	0x03	0xFF
SCI9	-	-	-	ACTR	Adjustment communication timing register	0x1D	8	R/W	0x00	0xFF
CRC	-	-	-	CRCCR0	CRC Control Register 0	0x00	8	R/W	0x00	0xFF
CRC	-	-	-	CRCCR1	CRC Control Register 1	0x01	8	R/W	0x00	0xFF
CRC	-	-	-	CRCDIR	CRC Data Input Register	0x04	32	R/W	0x00000000	0xFFFFFFFF
CRC	-	-	-	CRCDIR_BY	CRC Data Input Register	0x04	8	R/W	0x00	0xFF
CRC	-	-	-	CRCDOR	CRC Data Output Register	0x08	32	R/W	0x00000000	0xFFFFFFFF
CRC	-	-	-	CRCDOR_HA	CRC Data Output Register	0x08	16	R/W	0x0000	0xFFFF
CRC	-	-	-	CRCDOR_BY	CRC Data Output Register	0x08	8	R/W	0x00	0xFF
CRC	-	-	-	CRCSAR	Snoop Address Register	0x0C	16	R/W	0x0000	0xFFFF
GPT4-9	-	-	-	GTWP	General PWM Timer Write-Protection Register	0x00	32	R/W	0x00000000	0xFFFFFFFF
GPT4-9	-	-	-	GTSTR	General PWM Timer Software Start Register	0x04	32	R/W	0x00000000	0xFFFFFFFF
GPT4-9	-	-	-	GTSTP	General PWM Timer Software Stop Register	0x08	32	R/W	0xFFFFFFFF	0xFFFFFFFF
GPT4-9	-	-	-	GTCLR	General PWM Timer Software Clear Register	0x0C	32	W	0x00000000	0xFFFFFFFF
GPT4-9	-	-	-	GTSSR	General PWM Timer Start Source Select Register	0x10	32	R/W	0x00000000	0xFFFFFFFF
GPT4-9	-	-	-	GTPSR	General PWM Timer Stop Source Select Register	0x14	32	R/W	0x00000000	0xFFFFFFFF

Table 3.4 Register description (7 of 9)

Peripheral name	Dim	Dim inc.	Dim index	Register name	Description	Address offset	Size	R/W	Reset value	Reset mask
GPT4-9	-	-	-	GTCSR	General PWM Timer Clear Source Select Register	0x18	32	R/W	0x00000000	0xFFFFFFFF
GPT4-9	-	-	-	GTUPSR	General PWM Timer Up Count Source Select Register	0x1C	32	R/W	0x00000000	0xFFFFFFFF
GPT4-9	-	-	-	GTDNSR	General PWM Timer Down Count Source Select Register	0x20	32	R/W	0x00000000	0xFFFFFFFF
GPT4-9	-	-	-	GTICASR	General PWM Timer Input Capture Source Select Register A	0x24	32	R/W	0x00000000	0xFFFFFFFF
GPT4-9	-	-	-	GTICBSR	General PWM Timer Input Capture Source Select Register B	0x28	32	R/W	0x00000000	0xFFFFFFFF
GPT4-9	-	-	-	GTCR	General PWM Timer Control Register	0x2C	32	R/W	0x00000000	0xFFFFFFFF
GPT4-9	-	-	-	GTUDDTYC	General PWM Timer Count Direction and Duty Setting Register	0x30	32	R/W	0x00000001	0xFFFFFFFF
GPT4-9	-	-	-	GTIOR	General PWM Timer I/O Control Register	0x34	32	R/W	0x00000000	0xFFFFFFFF
GPT4-9	-	-	-	GTINTAD	General PWM Timer Interrupt Output Setting Register	0x38	32	R/W	0x00000000	0xFFFFFFFF
GPT4-9	-	-	-	GTST	General PWM Timer Status Register	0x3C	32	R/W	0x00008000	0xFFFFFFFF
GPT4-9	-	-	-	GTBER	General PWM Timer Buffer Enable Register	0x40	32	R/W	0x00000000	0xFFFFFFFF
GPT4-9	-	-	-	GTITC	General PWM Timer Interrupt and A/D Converter Start Request Skipping Setting Register	0x44	32	R/W	0x00000000	0xFFFFFFFF
GPT4-9	-	-	-	GTCNT	General PWM Timer Counter	0x48	32	R/W	0x00000000	0xFFFFFFFF
GPT4-9	-	-	-	GTCCRA	General PWM Timer Compare Capture Register A	0x4C	32	R/W	0x0000FFFF	0xFFFFFFFF
GPT4-9	-	-	-	GTCCRB	General PWM Timer Compare Capture Register B	0x50	32	R/W	0x0000FFFF	0xFFFFFFFF
GPT4-9	-	-	-	GTCCRC	General PWM Timer Compare Capture Register C	0x54	32	R/W	0x0000FFFF	0xFFFFFFFF
GPT4-9	-	-	-	GTCCRE	General PWM Timer Compare Capture Register E	0x58	32	R/W	0x0000FFFF	0xFFFFFFFF
GPT4-9	-	-	-	GTCCRD	General PWM Timer Compare Capture Register D	0x5C	32	R/W	0x0000FFFF	0xFFFFFFFF
GPT4-9	-	-	-	GTCCRF	General PWM Timer Compare Capture Register F	0x60	32	R/W	0x0000FFFF	0xFFFFFFFF
GPT4-9	-	-	-	GTPR	General PWM Timer Cycle Setting Register	0x64	32	R/W	0x0000FFFF	0xFFFFFFFF
GPT4-9	-	-	-	GTPBR	General PWM Timer Cycle Setting Buffer Register	0x68	32	R/W	0x0000FFFF	0xFFFFFFFF
GPT4-9	-	-	-	GTPDBR	General-purpose PWM timer cycle setting double buffer register	0x6C	32	R/W	0x0000FFFF	0xFFFFFFFF
GPT4-9	-	-	-	GTADTRA	A/D conversion start request timing register A	0x70	32	R/W	0x0000FFFF	0xFFFFFFFF
GPT4-9	-	-	-	GTADTBRA	A/D conversion start request timing buffer register A	0x74	32	R/W	0x0000FFFF	0xFFFFFFFF
GPT4-9	-	-	-	GTADTDBRA	A/D conversion start request timing buffer register A	0x78	32	R/W	0x0000FFFF	0xFFFFFFFF
GPT4-9	-	-	-	GTADTRB	A/D conversion start request timing register B	0x7C	32	R/W	0x0000FFFF	0xFFFFFFFF
GPT4-9	-	-	-	GTADTBRB	A/D conversion start request timing buffer register B	0x80	32	R/W	0x0000FFFF	0xFFFFFFFF
GPT4-9	-	-	-	GTADTDBRB	A/D conversion start request timing buffer register B	0x84	32	R/W	0x0000FFFF	0xFFFFFFFF
GPT4-9	-	-	-	GTDTCR	General PWM Timer Dead Time Control Register	0x88	32	R/W	0x00000000	0xFFFFFFFF
GPT4-9	-	-	-	GTDVU	General PWM Timer Dead Time Value Register U	0x8C	32	R/W	0x0000FFFF	0xFFFFFFFF

Table 3.4 Register description (8 of 9)

Peripheral name	Dim	Dim inc.	Dim index	Register name	Description	Address offset	Size	R/W	Reset value	Reset mask
GPT4-9	-	-	-	GTDVD	General purpose PWM timer dead time value register D	0x90	32	R/W	0x0000FFFF	0xFFFFFFFF
GPT4-9	-	-	-	GTDBU	General purpose PWM timer dead time buffer register U	0x94	32	R/W	0x0000FFFF	0xFFFFFFFF
GPT4-9	-	-	-	GTDBD	General purpose PWM timer dead time buffer register D	0x98	32	R/W	0x0000FFFF	0xFFFFFFFF
GPT4-9	-	-	-	GTSOS	General-purpose PWM timer output protection function status register	0x9C	32	R/W	0x00000000	0xFFFFFFFF
GPT4-9	-	-	-	GTSOTR	General-purpose PWM timer output protection function temporary release register	0xA0	32	R/W	0x00000000	0xFFFFFFFF
GPT4-9	-	-	-	GTSECSR	General-purpose PWM timer operation permission bit simultaneous control channel selection register	0xD0	32	R/W	0x00000000	0xFFFFFFFF
GPT4-9	-	-	-	GTSECR	General-purpose PWM timer operation permission bit simultaneous control register	0xD4	32	R/W	0x00000000	0xFFFFFFFF
GPT_OPS	-	-	-	OPSCR	Output Phase Switching Control Register	0x00	32	R/W	0x00000000	0xFFFFFFFF
ACMPHS0-1	-	-	-	CMPCTL	Comparator Control Register	0x00	8	R/W	0x00	0xFF
ACMPHS0-1	-	-	-	CMPSEL0	Comparator Input Select Register	0x04	8	R/W	0x00	0xFF
ACMPHS0-1	-	-	-	CMPSEL1	Comparator Reference Voltage Select Register	0x08	8	R/W	0x00	0xFF
ACMPHS0-1	-	-	-	CMPMON	Comparator Output Monitor Register	0x0C	8	R/W	0x00	0xFF
ACMPHS0-1	-	-	-	CPIOC	Comparator Output Control Register	0x10	8	R/W	0x00	0xFF
FLCN	-	-	-	FPMCR	Flash P/E Mode Control Register	0x0100	8	R/W	0x08	0xFF
FLCN	-	-	-	FASR	Flash Area Select Register	0x0104	8	R/W	0x00	0xFF
FLCN	-	-	-	FSARL	Flash Processing Start Address Register L	0x0108	16	R/W	0x0000	0xFFFF
FLCN	-	-	-	FSARH	Flash Processing Start Address Register H	0x0110	16	R/W	0x0000	0xFFFF
FLCN	-	-	-	FCR	Flash Control Register	0x0114	8	R/W	0x00	0xFF
FLCN	-	-	-	FEARL	Flash Processing End Address Register L	0x0118	16	R/W	0x0000	0xFFFF
FLCN	-	-	-	FEARH	Flash Processing End Address Register H	0x0120	16	R/W	0x0000	0xFFFF
FLCN	-	-	-	FRESETR	Flash Reset Register	0x0124	8	R/W	0x00	0xFF
FLCN	-	-	-	FSTATR00	Flash Status Register 00	0x0128	16	R	0x0000	0xFFFF
FLCN	-	-	-	FSTATR1	Flash Status Register 1	0x012C	8	R	0x04	0xFF
FLCN	-	-	-	FWBL0	Flash Write Buffer Register L0	0x0130	16	R/W	0x0000	0xFFFF
FLCN	-	-	-	FWBH0	Flash Write Buffer Register H0	0x0138	16	R/W	0x0000	0xFFFF
FLCN	-	-	-	FWBL1	Flash Write Buffer Register L1	0x0140	16	R/W	0x0000	0xFFFF
FLCN	-	-	-	FWBH1	Flash Write Buffer Register H1	0x0144	16	R/W	0x0000	0xFFFF
FLCN	-	-	-	FPR	Protection Unlock Register	0x0180	8	R/W	0x00	0x00
FLCN	-	-	-	FPSR	Protection Unlock Status Register	0x0184	8	R	0x00	0xFF
FLCN	-	-	-	FSECMR	Flash Security Flag Monitor Register	0x01C0	16	R	Unique value for each chip	0x9FFF
FLCN	-	-	-	FAWSMR	Flash Access Window Start Address Monitor Register	0x01C8	16	R	Unique value for each chip	0xF800
FLCN	-	-	-	FAWEMR	Flash Access Window End Address Monitor Register	0x01D0	16	R	Unique value for each chip	0xF800
FLCN	-	-	-	FISR	Flash Initial Setting Register	0x01D8	8	R/W	0x00	0xFF
FLCN	-	-	-	FEXCR	Flash Extra Area Control Register	0x01DC	8	R/W	0x00	0xFF
FLCN	-	-	-	FEAML	Flash Error Address Monitor Register L	0x01E0	16	R/W	0x0000	0xFFFF

Table 3.4 Register description (9 of 9)

Peripheral name	Dim	Dim inc.	Dim index	Register name	Description	Address offset	Size	R/W	Reset value	Reset mask
FLCN	-	-	-	FEAMH	Flash Error Address Monitor Register H	0x01E8	16	R/W	0x0000	0xFFFF
FLCN	-	-	-	TSCDR	Temperature Sensor Calibration Data Register	0x0228	16	R	Unique value for each chip	0x0000
FLCN	-	-	-	FENTRYR	Flash P/E Mode Entry Register	0x3FB0	16	R/W	0x0000	0xFFFF
FLCN	-	-	-	PFBER	Prefetch Buffer Enable Register	0x3FC8	8	R/W	0x00	0xFF
CLIC	-	-	-	cliccfg	CLIC Configuration Register	0x0000	8	R/W	0x01	0xFF
CLIC	-	-	-	clicinfo	CLIC Information Register	0x0004	32	R	0x00802033	0xFFFFFFFF
CLIC	-	-	-	mintthresh	CLIC Interrupt Level Threshold Register	0x0008	32	R/W	0x00000000	0xFFFFFFFF
CLIC	51	0x004	0-50	clicintip%s	CLIC Interrupt Pending Register	0x1000	8	R/W	0x00	0xFF
CLIC	51	0x004	0-50	clicintie%s	CLIC Interrupt Enable Register	0x1001	8	R/W	0x00	0xFF
CLIC	51	0x004	0-50	clicintattr%s	CLIC Interrupt Attribute Register	0x1002	8	R/W	0xC0	0xFF
CLIC	51	0x004	0-50	clicintctl%s	CLIC Interrupt Input Control Register	0x1003	8	R/W	0x0F	0xFF
IMT	-	-	-	mtime_lo	Machine Timer Counter Register Low	0x000	32	R/W	0x00000000	0xFFFFFFFF
IMT	-	-	-	mtime_hi	Machine Timer Counter Register High	0x004	32	R/W	0x00000000	0xFFFFFFFF
IMT	-	-	-	mtimecmp_lo	Machine Timer Comparator Register Low	0x008	32	R/W	0xFFFFFFFF	0xFFFFFFFF
IMT	-	-	-	mtimecmp_hi	Machine Timer Comparator Register High	0x00C	32	R/W	0xFFFFFFFF	0xFFFFFFFF
IMT	-	-	-	mtimestop	Machine Timer Stop Register	0xFF8	32	R/W	0x00000000	0xFFFFFFFF
IMT	-	-	-	msip	Machine Timer Triggering Software Interrupt Register	0xFFC	32	R/W	0x00000000	0xFFFFFFFF
DBG	8	0x004	0-7	progbuf%s	Program Buffer 0 to 7	0x0080	32	R/W	0x00000000	0xFFFFFFFF
DBG	4	0x004	0-3	data%s	Abstract Data 0 to 3	0x00C0	32	R/W	0x00000000	0xFFFFFFFF

Note: Peripheral name = Name of peripheral
Dim = Number of elements in an array of registers
Dim inc. = Address increment between two simultaneous registers of a register array in the address map
Dim index = Sub string that replaces the %s placeholder within the register name
Register name = Name of register
Description = Register description
Address offset = Address of the register relative to the base address defined by the peripheral of the register
Size = Bit width of the register
Reset value = Default reset value of a register
Reset mask = Identifies which register bits have a defined reset value

Revision History

Revision 1.00 — Feb 15, 2022

First edition, issued

Revision 1.10 — April 15, 2022

Appendix 3. I/O Registers:

- Updated table 3.1 Peripheral base address.
- Updated table 3.2 Access cycles for non-GPT modules.

General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Precaution against Electrostatic Discharge (ESD)
   A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.
2. Processing at power-on
   The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.
3. Input of signal during power-off state
   Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.
4. Handling of unused pins
   Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.
5. Clock signals
   After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.
6. Voltage application waveform at input pin
   Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).
7. Prohibition of access to reserved addresses
   Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.
8. Differences between products
   Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

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