NP50P04SLG

-40V – -50A – P-channel Power MOS FET
Application : Automotive

R07DS0241EJ0101
Rev.1.01
May. 20, 2022

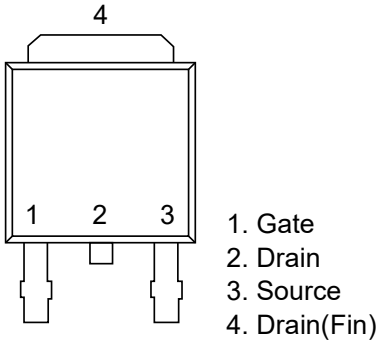
Description

This product is P-channel MOS Field Effect Transistor designed for high current switching applications.

Features

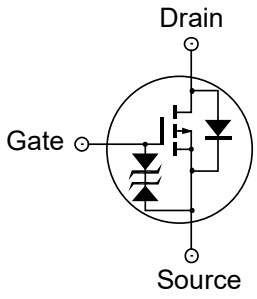
- Super low on-state resistance : $R_{DS(on)}$ = 9.6 mΩ Max. (V_{GS} = -10 V, I_D = -25 A)
  $R_{DS(on)}$ = 15 mΩ Max. (V_{GS} = -4.5 V, I_D = -25 A)
- Low input capacitance : Ciss = 3800 pF Typ.
- Built-in gate protection diode
- Designed for automotive application and AEC-Q101 qualified.
- Pb-free (This product does not contain Pb in the external electrode)

Outline



1. Gate
2. Drain
3. Source
4. Drain(Fin)

MP-3ZK (TO-252)



Equivalent circuit

Absolute Maximum Ratings

(T_a=25°C)

Item	Symbol	Ratings	Unit
Drain to Source Voltage (V_{GS} = 0 V)	V_{DSS}	-40	V
Gate to Source Voltage (V_{DS} = 0 V)	V_{GSS}	∓20	V
Drain Current (DC) (T_c = 25 °C)	$I_{D(DC)}$	∓50	A
Drain Current (pulse)	$I_{D(pulse)}$ Notes1	∓150	A
Total Power Dissipation (T_c = 25 °C)	P_{T1}	84	W
Total Power Dissipation (T_a = 25 °C)	P_{T2}	1.2	W
Channel Temperature	T_{ch}	175	°C
Storage Temperature	T_{stg}	-55 to 175	°C
Single Avalanche Current	I_{AS} Notes2	37	A
Single Avalanche Energy	E_{AS} Notes2	136	mJ

Notes 1. PW ≤ 10 μs , Duty Cycle ≤ 1%

2. Starting T_{ch}=25℃ , V_{DD} = -20V , R_G = 25 Ω , V_{GS} = -20 → 0V , L = 100μH

Thermal Resistance

Channel to Case Thermal Resistance	$R_{th(ch-c)}$ Notes3	1.78	°C/W
Channel to Ambient Thermal Resistance	$R_{th(ch-a)}$ Notes3	125	°C/W

Electrical Characteristics

(T_a=25°C)

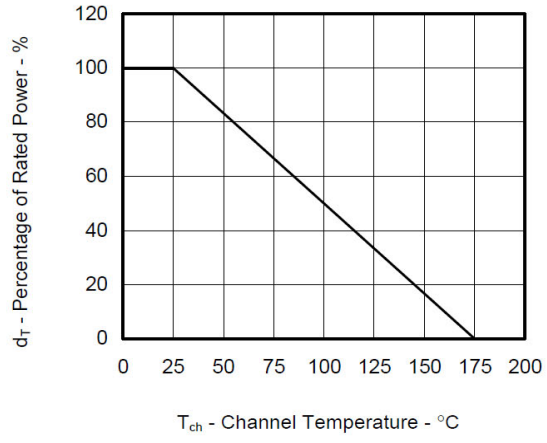
Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Zero Gate Voltage Drain Current	I_{DSS}	—	—	-1	μA	V_{DS} = -40 V, V_{GS} = 0 V
Gate Leakage Current	I_{GSS}	—	—	∓10	μA	V_{GS} = ∓ 20 V, V_{DS} = 0 V
Gate to Source Threshold Voltage	$V_{GS(th)}$	-1.0	-1.4	-2.5	V	V_{DS} = V_{GS}, I_D = -250 μ A
Forward Transfer Admittance	| yfs | Notes4	12	44	—	S	V_{DS} = -10 V, I_D = -25 A
Drain to Source On-state Resistance	$R_{DS(on)1}$ Notes4	—	8.2	9.6	mΩ	V_{GS} = -10 V, I_D = -25 A
	$R_{DS(on)2}$ Notes4	—	9.8	15	mΩ	V_{GS} = -4.5 V, I_D = -25 A
Input Capacitance	C_{iss} Notes3	—	3800	5700	pF	V_{DS} = -10 V
Output Capacitance	C_{oss} Notes3	—	740	1120	pF	V_{GS} = 0 V
Reverse Transfer Capacitance	C_{rss} Notes3	—	500	905	pF	f = 1 MHz
Turn-on Delay Time	$t_{d(on)}$ Notes3	—	11	24	ns	V_{DD} = -20 V
Rise Time	t_r Notes3	—	15	39	ns	I_D = -25 A
Turn-off Delay Time	$t_{d(off)}$ Notes3	—	250	505	ns	V_{GS} = -10 V
Fall Time	t_f Notes3	—	150	380	ns	R_G = 0 Ω
Total Gate Charge	Q_g Notes3	—	100	150	nC	V_{DD} = -32 V
Gate to Source Charge	Q_{gs}	—	13	—	nC	V_{GS} = -10 V
Gate to Drain Charge	Q_{gd}	—	30	—	nC	I_D = -50 A
Body Diode Forward Voltage	$V_{F(S-D)}$ Notes4	—	0.96	1.5	V	I_F = -50 A, V_{GS} = 0 V
Reverse Recovery Time	t_{rr}	—	50	—	ns	I_F = -50 A, V_{GS} = 0 V
Reverse Recovery Charge	Q_{rr}	—	63	—	nC	di/dt = -100 A/μs

Notes 3. Designed target value on Renesas measurement condition. Not subject to production test.

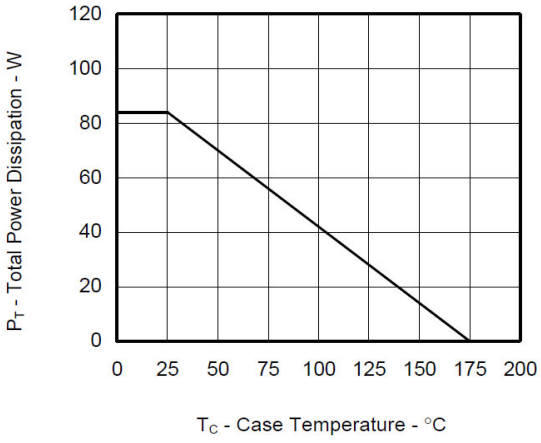
4. Pulse test.

Typical Characteristics

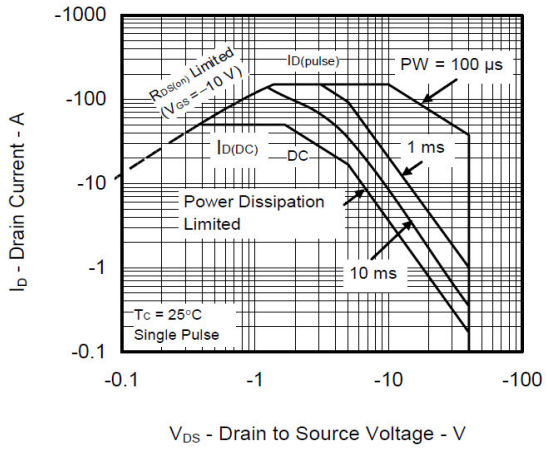
DERATING FACTOR OF FORWARD BIAS SAFE OPERATING AREA



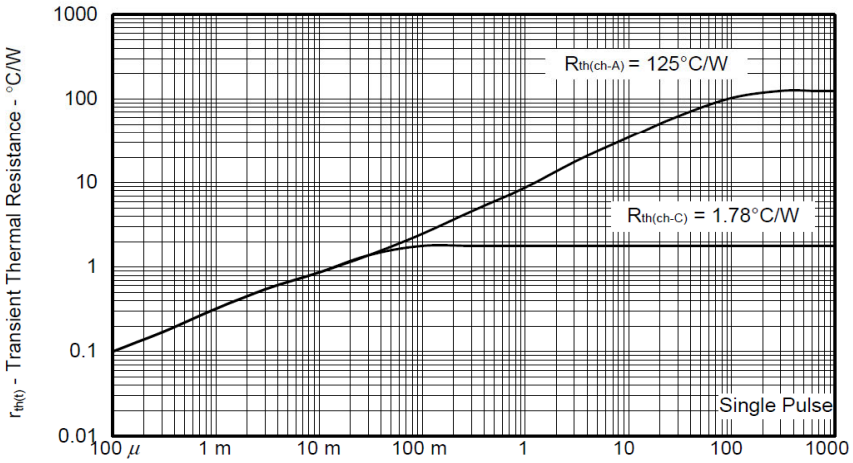
TOTAL POWER DISSIPATION vs. CASE TEMPERATURE



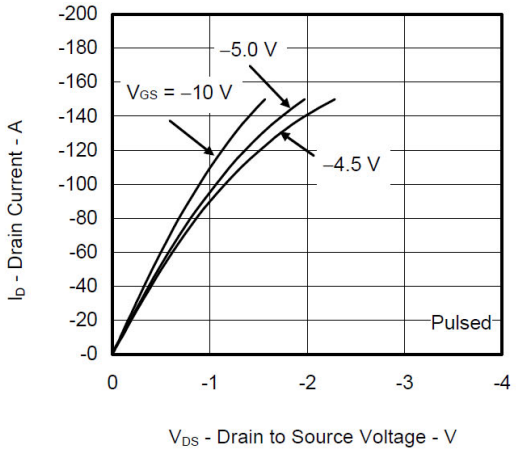
FORWARD BIAS SAFE OPERATING AREA



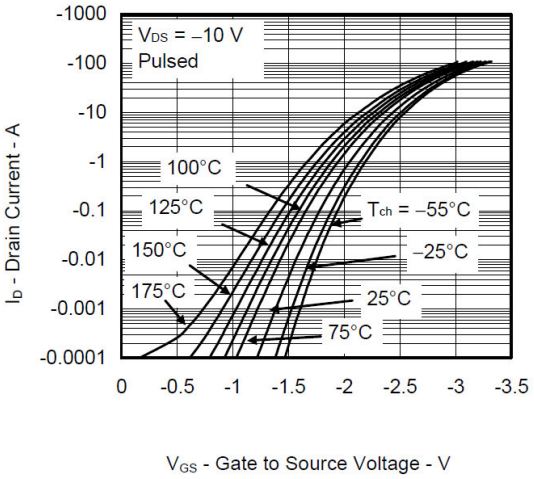
TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH



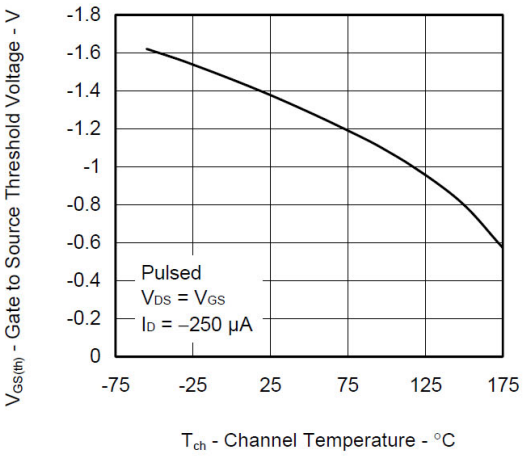
DRAIN CURRENT vs.
DRAIN TO SOURCE VOLTAGE



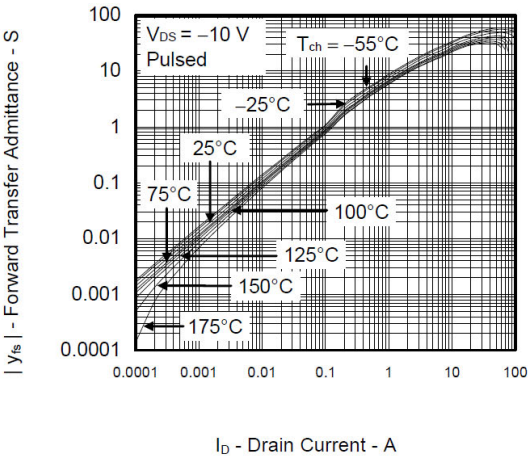
FORWARD TRANSFER CHARACTERISTICS



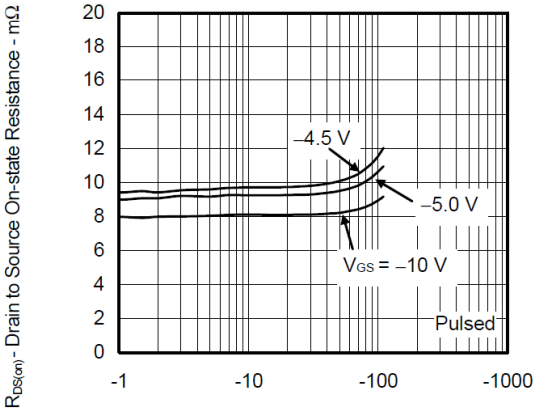
GATE TO SOURCE THRESHOLD VOLTAGE vs.
CHANNEL TEMPERATURE



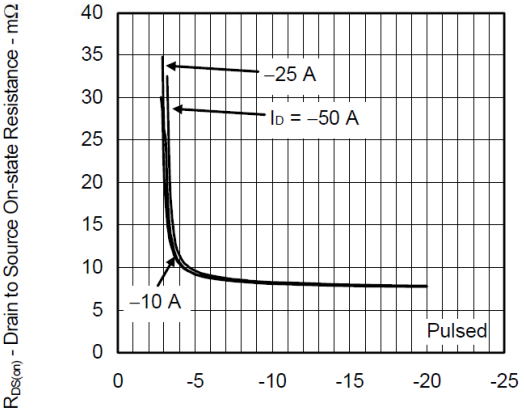
FORWARD TRANSFER ADMITTANCE vs.
DRAIN CURRENT



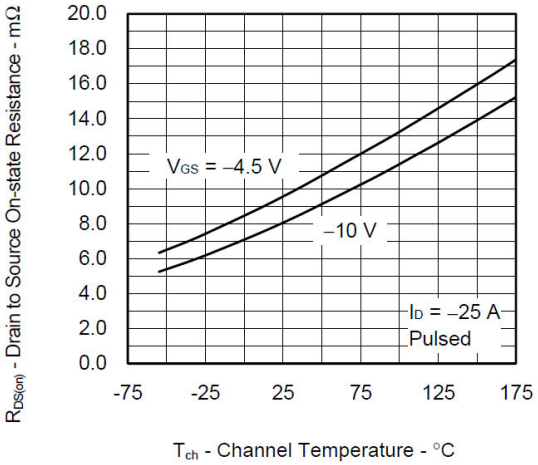
DRAIN TO SOURCE ON-STATE RESISTANCE vs.
DRAIN CURRENT



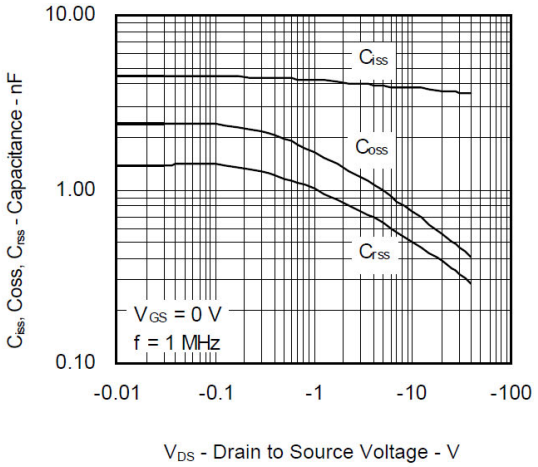
DRAIN TO SOURCE ON-STATE RESISTANCE vs.
GATE TO SOURCE VOLTAGE



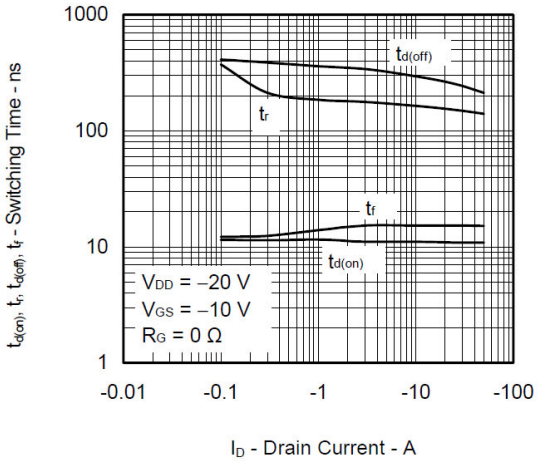
DRAIN TO SOURCE ON-STATE RESISTANCE vs. CHANNEL TEMPERATURE



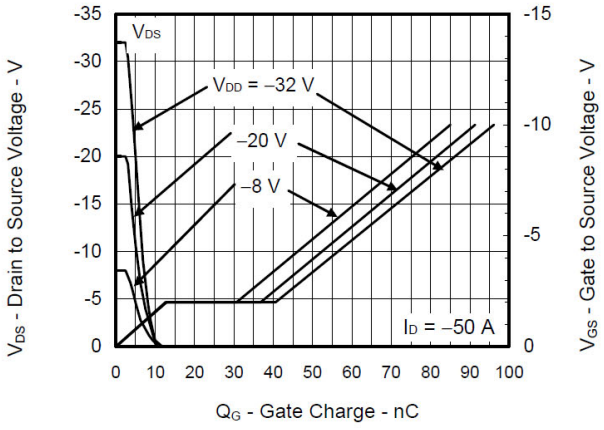
CAPACITANCE vs. DRAIN TO SOURCE VOLTAGE



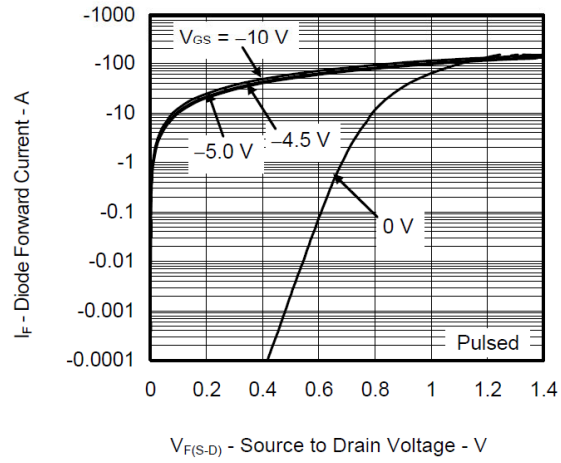
SWITCHING CHARACTERISTICS



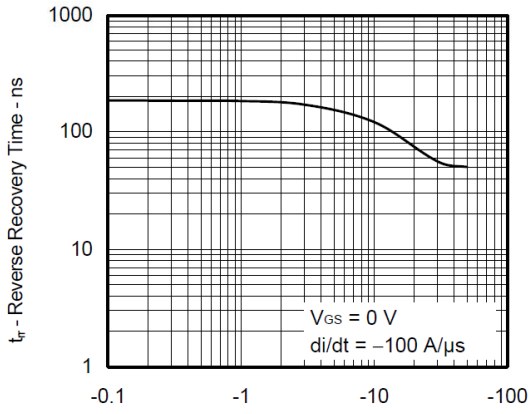
DYNAMIC INPUT/OUTPUT CHARACTERISTICS



SOURCE TO DRAIN DIODE FORWARD VOLTAGE



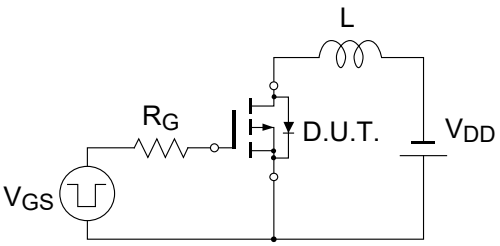
REVERSE RECOVERY TIME vs. DIODE FORWARD CURRENT



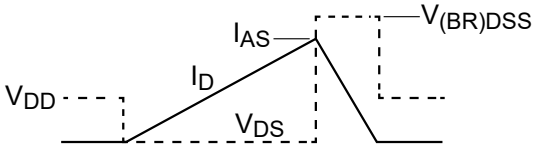
Test Circuit

Avalanche

Test Circuit



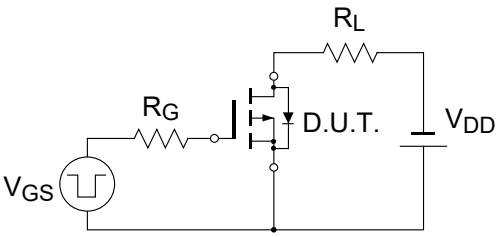
Waveform



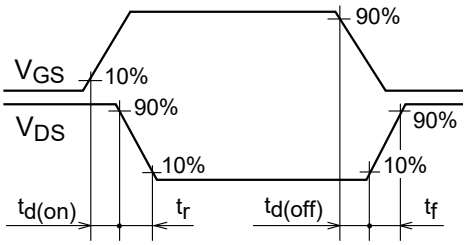
$$E_{AS} = \frac{1}{2} \cdot L \cdot I_{AS}^2 \cdot \frac{V_{(BR)DSS}}{V_{(BR)DSS} - V_{DD}}$$

Switching Time

Test Circuit

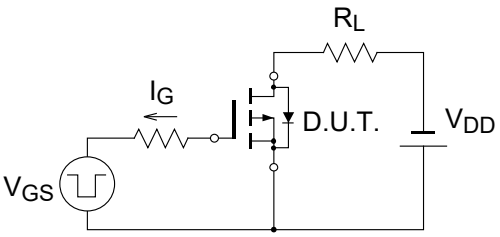


Waveform

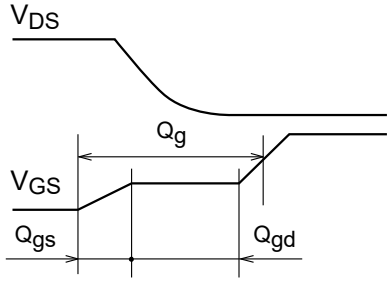


Gate Charge

Test Circuit

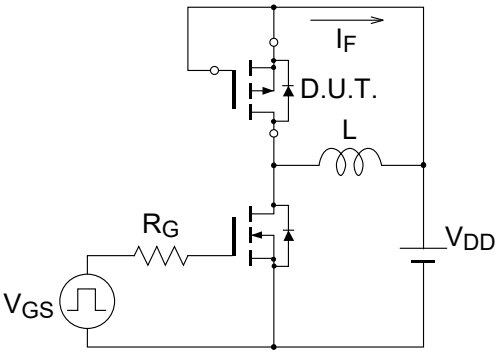


Waveform

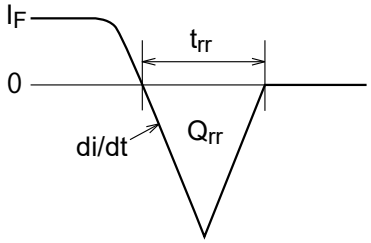


Reverce Recovery

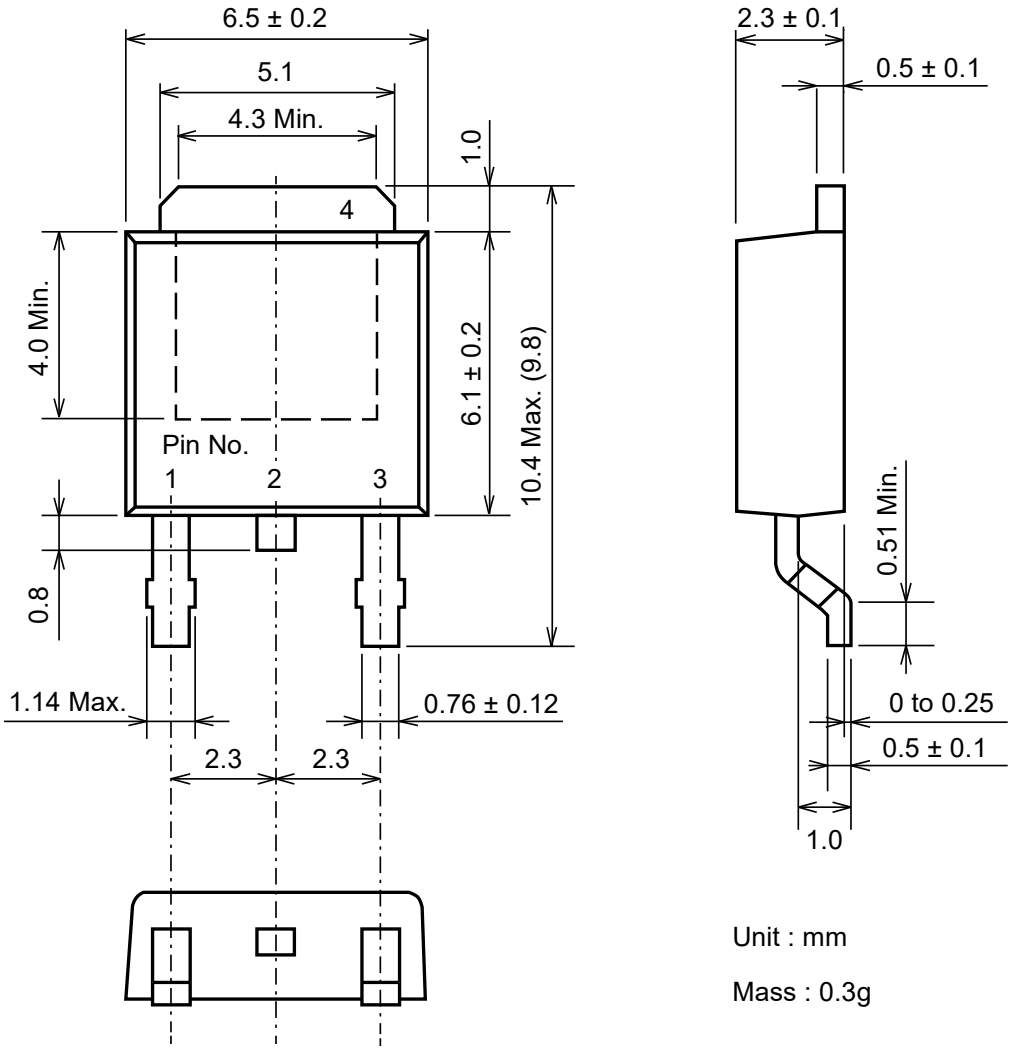
Test Circuit



Waveform



Package Dimensions



Ordering Information

Part No.	Quantity	Shipping container
NP50P04SLG-E1-AY	2500pcs/reel	Taping

Remark Strong electric field, when exposed to this device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred.

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Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
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