

NP100P04PLG

-40V – -100A – P-channel Power MOS FET

R07DS1513EJ0101

Application : Automotive

Rev.1.01

Jul. 14, 2022

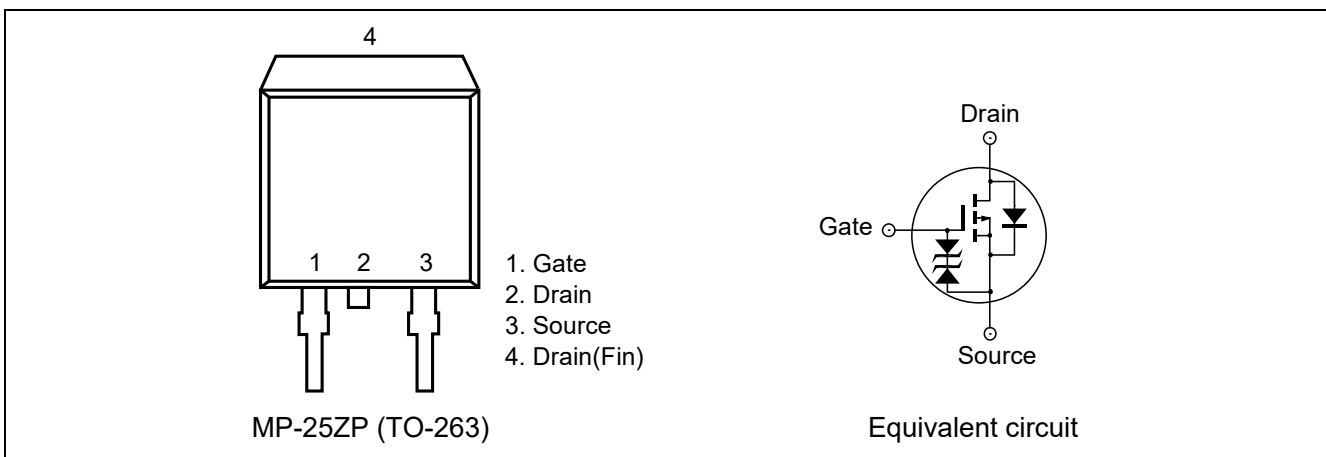
Description

This product is P-channel MOS Field Effect Transistor designed for high current switching applications.

Features

- Super low on-state resistance : $R_{DS(on)} = 3.7 \text{ m}\Omega \text{ Max. (} V_{GS} = -10 \text{ V, } I_D = -50 \text{ A)}$
 $R_{DS(on)} = 5.1 \text{ m}\Omega \text{ Max. (} V_{GS} = -4.5 \text{ V, } I_D = -50 \text{ A)}$
- Low input capacitance : $C_{iss} = 15100 \text{ pF Typ.}$
- Built-in gate protection diode
- Designed for automotive application and AEC-Q101 qualified.
- Pb-free (This product does not contain Pb in the external electrode)

Outline



Absolute Maximum Ratings

($T_a=25^\circ\text{C}$)

Item	Symbol	Ratings	Unit
Drain to Source Voltage ($V_{GS} = 0 \text{ V}$)	V_{DSS}	-40	V
Gate to Source Voltage ($V_{DS} = 0 \text{ V}$)	V_{GSS}	∓ 20	V
Drain Current (DC) ($T_c = 25^\circ\text{C}$)	$I_{D(DC)}$	∓ 100	A
Drain Current (pulse)	$I_{D(pulse)}$ ^{Notes1}	∓ 300	A
Total Power Dissipation ($T_c = 25^\circ\text{C}$)	P_{T1}	200	W
Total Power Dissipation ($T_a = 25^\circ\text{C}$)	P_{T2}	1.8	W
Channel Temperature	T_{ch}	175	$^\circ\text{C}$
Storage Temperature	T_{stg}	-55 to 175	$^\circ\text{C}$
Single Avalanche Current	I_{AS} ^{Notes2}	74	A
Single Avalanche Energy	E_{AS} ^{Notes2}	550	mJ

Notes 1. $PW \leq 10 \mu\text{s}$, Duty Cycle $\leq 1\%$

2. Starting $T_{ch}=25^\circ\text{C}$, $V_{DD} = -20\text{V}$, $R_G = 25 \Omega$, $V_{GS} = -20 \rightarrow 0\text{V}$, $L = 100\mu\text{H}$

Thermal Resistance

Channel to Case Thermal Resistance	$R_{th(ch-c)}$ ^{Notes3}	0.75	°C/W
Channel to Ambient Thermal Resistance	$R_{th(ch-a)}$ ^{Notes3}	83.3	°C/W

Electrical Characteristics

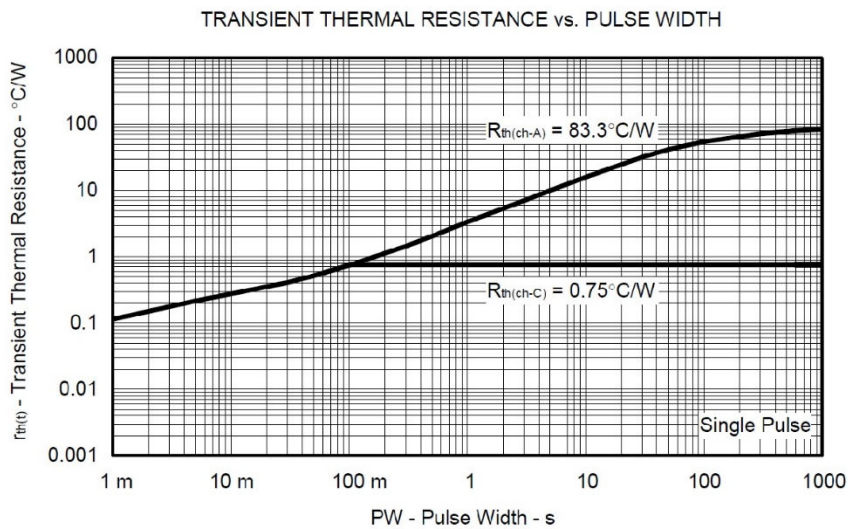
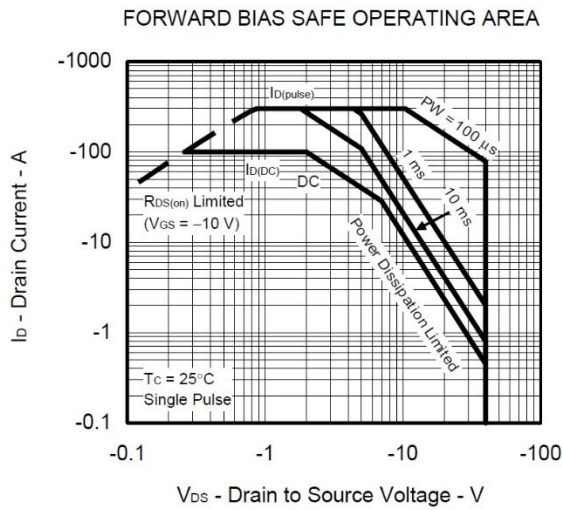
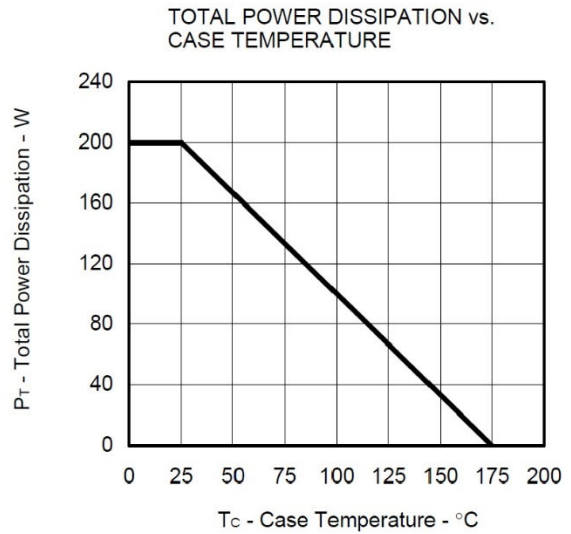
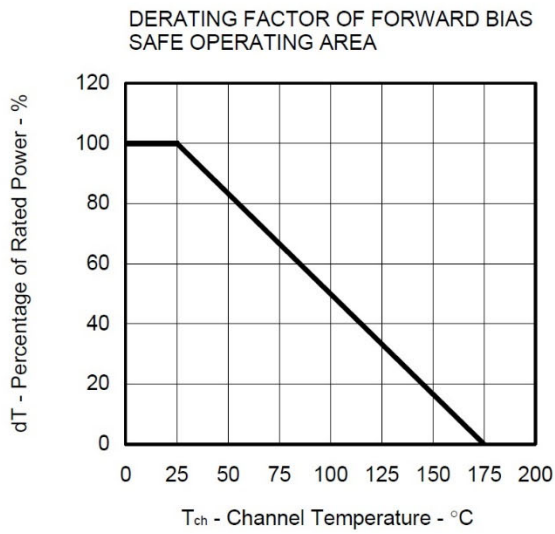
(T_a=25°C)

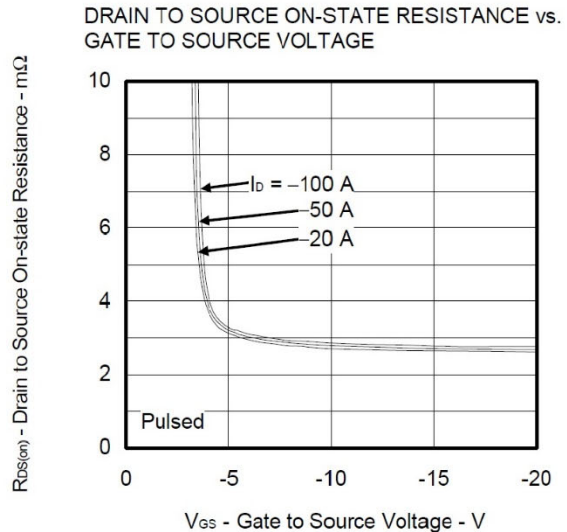
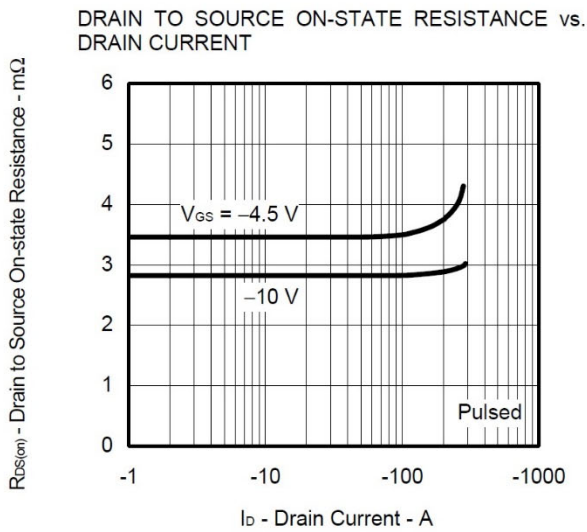
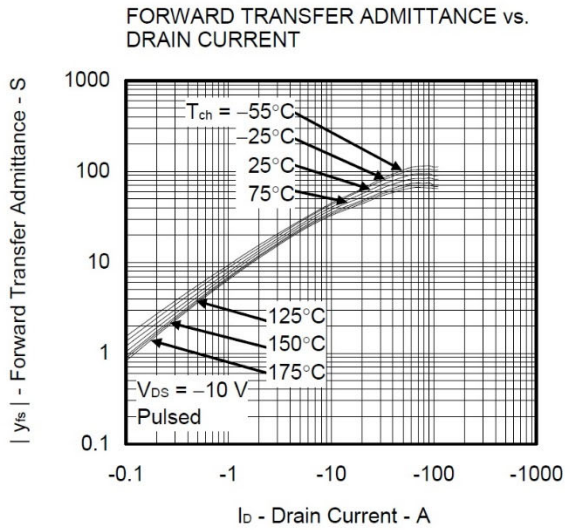
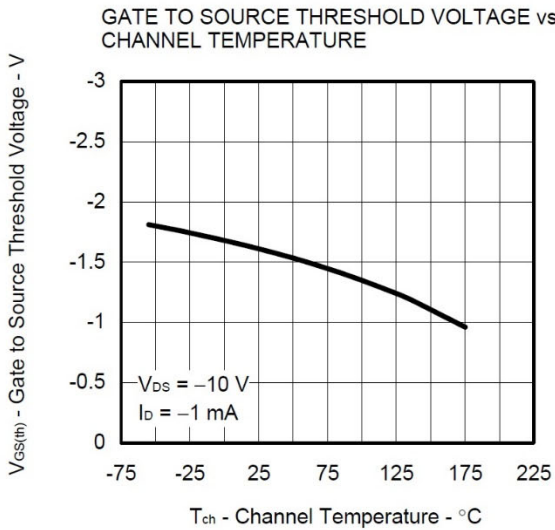
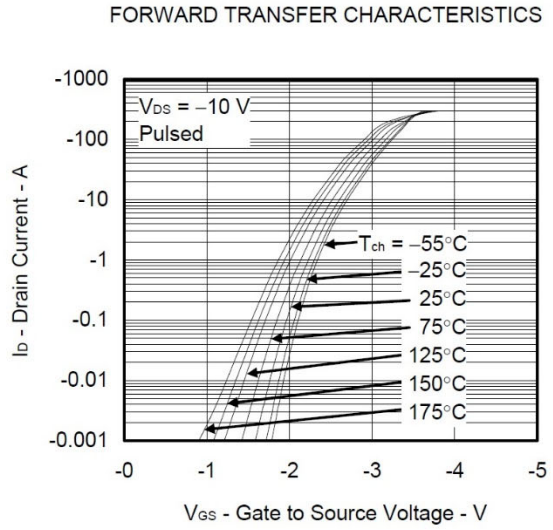
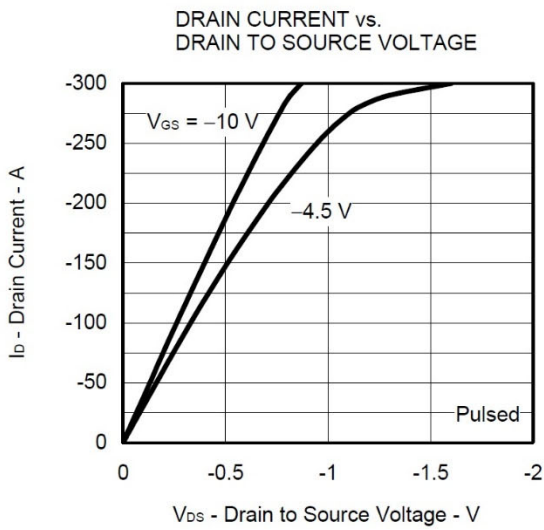
Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Zero Gate Voltage Drain Current	I_{DSS}	—	—	-10	μA	V _{DS} = -40 V, V _{GS} = 0 V
Gate Leakage Current	I_{GSS}	—	—	±10	μA	V _{GS} = ±20 V, V _{DS} = 0 V
Gate to Source Threshold Voltage	V _{GS(th)}	-1.0	-1.6	-2.5	V	V _{DS} = -10 V, I _D = -1 mA
Forward Transfer Admittance	y _{fs} ^{Notes4}	43	88	—	S	V _{DS} = -10 V, I _D = -50 A
Drain to Source On-state Resistance	R _{DS(on)1} ^{Notes4}	—	2.8	3.7	mΩ	V _{GS} = -10 V, I _D = -50 A
	R _{DS(on)2} ^{Notes4}	—	3.4	5.1	mΩ	V _{GS} = -4.5 V, I _D = -50 A
Input Capacitance	C _{iss}	—	15100	—	pF	V _{DS} = -10 V
Output Capacitance	C _{oss}	—	2400	—	pF	V _{GS} = 0 V
Reverse Transfer Capacitance	C _{rss}	—	1130	—	pF	f = 1 MHz
Turn-on Delay Time	t _{d(on)}	—	38	—	ns	V _{DD} = -20 V
Rise Time	t _r	—	30	—	ns	I _D = -50 A
Turn-off Delay Time	t _{d(off)}	—	300	—	ns	V _{GS} = -10 V
Fall Time	t _f	—	100	—	ns	R _G = 0 Ω
Total Gate Charge	Q _g	—	320	—	nC	V _{DD} = -32 V
Gate to Source Charge	Q _{gs}	—	37	—	nC	V _{GS} = -10 V
Gate to Drain Charge	Q _{gd}	—	85	—	nC	I _D = -100A
Body Diode Forward Voltage	V _{F(S-D)} ^{Notes4}	—	0.91	1.5	V	I _F = -100 A, V _{GS} = 0 V
Reverse Recovery Time	t _{rr}	—	70	—	ns	I _F = -100 A, V _{GS} = 0 V
Reverse Recovery Charge	Q _{rr}	—	123	—	nC	di/dt = -100 A/μs

Notes 3. Designed target value on Renesas measurement condition. Not subject to production test.

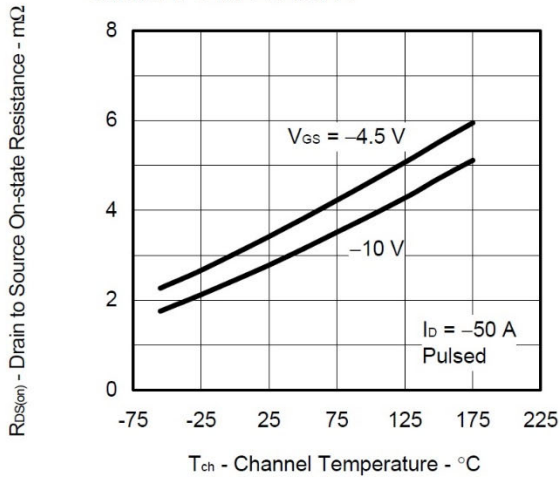
4. Pulse test.

Typical Characteristics

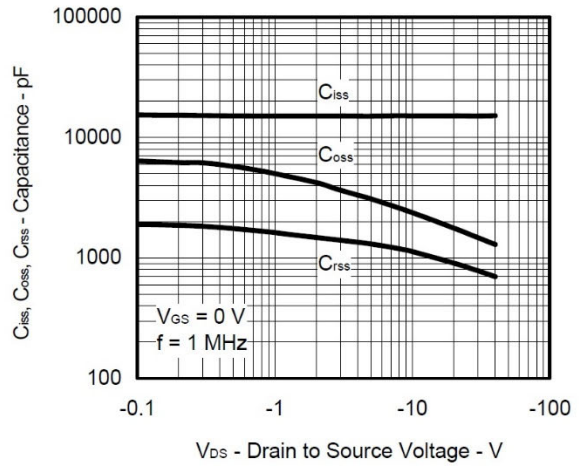




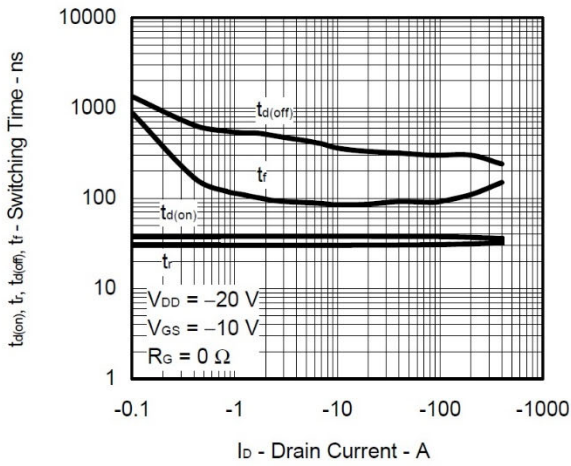
DRAIN TO SOURCE ON-STATE RESISTANCE vs. CHANNEL TEMPERATURE



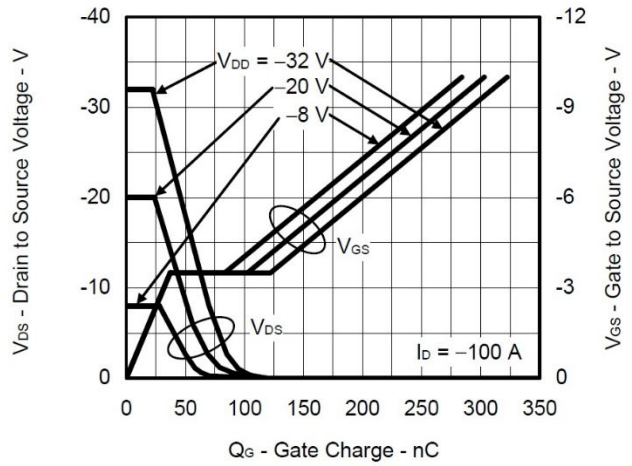
CAPACITANCE vs. DRAIN TO SOURCE VOLTAGE



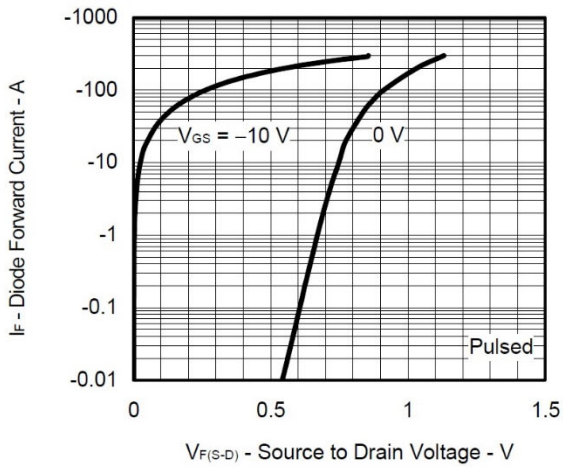
SWITCHING CHARACTERISTICS



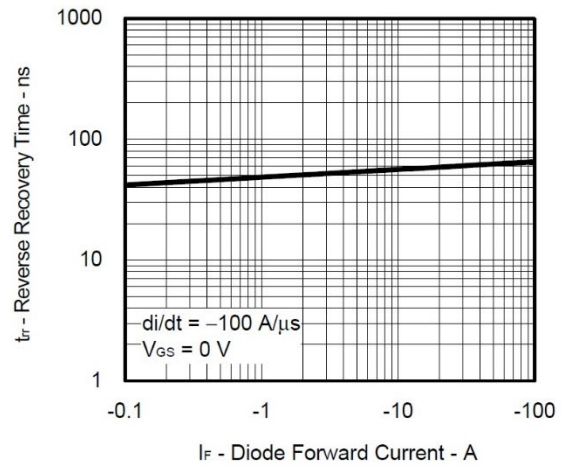
DYNAMIC INPUT/OUTPUT CHARACTERISTICS



SOURCE TO DRAIN DIODE FORWARD VOLTAGE



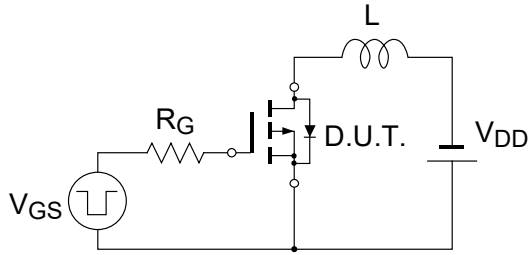
REVERSE RECOVERY TIME vs. DIODE FORWARD CURRENT



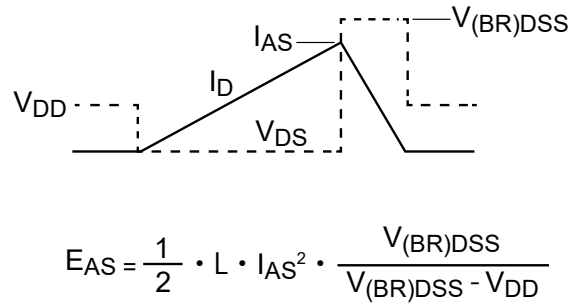
Test Circuit

Avalanche

Test Circuit

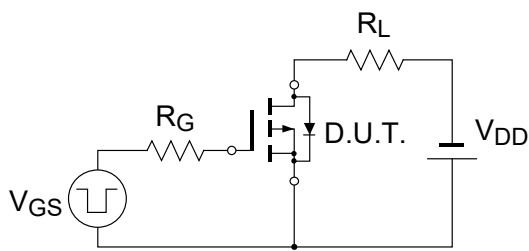


Waveform

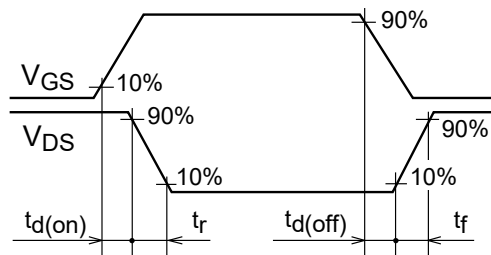


Switching Time

Test Circuit

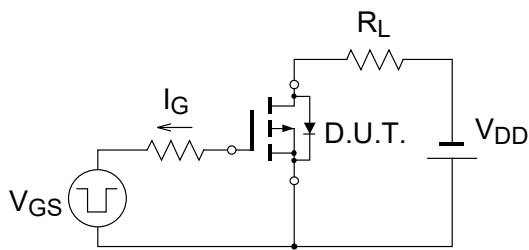


Waveform

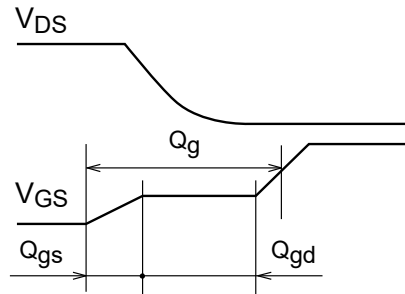


Gate Charge

Test Circuit

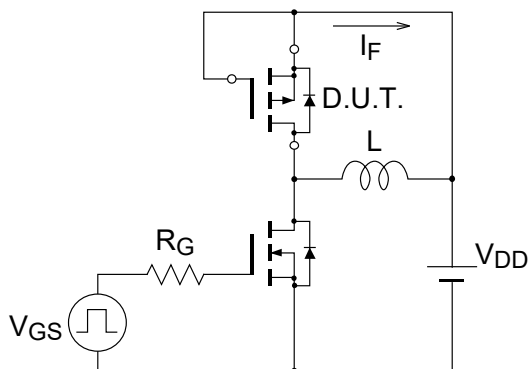


Waveform

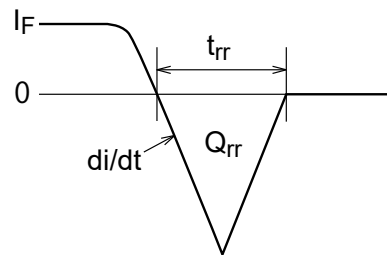


Reverse Recovery

Test Circuit



Waveform



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