

PLL Datasheet

Analog-PLL For Frequency Multiplying

Key Features

- Including Loop-filter
- VCO operating range : 2500MHz - 5000 MHz
- Output frequency range : 1250MHz - 2500 MHz
- Input frequency range : 12MHz - 320 MHz
- Multiplying (Output freq. / PFD freq.) : 64 - 127
- Divider
7bit feedback divider and 3bit input divider
- Power-down Mode
- Multiple outputs with post-divider
- Power-on sequence is constraint-free
- STBY sequence is constraint-free

TECHNOLOGY

Process: TSMC 28nm HPM/HPC

Available metallization technologies : 4X2Y2R and 5X2Y2R

OPERATING CONDITION

Parameter		Min	Max	Unit
Operating Voltage (AVDD)		1.62	1.98	V
Operating Voltage (VDD)		0.935	1.08	V
Junction Temperature		-40	125	°C
Input Clock	Duty	30	70	%
	Rise/Fall time	-	0.2	ns

**This IP is contract design IP. Please contact for detail.*